Legacy Device: *Signetics S8270, S8271*

DESCRIPTION

The 8270 is a 4-bit Shift Register with both serial and parallel data entry capability.

The data input lines are single-ended true input data lines which condition their specific register bit location after an enabled clocking transition. Since data transfer is synchronous with clock, data may be transferred in any serial/parallel input/output relationship.

The internal design uses level sensitive binaries which respond to the negative-going clock transition. A buffer clock driver has been included to minimize input clock loading.

Mode control logic is available to determine three possible control states. These register states are serial shift right mode, parallel enter mode, and no change or hold mode. These states accomplish logical decoding for system control. The truth table for the control modes is shown below.

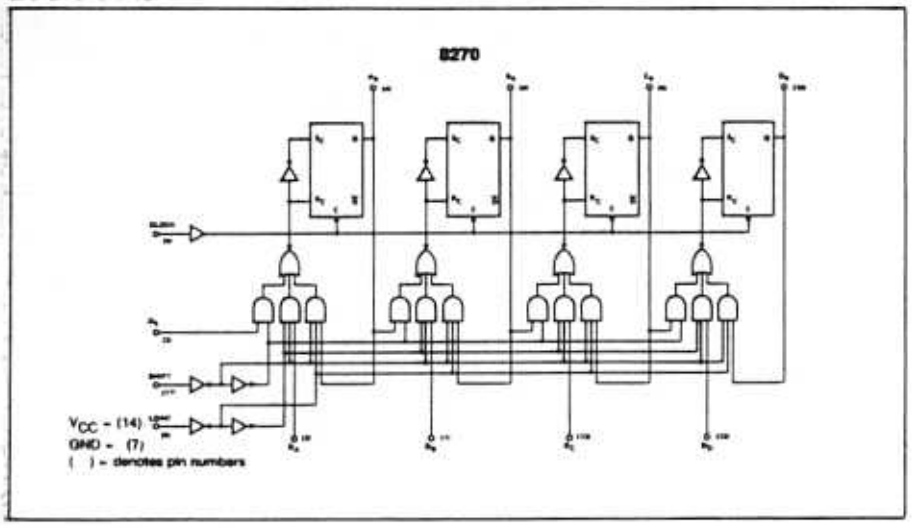
For applications not requiring the hold mode, the load input may be tied high and the shift input used as the mode control.

The 8271 provides a direct reset (R_D), and a $\overline{D_{out}}$ line in addition to the available outputs of the 8270 element. The fan-out specification for this output is the same as the true outputs of the 8270 element.

ORDERING CODE (See Section 9 for further Package and Ordering Information)

PACKAGES	PIN CONF.	COMMERCIAL RANGES V_{CC}=5V±5%; T_A=0°C to +75°C	MILITARY RANGES V_{CC}=5V±5%; T_A=−55°C to +125°C
Plastic DIP	Fig.A Fig.C	N8270N • N82S70N N8271N • N82S71N	
Ceramic DIP	Fig.A Fig.C	N8270F • N82S70F N8271F • N82S71F	S8270F S8271F
Flatpak	Fig.B Fig.A		S8270W S8271W

LOGIC DIAGRAM



PIN CONFIGURATIONS

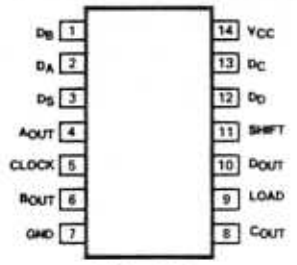


Figure A

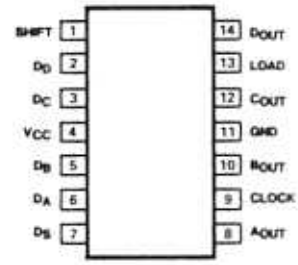


Figure B

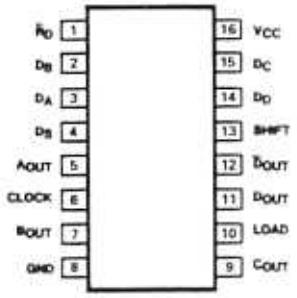


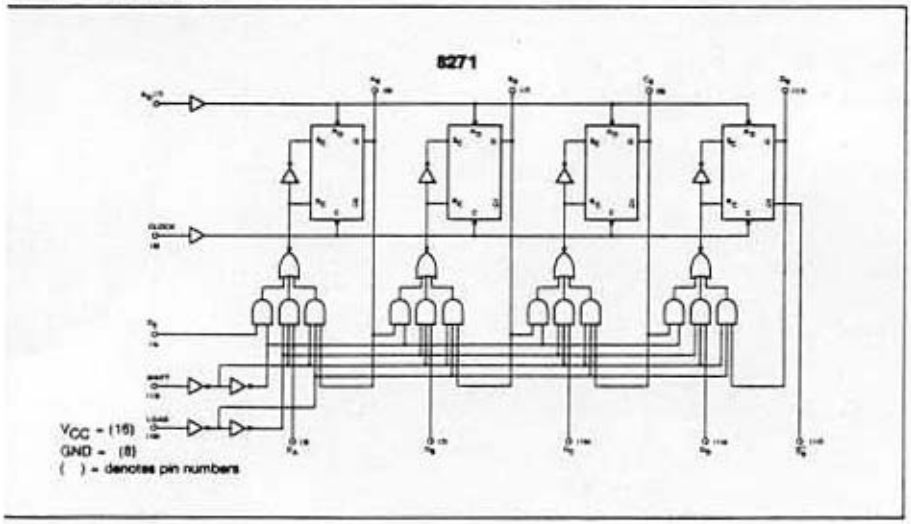
Figure C

MODE SELECT— FUNCTION TABLE

CONTROL STATE	LOAD	SHIFT
Hold	L	L
Parallel Entry	H	L
Shift Right	L	H
Shift Right	H	H

H = HIGH voltage level
L = LOW voltage level

LOGIC DIAGRAM



DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE[b]

PARAMETER		TEST CONDITIONS	8270		8271		UNIT
			Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = 4.75V, I_{OH} = −800μA	2.6		2.6		V
V_{OL}	Output LOW voltage	V_{CC} = 4.75V, I_{OL} = 11.2mA		0.4		0.4	V
I_{IH}	Input HIGH current Reset 8271 only	V_{CC} = 5.25V, V_{IN} = 4.5V		40		40 40	μA μA
I_{IL}	Input LOW current	V_{CC} = 5.25V, V_{IN} = 0.4V		−1.2		−1.2	mA
V_{BD}	Voltage breakdown	V_{CC} = 5.25V, I_{IN} = 10mA	5.5				V
I_{CC}	Supply current	V_{CC} = 5.25V		47		65	mA

DC CHARACTERISTICS OVER OPERATING TEMPERATURE RANGE[b]

PARAMETER		TEST CONDITIONS	82S70		82S71		UNIT
			Min	Max	Min	Max	
V_{OH}	Output HIGH voltage	V_{CC} = 4.75V, I_{OH} = 1.0mA	2.7		2.7		V
V_{OL}	Output LOW voltage	V_{CC} = 4.75V, I_{OL} = 20mA		0.5		0.5	V
I_{IH}	Input HIGH current Reset 82S71 only	V_{CC} = 5.25V		10		10 10	μA μA
I_{IL}	Input LOW current Load, Data, Clock inputs Shift,Reset(82S71only)	V_{CC} = 5.25V, V_{IN} = 0.5V		 −400 −800		 −400 −800	 μA μA
V_{BD}	Voltage breakdown	V_{CC} = 4.75V, I_{IN} = 1mA	5.5		5.5		V
V_{CD}	Input clamp voltage	V_{CC} = 4.75, I_{IN} = −18mA		−1.2		−1.2	V
I_{CC}	Supply current	V_{CC} = 5.25V		90		90	mA

Note

b. For family dc characteristics, see inside front cover for 54/74 and 54H/74H, and see inside back cover for 54S/74S and 54LS/74LS specifications.

AC CHARACTERISTICS: T_A = 25° C (See Section 4 for Waveforms and Conditions)

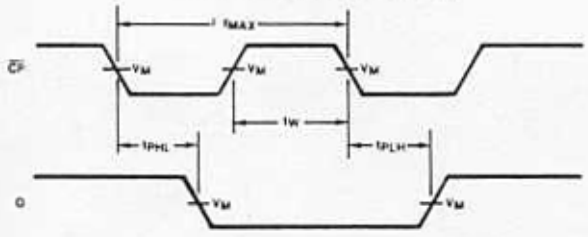
PARAMETER		TEST CONDITIONS	8270/71 C_L = 21pF R_1 = ∞Ω R_2 = 127Ω		82S70/S71 C_L = 15pF R_L = 280Ω		UNIT
			Min	Max	Min	Max	
f_{MAX}	Maximum clock frequency	Figure 1	15		40		MHz
t_{PLH} t_{PHL}	Propagation delay Clock to output	Figure 1		40 40		20 20	ns ns
t_{PLH} t_{PHL}	Propagation delay Reset to output	Figure 2		40 40		16 16	ns ns

AC SET-UP REQUIREMENTS: T_A = 25° C (See Section 4 for Waveforms and Conditions)

PARAMETER		TEST CONDITIONS	8270/71		82S70/S71		UNIT
			Min	Max	Min	Max	
t_W	Clock pulse width	Figure 1	20		8.0		ns
t_W	Reset pulse width	Figure 2	30		9.0		ns
t_s	Set-up time Data to clock	Figure 3	30		3.0		ns
t_h	Hold time Data to clock	Figure 3	0		2.0		ns
t_s	Set-up time Load or Shift to clock	Figure 3	15		6.0		ns
t_h	Hold time Load or Shift to clock	Figure 3	0		0		ns
t_{rec}	Recovery time MR to clock	Figure 3	30		10		ns

AC WAVEFORMS

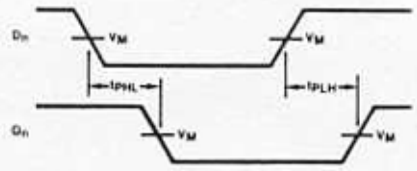
CLOCK TO OUTPUT DELAYS
AND CLOCK PULSE WIDTH



V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

Figure 1

PARALLEL DATA TO OUTPUT DELAYS



V_M = 1.5V for 54/74 and 54S/74S; V_M = 1.3V for 54LS/74LS

Figure 2

AC TEST FIGURE AND WAVEFORMS

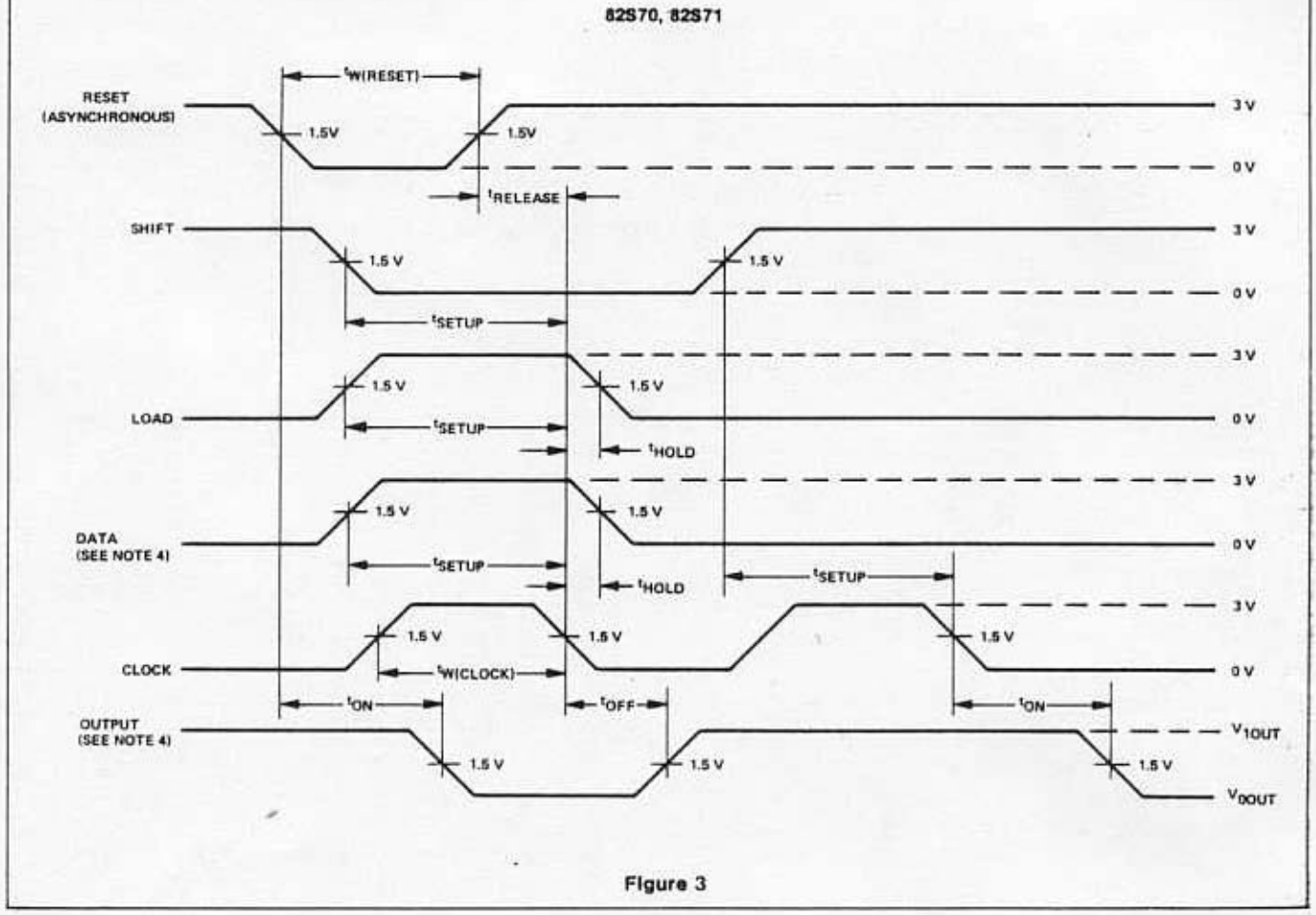


Figure 3

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