19-5785; Rev 2; 3/11

DS3170
DS3/E3 Single-Chip Transceiver

GENERAL DESCRIPTION

The DS3170 combines a DS3/E3 framer and an LIU (single-chip transceiver) to interface to a DS3/E3 physical copper line.

APPLICATIONS

Access Concentrators

Routers and Switches

SONET/SDH ADM

SONET/SDH Muxes

PBXs

PDH Multiplexer/ Demultiplexer

Multiservice Access Platforms (MSAPs)

Multiservice Protocol Platform (MSPPs)

Test Equipment

Digital Cross Connect

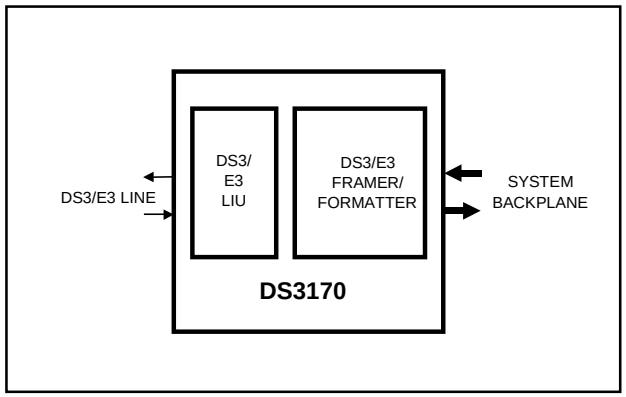
Integrated-Access Device (IAD)

ORDERING INFORMATION

PART	TEMP RANGE	PIN-PACKAGE
DS3170	0°C to +70°C	100 CSBGA
DS3170+	0°C to +70°C	100 CSBGA
DS3170N	-40°C to +85°C	100 CSBGA
DS3170N+	-40°C to +85°C	100 CSBGA

+Denotes a lead(Pb)-free/RoHS compliant package.

FUNCTIONAL DIAGRAM



FEATURES

- Single-Chip Transceiver for DS3 and E3
- Performs Receive Clock/Data Recovery and Transmit Waveshaping for DS3 and E3
- Jitter Attenuator can be Placed Either in the Receive or Transmit Path
- Interfaces to 75Ω Coaxial Cable at Lengths Up to 380 Meters or 1246 Feet (DS3), or 440 Meters or 1443 Feet (E3)
- Uses 1:2 Transformers on Both Tx and Rx
- On-Chip DS3 (M23 or C-Bit) and E3 (G.751 or G.832) Framer
- Built-In HDLC Controller with 256-Byte FIFO for the Insertion/Extraction of DS3 PMDL, G.751 Sn Bit, and G.832 NR/GC Bytes
- On-Chip BERT for PRBS and Repetitive Pattern Generation, Detection and Analysis
- Large Performance-Monitoring Counters for Accumulation Intervals of At Least 1 Second
- Flexible Overhead Insertion/Extraction Port for DS3, E3 Framers
- Loopbacks Include Line, Diagnostic, Framer, Payload, and Analog with Capabilities to Insert AIS in the Directions Away from Loopback Directions
- Integrated Clock Rate Adapter to Generate the Remaining Internally Required 44.736MHz (DS3) and 34.368MHz (E3) from a Single-Clock Reference Source
- CLAD Reference Clock can be 44.736MHz, 34.368MHz, 77.76MHz, 51.84MHz, or 19.44MHz
- Software Compatible with DS3171–DS3174 SCT Product Family
- 8-/16-Bit Parallel and Slave SPI Serial (≤ 10Mbps) Microprocessor Interface
- Low-Power (0.5W) 3.3V Operation (5V Tolerant I/O)
- 100-Pin Small 11mm x 11mm (1mm) CSBGA
- Industrial Temperature Operation: -40°C to +85°C
- IEEE 1149.1 JTAG Test Port

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, click here: www.maxim-ic.com/errata.*

TABLE OF CONTENTS

1 DETAILED DESCRIPTION 10
2 BLOCK DIAGRAMS 10
3 APPLICATIONS 12
4 FEATURE DETAILS 13
4.1 GLOBAL FEATURES 13
4.2 RECEIVE DS3/E3 LIU FEATURES 13
4.3 JITTER ATTENUATOR FEATURES 13
4.4 RECEIVE DS3/E3 FRAMER FEATURES 13
4.5 TRANSMIT DS3/E3 FORMATTER FEATURES 14
4.6 TRANSMIT DS3/E3 LIU FEATURES 14
4.7 CLOCK RATE ADAPTER FEATURES 14
4.8 HDLC CONTROLLER FEATURES 14
4.9 FEAC CONTROLLER FEATURES 14
4.10 TRAIL TRACE BUFFER FEATURES 15
4.11 BIT ERROR-RATE TESTER (BERT) FEATURES 15
4.12 LOOPBACK FEATURES 15
4.13 MICROPROCESSOR INTERFACE FEATURES 15
4.14 SLAVE SERIAL PERIPHERAL INTERFACE (SPI) FEATURES 15
4.15 TEST FEATURES 15
5 STANDARDS COMPLIANCE 16
6 ACRONYMS AND GLOSSARY 17
7 MAJOR OPERATIONAL MODES 18
7.1 DS3/E3 FRAMED LIU MODE 18
7.2 DS3/E3 UNFRAMED LIU MODE 20
7.3 DS3/E3 FRAMED POS/NEG MODE 21
7.4 DS3/E3 UNFRAMED POS/NEG MODE 22
7.5 DS3/E3 FRAMED UNI MODE 23
7.6 DS3/E3 UNFRAMED UNI MODE 24
8 PIN DESCRIPTIONS 25
8.1 SHORT PIN DESCRIPTIONS 25
8.2 DETAILED PIN DESCRIPTIONS 27
8.3 PIN FUNCTIONAL TIMING 37
8.3.1 Line IO 37
8.3.2 DS3/E3 Framing Overhead Functional Timing 40
8.3.3 DS3/E3 Serial Data Interface 41
8.3.4 Microprocessor Interface Functional Timing 43
8.3.5 JTAG Functional Timing 50
9 INITIALIZATION AND CONFIGURATION 51
9.1 MONITORING AND DEBUGGING 52
10 FUNCTIONAL DESCRIPTION 53
10.1 PROCESSOR BUS INTERFACE 53
10.1.1 SPI Serial Port Mode 53
10.1.2 8/16 Bit Bus Widths 53
10.1.3 Ready Signal ($\overline{RDY}$) 53
10.1.4 Byte Swap Modes 53
10.1.5 Read-Write/Data Strobe Modes 53
10.1.6 Clear on Read/Clear on Write Modes 53
10.1.7 Interrupt and Pin Modes 54
10.1.8 Interrupt Structure 54
10.2 CLOCKS 55
10.2.1 Line Clock Modes 55
10.2.2 Sources of Clock Output Pin Signals 57

10.2.3 Line IO Pin Timing Source Selection 59
10.2.4 Clock Structures On Signal IO Pins 62
10.2.5 Gapped Clocks 63
10.3 RESET AND POWER-DOWN 63
10.4 GLOBAL RESOURCES 66
10.4.1 Clock Rate Adapter (CLAD) 66
10.4.2 8 kHz Reference Generation 66
10.4.3 One Second Reference Generation 67
10.4.4 General-Purpose IO Pins 68
10.4.5 Performance Monitor Counter Update Details 69
10.4.6 Transmit Manual Error Insertion 70
10.5 PORT RESOURCES 71
10.5.1 Loopbacks 71
10.5.2 Loss Of Signal Propagation 73
10.5.3 AIS Logic 73
10.5.4 Loop Timing Mode 75
10.5.5 HDLC Overhead Controller 75
10.5.6 Trail Trace 75
10.5.7 BERT 75
10.5.8 System Port Pins 76
10.5.9 Framing Modes 77
10.5.10 Line Interface Modes 77
10.6 DS3/E3 FRAMER / FORMATTER 79
10.6.1 General Description 79
10.6.2 Features 79
10.6.3 Transmit Formatter 80
10.6.4 Receive Framer 80
10.6.5 C-bit DS3 Framer/Formatter 84
10.6.6 M23 DS3 Framer/Formatter 87
10.6.7 G.751 E3 Framer/Formatter 89
10.6.8 G.832 E3 Framer/Formatter 91
10.7 HDLC OVERHEAD CONTROLLER 96
10.7.1 General Description 96
10.7.2 Features 97
10.7.3 Transmit FIFO 97
10.7.4 Transmit HDLC Overhead Processor 98
10.7.5 Receive HDLC Overhead Processor 98
10.7.6 Receive FIFO 99
10.8 TRAIL TRACE CONTROLLER 99
10.8.1 General Description 99
10.8.2 Features 100
10.8.3 Functional Description 100
10.8.4 Transmit Data Storage 101
10.8.5 Transmit Trace ID Processor 101
10.8.6 Transmit Trail Trace Processing 101
10.8.7 Receive Trace ID Processor 101
10.8.8 Receive Trail Trace Processing 101
10.8.9 Receive Data Storage 102
10.9 FEAC CONTROLLER 102
10.9.1 General Description 102
10.9.2 Features 103
10.9.3 Functional Description 103
10.10 LINE ENCODER/DECODER 104
10.10.1 General Description 104
10.10.2 Features 105
10.10.3 B3ZS/HDB3 Encoder 105
10.10.4 Transmit Line Interface 105
10.10.5 Receive Line Interface 106
10.10.6 B3ZS/HDB3 Decoder 106

10.11 BERT 108
10.11.1 General Description 108
10.11.2 Features 108
10.11.3 Configuration and Monitoring 108
10.11.4 Receive Pattern Detection 109
10.11.5 Transmit Pattern Generation 111
10.12 LIU – LINE INTERFACE UNIT 112
10.12.1 General Description 112
10.12.2 Features 112
10.12.3 Detailed Description 112
10.12.4 Transmitter 113
10.12.5 Receiver 114
11 OVERALL REGISTER MAP 117
12 REGISTER MAPS AND DESCRIPTIONS 119
12.1 REGISTERS BIT MAPS 119
12.1.1 Global Register Bit Map 119
12.1.2 HDLC Register Bit Map 121
12.1.3 T3 Register Bit Map 123
12.1.4 E3 G.751 Register Bit Map 124
12.1.5 E3 G.832 Register Bit Map 125
12.2 GLOBAL REGISTERS 126
12.2.1 Register Bit Descriptions 126
12.3 PORT REGISTER 133
12.3.1 Register Bit Descriptions 133
12.4 BERT 144
12.4.1 BERT Register Map 144
12.4.2 BERT Register Bit Descriptions 144
12.5 B3ZS/HDB3 LINE ENCODER/DECODER 151
12.5.1 Transmit Side Line Encoder/Decoder Register Map 151
12.5.2 Receive Side Line Encoder/Decoder Register Map 152
12.6 HDLC 156
12.6.1 HDLC Transmit Side Register Map 156
12.6.2 HDLC Receive Side Register Map 159
12.7 FEAC CONTROLLER 163
12.7.1 FEAC Transmit Side Register Map 163
12.7.2 FEAC Receive Side Register Map 165
12.8 TRAIL TRACE 168
12.8.1 Trail Trace Transmit Side 168
12.8.2 Trail Trace Receive Side Register Map 169
12.9 DS3/E3 FRAMER 174
12.9.1 Transmit DS3 174
12.9.2 Receive DS3 Register Map 176
12.9.3 Transmit G.751 E3 183
12.9.4 Receive G.751 E3 Register Map 186
12.9.5 Transmit G.832 E3 Register Map 191
12.9.6 Receive G.832 E3 Register Map 194
13 JTAG INFORMATION 202
13.1 JTAG DESCRIPTION 202
13.2 JTAG TAP CONTROLLER STATE MACHINE DESCRIPTION 203
13.3 JTAG INSTRUCTION REGISTER AND INSTRUCTIONS 205
13.4 JTAG ID CODES 206
13.5 JTAG FUNCTIONAL TIMING 207
13.6 IO PINS 207
14 PIN CONFIGURATIONS 208
15 DC ELECTRICAL CHARACTERISTICS 211
16 AC TIMING CHARACTERISTICS 213

16.1 FRAMER DATA PATH AC CHARACTERISTICS 215
16.2 OVERHEAD PORT AC CHARACTERISTICS 216
16.3 MICRO INTERFACE AC CHARACTERISTICS 217
16.3.1 SPI Bus Mode 217
16.3.2 Parallel Bus Mode 219
16.4 CLAD JITTER CHARACTERISTICS 222
16.5 LIU INTERFACE AC CHARACTERISTICS 222
16.5.1 Waveform Templates 222
16.5.2 LIU Input/Output Characteristics 225
16.6 JTAG INTERFACE AC CHARACTERISTICS 227
17 PACKAGE INFORMATION 228
18 THERMAL INFORMATION 229
19 REVISION HISTORY 230

LIST OF FIGURES

Figure 2-1. LIU External Connections for the DS3/E3 Port of DS3170 10
Figure 2-2. Block Diagram 11
Figure 3-1. DS3/E3 Line Card 12
Figure 7-1. DS3/E3 Framed LIU Mode 19
Figure 7-2. DS3/E3 Unframed LIU Mode 20
Figure 7-3. DS3/E3 Framed POS/NEG Mode 21
Figure 7-4. DS3/E3 Unframed POS/NEG Mode 22
Figure 7-5. DS3/E3 Framed UNI Mode 23
Figure 7-6. DS3/E3 Unframed UNI Mode 24
Figure 8-1. Tx Line IO B3ZS Functional Timing Diagram 37
Figure 8-2. Tx Line IO HDB3 Functional Timing Diagram 38
Figure 8-3. Rx Line IO B3ZS Functional Timing Diagram 38
Figure 8-4. Rx Line IO HDB3 Functional Timing Diagram 39
Figure 8-5. Tx Line IO UNI Functional Timing Diagram 39
Figure 8-6. Rx Line IO UNI Functional Timing Diagram 40
Figure 8-7. DS3 Framing Receive Overhead Port Timing 40
Figure 8-8. E3 G.751 Framing Receive Overhead Port Timing 40
Figure 8-9. E3 G.832 Framing Receive Overhead Port Timing 40
Figure 8-10. DS3 Framing Transmit Overhead Port Timing 41
Figure 8-11. E3 G.751 Framing Transmit Overhead Port Timing 41
Figure 8-12. E3 G.832 Framing Transmit Overhead Port Timing 41
Figure 8-13. DS3 Framed Mode Transmit Serial Interface Pin Timing 42
Figure 8-14. E3 G.751 Framed Mode Transmit Serial Interface Pin Timing 42
Figure 8-15. E3 G.832 Framed Mode Transmit Serial Interface Pin Timing 42
Figure 8-16. DS3 Framed Mode Receive Serial Interface Pin Timing 43
Figure 8-17. E3 G.751 Framed Mode Receive Serial Interface Pin Timing 43
Figure 8-18. E3 G.832 Framed Mode Receive Serial Interface Pin Timing 43
Figure 8-19. SPI Serial Port Access For Read Mode, SPI_CPOL=0, SPI_CPHA = 0 44
Figure 8-20. SPI Serial Port Access For Read Mode, SPI_CPOL = 1, SPI_CPHA = 0 44
Figure 8-21. SPI Serial Port Access For Read Mode, SPI_CPOL = 0, SPI_CPHA = 1 44
Figure 8-22. SPI Serial Port Access For Read Mode, SPI_CPOL = 1, SPI_CPHA = 1 44
Figure 8-23. SPI Serial Port Access For Write Mode, SPI_CPOL = 0, SPI_CPHA = 0 45
Figure 8-24. SPI Serial Port Access For Write Mode, SPI_CPOL = 1, SPI_CPHA = 0 45
Figure 8-25. SPI Serial Port Access For Write Mode, SPI_CPOL = 0, SPI_CPHA = 1 45
Figure 8-26. SPI Serial Port Access For Write Mode, SPI_CPOL = 1, SPI_CPHA = 1 45
Figure 8-27. 16-Bit Mode Write 46
Figure 8-28. 16-Bit Mode Read 46
Figure 8-29. 8-Bit Mode Write 47
Figure 8-30. 8-Bit Mode Read 47
Figure 8-31. 16-Bit Mode without Byte Swap 48
Figure 8-32. 16-Bit Mode with Byte Swap 48
Figure 8-33. Clear Status Latched Register on Read 49
Figure 8-34. Clear Status Latched Register on Write 49
Figure 8-35. $\overline{\text{RDY}}$ Signal Functional Timing Write 50
Figure 8-36. $\overline{\text{RDY}}$ Signal Functional Timing Read 50
Figure 10-1. Interrupt Structure 55
Figure 10-2. Internal Tx Clock 58
Figure 10-3. Internal Rx Clock 59
Figure 10-4. Example IO Pin Clock Muxing 63
Figure 10-5. Reset Sources 64
Figure 10-6. 8KREF Logic 67
Figure 10-7. Performance Monitor Update Logic 70
Figure 10-8. Transmit Error Insert Logic 71
Figure 10-9. Loopback Modes 72
Figure 10-10. ALB Mux 72
Figure 10-11. AIS Signal Flow 74
Figure 10-12. Framer Detailed Block Diagram 79

Figure 10-13. DS3 Frame Format 81
Figure 10-14. DS3 Subframe Framer State Diagram 81
Figure 10-15. DS3 Multiframe Framer State Diagram 82
Figure 10-16. G.751 E3 Frame Format 89
Figure 10-17. G.832 E3 Frame Format 92
Figure 10-18. MA Byte Format 92
Figure 10-19. HDLC Controller Block Diagram 97
Figure 10-20. Trail Trace Controller Block Diagram 100
Figure 10-21. Trail Trace Byte (DT = Trail Trace Data) 102
Figure 10-22. FEAC Controller Block Diagram 103
Figure 10-23. FEAC Codeword Format 104
Figure 10-24. Line Encoder/Decoder Block Diagram 105
Figure 10-25. B3ZS Signatures 107
Figure 10-26. HDB3 Signatures 107
Figure 10-27. BERT Block Diagram 108
Figure 10-28. PRBS Synchronization State Diagram 110
Figure 10-29. Repetitive Pattern Synchronization State Diagram 111
Figure 10-30. LIU Functional Diagram 112
Figure 10-31. DS3/E3 LIU Block Diagram 113
Figure 10-32. Receiver Jitter Tolerance 116
Figure 13-1. JTAG Block Diagram 202
Figure 13-2. JTAG TAP Controller State Machine 203
Figure 13-3. JTAG Functional Timing 207
Figure 14-1. DS3170 Pin Assignments—100-Ball CSBGA (Top View) 210
Figure 16-1. Clock Period and Duty Cycle Definitions 213
Figure 16-2. Rise Time, Fall Time, and Jitter Definitions 213
Figure 16-3. Hold, Setup, and Delay Definitions (Rising Clock Edge) 213
Figure 16-4. Hold, Setup, and Delay Definitions (Falling Clock Edge) 214
Figure 16-5. To/From Hi Z Delay Definitions (Rising Clock Edge) 214
Figure 16-6. To/From Hi Z Delay Definitions (Falling Clock Edge) 214
Figure 16-7. SPI Interface Timing Diagram 218
Figure 16-8. Micro Interface Nonmultiplexed Read/Write Cycle 220
Figure 16-9. Micro Interface Multiplexed Read Cycle 221
Figure 16-10. DS3 Pulse Mask Template 223
Figure 16-11. E3 Waveform Template 224

LIST OF TABLES

Table 5-1. Standards Compliance 16
Table 8-1. DS3170 Short Pin Descriptions 25
Table 8-2. Detailed Pin Descriptions 27
Table 9-1. Configuration of Port Register Settings 52
Table 10-1. LIU Enable Table 57
Table 10-2. All Possible Clock Sources Based on Mode and Loopback 57
Table 10-3. Source Selection of TLCLK Clock Signal 58
Table 10-4. Source Selection of TCLKO (Internal Tx Clock) 59
Table 10-5. Source Selection of RCLKO Clock Signal (Internal Rx Clock) 59
Table 10-6. Transmit Line Interface Signal Pin Valid Timing Source Select 60
Table 10-7. Transmit Framer Pin Signal Timing Source Select 61
Table 10-8. Receive Line Interface Pin Signal Timing Source Select 61
Table 10-9. Receive Framer Pin Signal Timing Source Select 62
Table 10-10. Reset and Power-Down Sources 65
Table 10-11. CLAD Clock Source Settings 66
Table 10-12. Global 8 kHz Reference Source Table 67
Table 10-13. Port 8 kHz Reference Source Table 67
Table 10-14. GPIO Global Signals 68
Table 10-15. GPIO Pin Global Mode Select Bits 68
Table 10-16. GPIO Port Alarm Monitor Select 69
Table 10-17. Loopback Mode Selections 71
Table 10-18. Line AIS Enable Modes 75
Table 10-19. Payload (Downstream) AIS Enable Modes 75
Table 10-20. TSOFI Input Pin Functions 76
Table 10-21. TSOFO/TDEN/Output Pin Functions 76
Table 10-22 TCLKO/TGCLK Output Pin Functions 76
Table 10-23. RSOFO/RDEN Output Pin Functions 77
Table 10-24. RCLKO/RGCLK Output Pin Functions 77
Table 10-25. Framing Mode Select Bits FM[2:0] 77
Table 10-26. Line Mode Select Bits LM[2:0] 78
Table 10-27. C-Bit DS3 Frame Overhead Bit Definitions 85
Table 10-28. M23 DS3 Frame Overhead Bit Definitions 87
Table 10-29. G.832 E3 Frame Overhead Bit Definitions 92
Table 10-30. Payload Label Match Status 96
Table 10-31. Pseudo-Random Pattern Generation 109
Table 10-32. Repetitive Pattern Generation 109
Table 10-33. Transformer Characteristics 114
Table 10-34. Recommended Transformers 115
Table 11-1. Register Address Map 117
Table 12-1. Global Register Bit Map 119
Table 12-2. Port Register Bit Map 119
Table 12-3. BERT Register Bit Map 120
Table 12-4. Line Register Bit Map 121
Table 12-5. HDLC Register Bit Map 121
Table 12-6. FEAC Register Bit Map 122
Table 12-7. Trail Trace Register Bit Map 123
Table 12-8. T3 Register Bit Map 123
Table 12-9. E3 G.751 Register Bit Map 124
Table 12-10. E3 G.832 Register Bit Map 125
Table 12-11. Global Register Map 126
Table 12-12. Port Register Map 133
Table 12-13. BERT Register Map 144
Table 12-14. Transmit Side B3ZS/HDB3 Line Encoder/Decoder Register Map 151
Table 12-15. Receive Side B3ZS/HDB3 Line Encoder/Decoder Register Map 152
Table 12-16. Transmit Side HDLC Register Map 156
Table 12-17. Receive Side HDLC Register Map 159
Table 12-18. FEAC Transmit Side Register Map 163

Table 12-19. FEAC Receive Side Register Map 165
Table 12-20. Transmit Side Trail Trace Register Map 168
Table 12-21. Trail Trace Receive Side Register Map 169
Table 12-22. Transmit DS3 Framer Register Map 174
Table 12-23. Receive DS3 Framer Register Map 176
Table 12-24. Transmit G.751 E3 Framer Register Map 183
Table 12-25. Receive G.751 E3 Framer Register Map 186
Table 12-26. Transmit G.832 E3 Framer Register Map 191
Table 12-27. Receive G.832 E3 Framer Register Map 194
Table 13-1. JTAG Instruction Codes 205
Table 13-2. JTAG ID Codes 206
Table 14-1. DS3170 Pin Assignments for 100-Ball CSBGA (Sorted by Signal Name) 208
Table 14-2. DS3170 Pin Assignments for 100-Ball CSBGA (Sorted by Ball #) 209
Table 15-1. Recommended DC Operating Conditions 211
Table 15-2. DC Electrical Characteristics 211
Table 15-3. Output Pin Drive 212
Table 16-1. Framer Interface Timing 215
Table 16-2. System Port Interface Timing 215
Table 16-3. Misc Timing 216
Table 16-4. Overhead Port Timing 216
Table 16-5. SPI Bus Mode Timing 217
Table 16-6. Micro Interface Timing 219
Table 16-7. DS3 Waveform Template 222
Table 16-8. DS3 Waveform Test Parameters and Limits 222
Table 16-9. E3 Waveform Test Parameters and Limits 223
Table 16-10. Receiver Input Characteristics—DS3 Mode 225
Table 16-11. Receiver Input Characteristics—E3 Mode 225
Table 16-12. Transmitter Output Characteristics—DS3 Modes 226
Table 16-13. Transmitter Output Characteristics—E3 Mode 226
Table 16-14. JTAG Interface Timing 227
Table 18-1. Thermal Information 229

1 DETAILED DESCRIPTION

The DS3170 is a software-configured, DS3/E3, single-chip transceiver (SCT). The line interface unit (LIU) has independent receive and transmit paths. The receiver LIU block performs clock and data recovery from a B3ZS- or HDB3-coded AMI signal and monitors for loss of the incoming signal, and can be bypassed for direct clock and data input. The receiver LIU block optionally performs B3ZS/HDB3 decoding. The transmitter LIU drives standard pulse-shape waveforms onto 75Ω coaxial cable and can be bypassed for direct clock and data output. The jitter attenuator can be put in the transmit or receive data path when the LIU is enabled. Built-in DS3/E3 framers transmit and receive data in properly formatted C-bit DS3, M23 DS3, G.751 E3 or G.832 E3 data streams. Functions not used are powered down to reduce system power requirements. The DS3170 conforms to the telecommunications standards listed in Table 5-1.

2 BLOCK DIAGRAMS

Figure 2-1 shows the external components required at the LIU interface for proper operation. Figure 2-2 shows the functional block diagram of the one channel DS3/E3 SCT.

Figure 2-1. LIU External Connections for the DS3/E3 Port of DS3170

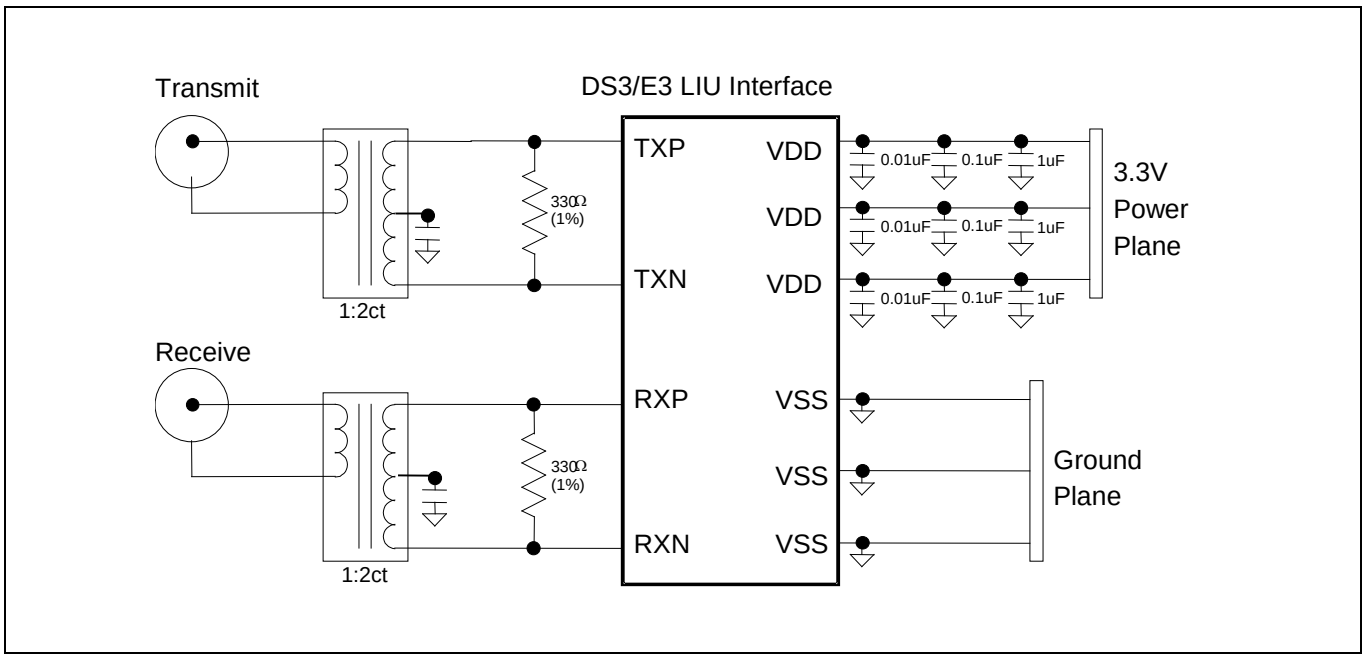
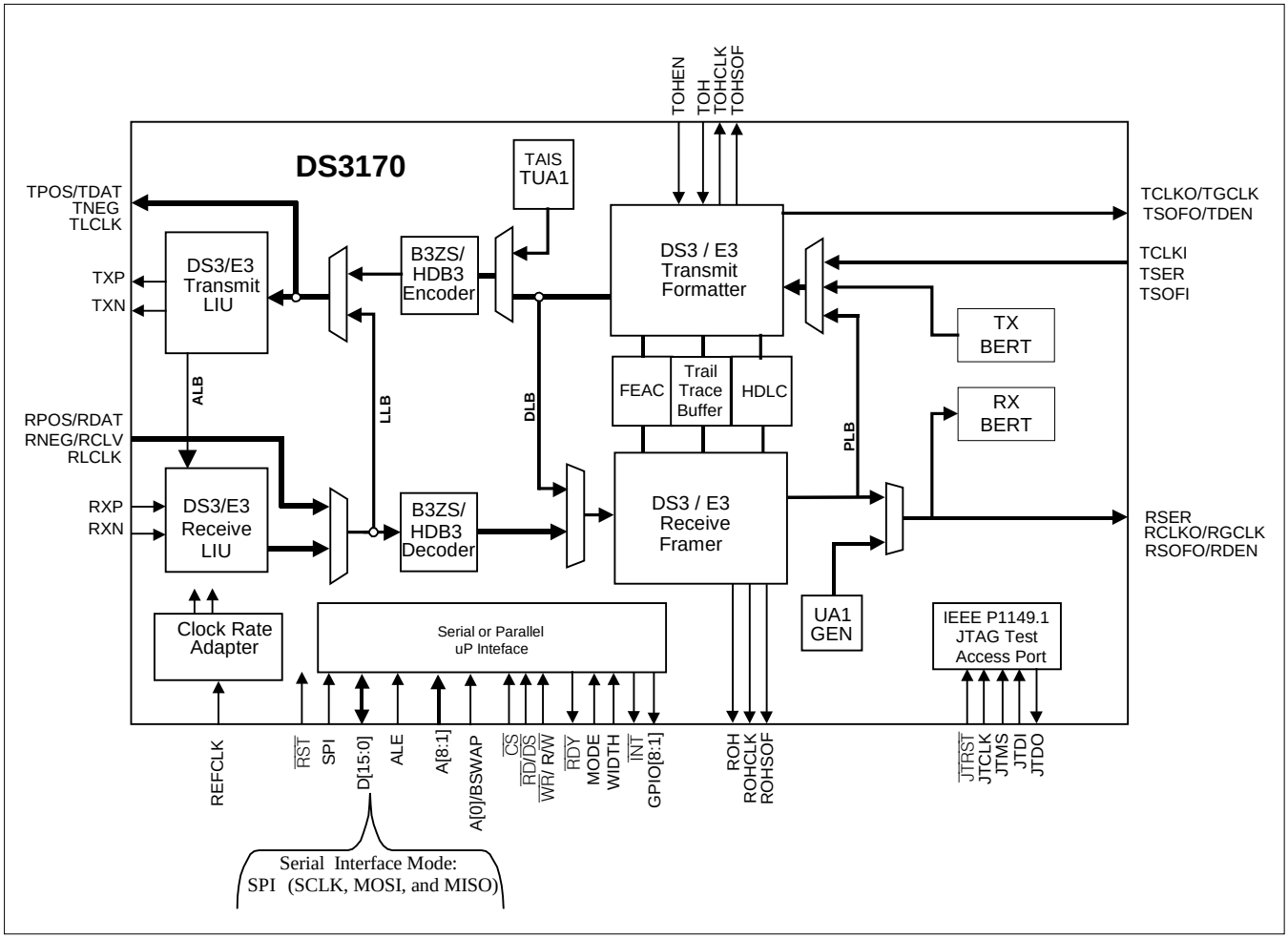


Figure 2-2. Block Diagram

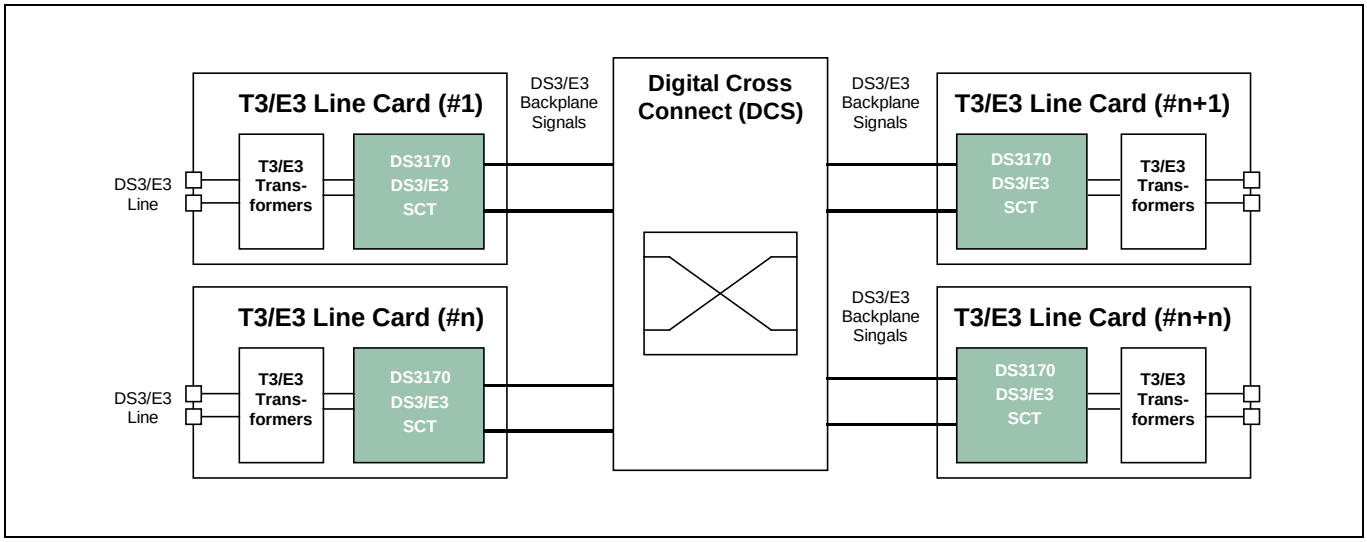


3 APPLICATIONS

- Access Concentrators
- Multiservice Access Platforms
- ATM and Frame Relay Equipment
- Routers and Switches
- SONET/SDH ADM
- SONET/SDH Muxes
- PBXs
- Digital Cross Connect
- PDH Multiplexer/Demultiplexer
- Test Equipment
- Integrated Access Device (IAD)

Figure 3-1 show s a DS3170 application.

Figure 3-1. DS3/E3 Line Card



4 FEATURE DETAILS

The following sections describe the features provided by the DS3170 SCT.

4.1 Global Features

- Supports the following transmission formats:
  - C-Bit DS3
  - M23 DS3
  - G.751 E3
  - G.832 E3
- All controls and status fields are software accessible over either an 8/16-bit microprocessor port or a slave serial bus communication port up to 10 Mbps (SPI)
- On-chip clock rate adapter incorporates two separate internal PLLs to generate the necessary DS3 or E3 clock used internally from an input clock reference (DS3, E3, 51.84 MHz, 77.76 MHz, or 19.44 MHz)
- Optional transmit loop timed clock mode using the receive clock
- Optional transmit clock mode using references generated by the internal Clock Rate Adapter (CLAD)
- Clock, data and control signals can be inverted to allow a glueless interface to other devices
- Detection of loss of transmit clock and loss of receive clock
- Supports gapped 52 MHz clock rates for signals embedded in SONET/SDH
- Jitter attenuator can be placed in either transmit or receive path when the LIU is enabled.
- Automatic one-second, external or manual update of performance monitoring counters
- Framing and line code error insertion available

4.2 Receive DS3/E3 LIU Features

- Performs equalization, gain control, and clock and data recovery for incoming DS3 and E3 signals
- AGC/Equalizer block handles from 0 dB to 15 dB of cable loss
- Interfaces directly to a DSX-3 monitor signal (20 dB flat loss) using built-in pre-amp
- Digital and analog Loss of Signal (LOS) detectors (ANSI T1.231 and ITU G.775)
- Loss-of-lock status indication for internal phase-locked loop

4.3 Jitter Attenuator Features

- Fully integrated, requires no external components
- Standards-compliant jitter attenuation/jitter transfer
- Can be inserted into the receive path or the transmit path
- 16-bit buffer depth

4.4 Receive DS3/E3 Framer Features

- B3ZS/HDB3 decoding
- Frame synchronization for M23 and C-bit Parity DS3, G.751 E3 and G.832 E3
- Detection of RAI, AIS, DS3 idle signal, loss of signal (LOS), severely errored framing event (SEFE), change of frame alignment (COFA), receipt of B3ZS/HDB3 codewords, DS3 application ID bit, DS3 M23/C-bit format mismatch, G.751 national bit, and G.832 RDI (FERF), payload type, and timing marker bits
- Detection and accumulation of bipolar violations (BPV), code violations (CV), excessive zeroes occurrences (EXZ), F-bit errors, M-bit errors, FAS errors, LOF occurrences, P-bit parity errors, CP-bit parity errors, BIP-8 errors, and far end block errors (FEBE)
- Manual or automatic one-second update of performance monitoring counters
- The E3 national bit (Sn) is forwarded to a status register bit, the HDLC controller or the FEAC controller
- HDLC controller with 256 byte FIFO for DS3 path maintenance data link (PMDL), G.751 national bit, or G.832 NR or GC channels
- FEAC controller with four-codeword FIFO for DS3 FEAC channel
- 16-byte Trail Trace Buffer compares and stores G.832 trail access point identifier
- DS3 M23 C-bits configurable as payload or overhead, stored in registers for software inspection
- Most framing overhead fields presented on the receive overhead port
- Framer pass-through mode for clear-channel applications and externally defined frame formats

4.5 Transmit DS3/E3 Formatter Features

- Frame insertion for M23 and C-bit parity DS3, G.751 E3 and G.832 E3
- B3ZS/HDB3 encoding
- Formatter pass-through mode for clear channel applications and externally defined frame formats
- Generation of RAI, AIS, DS3 idle signal, and G.832-E3 RDI
- Automatic or manual insertion of bipolar violations (BPVs), excessive zeroes (EXZ) occurrences, F-bit errors, M-bit errors, FAS errors, P-bit parity errors, CP-bit parity errors, BIP-8 errors, and far end block errors (FEBE)
- The E3 national bit (Sn) can be sourced from a control register, from the HDLC controller, or from the FEAC controller
- Most framing overhead fields can be sourced from transmit overhead port
- HDLC controller with 256 byte FIFO for DS3 path maintenance data link (PMDL), G.751 national bit, or G.832 NR or GC channels
- FEAC controller for DS3 FEAC channel can be configured to send one codeword, one codeword continuously, or two different codewords back-to-back to send DS3 Line Loopback commands
- 16-byte Trail Trace Buffer sources the G.832 trail access point identifier
- Insertion of G.832 payload type, and timing marker bits from registers
- DS3 M23 C-bits configurable as payload or overhead; as overhead they can be controlled from registers or the transmit overhead port

4.6 Transmit DS3/E3 LIU Features

- Drives standards-compliant DS3 and E3 waveshapes onto 75Ω coaxial cable
- Waveshape template compliance over all cable lengths without LBO adjustment
- Tri-state line driver outputs support protection switching applications
- Line driver monitor circuit and alarm output
- Wide 50±20% transmit clock duty cycle
- Line Build-Out (LBO) control
- Output driver monitor

4.7 Clock Rate Adapter Features

- Generation of the internally needed DS3 (44.736 MHz) and E3 (34.368 MHz) clocks a from single input reference clock
- Input reference clock can be 77.76 MHz, 51.84 MHz, 44.736MHz, 34.368 MHz, or 19.44 MHz
- Internally derived clock can be used as references for LIU and jitter attenuator
- Derived clock can be transmitted off-chip for external system use through TCLKO pin
- Standards-compliant jitter and wander requirements

4.8 HDLC Controller Features

- Designed to handle multiple LAPD messages without Host intervention
- 256 byte receive and transmit FIFOs are large enough to handle the three DS3 PMDL messages (Path ID, Idle Signal ID, and Test Signal ID) that are sent and received once per second
- Handles all of the normal Layer 2 tasks including zero stuffing/destuffing, FCS generation/checking, abort generation/checking, flag generation/detection, and byte alignment
- Programmable high or low water marks for the transmit and receive FIFOs
- Terminates the Path Maintenance Data Link in DS3 C-bit Parity mode or the G.751 Sn bit or the G.832 NR or GC channels

4.9 FEAC Controller Features

- Designed to handle multiple FEAC codewords without Host intervention
- Receive FEAC automatically validates incoming codewords and stores them in a 4-codeword FIFO
- Transmit FEAC can be configured to send one codeword, one codeword continuously, or two different codewords back-to-back to send DS3 Line Loopback commands
- Terminates the FEAC channel in DS3 C-Bit Parity mode or the Sn bit in E3 mode

4.10 Trail Trace Buffer Features

- Extraction and storage of the incoming G.832 trail access point identifier in a 16-byte receive register
- Insertion of the outgoing trail access point identifier from a 16-byte transmit register
- Receive trace identifier unstable status indication

4.11 Bit Error-Rate Tester (BERT) Features

- Generates and detects pseudo-random patterns and repetitive patterns from 1 to 32 bits in length
- Supports pattern insertion/extraction in DS3/E3 payload, or entire data stream
- Large 24-bit error counter allows testing to proceed for long periods without host intervention
- Errors can be inserted in the generated BERT patterns for diagnostic purposes (single bit errors or specific bit-error rates)
- Off-line monitoring on the Receive BERT

4.12 Loopback Features

- LIU terminal loopback (transmit to receive) - ALB
- Line facility loopback (receive to transmit) with optionally transmitting unframed all-one payload toward system/trunk interface - LLB
- Framer diagnostic loopback (transmit to receive) with optionally transmitting unframed all-one signal toward line/tributary interface - DLB
- Simultaneous line facility loopback (LLB) and framer diagnostic loopback (DLB)
- Framer payload loopback (receive to transmit) with optionally transmitting unframed all-one payload toward system/trunk interface - PLB

4.13 Microprocessor Interface Features

- Multiplexed or nonmultiplexed 8- or 16-bit control port
- Intel and Motorola bus compatible
- Global reset input pin
- Global interrupt output pin
- Eight programmable I/O pins (GPIOx)

4.14 Slave Serial Peripheral Interface (SPI) Features

- Three-wire synchronous serial data link operating in full duplex slave mode up to 10 Mbps
- Glueless connection and fully compliant to Motorola popular communication processors such as MPC8260 and microcontrollers such as M68HC11
- Software provision ability for active phase of the serial clock (i.e. rising edge versus falling edge), bit ordering of the serial data (most significant first versus least significant bit first)

4.15 Test Features

- Five pin JTAG port
- All functional pins are inout pins in JTAG mode
- Standard JTAG instructions: SAMPLE/PRELOAD, BYPASS, EXTEST, CLAMP, HIGHZ, IDCODE
- Custom JTAG instructions to use RAM BIST
- RAM BIST on all internal RAM
- HIZ pin to force all digital output and inout pins into HIZ
- TEST pin for manufacturing scan test modes

5 STANDARDS COMPLIANCE

Table 5-1. Standards Compliance

SPECIFICATION	SPECIFICATION TITLE
ANSI	
T1.102-1993	*Digital Hierarchy – Electrical Interfaces*
T1.107-1995	*Digital Hierarchy – Formats Specification*
T1.231-1997	*Digital Hierarchy – Layer 1 In-Service Digital Transmission Performance Monitoring*
T1.404-1994	*Network-to-Customer Installation – DS3 Metallic Interface Specification*
T1.646-1995	*Broadband ISDN – Physical Layer Specification for User-Network Interfaces Including DS1/ATM*
ATM Forum	
af-phy-0034.000	*E3 Public UNI,* August, 1995
af-phy-0054.000	*DS3 Physical Layer Interface Specification,* January, 1996
ETSI	
ETS 300 686	*Business TeleCommunications; 34Mbps and 140Mbits/s digital leased lines (D34U, D34S, D140U and D140S); Network interface presentation, 1996*
TBR 24	*Business TeleCommunications; 34Mbit/s digital unstructured and structured lease lines; attachment requirements for terminal equipment interface*, 1997
ETS EN 300 689	*Access and Terminals (AT); 34Mbps Digital Leased Lines (D34U and D34S); Terminal equipment interface,* July 2001
ETS 300 689	*Business TeleCommunications (BTC); 34 Mbps digital leased lines (D34U and D34S), Terminal equipment interface*, V 1.2.1, 2001-07
IETF	
RFC 2496	*Definition of Managed Objects for the DS3/E3 Interface Type*, January, 1999
ISO	
ISO 3309:1993	*Information Technology – Telecommunications & information exchange between systems – High Level Data Link Control (HDLC) procedures – Frame structure*, Fifth Edition, 1993
ITU-T	
G.703	*Physical/Electrical Characteristics of Hierarchical Digital Interfaces,* 1991
G.704	*Synchronous Frame Structures Used at 1544, 6312, 2048, 8488 and 44 736 kbit/s Hierarchical Levels,* July, 1995
G.751	*Digital Multiplex Equipment Operating at the Third Order Bit Rate of 34,368 kbit/s and the Fourth Order bit Rate of 139,264 kbit/s and Using Positive Justification,* 1993
G.775	*Loss Of Signal (LOS) and Alarm Indication Signal (AIS) Defect Detection and Clearance Criteria,* November, 1994
G.823	*The Control of Jitter and Wander Within Digital Networks Which are Based on the 2048 kbit/s Hierarchy*, 1993
G.824	*The Control of Jitter and Wander within Digital Networks that are Based on the 1544kbps Hierarchy*, 1993
G.832	*Transport of SDH Elements on PDH Networks – Frame and Multiplexing Structures,* November, 1995
I.432	*B-ISDN User-Network Interface – Physical Layer Specification,* March, 1993
O.151	*Error Performance Measuring Equipment Operating at the Primary Rate and Above,* October, 1992
Q.921	*ISDN User-Network Interface – Data Link Layer Specification*, March 1993
TELCORDIA	
GR-499-CORE	*Transport Systems Generic Requirements (TSGR): Common Requirements,* Issue 2, December 1998
GR-820-CORE	*Generic Digital Transmission Surveillance*, Issue 1, November 1994
IEEE	
IEEE Std 1149-1990	*IEEE Standard Test Access Port and Boundary-Scan Architecture, (Includes IEEE Std 1149-1993)* October 21, 1993

6 ACRONYMS AND GLOSSARY

Definition of the terms used in this data sheet:

- CCM—Clear-Channel Mode
- CLAD—Clock Rate Adapter
- Clear Channel—A Datastream with no framing included, also known as Unframed
- FRM—Frame Mode
- FSCT—Framer Single-Chip Transceiver Mode
- HDLC—High-Level Data-Link Control
- Packet—HDLC Packet
- SCT—Single-Chip Transceiver (Framer and LIU)
- SCT Mode—DS3/E3 Framer and LIU
- Unchannelized—See Clear Channel

7 MAJOR OPERATIONAL MODES

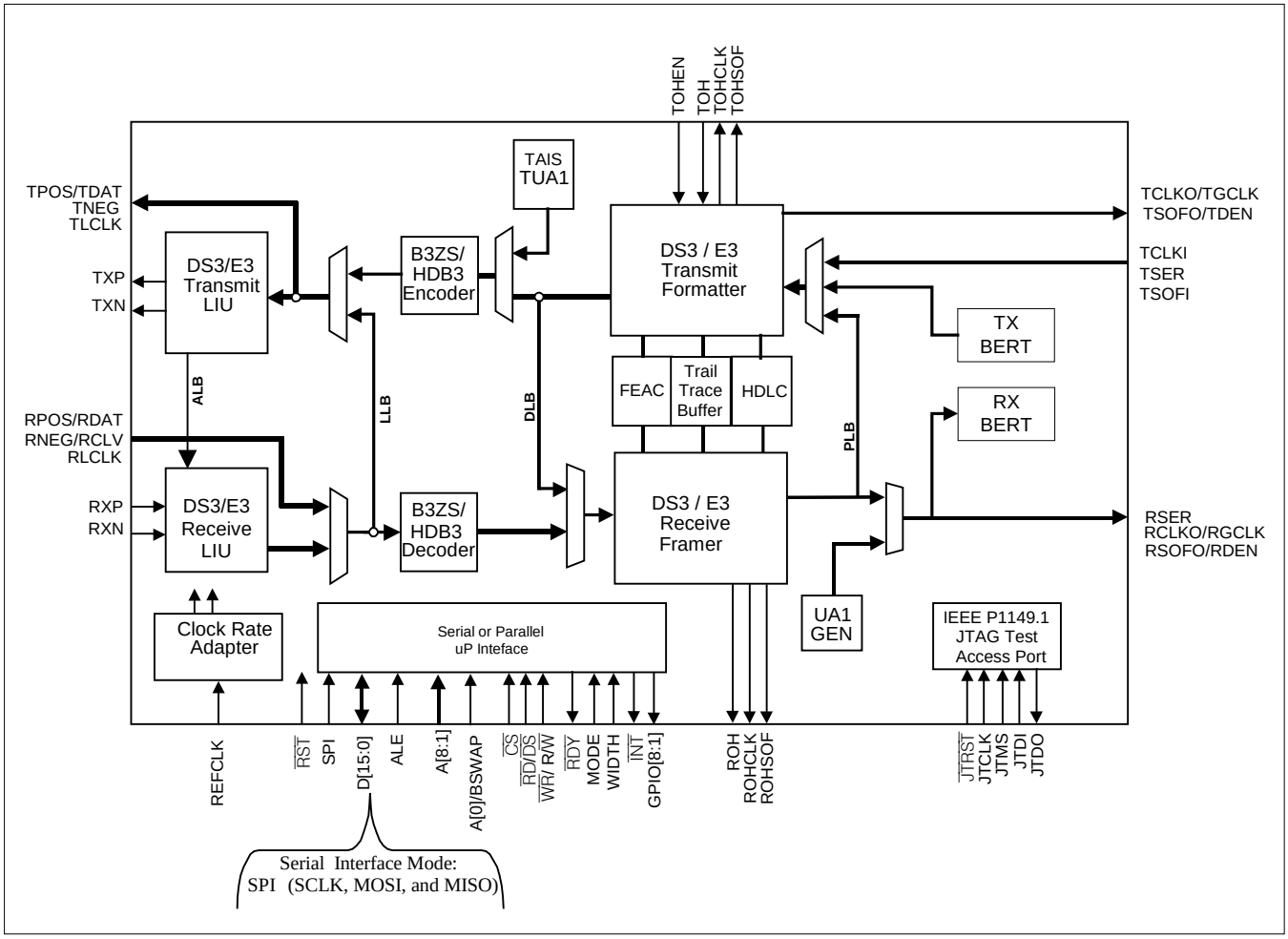
The major operational modes are determined by the FM[2:0] framer mode bits, as well as a few other control bits. Unused features are powered down and the data paths are held in reset. The configuration registers of the unused features can be written to and read from. Some of the IO pins change functions in different operational modes. The line interface operational modes are determined by the LM[2:0] bits.

7.1 DS3/E3 Framed LIU Mode

FRAME MODE	FM[2:0]
DS3 C-bit Framed	000
DS3 M23 Framed	001
E3 G.751 Framed	010
E3 G.832 Framed	011

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
JA Off, B3ZS or HDB3	001	0	0
JA RX, B3ZS or HDB3	010	0	0
JA TX, B3ZS or HDB3	011	0	0
JA Off, AMI	001	1	0
JA RX, AMI	010	1	0
JA TX, AMI	011	1	0

Figure 7-1. DS3/E3 Framed LIU Mode



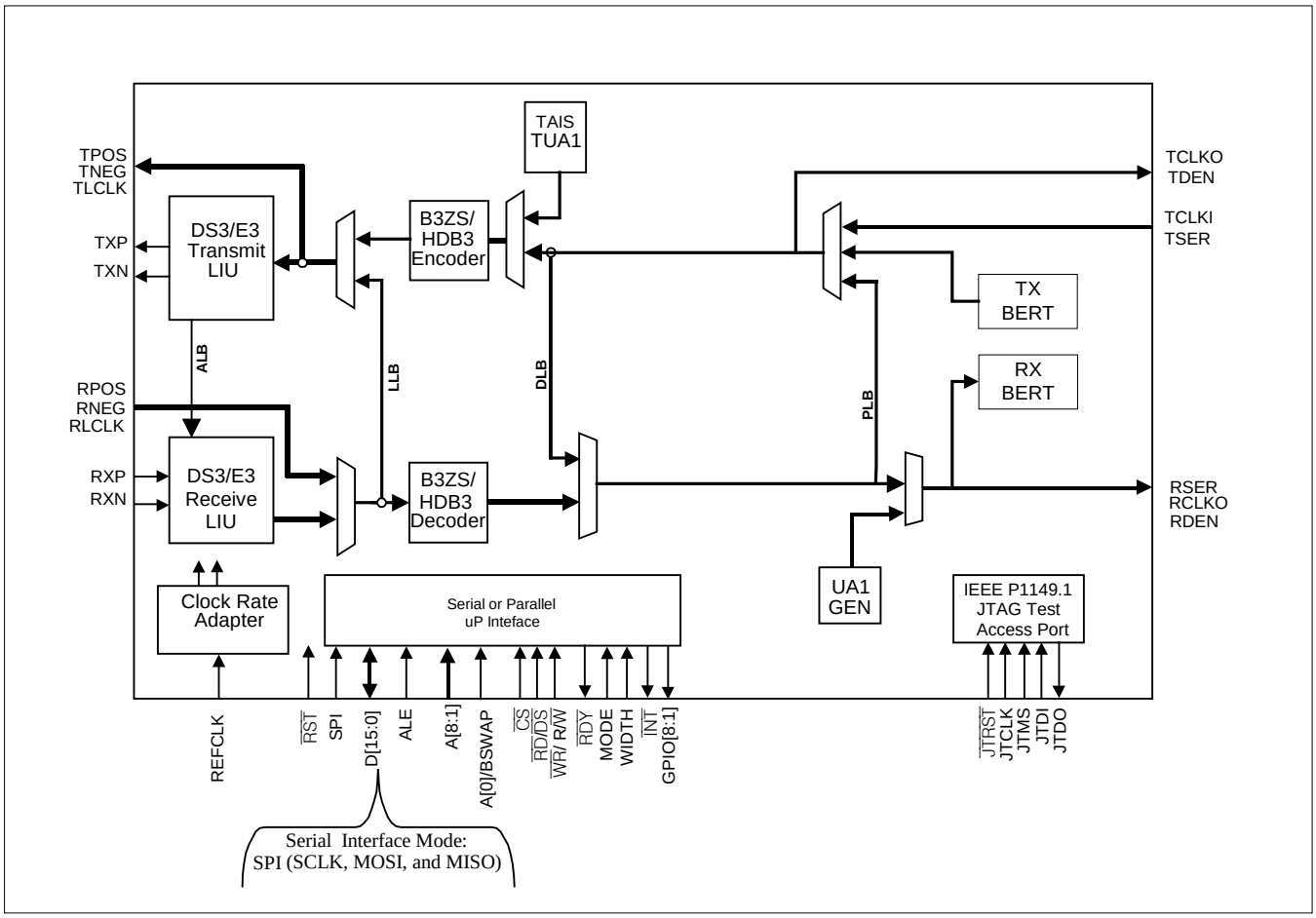
7.2 DS3/E3 Unframed LIU Mode

The frame mode determines the CLAD clock rate, LIU mode and selects B3ZS or HDB3.

FRAME MODE	FM[2:0]
DS3 Unframed	100
E3 Unframed	110

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
JA Off, B3ZS or HDB3	001	0	0
JA RX, B3ZS or HDB3	010	0	0
JA TX, B3ZS or HDB3	011	0	0
JA Off, AMI	001	1	0
JA RX, AMI	010	1	0
JA TX, AMI	011	1	0

Figure 7-2. DS3/E3 Unframed LIU Mode

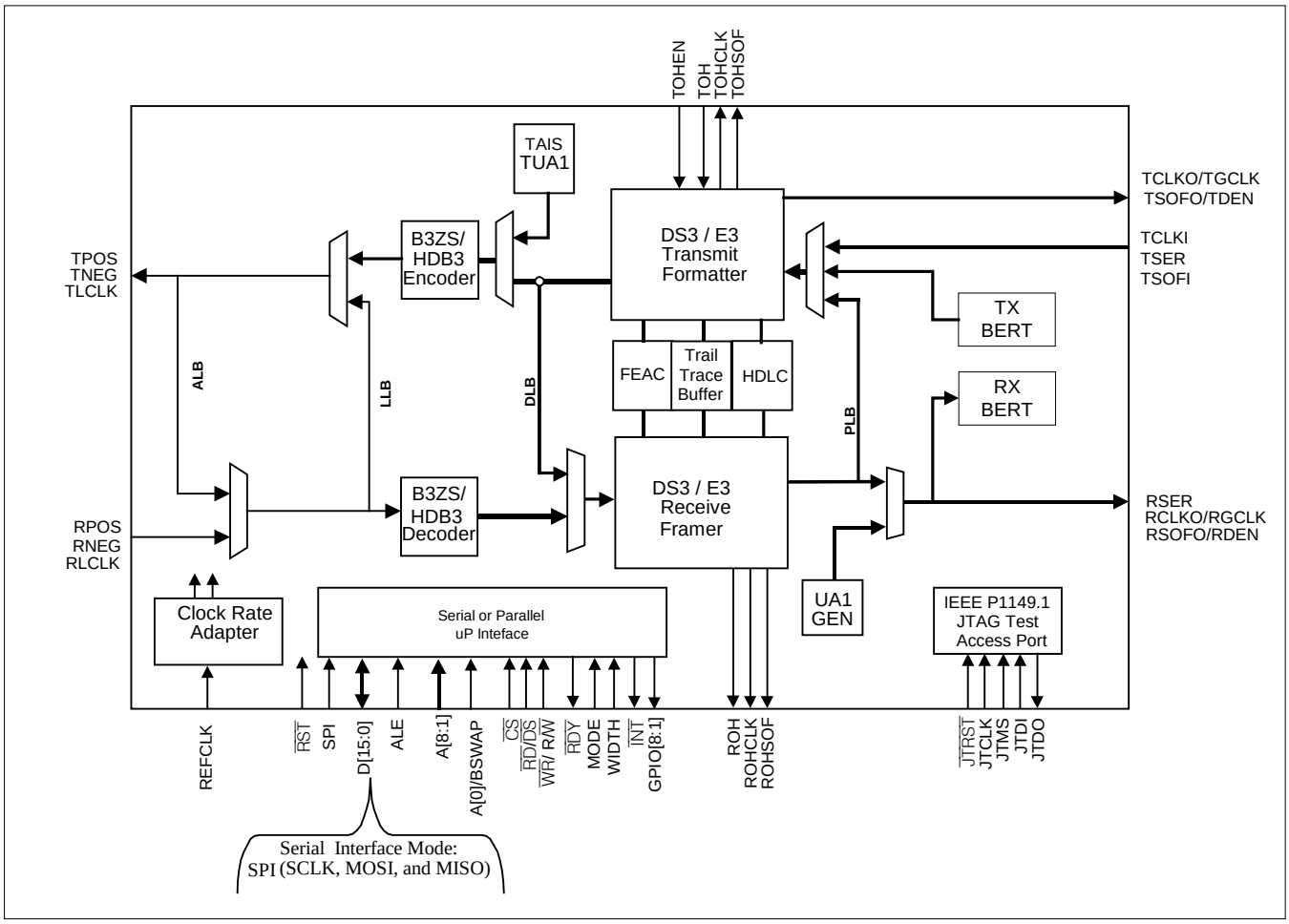


7.3 DS3/E3 Framed POS/NEG Mode

FRAME MODE	FM[2:0]
DS3 C-bit Framed	000
DS3 M23 Framed	001
E3 G.751 Framed	010
E3 G.832 Framed	011

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
LIU Off, B3ZS or HDB3	000	0	1
LIU Off, AMI	000	1	1

Figure 7-3. DS3/E3 Framed POS/NEG Mode



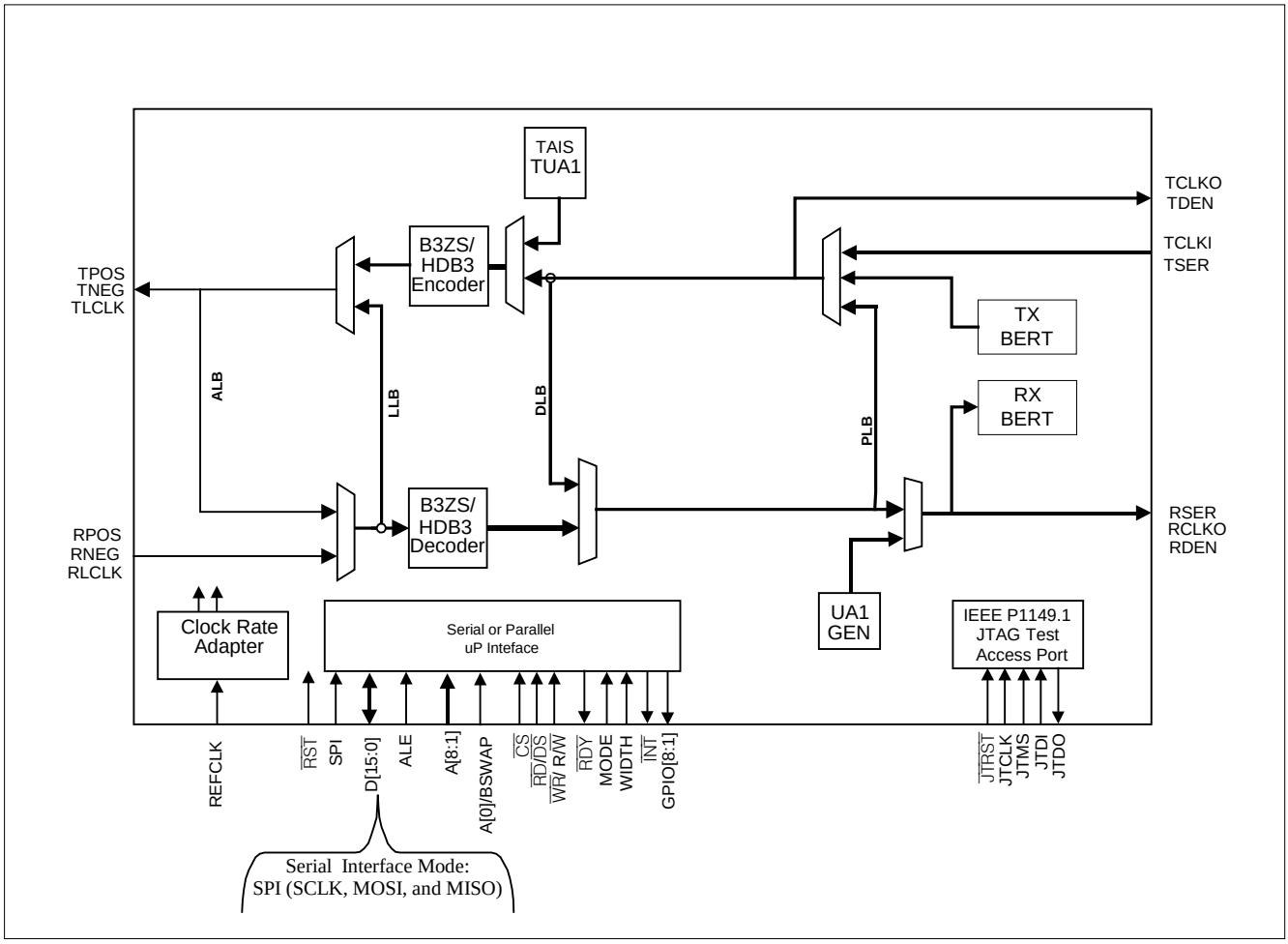
7.4 DS3/E3 Unframed POS/NEG Mode

The frame mode determines the CLAD clock rate if used as the transmit clock and selects B3ZS or HDB3.

FRAME MODE	FM[2:0]
DS3 Unframed	100
E3 Unframed	110

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
LIU Off, B3ZS or HDB3	000	0	1
LIU Off, AMI	000	1	1

Figure 7-4. DS3/E3 Unframed POS/NEG Mode

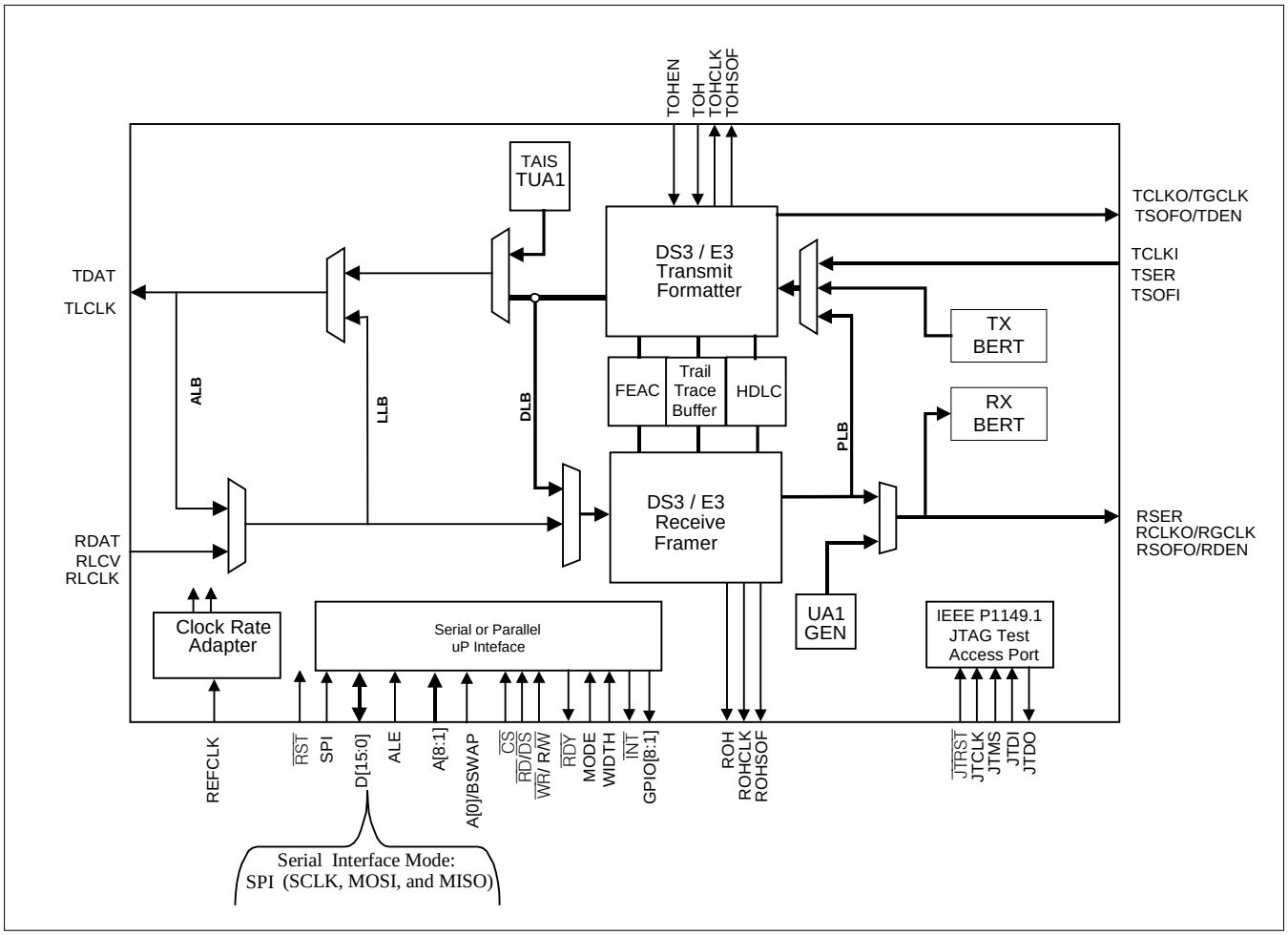


7.5 DS3/E3 Framed UNI Mode

FRAME MODE	FM[2:0]
DS3 C-bit Framed	000
DS3 M23 Framed	001
E3 G.751 Framed	010
E3 G.832 Framed	011

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
Unipolar Mode	1XX	X	1

Figure 7-5. DS3/E3 Framed UNI Mode



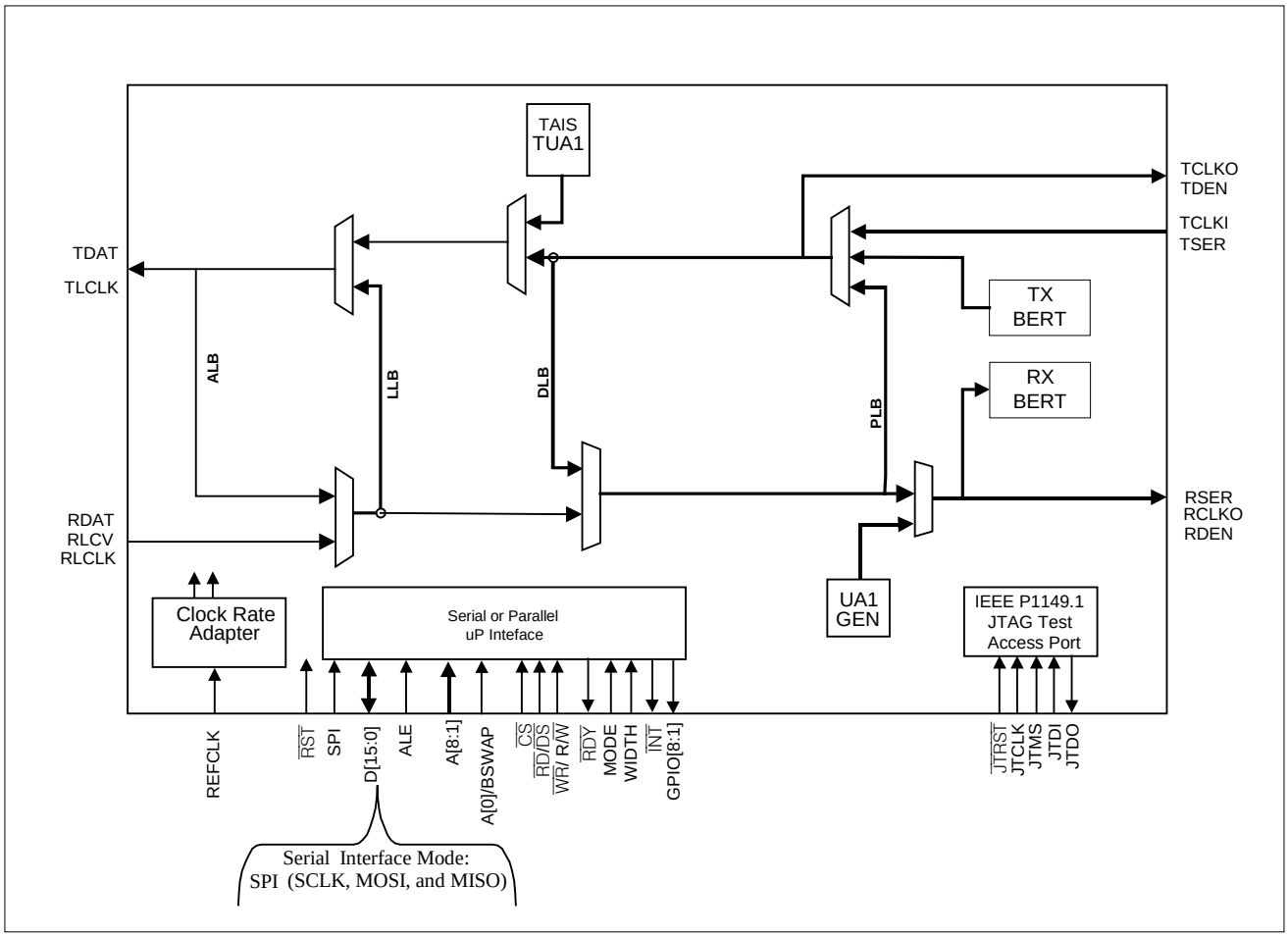
7.6 DS3/E3 Unframed UNI Mode

The frame mode determines the CLAD clock rate if used as the transmit clock.

FRAME MODE	FM[2:0]
DS3 Unframed	100
E3 Unframed	110

LIU MODE	LM[2:0]	TZSD & RZSD	TLEN PORT.CR2
Unipolar Mode	1XX	X	1

Figure 7-6. DS3/E3 Unframed UNI Mode



8 PIN DESCRIPTIONS

Note: In JTAG mode, all digital pins are bidirectional to increase the effectiveness of board level ATPG patterns for isolation of interconnect failures.

8.1 Short Pin Descriptions

Table 8-1. DS3170 Short Pin Descriptions

Ipu (input with pullup), Oz (output tri-stateable), Oa (Analog output), Ia (analog input), IO (Bidirectional in/out)

NAME	PIN	TYPE	FUNCTION
LINE I/O			
TLCLK	B7	O	Transmit Line Clock Output
TPOS/TDAT	E9	O	Transmit Positive AMI/Data
TNEG	D9	O	Transmit Negative AMI
TXP	E1, E2	Oa	Transmit Positive analog
TXN	F1, F2	Oa	Transmit Negative analog
RLCLK	A8	I	Receive Clock Input
RXP	A4	Ia	Receive Positive Analog
RXN	A3	Ia	Receive Negative Analog
RPOS/RDAT	F10	Ia	Positive AMI/Data
RNEG/RLCV	F9	Ia	Negative AMI/Line Code Violation
DS3/E3 OVERHEAD INTERFACE			
TOH	C7	I	Transmit Overhead
TOHEN	E10	I	Transmit Overhead Enable
TOHCLK	D7	O	Transmit Overhead Clock
TOHSOF	G9	O	Transmit Overhead Start Of Frame
ROH	B6	O	Receive Overhead
ROHCLK	C9	O	Receive Overhead Clock
ROHSOF	F8	O	Receive Overhead Start Of Frame
DS3/E3 SERIAL DATA			
TCLKI	C10	I	Transmit Line Clock Input
TSOFI	A9	I	Transmit Start Of Frame Input
TSER	B10	I	Transmit Serial Data
TCLKO/TGCLK	B9	O	Transmit Clock Output/Gapped Clock
TSOFO/TDEN	C8	O	Transmit Framer Start Of Frame/Data Enable
RSER	C6	O	Receive Serial Data
RCLKO/RGCLK	A6	O	Receive/Clock Output/Gapped Clock
RSOFO/RDEN	B8	O	Receive Framer Start Of Frame/Data Enable
MICROPROCESSOR INTERFACE			
D[15]	G8	IO	Data [15]
D[14]	H10	IO	Data [14]
D[13]	H9	IO	Data [13]
D[12]	H8	IO	Data [12]
D[11]	J10	IO	Data [11]
D[10]	J9	IO	Data [10]
D[9]	G6	IO	Data [9]

NAME	PIN	TYPE	FUNCTION
D[8]	J8	IO	Data [8]
D[7]/SPI_CPOL	K8	IO	Data [7]/SPI Interface Clock Polarity
D[6]/SPI_CPHA	H7	IO	Data [6]/SPI Interface Clock Phase
D[5]/SPI_SWAP	J7	IO	Data [5:3]/SPI Bit Order Swap
D[4]	K7	IO	Data [4]
D[3]	H6	IO	Data [3]
D[2]/SPI_SCLK	J6	IO	Data [2]/SPI Serial Interface Clock $\leq$ 10 MHz
D[1]/SPI_MOSI	K9	IO	Data [1] SPI Serial Interface Data Master Out-Slave In
D[0]SPI_MISO	J5	IO	Data [0]/SPI Serial Interface Data Master In-Slave Out
A[8:1]	H5, J4, H4, K3, J3, H3, K2, J2	I	Address [8:1]
A[0]/BSWAP	K5		Address [0]/Byte Swap mode
ALE	G4	I	Address Latch Enable
$\overline{CS}$	A1	I	Chip Select (active low)
$\overline{RD}/\overline{DS}$	B2	I	Read Strobe (Active Low) / Data Strobe (Active Low)
$\overline{WR}$/R/$\overline{W}$	C2	I	Write Strobe (Active Low)/R/W Select
$\overline{RDY}$	J1	Oz	Ready Handshake (Active Low)
$\overline{INT}$	D8	O	Interrupt (Open Drain Active Low)
MODE	F3	I	Mode Select (RD/WR or DS Strobe Mode)
WIDTH	H2	I	Width Select (8- or 16-Bit Interface)
SPI	C3	I	SPI Serial Bus Mode
MISC I/O			
GPIO[8:0|	D4, D3, G5, F6, G7, F7, E7, E8	IO	General-Purpose IO [8:1]
$\overline{TEST}$	F5	I	Test Enable (Active Low)
$\overline{HIZ}$	B4	I	High-Impedance Test Enable (Active Low)
$\overline{RST}$	E6	I	Reset (Active Low)
JTAG			
JTCLK	A5	I	JTAG Clock
JTMS	B3	Ipu	JTAG Mode Select (with Pullup)
JTDI	C4	Ipu	JTAG Data Input (with Pullup)
JTDO	D5	Oz	JTAG Data Output
$\overline{JTRST}$	E5	Ipu	JTAG Reset (Active Low with Pullup)
CLAD			
REFCLK	H1	I	Reference Clock
POWER			
V_{SS}	C1, K1, K6, G10, A10, A2	PWR	Ground, 0V Potential
V_{DD}	B1, D1, K4, K10, D10, A7	PWR	Digital 3.3V
AVDDR	C5	PWR	Analog 3.3V for Receive LIU
AVDDT	F4	PWR	Analog 3.3V for Transmit LIU

NAME	PIN	TYPE	FUNCTION
AVDDJ	E3	PWR	Analog 3.3V for Jitter Attenuator
AVDDC	G3	PWR	Analog 3.3V for CLAD
AVSSR	B5	PWR	Analog Ground for Receive LIU
AVSST	E4	PWR	Analog Ground for Transmit LIU
AVSSJ	D2	PWR	Analog Ground for Jitter Attenuator
AVSSC	G1	PWR	Analog Ground for CLAD
UNUSED			
UNUSED1	D6	N/A	Unused
UNUSED2	G2	N/A	Unused

8.2 Detailed Pin Descriptions

Table 8-2. Detailed Pin Descriptions

Ipu (input with pullup), Oz (output tri-stateable), Oa (Analog output), Ia (analog input), IO (Bidirectional inout)

PIN NAME	TYPE	PIN DESCRIPTION
		Line IO
TLCLK	O	Transmit Line Clock Output **TLCLK**: This signal is available when the transmit line interface pins are enabled (PORT.CR2.TLEN). This clock is typically used as the clock reference for the TDAT and TNEG signals, but can also be used as the reference for the TSOFI, TSER, and TSOFO / TDEN signals. This output signal can be inverted. o DS3: 44.736 MHz ±20 ppm o E3: 34.368 MHz ±20 ppm
TPOS / TDAT	O	Transmit Positive AMI / Data Output **TPOS**: When the port line interface is configured for B3ZS, HDB3 or AMI mode and the transmit line interface pins are enabled (PORT.CR2.TLEN), a high on this pin indicates that a positive pulse should be transmitted on the line. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TLCLK line clock output pins, but it can be referenced to the TCLKO, TCLKI, RLCLK or RCLKO pins. This output signal can be disabled when the TX LIU is enabled. This output signal can be inverted. **TDAT**: When the port line interface is configured for UNI mode and the transmit line interface pins are enabled (PORT.CR2.TLEN), the un-encoded transmit signal is output on this pin. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TLCLK line clock output pins, but it can be referenced to the TCLKO, TCLKI, RLCLK or RCLKO pins This output signal can be inverted. o DS3: 44.736 Mbps ±20ppm o E3: 34.368 Mbps ±20ppm

PIN NAME	TYPE	PIN DESCRIPTION
TNEG	O	Transmit Negative AMI / Line OH Mask **TNEG**: When the port line is configured for B3ZS, HDB3 or AMI mode and the transmit line interface pins are enabled (PORT.CR2.TLEN), a high on this pin indicates that a negative pulse should be transmitted on the line. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TLCLK line clock output pins, but it can be referenced to the TCLKO, TCLKI, RLCLK or RCLKO pins. This output signal can be inverted. o DS3: 44.736 Mbps ±20ppm o E3: 34.368 Mbps ±20ppm
TXP	Oa	Transmit Positive Analog **TXP**: This pin and the TXN pin form a differential AMI output which is coupled to the outbound 75Ω coaxial cable through a 2:1 step-down transformer (Figure 2-1). This output is enabled when the TX LIU is enabled and the output is enabled to be driven. When it is not enabled, it is in a high impedance state. o DS3: 44.736 Mbps ±20ppm o E3: 34.368 Mbps ±20ppm
TXN	Oa	Transmit Negative Analog **TXN**: This pin and the TXP pin form a differential AMI output which is coupled to the outbound 75Ω coaxial cable through a 2:1 step-down transformer (Figure 2-1). This output is enabled when the TX LIU is enabled and the output is enabled to be driven. When it is not enabled, it is in a high impedance state. o DS3: 44.736 Mbps ±20ppm o E3: 34.368 Mbps ±20ppm
RXP	Ia	Receive Positive analog **RXP**: This pin and the RXN pin form a differential AMI input which is coupled to the outbound 75Ω coaxial cable through a 2:1 step-up transformer (Figure 2-1). This input is used when the RX LIU is enabled and is ignored when the LIU is disabled. o DS3: 44.736 Mbps ±20ppm o E3: 34.368 Mbps ±20ppm
RXN	Ia	Receive Negative analog **RXN**: This pin and the RXP pin form a differential AMI input which is coupled to the outbound 75Ω coaxial cable through a 2:1 step-up transformer (Figure 2-1). This input is used when the LIU is enabled and is ignored when the LIU is disabled. o DS3: 44.736 Mbps ±20ppm o E3: 34.368 Mbps ±20ppm
RLCLK	I	Receive Line Clock Input **RLCLK**: This clock is typically used for the reference clock for the RPOS / RDAT, RNEG / RLCV signals but can also be used as the reference clock for the RSER, RSOFO / RDEN, TSOFI, TSER, TSOFO / TDEN, TPOS / TDAT and TNEG signals. This input is ignored when the LIU is enabled. This input signal can be inverted. o DS3: 44.736 MHz ±20 ppm o E3: 34.368 MHz ±20 ppm

PIN NAME	TYPE	PIN DESCRIPTION
RPOS / RDAT	Iad	Receive Positive AMI / Data **RPOS**: When the port line is configured for B3ZS, HDB3 or AMI mode and the LIU is disabled, a high on this pin indicates that a positive pulse has been detected using an external LIU. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the RLCLK line clock input pins, but it can be referenced to the RCLKO output pins. This input signal can be inverted. **RDAT**: When the port line interface is configured for UNI mode, the un-encoded receive signal is input on this pin. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the RLCLK line clock input pins, but it can be referenced to the RCLK output pins. This input signal can be inverted. o DS3: 44.736 Mbps ±20ppm o E3: 34.368 Mbps ±20ppm
RNEG / RLCV	Iad	Receive Negative AMI / Line Code Violation / Line OH Mask input **RNEG**: When the port line is configured for B3ZS, HDB3 or AMI mode and the LIU is disabled, a high on this pin indicates that a negative pulse has been detected using an external LIU. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the RLCLK line clock input pins, but it can be referenced to the RCLKO output pins. This input signal can be inverted. o DS3: 44.736 Mbps ±20ppm o E3: 34.368 Mbps ±20ppm **RLCV**: When the port line interface is configured for UNI mode, the BPV counter in the encoder/decoder block is incremented each clock when this signal is high. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the RLCLK line clock input pins, but it can be referenced to the RCLKO output pins. This input signal can be inverted.
DS3/E3 Overhead Interface		
TOH	I	Transmit Overhead **TOH**: When the port framer is configured for one of the DS3 or E3 framing modes, this signal will be used to over-write the DS3 or E3 framing overhead bits when TOHEN is active. In T3 mode, the X-bits, P-bits, M-bits, F-bits, and C-bits are input. In G.751 E3 mode, all of the FAS, RAI, and National Use bits are input. In G.832 E3 mode, all of the FA1, FA2, EM, TR, MA, NR, and GC bytes are input. The TOHSOF signal marks the start of the framing bit sequence. This signal is sampled at the same time as the TOHCLK signal transitions high to low. This signal can be inverted.
TOHEN	I	Transmit Overhead Enable / Start Of Frame Input **TOHEN**: When the port framer is configured for one of the DS3 or E3 framing modes, this signal will be used the determine which DS3 or E3 framing overhead bits to over-write with the signal on the TOH pin. The TOHSOF signal marks the start of the framing bit sequence. This signal is sampled at the same time as the TOHCLK signal transitions high to low. This signal can be inverted.

PIN NAME	TYPE	PIN DESCRIPTION
TOHCLK	O	Transmit Overhead Clock **TOHCLK**: When the port framer is configured for one of the DS3 or E3 framing modes, this clock is used for the transmit overhead port signals TOH, TOHEN and TOHSOF. The TOHSOF output signal is updated and the TOH and TOHEN input signals are sampled at the same time this clock signal transitions from high to low. The external logic is expected to sample TOHSOF signal and update the TOH and TOHEN signals on the rising edge of this clock signal. This clock is a low frequency clock. This signal can be inverted.
TOHSOF	O	Transmit Overhead Start Of Frame **TOHSOF**: When the port framer is configured for one of the DS3 or E3 framing modes, this signal is used to mark the start of a DS3 or E3 overhead sequence on the TOH pin. In T3 mode, the first X-bit is marked. In G.751 E3 mode, the first bit of the FAS word is marked. In G.832 E3 mode, the first bit of the FA1 byte is marked. The sequence starts on the same high to low transition of the TOHCLK clock that this signal is high. This signal is updated at the same time as the TOHCLK signal transitions high to low. This signal can be inverted.
ROH	O	Receive Overhead **ROH**: When the port framer is configured for one of the DS3 or E3 framing modes, this signal outputs the value of the receive overhead bits. The ROHSOF signal marks the start of the framing bit sequence. In T3 mode, the X-bits, P-bits, M-bits, F-bits, and C-bits are output (Note: In M23 mode, the C-bits are extracted even though they are marked as data at the payload interface). In G.751 E3 mode, all of the FAS, RAI, and National Use bits are output. In G.832 E3 mode, all of the FA1, FA2, EM, TR, MA, NR, and GC bytes are output. This signal is updated at the same time as the ROHCLK signal transitions high to low. This signal can be inverted.
ROHCLK	O	Receive Overhead Clock **ROHCLK**: When the port framer is configured for one of the DS3 or E3 framing modes, this clock is used for the receive overhead port signals ROH and ROHSOF. The ROHSOF and ROH output signals are updated at the same time this clock signal transitions from high to low. The external logic is expected to sample ROHSOF and ROH signal on the rising edge of this clock signal. This clock is a low frequency clock. This signal can be inverted.
ROHSOF	O	Receive Overhead Start Of Frame **ROHSOF**: When the port framer is configured for one of the DS3 or E3 framing modes this signal is used to mark the start of a DS3 or E3 overhead sequence on the ROH pins. In T3 mode, the first X-bit is marked. In G.751 E3 mode, the first bit of the FAS word is marked. In G.832 E3 mode, the first bit of the FA1 byte is marked. The sequence starts on the same high to low transition of the ROHCLK clock that this signal is high. This signal is updated at the same time as the ROHCLK signal transitions high to low. This signal can be inverted.
DS3/E3 Serial Data Overhead Interface		
TCLKI	I	Transmit Line Clock Input **TCLKI**: This clock is typically used for the reference clock for the TSOFI, TSER, and TSOFO / TDEN signals but can also be used as the reference for the TPOS / TDAT and TNEG signals. This clock is not used when the part is in loop time mode or the CLAD clocks are used as the transmit clock source. (*PORT.CR3*.CLADC) This input signal can be inverted. o DS3: 44.736 MHz ±20 ppm o E3: 34.368 MHz ±20 ppm

PIN NAME	TYPE	PIN DESCRIPTION
TSOFI	I	Transmit Start Of Frame Input See Table 10-20. **TSOFI**: This signal can be used to align the start of the DS3 or E3 frames on the TSER pin to an external signal. In framed modes, the TSOFI signal can be used to align the start of frame signal position on the TSER/TOH pin to the rising edge of a signal on this pin. The signal edge does not need to occur on every frame and can be tied high or low. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the TCLKI transmit clock input pins, but it can be referenced to the TLCLK, TCLKO, RCLKO and RLCLK clock pins. This signal can be inverted.
TSER	I	Transmit Serial Data **TSER**: When the port framer is configured for either the DS3 or E3 framed modes, this pin is used as the source of the DS3/E3 payload data. When the port is configured for a clear channel mode, this pin is used as the source of the DS3/E3 data signal. The signal is sampled on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is sampled on the falling edge of the clock. The signal is typically referenced to the TCLKI transmit clock input pins, but it can be referenced to the TLCLK, TCLKO / TGCLK, RCLKO and RLCLK clock pins This signal can be inverted. o DS3: 44.736 Mbps ±20ppm o E3: 34.368 Mbps ±20ppm
TCLKO / TGCLK	O	Transmit Clock Output / Gapped Clock See Table 10-22. **TCLKO**: When TCLKO is selected by PORT.CR3.TCLKS, this clock output is enabled. This clock is the same clock as the internal framer transmit clock. This clock is typically used for the reference clock for the TSOFI, TSER, and TSOFO / TDEN signals but can also be used as the reference for the TPOS / TDAT and TNEG signals. This signal can be inverted. o DS3: 44.736 MHz ±20 ppm o E3: 34.368 MHz ±20 ppm **TGCLK**: When TGCLK is selected by PORT.CR3.TCLKS, this gated output clock is enabled. This gapped clock is the same clock as the internal framer transmit clock and is gated by TDEN. This clock is typically used for the reference clock for the TSER signal. This signal can be inverted.

PIN NAME	TYPE	PIN DESCRIPTION
TSOFO / TDEN	O	Framer Start Of Frame / Data Enable See Table 10-21. **TSOFO**: When the port framer is configured for the DS3 or E3 framed modes and the TSOFO pin function is selected, this signal is used to indicate the start of the DS3/E3 frame on the TSER pin. This signal pulses high three clocks before the first overhead bit in a DS3 or E3 frame that will be input on TSER. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TCLKI transmit clock input pins, but it can be referenced to the TLCLK, TCLKO, RCLKO and RLCLK clock pins. This signal can be inverted. **TDEN**: When the port framer is configured for the DS3 or E3 framed modes and the TDEN pin function is selected, this signal is used to mark the DS3/E3 frame bits on the TSER pin. The signal goes high three clocks before the start of DS3/E3 payload bits and goes low three clocks before the end of the DS3/E3 payload bits. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the TCLKI transmit clock input pins, but it can be referenced to the TLCLK, TCLKO, RCLKO and RLCLK clock pins. This signal can be inverted.
RSER	O	Receive Serial Data **RSER**: When the port framer is configured for the DS3 or E3 framed modes, this pin outputs the receive data signal from the LIU or receive line pins. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the RCLKO receive clock output pin, but it can be referenced to the RGCLK and RLCLK clock pins. This signal can be inverted o DS3: 44.736 Mbps ±20ppm o E3: 34.368 Mbps ±20ppm
RCLKO / RGCLK	O	Receive Clock Output / Gapped Clock See Table 10-24. **RCLKO**: When the port framer is configured for the DS3 or E3 framed modes and RCLKO is selected, this clock output signal is active. It is the same as the internal receive framer clock. This clock is typically used for the reference clock for the RSER, RSOFO / RDEN signals but can also be used as the reference for the RPOS / RDAT, RNEG / RLCV, TSOFI, TSER, TSOFO / TDEN, TPOS / TDAT and TNEG signals. This signal can be inverted. o DS3: 44.736 MHz ±20 ppm o E3: 34.368 MHz ±20 ppm **RGCLK**: When the port is configured for DS3/E3 framed mode and RGCLK is selected, this gated clock output signal is active. It is the same as the internal receive framer clock gated by RDEN. This clock is typically used for the reference clock for the RSER. This signal can be inverted
RSOFO / RDEN	O	Receive Framer Start Of Frame /Data Enable See Table 10-23. **RSOFO**: When the port framer is configured for the DS3 or E3 framed modes and the RSOFO pin function is enabled, this signal is used to indicate the start of the DS3/E3 frame. This signal indicates the first DS3/E3 overhead bit on the RSER pin when high. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the RCLKO receive clock output pin, but it can be referenced to the RLCLK clock input pin. This signal can be inverted. **RDEN**: When the port framer is configured for the DS3 or E3 framed modes and the RDEN pin function is enabled, this signal is used to indicate the DS3/E3 payload bit

PIN NAME	TYPE	PIN DESCRIPTION
		positions of the data on the RSER pin. The signal goes high during each DS3/E3 payload bit and goes low during each DS3/E3 overhead bit. The signal is updated on the positive clock edge of the referenced clock pin if the clock pin signal is not inverted, otherwise it is updated on the falling edge of the clock. The signal is typically referenced to the RCLKO receive clock output pin, but it can be referenced to the RLCLK clock input pin. This signal can be inverted.
Microprocessor Interface		
D[15:8]	IO	Upper 8 Bits of the Bi-directional 16 or 8 bit data bus **D[15:8]**: Upper bits of the 16-bit or 8-bit data bus used to input data during register writes, and data outputs during register reads. The upper 8 bits are not used in 8 bit bus mode. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0.
D[7]/ SPI_CPOL	IO	Bit 7 of Bi-directional data bus / SPI Bus Clock Polarity **D[7]**: Bit 7 of the 16-bit or 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_CPOL:** This signal selects the clock polarity when SPI = 1. See Section **8.3.4.1** for detailed timing and functionality information. Default setting is low.
D[6]/ SPI_CPHA	IO	Bit 6 of Bi-directional data bus / SPI Bus Clock Phase **D[6]**: Bit 6 of the 16-bit or 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_CPHA:** This signal selects the clock phase when SPI = 1. See Section **8.3.4.1** for detailed timing and functionality information. Default setting is low.
D[5]/ SPI_SWAP	IO	Bit 5 of Bi-directional data bus / SPI Bit Order Swap **D[5]**: Bit 5 of the 16-bit or 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_SWAP**: This signal is active when SPI=1. The address and data bit order is swapped when SPI_SWAP is high. The R/W and B bit positions are never changed in the control word. 0 = MSB is transmitted and received first. 1 = LSB is transmitted and received first.
D[4:3]	IO	Bits 4,3 of Bi-directional data bus **D[4:3]**: Bits 3,4 of the 16-bit or 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0.
D[2]/ SPI_SCLK	IO	Bit 2 of Bi-directional data bus / SPI Serial Clock Input $\leq$ 10 MHz **D[2]**: Bit 2 of the 16-bit or 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_SCLK:** SPI Serial Clock Input when SPI = 1.
D[1]/ SPI_MOSI	IO	Bit 1 of Bi-directional data bus / SPI Serial Bus Master-out Slave-in **D[1]**: Bit 1 of the 16-bit or 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_MOSI:** SPI Serial Data Input (Master-out Slave-in) when SPI = 1.
D[0]/ SPI_MISO	IO	Bit 0 of Bi-directional data bus / SPI Serial Bus Master-in Slave-out **D[0]**: Bit 0 of the 16-bit or 8-bit data bus used to input data during register writes, and data outputs during register reads. Not driven when $\overline{CS}$=1 or $\overline{RST}$=0. **SPI_MISO:** SPI Serial Data Output (Master-in Slave-Out) when SPI = 1.
A[8:1]	I	Address bus (minus LSB) / Device Address [8:1] **A[8:1]**: identifies the specific 16 bit registers, or group of 8 bit registers, being accessed.
A[0] / BSWAP		Address bus LSB / Byte Swap / Device Address [0] **A[0]**: This signal is connected to the lower address bit in 8 bit systems. (WIDTH=0) 1 = Output register bits 15:8 on D[7:0], D[15:8] not driven 0 = Output register bits 7:0 on D[7:0], D[15:8] not driven **BSWAP**: This signal is tied high or low in 16 bit systems. (WIDTH=1) 1 = Output register bits 15:8 on D[7:0], 7:0 on D[15:8] 0 = Output register bits 7:0 on D[7:0], 15:8 on D[15:8]
ALE	I	Address Latch Enable **ALE**: This signal is used to latch the address on the A[10:0] pins in multiplexed

PIN NAME	TYPE	PIN DESCRIPTION
		address systems. When it is high the address is fed through the address latch to the internal logic. When it transitions to low, the address is latched and held internally until the signal goes back high. ALE should be tied high for nonmultiplexed address systems.
$\overline{CS}$	I	Chip Select (active low) $\overline{CS}$: This signal must be low during all accesses to the registers
$\overline{RD}$ / $\overline{DS}$	I	Read Strobe (active low) / Data Strobe (active low) $\overline{RD}$: Read Strobe mode (MODE=0): $\overline{RD}$ is low during a register read. $\overline{DS}$: Data Strobe mode (MODE=1): $\overline{DS}$ is low during either a register read or a write.
$\overline{WR}$ / R/$\overline{W}$	I	Write Strobe (active low) / R/W Select $\overline{WR}$: Write Strobe mode (MODE=0): $\overline{WR}$ is low during a register write. **R/$\overline{W}$**: Data Strobe mode (MODE=1): R/$\overline{W}$ is high during a register read cycle, and low during a register write cycle.
$\overline{RDY}$	Oz	Ready handshake (active low) $\overline{RDY}$: This ready signal is driven low when the current read or write cycle can progress. When the current read or write cycle is not ready it is driven high. When device is not selected it is not driven. Not driven when $\overline{RST}$=0 or $\overline{CS}$=1.
$\overline{INT}$	Oz	Interrupt (active low) $\overline{INT}$: This interrupt signal is driven low when an event is detected on any of the enabled interrupt sources in any of the register banks. When there are no active and enabled interrupt sources, the pin can be programmed to either drive high or not drive high. The reset default is to not drive high when there are no active and enabled interrupt source. All interrupt sources are disabled when $\overline{RST}$ =0 and they must be programmed to be enabled. Not driven when $\overline{RST}$=0.
MODE	I	Mode select $\overline{RD}$/$\overline{WR}$ or $\overline{DS}$ strobe mode **MODE**: 1 = Data Strobe Mode, 0 = Read/Write Strobe Mode
WIDTH	I	Data bus width select 8 or 16-bit interface **WIDTH**: 1 = 16-bits, 0 = 8 bits
SPI	I	SPI Serial Bus Mode Select **SPI**: 1 = SPI Serial Bus Mode, 0 = Parallel Bus Mode
Misc I/O		
GPIO1	IO	General Purpose IO 1 **GPIO1**: This signal is configured to be a general purpose IO pin, or an alarm output signal.
GPIO2	IO	General Purpose IO 2 **GPIO2**: This signal is configured to be a general purpose IO pin, or the 8KREFO output signal, or an alarm output signal.
GPIO3	IO	General Purpose IO 3 **GPIO3**: This signal is configured to be a general purpose IO pin.
GPIO4	IO	General Purpose IO 4 **GPIO4**: This signal is configured to be a general purpose IO pin, or the 8KREFI input signal. When configured for 8KREFI mode the signal frequency should be 8,000 Hz +/- 500 ppm and about 50% duty cycle.
GPIO5	IO	General Purpose IO 5 **GPIO5**: This signal is configured to be a general purpose IO pin, or an alarm output signal.
GPIO6	IO	General Purpose IO 6 **GPIO6**: This signal is configured to be a general purpose IO pin, or the TMEI input signal. When configured for TMEI input, the signal low time and high time must be greater than 500 nsec.
GPIO7	IO	General Purpose IO 7

PIN NAME	TYPE	PIN DESCRIPTION
		GPIO7: This signal is configured to be a general purpose IO pin.
GPIO8	IO	General Purpose IO 8 **GPIO8**: This signal is configured to be a general purpose IO pin, or the PMU input signal. When configured for PMU input, the signal low time and high time must be greater than 500 nsec.
$\overline{\text{TEST}}$	I	Test enable (active low) $\overline{\text{TEST}}$: This signal enables the internal scan test mode when low. For normal operation tie high. This is an asynchronous input.
$\overline{\text{HIZ}}$	I	High impedance test enable (active low) $\overline{\text{HIZ}}$: This signal puts all digital output and bi-directional pins in the high impedance state when it low and $\overline{\text{JTRST}}$ is low. For normal operation tie high. This is an asynchronous input.
$\overline{\text{RST}}$	I	Reset (active low) $\overline{\text{RST}}$: This signal resets all the internal processor registers and logic when low. This pin should be low while power is applied and set high after the power is stable. This is an asynchronous input.
		JTAG
JTCLK	I	JTAG Clock **JTCLK**: This clock input is typically a low frequency (less than 10 MHz) 50% duty cycle clock signal.
JTMS	Ipu	JTAG Mode Select (with pullup) **JTMS**: This input signal is used to control the JTAG controller state machine and is sampled on the rising edge of JTCLK.
JTDI	Ipu	JTAG Data Input (with pullup) **JTDI**: This input signal is used to input data into the register that is enabled by the JTAG controller state machine and is sampled on the rising edge of JTCLK.
JTDO	Oz	JTAG Data Output **JTDO**: This output signal is the output of an internal scan shift register enabled by the JTAG controller state machine and is updated on the falling edge of JTCLK. The pin is in the high impedance mode when a register is not selected or when the $\overline{\text{JTRST}}$ signal is high. The pin goes into and exits the high impedance mode after the falling edge of JTCLK
$\overline{\text{JTRST}}$	Ipu	JTAG Reset (active low with pullup) $\overline{\text{JTRST}}$: This input forces the JTAG controller logic into the reset state and forces the JTDO pin into high impedance when low. This pin should be low while power is applied and set high after the power is stable. The pin can be driven high or low for normal operation, but must be high for JTAG operation.
		CLAD
REFCLK	I	Reference Clock **CLKI**: This pin must have a clock which is either 44.736 MHz, 34.368 MHz, 77.76 MHz, 51.84 MHz or 19.44 MHz +/- 20 ppm and transmission quality jitter and wander. No IO pins have a timing relationship to this pin.
		POWER
VSS	PWR	Ground, 0 Volt potential Common to digital core, digital IO and all analog circuits
VDD	PWR	Digital 3.3V Common to digital core and digital IO
AVDDR	PWR	Analog 3.3V for receive LIU Powers receive LIU
AVDDT	PWR	Analog 3.3V for transmit LIU Powers transmit LIU
AVDDJ	PWR	Analog 3.3V for jitter attenuator Powers jitter attenuator
AVDDC	PWR	Analog 3.3V for CLAD Powers clock rate adapter

PIN NAME	TYPE	PIN DESCRIPTION
AVSSR	PWR	Analog Ground for receive LIU
AVSST	PWR	Analog Ground for transmit LIU
AVSSJ	PWR	Analog Ground for jitter attenuator
AVSSC	PWR	Analog Ground for CLAD

8.3 Pin Functional Timing

8.3.1 Line IO

8.3.1.1 B3ZS/HDB3/AMI Mode Transmit Pin Functional Timing

There is no suggested time alignment between the TXP, TXN and TX LINE signals and the TLCLK clock signal. The TX DATA signal is not a readily available signal, it is meant to represent the data value of the other signals.

The TXP and TXN signals are only available when the line is in B3ZS/HDB3 or AMI mode and the LIU is enabled. The TPOS, TNEG and TLCLK signals are only available when the line is in B3ZS/HDB3 or AMI mode and the transmit line pins are enabled. The TPOS, TNEG and TLCLK pins can be enabled at the same as the LIU is enabled.

The TPOS and TNEG signals change a small delay after the positive edge of the reference clock if the clock pin is not inverted, otherwise they change after the negative edge. The TLCLK clock pin is the clock reference typically used for the TPOS and TNEG signals, but they can be time referenced to the TCLKI, TCLKO, RLCLK or RCLKO clock pins. The TPOS and TNEG pins can be inverted, but the polarity of TXP and TXN can not be inverted.

TXP and TXN are differential analog output pins. They are biased around ½ VDD and pulse above and below the bias voltage by about 1 Volt. These signals are connected to the windings of a 1:2 step down transformer and the other winding of the transformer creates the TX LINE signal. The TX LINE signal is a bipolar signal that pulses about 1 Volt positive and 1 Volt negative above and below ground (0 volts). See Figure 2-1 for a diagram of the external connections.

Figure 8-1 and Figure 8-2 show the relationship between the analog and the digital outputs.

Figure 8-1. Tx Line IO B3ZS Functional Timing Diagram

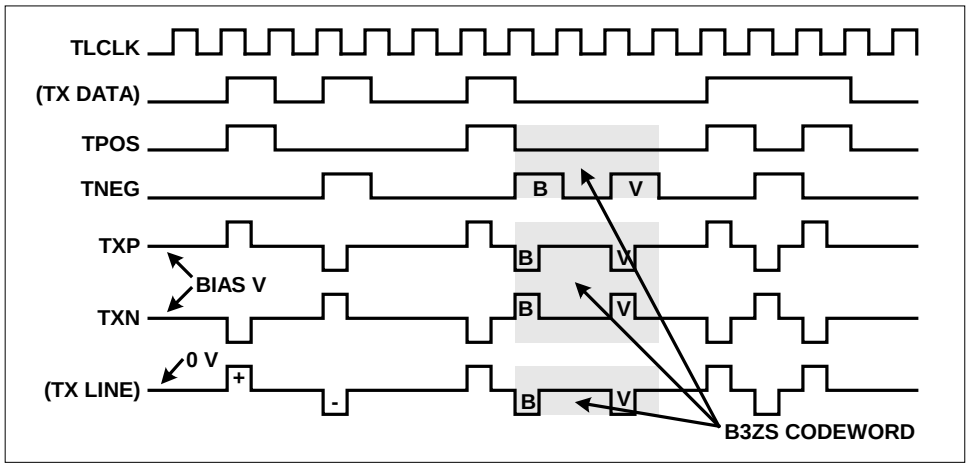
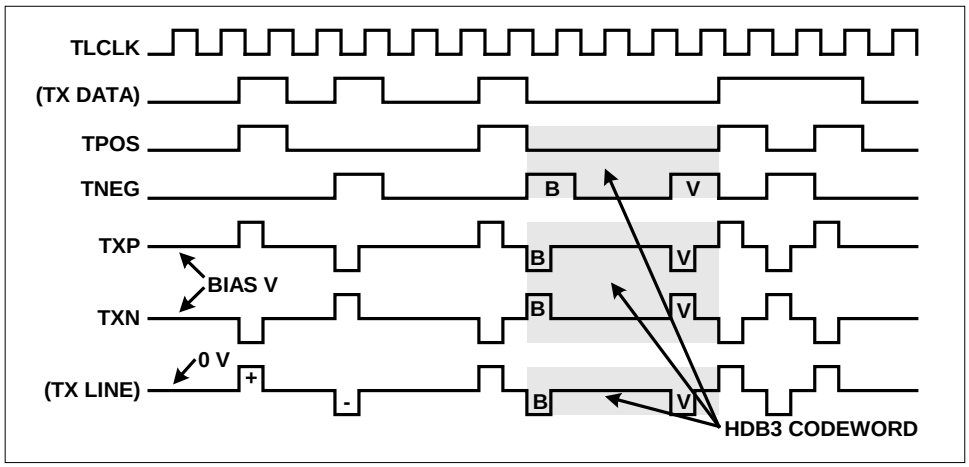


Figure 8-2. Tx Line IO HDB3 Functional Timing Diagram



8.3.1.2 B3ZS/HDB3/AMI Mode Receive Pin Functional Timing

There is no suggested time alignment between the RXP, RXN and RX LINE signals and the RLCLK clock signal. The RX DATA signal is not an always readily available signal, it is meant to represent the data value of the other signals. The signal on RSER in framed mode will be the same as the RX DATA signal except delayed.

The RXP and RXN pins are only available when the line is in B3ZS/HDB3 or AMI mode and the LIU is enabled. The RPOS, RNEG and RLCLK pins are only available when the line is in B3ZS/HDB3 or AMI mode and the LIU is disabled.

The RPOS and RNEG signals are sampled at the rising edge of the reference clock signal if the clock pin is not inverted, otherwise they are sampled at the negative edge. The RLCLK clock pin is the clock reference used for the RPOS and RNEG signals. The RPOS and RNEG pins can be inverted.

RXP and RXN are differential analog input pins. They are biased around ½ VDD and pulse above and below the bias voltage by about 1 Volt with zero cable length. These signals are connected to the windings of a 1:2 step up transformer and the other winding of the transformer is connected to the RX LINE signal. The RX LINE signal is a bipolar signal that pulses about 1 Volt positive and 1 Volt negative above and below ground (0 volts) with zero cable length. See Figure 2-1 for a diagram of the external connections.

Figure 8-3 and Figure 8-4 show the relationship between the analog and the digital outputs.

Figure 8-3. Rx Line IO B3ZS Functional Timing Diagram

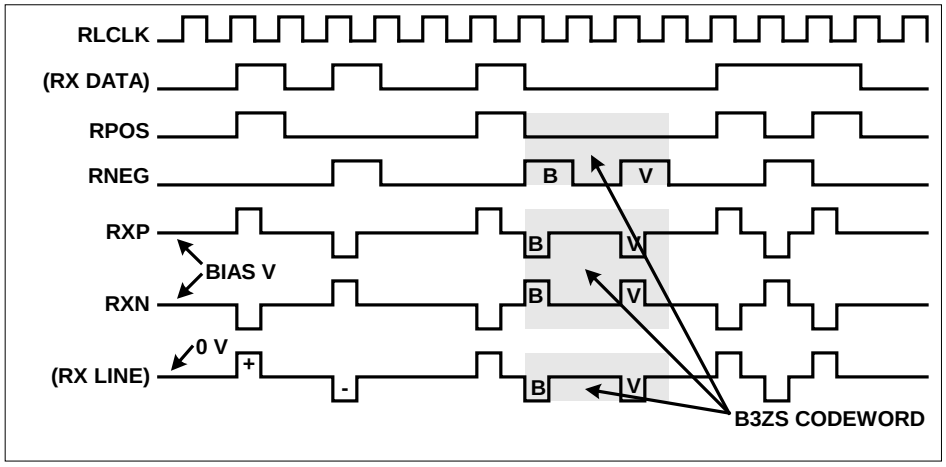
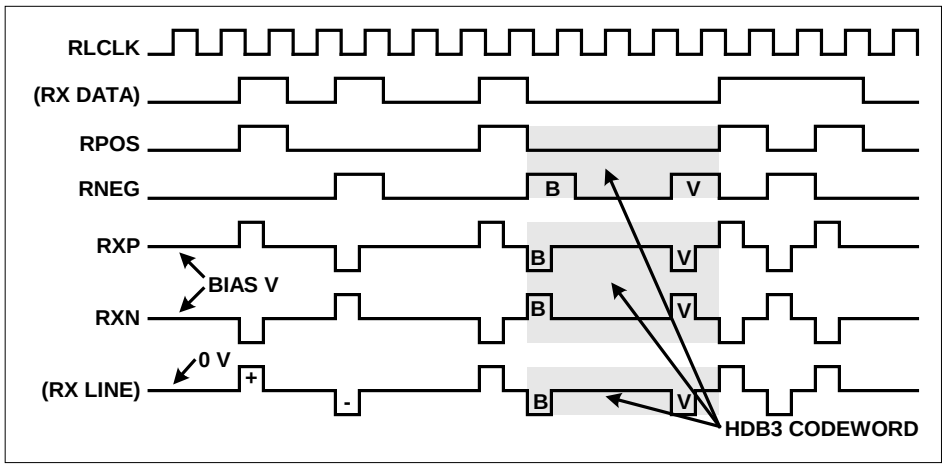


Figure 8-4. Rx Line IO HDB3 Functional Timing Diagram

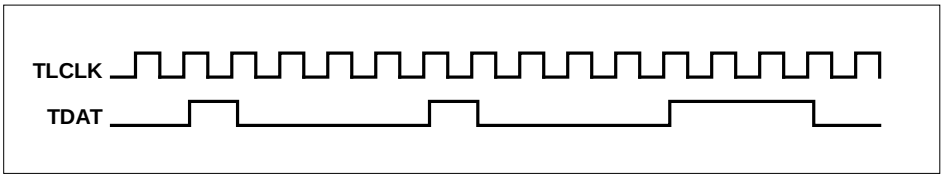


8.3.1.3 UNI Mode Transmit Pin Functional Timing

The TDAT pin is available when the line interface is in the UNI mode and the transmit line pins are enabled

The TDAT signal changes a small delay after the positive edge of the reference clock signal if the clock pin is not inverted, other wise they change after the negative edge. The TLCLK clock pin is the clock reference typically used for the TDAT signal, but the TDAT can be time referenced to the TCLKI, TCLKO, RLCLK or RCLKO clock pins. The TDAT pin can be inverted. Please refer to Figure 8-5 .

Figure 8-5. Tx Line IO UNI Functional Timing Diagram



8.3.1.4 UNI Mode Receive Pin Functional Timing

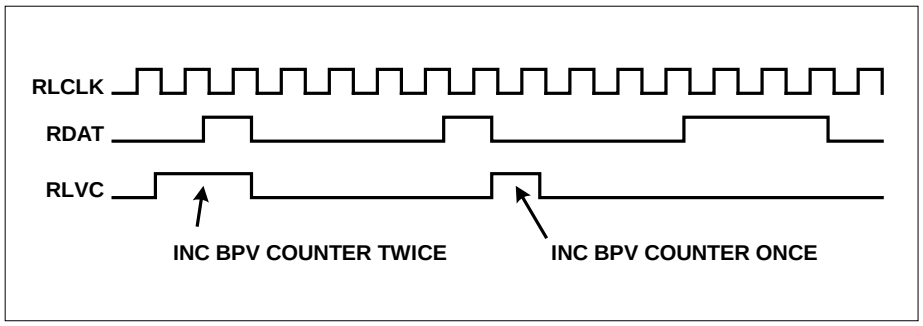
The RDAT pin is available when the line interface is in the UNI mode. The RLCV pin is available when the line interface is in the UNI Mode.

All bits on the RDAT pin, will come out the RSER pin, if the RSER pin is enabled.

The signal on the RLCV pin enables the BPV counter, which is in the line interface, to increment each clock it is high.

The RDAT and RLCV signals are sampled at the rising edge of the reference clock signal if the clock pin is not inverted, otherwise they are sampled at the negative edge. The RLCLK clock pin is the clock reference used for the RDAT and RLCV signals. The RDAT and RLCV pins can be inverted. Please refer to Figure 8-6 .

Figure 8-6. Rx Line IO UNI Functional Timing Diagram



8.3.2 DS3/E3 Framing Overhead Functional Timing

Figure 8-7 shows the relationship between the DS3 receive overhead port pins.

Figure 8-7. DS3 Framing Receive Overhead Port Timing

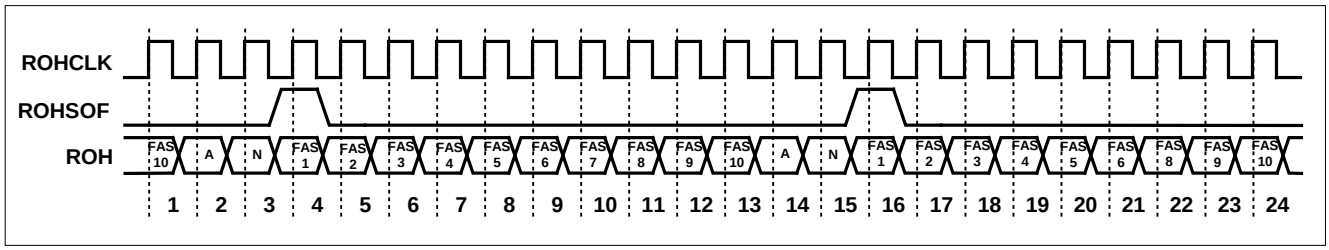


Figure 8-8 shows the relationship between the E3 G.751 receive overhead port pins.

Figure 8-8. E3 G.751 Framing Receive Overhead Port Timing

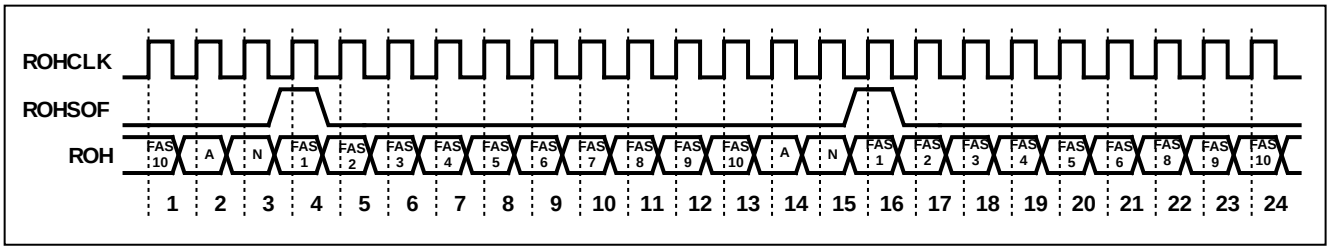


Figure 8-9 shows the relationship between the E3 G.832 receive overhead port pins.

Figure 8-9. E3 G.832 Framing Receive Overhead Port Timing

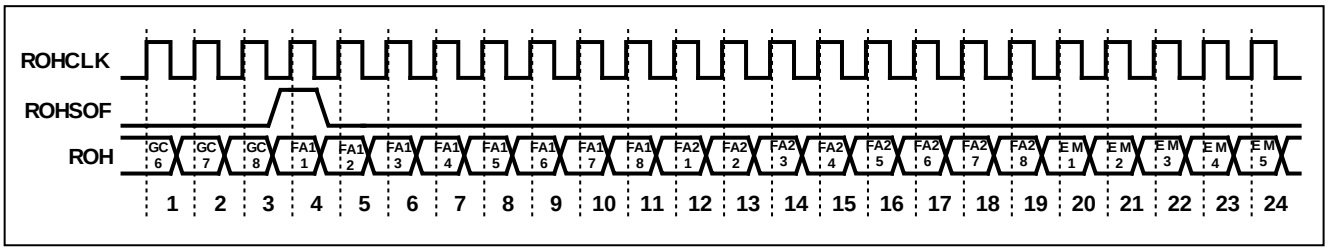


Figure 8-10 shows the relationship between the DS3 transmit overhead port pins.

Figure 8-10. DS3 Framing Transmit Overhead Port Timing

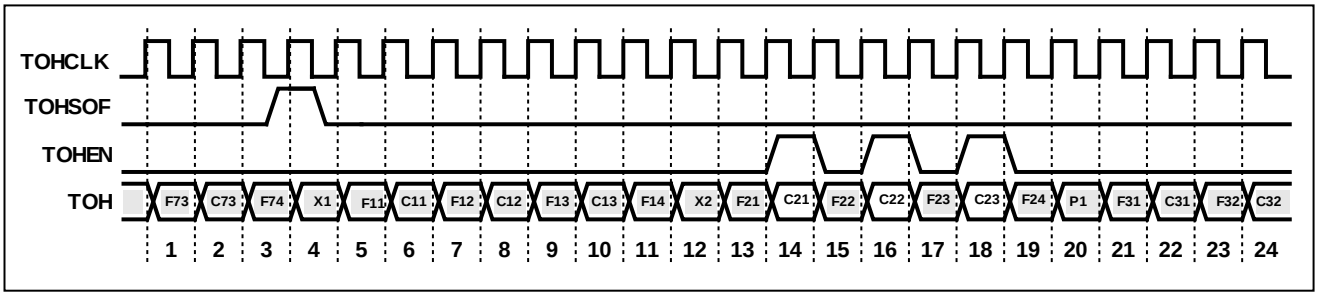


Figure 8-11 shows the relationship between the E3 G.751 transmit overhead port pins.

Figure 8-11. E3 G.751 Framing Transmit Overhead Port Timing

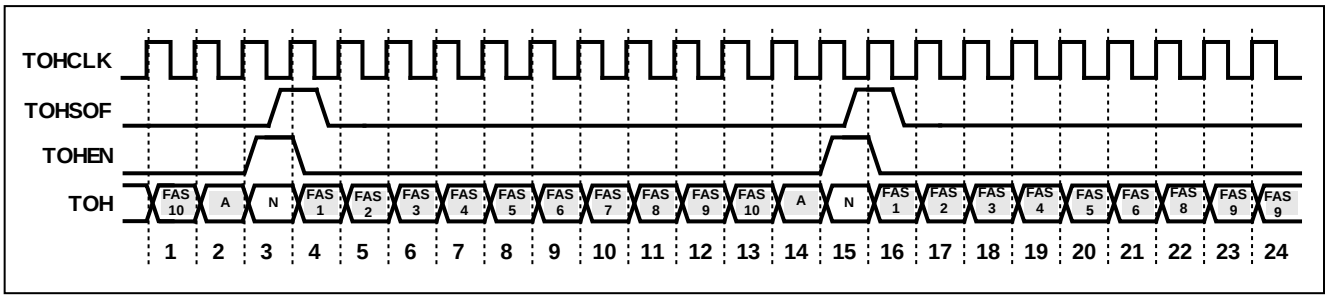
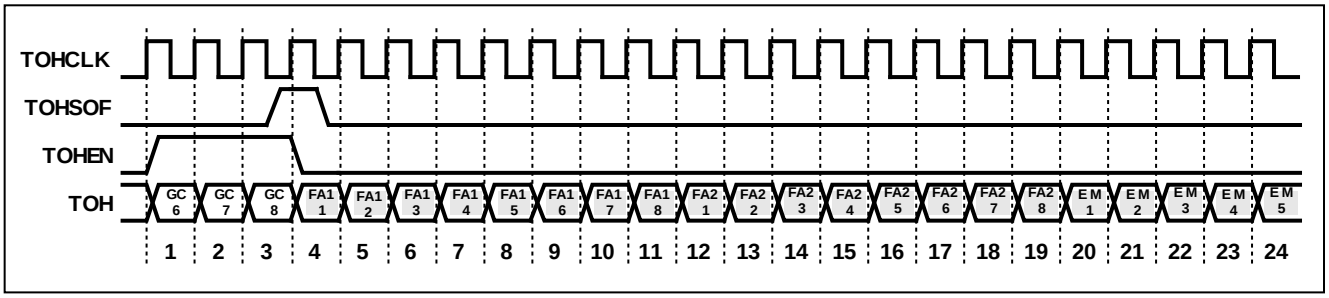


Figure 8-12 shows the relationship between the E3 G.832 transmit overhead port pins.

Figure 8-12. E3 G.832 Framing Transmit Overhead Port Timing



8.3.3 DS3/E3 Serial Data Interface

8.3.3.1 DS3/E3 Framed Mode Transmit Serial Interface Pin Functional Timing

The TSER pin is used to input DS3 or E3 payload data bits in all framing modes as well as the C-bits, which can be treated as payload, in DS3 M23 and E3 G.751 framing modes. The TDEN signal is used to determine the DS3 or E3 payload bit positions on TSER. The TDEN signal goes high three clocks before the first bit of a payload sequence is clocked into the TSER pin and it goes low three clocks before the payload sequence is stopped being clocked in to the TSER pin. The TSOFO signal pulses high three clocks before the start of the DS3 or E3 overhead bit position on TSER. The TSOFI pin is used to set the DS3 or E3 frame position. When the TSOFI pin transitions low to high, the first DS3/E3 overhead bit position on TSER will be forced to align to it

Figure 8-13 to Figure 8-15 show the relationship between the transmit serial interface pins.

Figure 8-13. DS3 Framed Mode Transmit Serial Interface Pin Timing

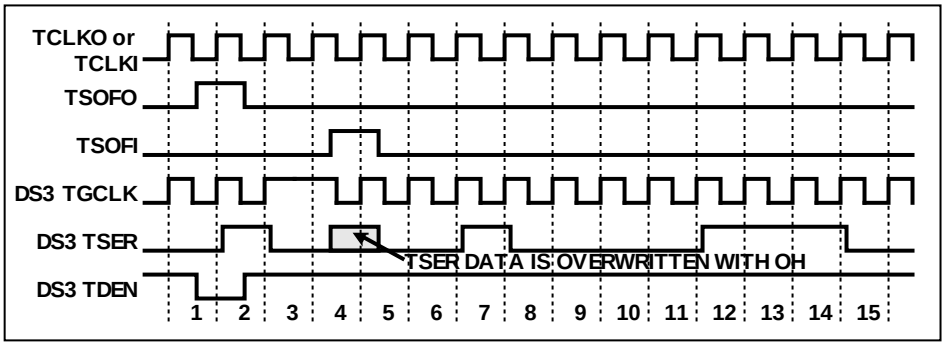


Figure 8-14. E3 G.751 Framed Mode Transmit Serial Interface Pin Timing

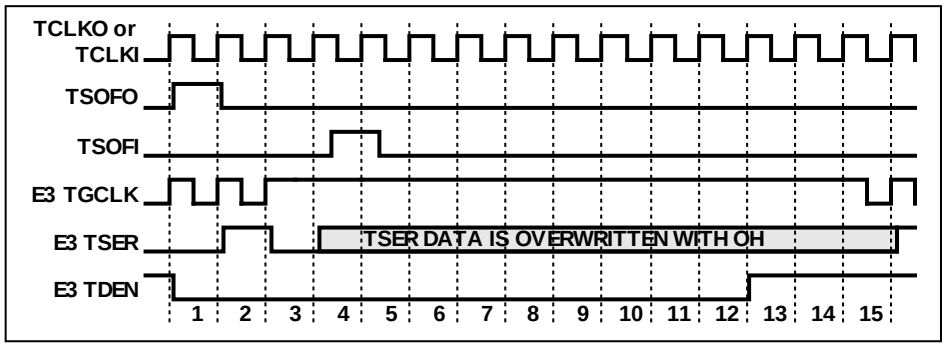
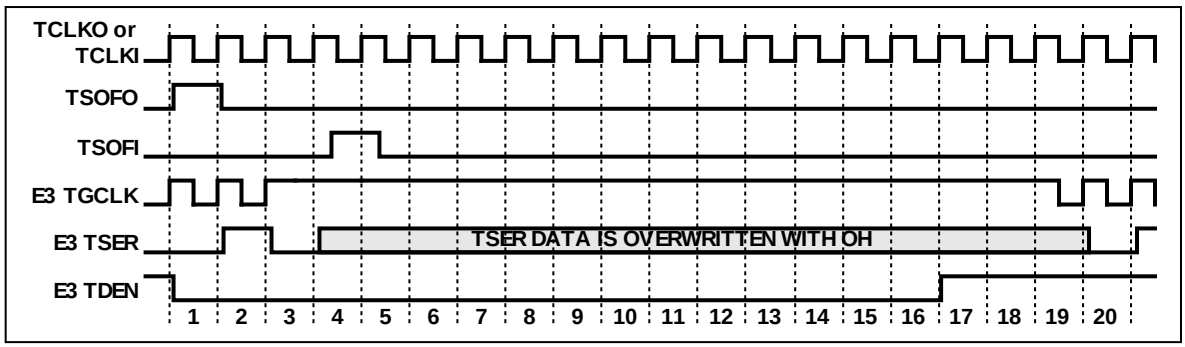


Figure 8-15. E3 G.832 Framed Mode Transmit Serial Interface Pin Timing



8.3.3.2 DS3/E3 Framed Mode Receive Serial Interface Pin Functional Timing

The RSER signal has the DS3 or E3 payload as well as the DS3 or E3 overhead bits. The RDEN signal is used to enable external logic for payload processing and will be high during the DS3 or E3 payload bits and low during the DS3 or E3 overhead bits. The RGCLK signal can also be used to clock only the DS3 or E3 payload bits into external logic since the clock is stopped during the DS3 or E3 overhead bits. The RSOFO signal marks the first overhead bit of the DS3 or E3 frame.

Figure 8-16 to Figure 8-18 show the relationship between the receive serial interface pins.

Figure 8-16. DS3 Framed Mode Receive Serial Interface Pin Timing

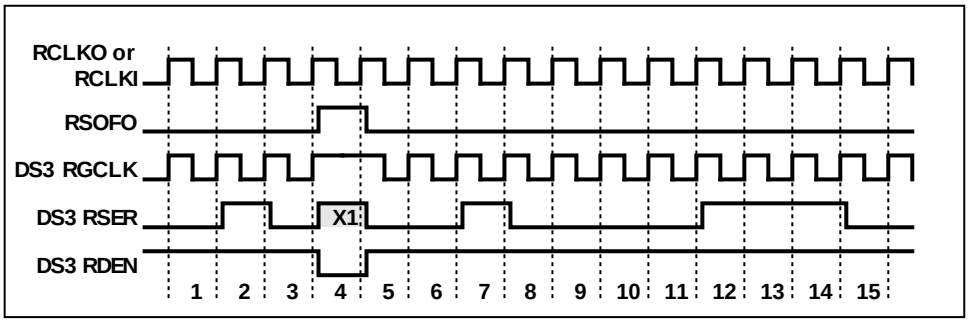


Figure 8-17. E3 G.751 Framed Mode Receive Serial Interface Pin Timing

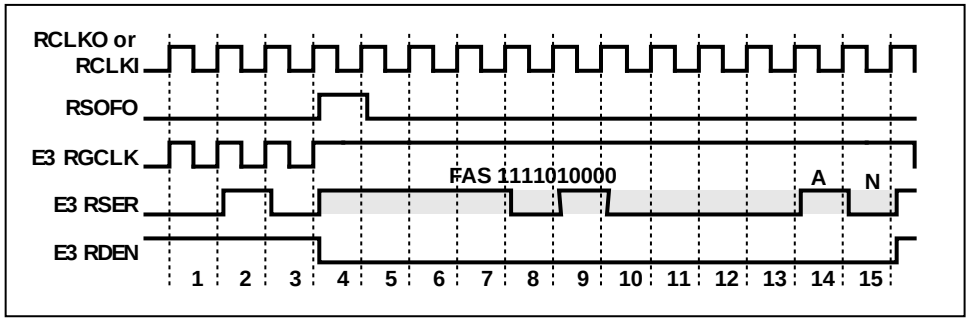
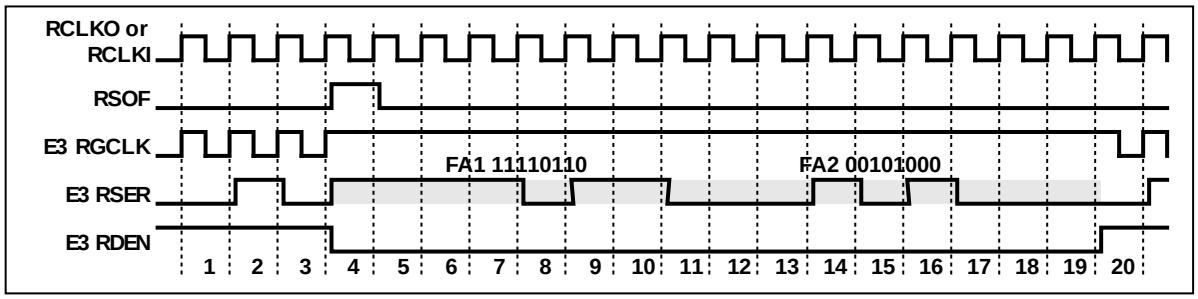


Figure 8-18. E3 G.832 Framed Mode Receive Serial Interface Pin Timing



8.3.4 Microprocessor Interface Functional Timing

8.3.4.1 SPI Functional Timing Diagrams

NOTE: The transmit and receive order of the address and data bits are selected by the D[5]/SPI_SWAP pin. The R/W (read/write) MSB bit and B (burst) LSB bit position is not effected by the D[5]/SPI_SWAP pin setting.

8.3.4.1.1 SPI Transmission Format and CPHA Polarity

When CPHA = 0, $\overline{CS}$ may be de-asserted between accesses. An access is defined as one or two control bytes followed by a data byte. $\overline{CS}$ cannot be de-asserted between the control bytes, or between the last control byte and the data byte. When CPHA = 0, $\overline{CS}$ may also remain asserted between accesses. If it remains asserted and the BURST bit is set, no additional control bytes are expected after the first control byte(s) and data are transferred. If the BURST bit is set, the address will be incremented for each additional byte of data transferred until $\overline{CS}$ is de-asserted. If $\overline{CS}$ remains asserted and the BURST bit is not set, a control byte(s) is expected following the data byte, and the address for the next access will be received from that. Anytime $\overline{CS}$ is de-asserted, the BURST access is terminated.

When CPHA = 1, $\overline{CS}$ may remain asserted for more than one access without being toggled high and then low again between accesses. If the BURST bit is set, the address should increment and no additional control bytes are

expected. If the BURST bit is not set, each data byte will be followed by the control byte(s) for the next access. Additionally, $\overline{CS}$ may also be de-asserted between accesses when CPHA =1. In the case, any BURST access is terminated, and the next byte received when $\overline{CS}$ is re-asserted will be a control byte.

The following diagrams describe the functionality of the SPI port for the four combinations of SPI_CPOL and SPI_CPHA. They indicate the clock edge that samples the data and the level of the clock during no-transfer events (high or low). Since the SPI port of the DS3170 acts as a slave device, the master device provides the clock. The user must configure the SPI_CPOL and SPI_CPHA pins to describe which type of clock that the master device is providing.

Figure 8-19. SPI Serial Port Access For Read Mode, SPI_CPOL=0, SPI_CPHA = 0

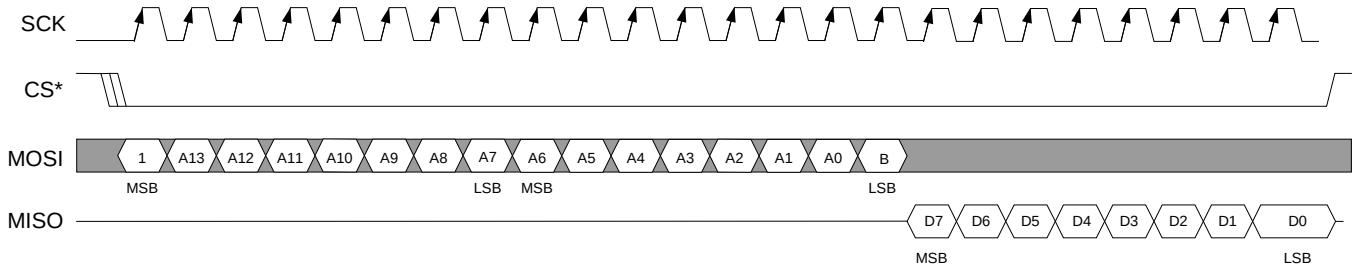


Figure 8-20. SPI Serial Port Access For Read Mode, SPI_CPOL = 1, SPI_CPHA = 0

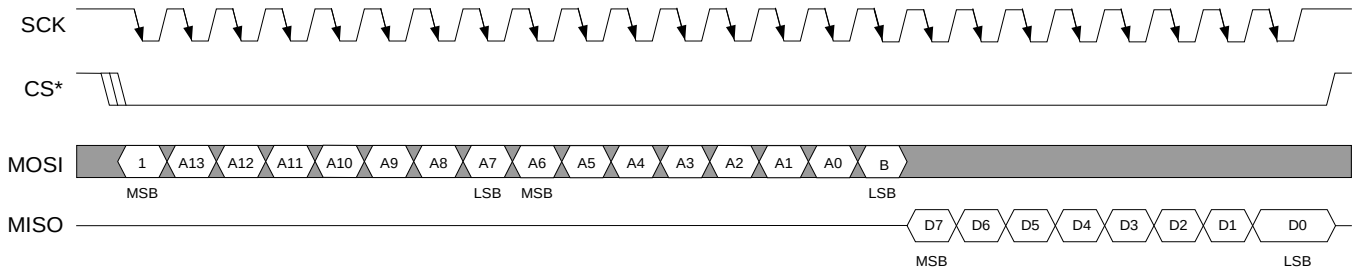


Figure 8-21. SPI Serial Port Access For Read Mode, SPI_CPOL = 0, SPI_CPHA = 1

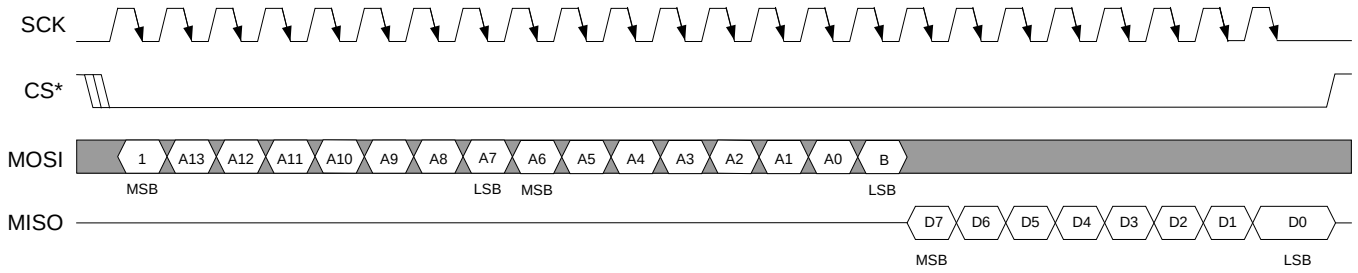


Figure 8-22. SPI Serial Port Access For Read Mode, SPI_CPOL = 1, SPI_CPHA = 1

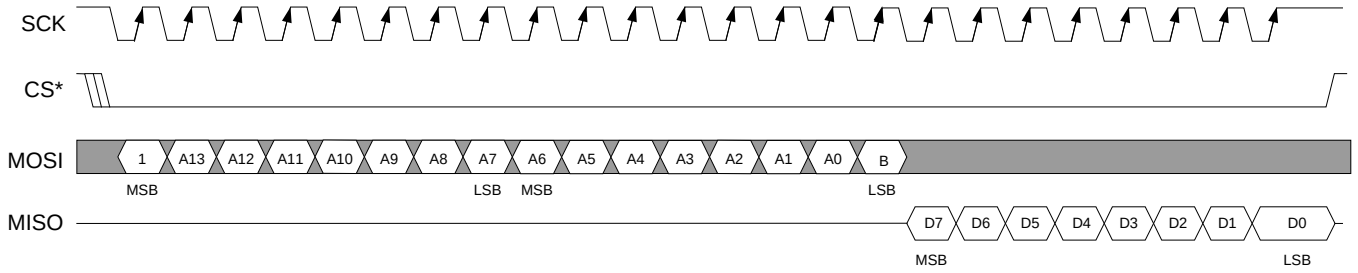


Figure 8-23. SPI Serial Port Access For Write Mode, SPI_CPOL = 0, SPI_CPHA = 0

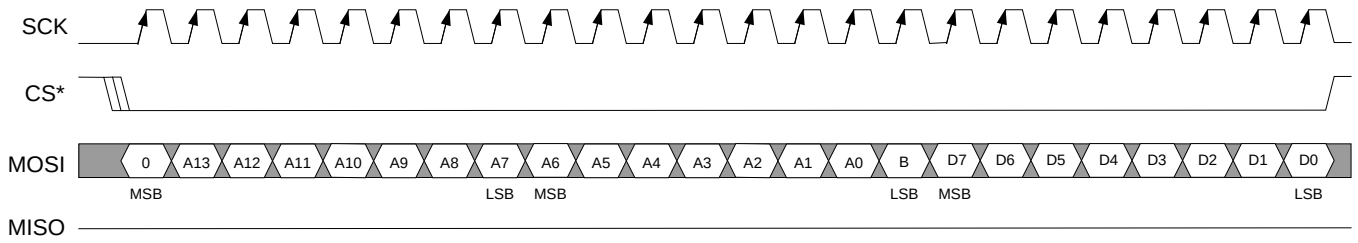


Figure 8-24. SPI Serial Port Access For Write Mode, SPI_CPOL = 1, SPI_CPHA = 0

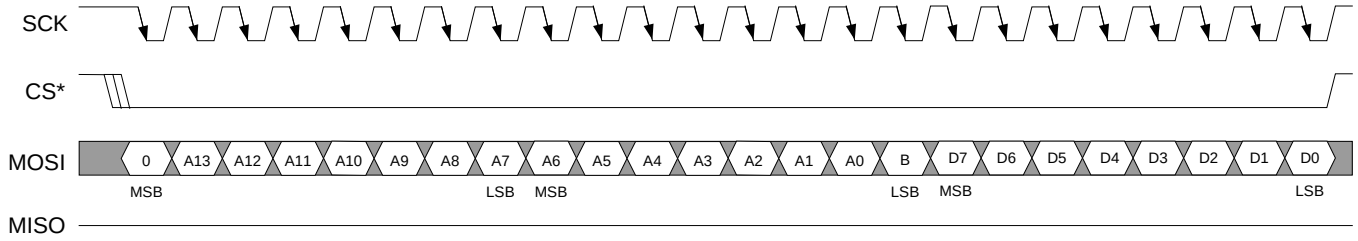


Figure 8-25. SPI Serial Port Access For Write Mode, SPI_CPOL = 0, SPI_CPHA = 1

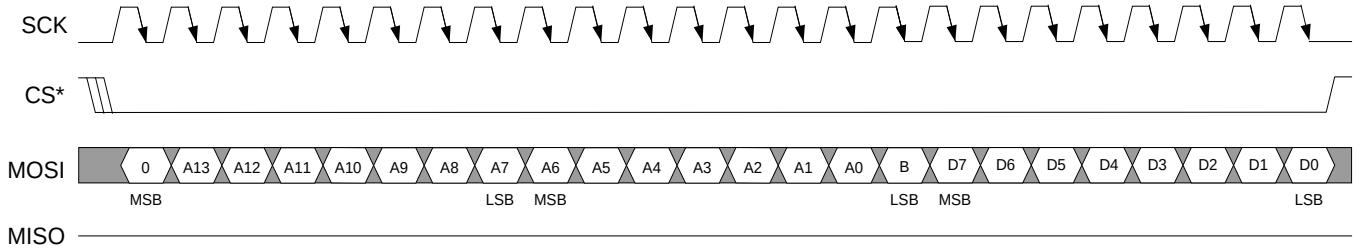
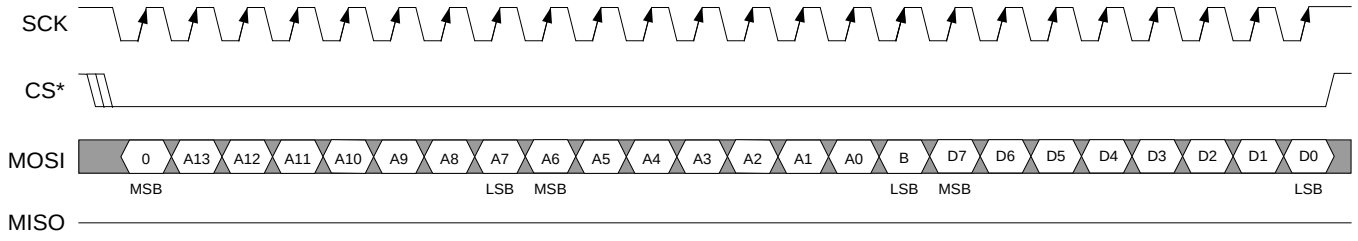


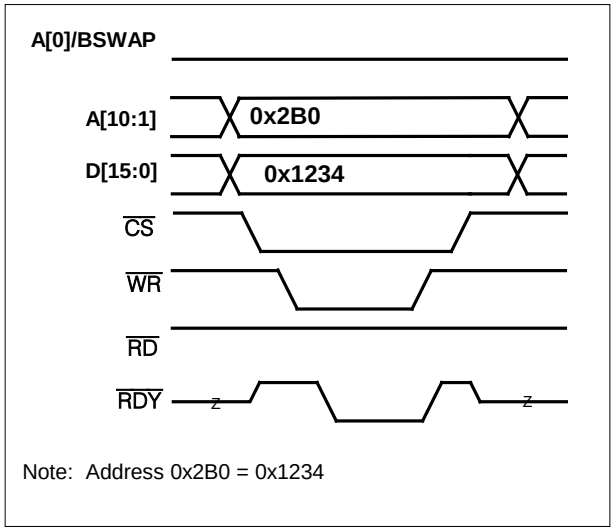
Figure 8-26. SPI Serial Port Access For Write Mode, SPI_CPOL = 1, SPI_CPHA = 1



8.3.4.2 Parallel Port Interface Diagrams

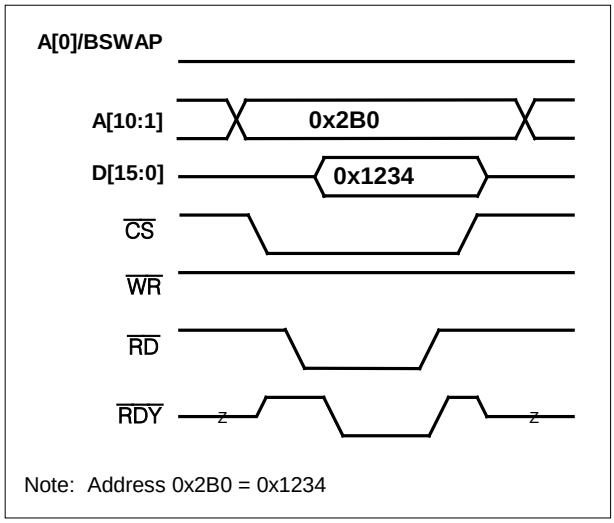
Figure 8-27 and Figure 8-29 show examples of a 16-bit databus and an 8-bit databus, respectively. In 16-bit mode, the A[0]/BSWAP signal controls whether or not to byte swap. In 8-bit mode, the A[0]/BSWAP signal is used as the LSB of the address bus (A[0]). The selection of databus size is determined by the WIDTH input signal. See also Section 10.1.1.

Figure 8-27. 16-Bit Mode Write



Note: Address 0x2B0 = 0x1234

Figure 8-28. 16-Bit Mode Read



Note: Address 0x2B0 = 0x1234

Figure 8-29. 8-Bit Mode Write

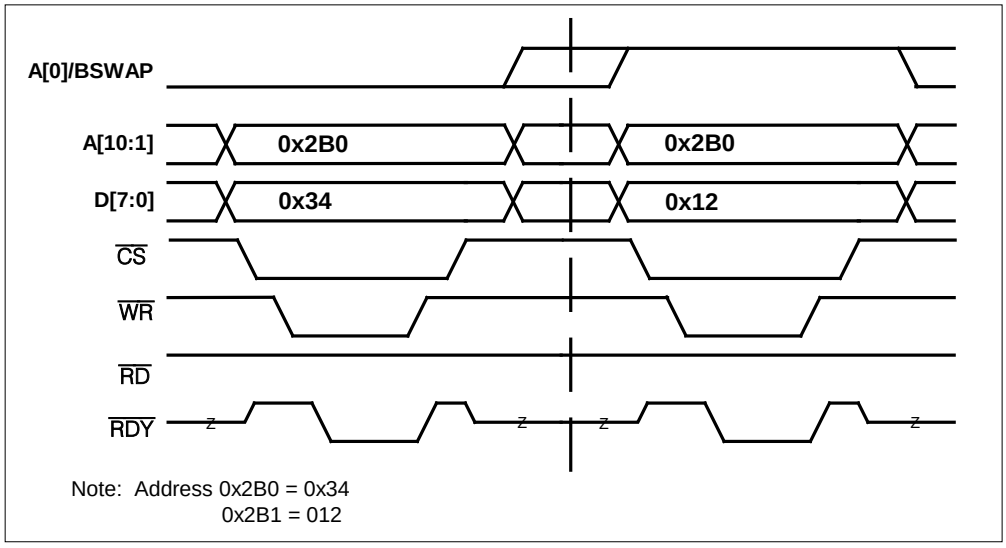


Figure 8-30. 8-Bit Mode Read

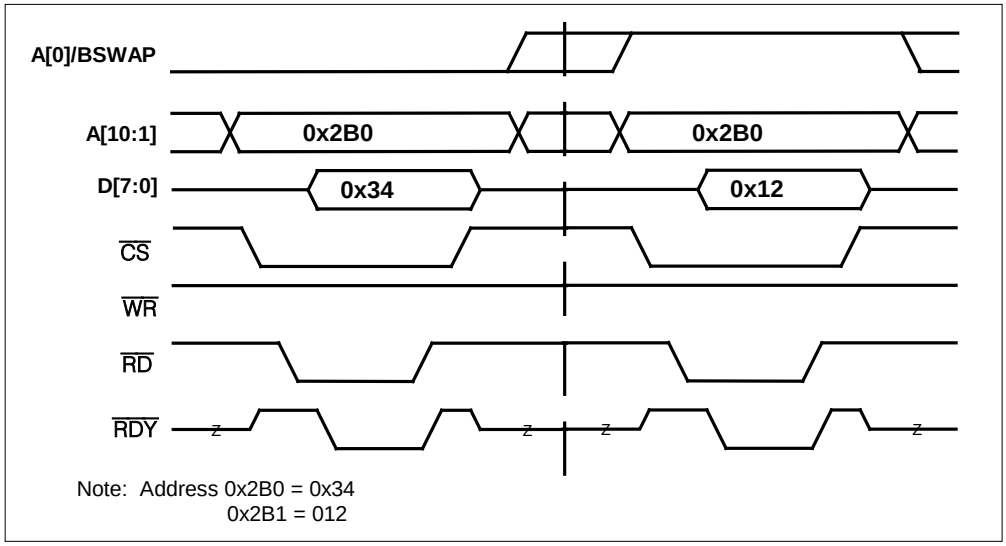


Figure 8-31 and Figure 8-32 are examples of databuses without and with byte swapping enabled, respectively. When the A[0]/BSWAP pin is set to 0, byte swapping is disabled, and when one, byte swapping is enabled. This pin should be static and not change while operating. Note: Address bit A[0] is not used in 16-bit mode. See also Section 10.1.3.

Figure 8-31. 16-Bit Mode without Byte Swap

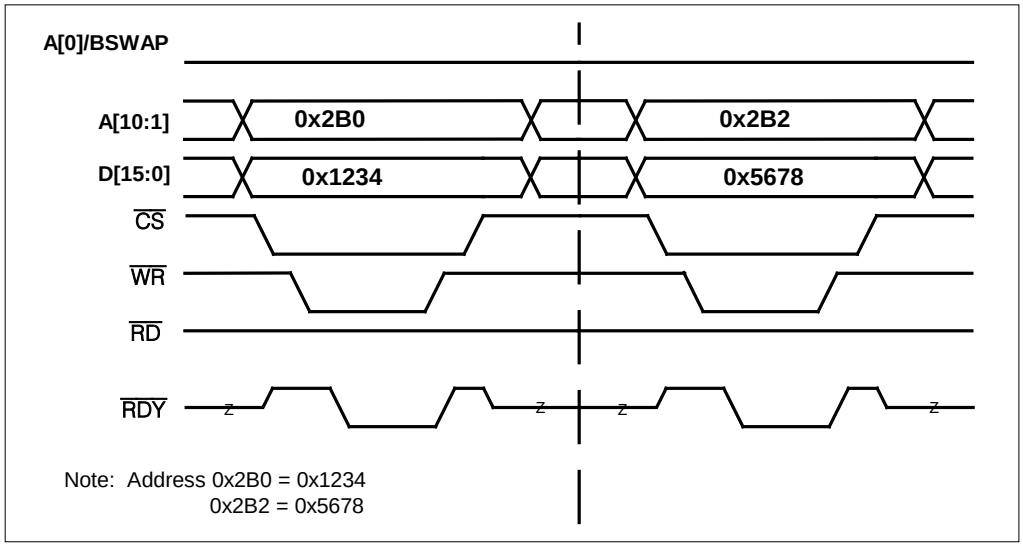
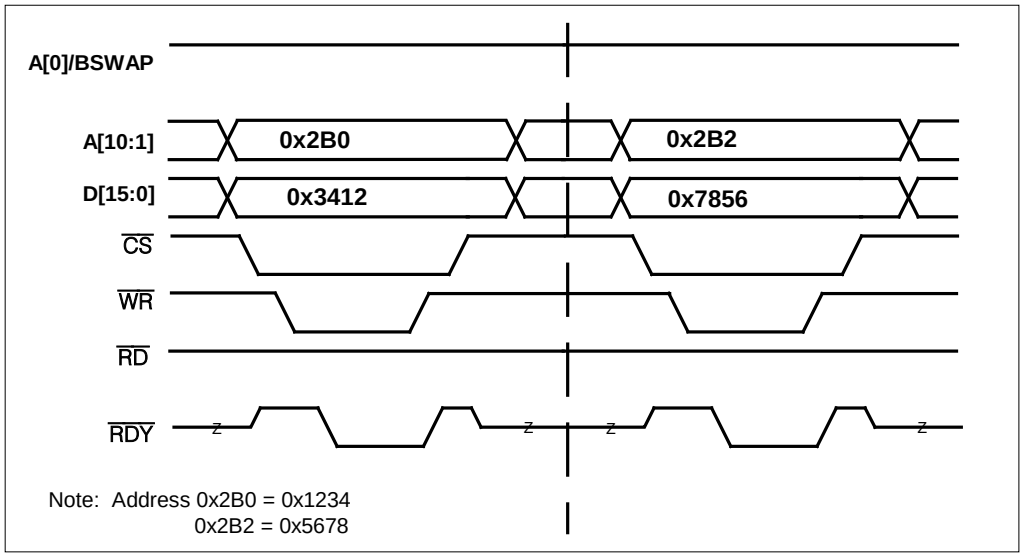


Figure 8-32. 16-Bit Mode with Byte Swap



Clearing status latched registers on a read or write access is selectable via the GL.CR1.LSBCRE register bit. Clearing on read clears all bits in the register, while the clear on write clears only those bits which are written with a '1' when the user writes to the status latched register.

To use the Clear on Read method, the user must only read the status latched register. All bits are set to zero after the read. Figure 8-33 shows a read of a status latched register and another read of the same register verifying the register has cleared.

To use the Clear on Write method, the user must write the register with ones in the bit locations that he desires to clear. Figure 8-34 shows a read, a write, and then a subsequent read revealing the results of clearing of the bits, which he wrote a '1.' See also Section 10.1.6.

Figure 8-33. Clear Status Latched Register on Read

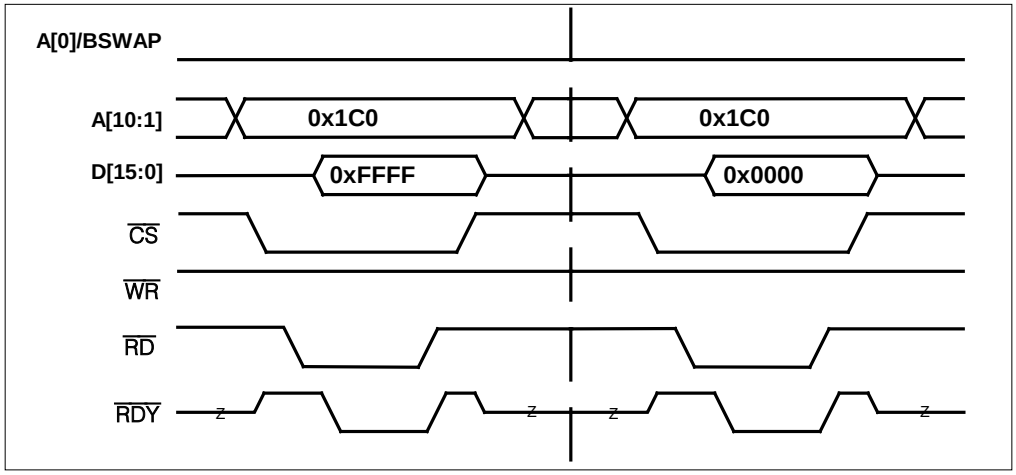


Figure 8-34. Clear Status Latched Register on Write

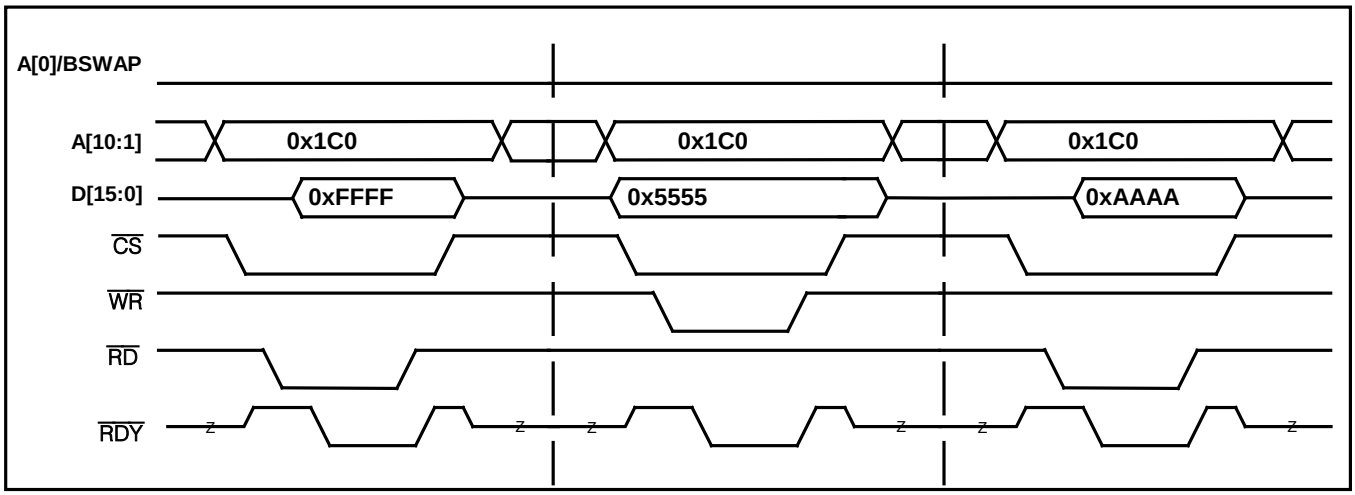


Figure 8-35 and Figure 8-36 show exaggerated views of the Ready Signal to describe the difference in access times to write or read to or from various memory locations on the DS3170 device. Some registers will have a faster access time than others and if needed, the user can implement the RDY signal to maximize efficiency of read and write accesses.

Figure 8-35. $\overline{RDY}$ Signal Functional Timing Write

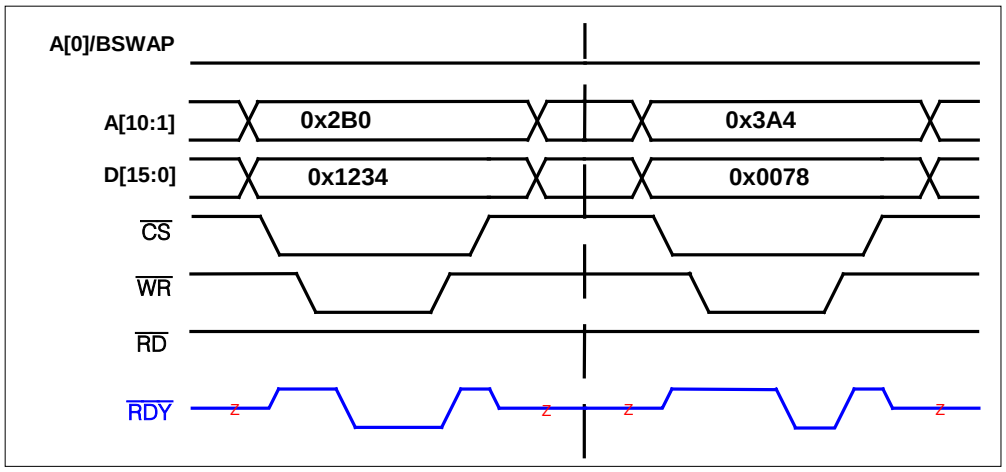
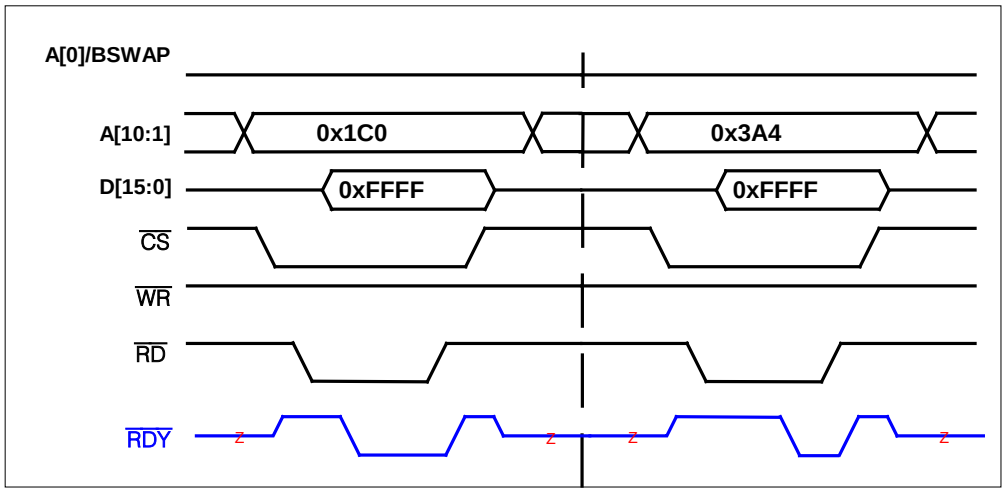


Figure 8-36. $\overline{RDY}$ Signal Functional Timing Read



See also Figure 16-8 and Figure 16-9.

8.3.5 JTAG Functional Timing

See Section 13.5.

9 INITIALIZATION AND CONFIGURATION

STEP 1: Check Device ID Code.

Before any testing can be done, the device ID code, which is stored in GL.IDR, shoud be checked against the device ID code shown below to ensure correct device is being used.

Current device ID codes is:

- **DS3170 rev 1.0: 004Fh**

STEP 2: Initialize the Device.

Before configuring for operation, make sure the device is in a known condition with all registers set to their default value by initiating a Global Reset. (See Section 10.3.) A Global Reset can be initiated via the RST pin or by the Global Reset bit (*GL.CR1*.RST). A Port Reset is not necessary since the global reset includes a reset of the port to its default values.

STEP 3: Clear the Reset.

It is necessary to clear the RST bit to begin normal operation.

After clearing the RST bit, the device is configured for default mode.

Default mode:

Framer: C-bit DS3
LIU: Disabled

STEP 4: Clear the Data Path Resets and the Port Power-Down bit.

The default value of the Data Path Resets is one, which keeps the internal logic in the reset status. The user needs to clear the following bits:

GL.CR1.RSTDP = 0
PORT.CR1.RSTDP = 0
PORT.CR1.PD = 0

STEP 5: Configure the CLAD

If using the LIU, configure the CLAD (which supplies the clock to the Receive LIU) via the CLAD bits in the GL.CR2 register.
Note: The user must supply a DS3, E3, STS-1, 77.76 MHz, or 19.44 MHz clock to the REFCLK pin.

STEP 6: Select the clock source for the transmitter.

Loop Time (use the receive clock): Set PORT.CR3.LOOPT = 1
CLAD Source: Set PORT.CR3.CLADC = 0
TCLKI Source: Set PORT.CR3.CLADC = 1
If using the CLAD, properly configure the CLAD by setting the CLAD bits in GL.CR2.

STEP 7: Configure the Framing Mode and the Line Mode..

PORT.CR2.LM[2:0] = 011 (LIU on, JA in rx side) or another setting. See Table 10-26
*PORT.CR2.*FM[2:0] set to correct mode. See Table 10-25.

STEP 8: Disable Payload AIS (downstream AIS) and Line AIS

PORT.CR1.PAIS[2:0] = 111
PORT.CR1.LAIS[1:0] = 11

STEP 9: Enable the port (for non-LIU modes)

PORT.CR2.TLEN = 1

Table 9-1. Configuration of Port Register Settings

MODE	PORT.CR1 0x040	PORT.CR2 0x042	PORT.CR3 0x044	PORT.CR4 0x046
DS3 C-Bit Framed	0x2000	0000 0011 0000 0111	0x0000	0x0000
DS3 M13 Framed	0x2000	0000 0011 0000 1111	0x0000	0x0000
E3.751 Framed	0x2000	0000 0011 0001 0111	0x0000	0x0000
E3.823 Framed	0x2000	0000 0011 0001 111X	0x0000	0x0000

Note: *The Line Mode has been configured with the LIU enabled and the JA in the receive path (LM[2:0] = 011) for all modes.*

9.1 Monitoring and Debugging

To determine if the device is receiving a good signal and that the chip is correctly configured for its environment, check the following status registers.

Receive Loss of Lock – PORT.SR.RLOL: The clock recovery circuit of the LIU was unable to recover the clock from the incoming signal. This may indicate that the LIU's master clock does not match the frequency of the incoming signal. Verify that the CLAD is configured to match the clock input on the REFCLK pin (DS3, E3, STS-1). See Table 10-11.

Loss of Signal – LINE.RSR.LOS: This indicates that the LIU is unable to recover the clock and data because there is no signal on the line, or that the signal is attenuated beyond recovery.

Loss of Frame – T3.RSR1.LOF (or E3751.RSR1 or E3832.RSR1): This indicates that the framer was unable to synchronize to the incoming data. Verify that the FM bits have been correctly configured for the correct mode of traffic (DS3, E3 G.751, E3 G.832)

Other helpful techniques to utilize in diagnosing a problem include using Line Loopback and Diagnostic Loopback. These features help to isolate and identify the source of the problem. Line Loopback will loop the receive input to the transmit output, eliminating the transmit side input from the equation. Diagnostic Loopback will loop the transmit output before the LIU to the receive framer, eliminating the analog Receive LIU and the receive side analog circuitry.

One other potential problem is the **Line Encoding/Decoding**. The device needs to be configured in the same mode as the far end piece of equipment. If the far end piece of equipment is transmitting and receiving HDB3/B3ZS encoded data, the DS3170 also must be configured to do the same. This is controlled by the *LINE.TCR*.TZSD and the *LINE.RCR*.RZSD bits.

10 FUNCTIONAL DESCRIPTION

10.1 Processor Bus Interface

10.1.1 SPI Serial Port Mode

The external processor bus can be configured to operate in SPI serial bus mode. See the section 8.3.4.1 for detailed timing diagrams.

When SPI = 1, SPI bus mode is implemented using four signals: clock (CLK), master-out slave-in data (MOSI), master-in slave-out data (MISO), and chip select ($\overline{CS}$). Clock polarity and phase can be set by the D[7]/SPI_CPOL and D[6]/SPI_CPHA pins.

The order of the address and data bits in the serial stream is selectable using the D[5]/SPI_SWAP pin. The R/W bit is always first and B bit is always last in the initial control word and are not effected by the D[5]/SPI_SWAP pin setting.

10.1.2 8/16 Bit Bus Widths

The external processor bus can be sized for 8 or 16 bits using the WIDTH pin. When in 8-bit mode (WIDTH=0), the address is composed of all the address bits including A[0], the lower 8 data lines D[7:0] are used and the upper 8 data lines D[15:8] are not used and never driven during a read cycle. When in 16-bit mode (WIDTH=1), the address bus does not include A[0] (the LSB of the address bus is not routed to the chip) and all 16 data lines D[15:0] are used. See Figure 8-27 and Figure 8-29 for functional timing diagrams.

10.1.3 Ready Signal ($\overline{RDY}$)

The $\overline{RDY}$ signal allows the microprocessor to use the minimum bus cycle period for maximum efficiency. When this signal goes low, the $\overline{RD}$ or $\overline{WR}$ cycle can be terminated. See Figure 8-35 for functional timing diagrams.

Note: The $\overline{RDY}$ signal will not go active if the user attempts to read or write unused registers not assigned to any design blocks. The $\overline{RDY}$ signal will go active if the user writes or reads reserved registers or unused registers within design blocks.

10.1.4 Byte Swap Modes

The processor interface can operate in byte swap mode when the data bus is configured for 16-bit operation. The A[0]/BSWAP pin is used to determine whether byte swapping is enabled. This pin should be static and not change while operating. When the A[0]/BSWAP pin is low the upper register bits REG[15:8] are mapped to the upper external data bus lines D[15:8], and the lower register bits REG[7:0] are mapped to the lower external data bus lines D[7:0]. When the A[0]/BSWAP pin is high the upper register bits REG[15:8] are mapped to the lower external data bus lines D[7:0], and the lower register bits REG[7:0] are mapped to the upper external data bus lines D[15:8]. See Figure 8-31 and Figure 8-32 for functional timing diagrams.

10.1.5 Read-Write/Data Strobe Modes

The processor interface can operate in either read-write strobe mode or data strobe mode. When MODE=0 the read-write strobe mode is enabled and a negative pulse on $\overline{RD}$ performs a read cycle, and a negative pulse on $\overline{WR}$ performs a write cycle. When MODE=1 the data strobe mode is enabled and a negative pulse on $\overline{DS}$ when R/$\overline{W}$ is high performs a read cycle, and a negative pulse on $\overline{DS}$ when R/$\overline{W}$ is low performs a write cycle. The read-write strobe mode is commonly called the “Intel” mode, and the data strobe mode is commonly called the “Motorola” mode.

10.1.6 Clear on Read/Clear on Write Modes

The latched status register bits can be programmed to clear on a read access or clear on a write access. The global control register bit *GL.CR1*.LSBCRE controls the mode that all of the latched registers are cleared. When LSBCRE=0, the latched register bits will be cleared when the register is written to and the write data has the register bits to clear set. When LSBCRE=1, the latched register bits that are set will be cleared when the register is read.

The clear on write mode expects the user to use the following protocol:

1. Read the latched status register
2. Write to the registers with the bits set that need to be cleared.

This protocol is useful when multiple uncoordinated software tasks access the same latched register. Each task should only clear the bits with which it is concerned; the other tasks will clear the bits with which they are concerned.

The clear on read mode is simpler since the bits that were read as being set will be cleared automatically. This method will work well in a software system where multiple tasks do not read the same latched status register. The latched status register bits in clear on read mode are carefully designed not to miss events that occur while a register is being read when the latched bit has not already been set. Refer to Figure 8-33 and Figure 8-34.

10.1.7 Interrupt and Pin Modes

The interrupt ($\overline{INT}$) pin is configurable to drive high or high impedance when inactive. The GL.CR1.INTM bit controls the pin configuration. If it is set, the $\overline{INT}$ pin will drive high when inactive. After a reset, the $\overline{INT}$ pin will be in high impedance mode until an interrupt source is active and enabled to drive the interrupt pin.

10.1.8 Interrupt Structure

The interrupt structure is designed to efficiently guide the user to the source of an enabled interrupt source. The status bits in the global status (*GL.SR*) and global status latched register (*GL.SRL*) are read to determine if the interrupt source is a global event, a global performance monitor update or whether it came from the port. If the interrupt event came from the port then the port status register (*PORT.SR*) and port status register latched (*PORT.SRL*) can be read to determine if the interrupt source is a common port event like the performance monitor update or LIU or whether it came from the DS3/E3 Framers, BERT, HDLC, FEAC or Trail Trace status registers. If the interrupt came from the DS3/E3 Framers, BERT, HDLC, FEAC or Trail Trace status registers, then those registers will need to be read to determine the event that caused the interrupt.

The source of an interrupt can be determined by reading three status registers: the global, port and block status registers.

When a mode is not enabled, then interrupts from that source will not occur. For example, if E3 framing mode is enabled, an interrupt source that is defined in DS3 framing, but not in E3 framing, cannot create a new interrupt. Note that when modes are changed, the latched status bits of the new mode, as well as any other mode, may get set. If the data path reset is set during or after the mode change, the latched status bits will be automatically cleared. If the data path reset is not used to clear the latched status bits, then the registers must be cleared by reading or writing to them based on the register clear method selected.

Figure 10-1. Interrupt Structure

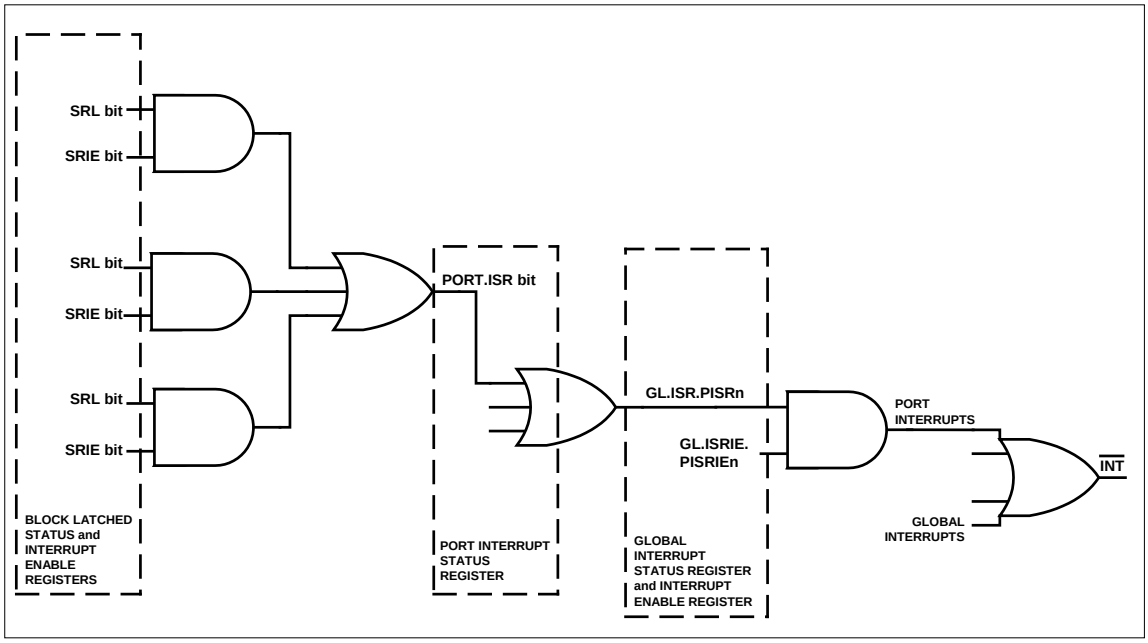


Figure 10-1 not only tells the user how to determine which event caused the interrupt, it also tells the user how to enable a particular interrupt. Each block has a Status Register Interrupt Enable register which must be set in order to enable an interrupt. The next step is to unmask the interrupt at the port level. This is controlled in the Global Interrupt Status Register Interrupt Enable register (GL.ISRIE). Now the device is ready to drive the INT pin low when a particular status bit gets set.

For example, in order to enable DS3 Out of Frame interrupts, the following registers would need to be written:

Register bit	Address	Value Written	Note
T3.RSRIE1.OOFIE	0x12C	0x0002	Unmask OOF interrupt
GL.ISRIE.PISRIE	0x012	0x0010	Unmask Port interrupts

The following status registers bits will be set upon reception of OOF:

Register bit	Address	Value Read	Note
T3.RSRL1.OOFL	0x128	0x0002	DS3 Out of Frame
PORT.ISR.FMSR	0x050	0x0001	Framer Block Interrupt Active
GL.ISR.PISR	0x010	0x0010	Port Interrupt Active

10.2 Clocks

10.2.1 Line Clock Modes

10.2.1.1 Loop Timing Enabled

When loop timing is enabled (PORT.CR3.LOOPT), the transmit clock source is the same as the receive clock source. The TCLKI pin is not used as a clock source. Because loop timing is enabled, the loopback functions (LLB, PLB and DLB) do not cause the clock sources to switch when they are activated. The transmit and receive signal pins can be timed to a single clock reference without concern about having the clock source change during loopbacks.

10.2.1.1.1 LIU Enabled, Loop Timing Enabled

In this mode, the receive LIU sources the clock for both the receive and transmit logic. The RCLKO, TCLKO and TLCLK clock output pins will be the same. The transmit or receive line payload signal pins can be timed to any of these clock. The use of the RCLKO pin as the timing source is suggested. If RCLKO is used as the timing source, be sure to set PORT.CR3.RFTS = 0 for output timing.

10.2.1.1.2 LIU Disabled, Loop Timing Enabled

In this mode, the RLCLK pin are the source of the clock for both the receive and transmit logic. The RCLKO, TCLKO and TLCLK clock output pins will both be the same as the RLCLK clock. The transmit or receive line payload signals can be timed to any of these clock pins. The use of the RLCLK pin as the timing source is suggested. If RLCLK is used as the timing source, be sure to set PORT.CR3.RFTS = 1 for input timing.

10.2.1.2 Loop Timing Disabled

When loop timing is disabled, the transmit clock source can be different than the receive clock source. The loopback functions, LLB, PLB and DLB, will cause the clock sources to switch when they are activated. Care must be taken when selecting the clock reference for the transmit and receive signals.

The most versatile clocking option has the receive line interface signals timed to RLCLK, the transmit line interface signals timed to TLCLK, the receive framer signals timed to RCLKO, and the transmit framer signals timed to TCLKO. This clocking arrangement works in all modes.

When LLB is enabled, the clock on the TLCLK pin will switch to the clock from the RLCLK pin or RX LIU. It is recommended that the transmit line interface signals be timed to the TLCLK pins. If TLCLK is used as the timing source, be sure to set PORT.CR3.TLTS = 0 for output timing.

When PLB is enabled, the TCLKI pin will not be used and the internal transmit clock is switched to the internal receive clock. The clock on the TCLKO pin will switch to the clock from the RLCLK pins or RX LIU. The framer input signals will be ignored while PLB is enabled. It is recommended that the transmit line interface signals be timed to the TCLKO pins.

When DLB is enabled, the internal receive clock is switched to the internal transmit clock which is sourced from the TCLKI pin or one of the CLAD clocks, and the clock on the RLCLK pin or from the RX LIU will not be used. The clock on the RCLKO pin will switch to the clock on the TCLKI pins or one of the CLAD clocks. The receive line signals from the RX LIU or line interface pins will be ignored. It is recommended that the receive framer pins be timed to the RCLKO pin. If TCLKO is used as the timing source, be sure to set PORT.CR3.TFTS = 0 for output timing.

When both DLB and LLB are enabled, the TLCLK clock pin are connected to either the RX LIU recovered clock or the RLCLK clock pin, and the RCLKO clock pin will be connected to the TCLKI clock pin or one of the CLAD clocks. It is recommended that the transmit line signals be timed to the TLCLK pin, the receive line interface signals be timed to the RLCLK pin, the receive framer signals be timed to the RCLKO pin, and the transmit framer signals be timed to the TCLKO pin.

10.2.1.2.1 LIU Enabled - CLAD Timing Disabled – no LB

In this mode, the receive LIU sources the clock for the receive logic and the TCLKI pin sources the clock for the transmit logic.

10.2.1.2.2 LIU Enabled - CLAD Timing Enabled – no LB

In this mode, the receive LIU sources the clock for the receive logic and one of the CLAD clocks sources the clock for the transmit logic.

10.2.1.2.3 LIU Disabled - CLAD Timing Disabled – no LB

In this mode, the RLCLK pin source the clock for the receive logic and the TCLKI pin sources the clock for the transmit logic.

10.2.1.2.4 LIU Disabled - CLAD Timing Enabled – no LB

In this mode, the RLCLK pin source the clock for the receive logic and one of the CLAD clocks sources the clock for the transmit logic.

10.2.2 Sources of Clock Output Pin Signals

The clock output pins can be sourced from many clock sources. The clock sources are the transmit input clocks pin (TCLKI), the receive clock input pin (RLCLK), the recovered clock in the receive LIU, and the clock signals in the clock rate adapter circuit (CLAD). The default clock source for the receive logic is the RLCLK pin if the LIU is disabled; otherwise the default clock is sourced from the Rx LIU clock when the RX LIU is enabled. The default clock source for the transmit logic is the CLAD clocks.

The LIU is enabled based on the line mode bits(LM[2:0]) (see Table 10-26). The bits LM[2:0], LBM[2:0], LOOPT and CLADC are located in the port configuration registers. LIUEN is not a register bit; it is a variable based on the line mode bits. Table 10-1 decodes the LM bits for LiUEN selection.

Table 10-1. LIU Enable Table

LM[2:0]	LIUEN	LIU STATUS
000	0	Disabled
001	1	Enabled
010	1	Enabled
011	1	Enabled
1XX	0	Disabled

Table 10-2 identifies the framer clock source and the line clock source depending on the mode that the device is configured. Putting the device in loopback will typically mux in a different clock than the normal clock source.

Table 10-2. All Possible Clock Sources Based on Mode and Loopback

MODE	LOOPBACK	Rx FRAMER CLOCK SOURCE	Tx FRAMER CLOCK SOURCE	Tx LINE CLOCK SOURCE
Loop Timed	Any	RLCLK or RXLIU	Same as RX	Same as Rx
Normal	None	RLCLK or RXLIU	TCLKI or CLAD	Same as Tx
Normal	LLB	RLCLK or RXLIU	TCLKI or CLAD	Same as Rx
Normal	PLB	RLCLK or RXLIU	Same as RX	Same as Rx
Normal	DLB	Same as Tx	TCLKI or CLAD	Same as Tx
Normal	LLB and DLB	Same as Tx	TCLKI or CLAD	RLCLK or RXLIUn

Table 10-3 identifies the source of the output signal TLCLK based on certain variables and register bits.

Table 10-3. Source Selection of TLCLK Clock Signal

SIGNAL	LOOPT (PORT.CR3)	LBM[2:0] (PORT.CR4)	LLB or PLB	LIUEN	CLADC (PORT.CR3)	SOURCE
TLCLK	1	XXX	NA	1	X	Rx LIU
	1	XXX	NA	0	X	RLCLK
	0	010	LLB	1	X	Rx LIU
	0	110	LLB	1	X	Rx LIU
	0	010	LLB	0	X	RLCLK
	0	110	LLB	0	X	RLCLK
	0	011	PLB	1	X	Rx LIU
	0	011	PLB	0	X	RLCLK
	0	000	NO	X	0	CLAD
	0	001	NO	X	0	CLAD
	0	100	NO	X	0	CLAD
	0	10X	NO	X	0	CLAD
	0	111	NO	X	0	CLAD
	0	000	NO	X	1	TCLKI
	0	001	NO	X	1	TCLKI
	0	100	NO	X	1	TCLKI
	0	10X	NO	X	1	TCLKI
	0	111	NO	X	1	TCLKI

Figure 10-2 shows the source of the TCLKO signals.

Figure 10-2. Internal Tx Clock

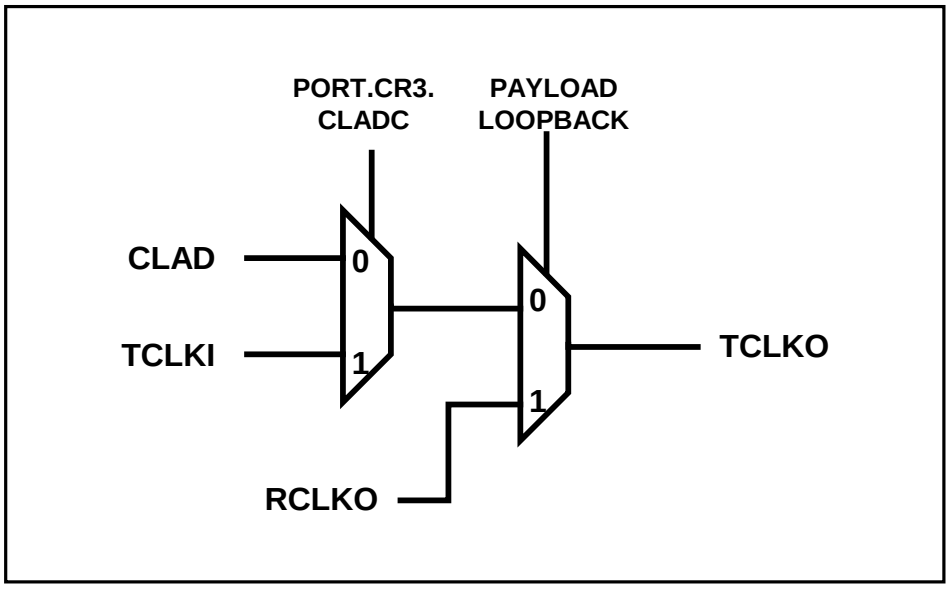


Table 10-4 identifies the source of the output signal TCLKO based on certain variables and register bits.

Table 10-4. Source Selection of TCLKO (Internal Tx Clock)

SIGNAL	LOOPT PORT.CR3	LBM[2:0] (PORT.CR4)	LIUEN	CLADC (PORT.CR3)	SOURCE
TCLKO	1	XXX	1	X	Rx LIU
	1	XXX	0	X	RLCLK
	0	PLB (011)	1	X	Rx LIU
	0	PLB (011)	0	X	RLCLK
	0	PLB disabled	X	0	CLAD
	0	PLB disabled	X	1	TCLKI

Figure 10-3 shows the source of the RCLKO signals.

Figure 10-3. Internal Rx Clock

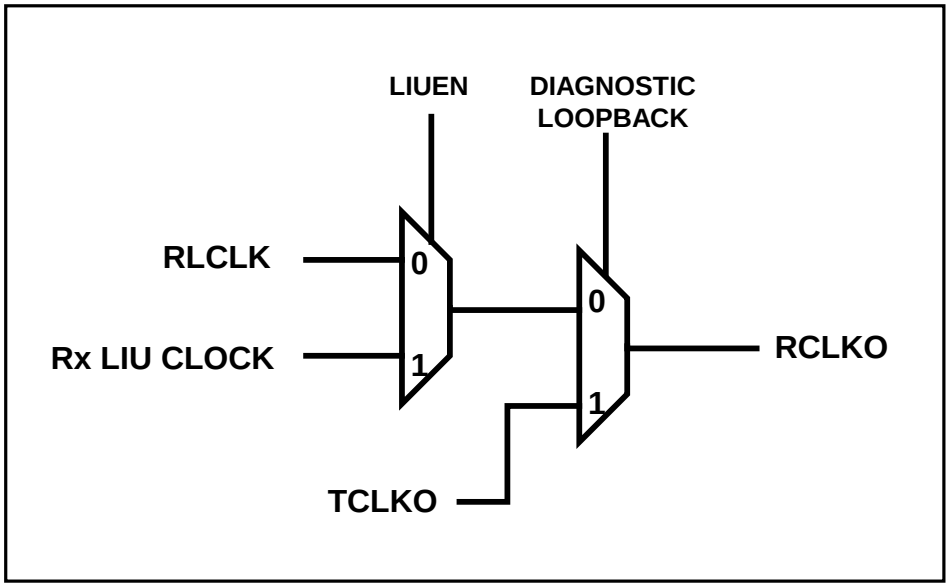


Table 10-5 identifies the source of the output signal RCLKO based on certain variables and register bits.

Table 10-5. Source Selection of RCLKO Clock Signal (Internal Rx Clock)

SIGNAL	LOOPT PORT.CR3	LBM[2:0] (PORT.CR4)	LIUEN	CLADC (PORT.CR3)	SOURCE
RCLKO	1	XXX	1	X	Rx LIU
	1	XXX	0	X	RLCLK
	0	DLB disabled	1	X	Rx LIU
	0	DLB disabled & ALB disabled	0	X	RLCLK
	0	DLB (1XX)	X	0	CLAD
	0	DLB (1XX) or ALB (001)	0	1	TCLKI
	0	DLB (1XX)	1	1	TCLKI

10.2.3 Line IO Pin Timing Source Selection

The line IO pins can use any input clock pin (RLCLK or TCLKI) or output clock pin (TLCLK, RCLKO, or TCLKO) for its clock pin and meet the AC timing specifications as long as the clock signal is valid for the mode the part is in. The clock select bit for the transmit line IO signal group PORT.CR3.TLTS selects the correct input or output clock timing.

10.2.3.1 Transmit Line Interface Pins Timing Source Selection

(TPOS/TDAT, TNEG)

The transmit line interface signal pin group has the same functional timing clock source as the TLCLK pin described in Table 10-3. Other clock pins can be used for the external timing. The TLCLK transmit line clock output pin is always a valid output clock for external logic to use for these signals when PORT.CR3.TLTS=0.

The transmit line timing select bit (TLTS) is used to select input or output clock pin timing. When TLTS=0, output clock timing is selected. When TLTS=1, input clock timing is selected. If TLTS is set for input clock timing and an output clock pin is used, or if TLTS is set for output clock timing and an input clock pin is used, then the setup, hold and delay timings, as specified in Table 16-1, will not be valid. There are some combinations of TLTS=1 and other modes in which there is no input clock pin available for external timing since the clock source is derived internally from the RX LIU or the CLAD.

Table 10-6. Transmit Line Interface Signal Pin Valid Timing Source Select

LOOPT	LBM[2:0]	LIUEN	CLADC	TLTS	VALID TIMING TO THESE CLOCK PINS
1	XXX	X	X	0	TLCLK, TCLKO, RCLKO
1	XXX	0	X	1	RLCLK
1	XXX	1	X	1	No valid timing to any input clock pin
0	DLB (100)	X	X	0	TLCLK, TCLKO, RCLKO
0	LLB (010) or PLB (011)	X	X	0	TLCLK, RCLKO
0	DLB & LLB (110)	X	X	0	TLCLK
0	not DLB (100), not LLB (010), not PLB (011) and not LLB & DLB (110)	X	X	0	TLCLK, TCLKO (default)
0	not LLB (010) and not PLB (011) and not LLB & DLB (110)	X	0	1	No valid timing to any input clock pin
0	not LLB (010) and not PLB (011) and not LLB & DLB (110)	X	1	1	TCLKI
0	LLB (010) or PLB (011) or DLB & LLB (110)	0	X	1	RLCLK
0	LLB (010) or PLB (011) or DLB & LLB (110)	1	X	1	No valid timing to any input clock pin

10.2.3.2 Transmit Framer Pin Timing Source Selection

(TSER, TSOFI, TSOFO/TDEN)

The transmit framer signal pin group has the same functional timing clock source as the TCLKO pin described in Table 10-4. Other clock pins can be used for the external timing. The TCLKO transmit clock output pin is always a valid output clock for external logic to use for these signals when TFTS=0.

The transmit framer select bit (TFTS) is used to select input or output clock pin timing. When TFTS=0, output clock timing is selected. When TFTS=1, input clock timing is selected. If TFTS is set for input clock timing and an output clock pin is used, or If TFTS is set for output clock timing and an input clock pin is used, then the setup, hold and delay timings, as specified in Table 16-1, will not be valid. There are some combinations of TFTS=1 and other modes in which there is no input clock pin available for external timing since the clock source is derived internally from the RX LIU or the CLAD.

Table 10-7. Transmit Framer Pin Signal Timing Source Select

LOOPT	LBM[2:0]	LIUEN	CLADC	TFTS	VALID TIMING TO THESE CLOCK PINS
1	XXX	X	X	0	TCLKO, TLCLK, RCLKO
1	XXX	0	X	1	RLCLK
1	XXX	1	X	1	No valid timing to any input clock pin
0	PLB (011) or DLB (100) or ALB 001)	0	X	0	TCLKO, TLCLK, RCLKO
0	PLB (011) or DLB (100)	1	X	0	TCLKO, TLCLK, RCLKO
0	DLB & LLB (110)	X	X	0	TCLKO, RCLKO
0	LLB (010)	X	X	0	TCLKO
0	not LLB, DLB or PLB (00X)	X	X	0	TCLKO, TLCLK
0	not PLB (011)	X	0	1	No valid timing to any input clock pin
0	not PLB (011)	X	1	1	TCLKI
0	PLB (011)	0	X	1	RLCLK
0	PLB (011)	1	X	1	No valid timing to any input clock pin

10.2.3.3 Receive Line Interface Pin Timing Source Selection

(RPOS/RDAT, RNEG/RLCV)

The receive line interface signal pin group must clocked in with the RLCLK clock input pin. When the LIU is enabled, the receive line interface pins are not used so there is no valid clock reference.

Table 10-8. Receive Line Interface Pin Signal Timing Source Select

LOOPT	LBM[2:0]	LIUEN	CLADC	VALID TIMING TO THESE CLOCK PINS
X	XXX	0	X	RLCLK
X	XXX	1	X	No valid timing to any clock pin

10.2.3.4 Receiver Framer Pin Timing Source Selection

(RSER, RSOFO/RDEN)

The receive framer signal pin group has the same functional timing clock source as the RCLKO pin described in Table 10-5.

Other clock pins can be used for the external timing. The RCLKO receive clock output pin is always a valid output clock for external logic to use for these signals when PORT.CR3.RFTS=0.

The receive framer timing select bit (RFTS) is used to select input or output clock pin timing. When RFTS=0, output clock timing is selected. When RFTS=1, input clock timing is selected. If RFTS is set for input clock timing and an output clock pin is used, or If RFTS is set for output clock timing and an input clock pin is used, then the setup, hold and delay timings, as specified in Table 16-1, will not be valid. There are some combinations of RFTS=1 and other modes in which there is no input clock pin available for external timing since the clock source is derived internally from the RX LIU or the CLAD.

Table 10-9. Receive Framer Pin Signal Timing Source Select

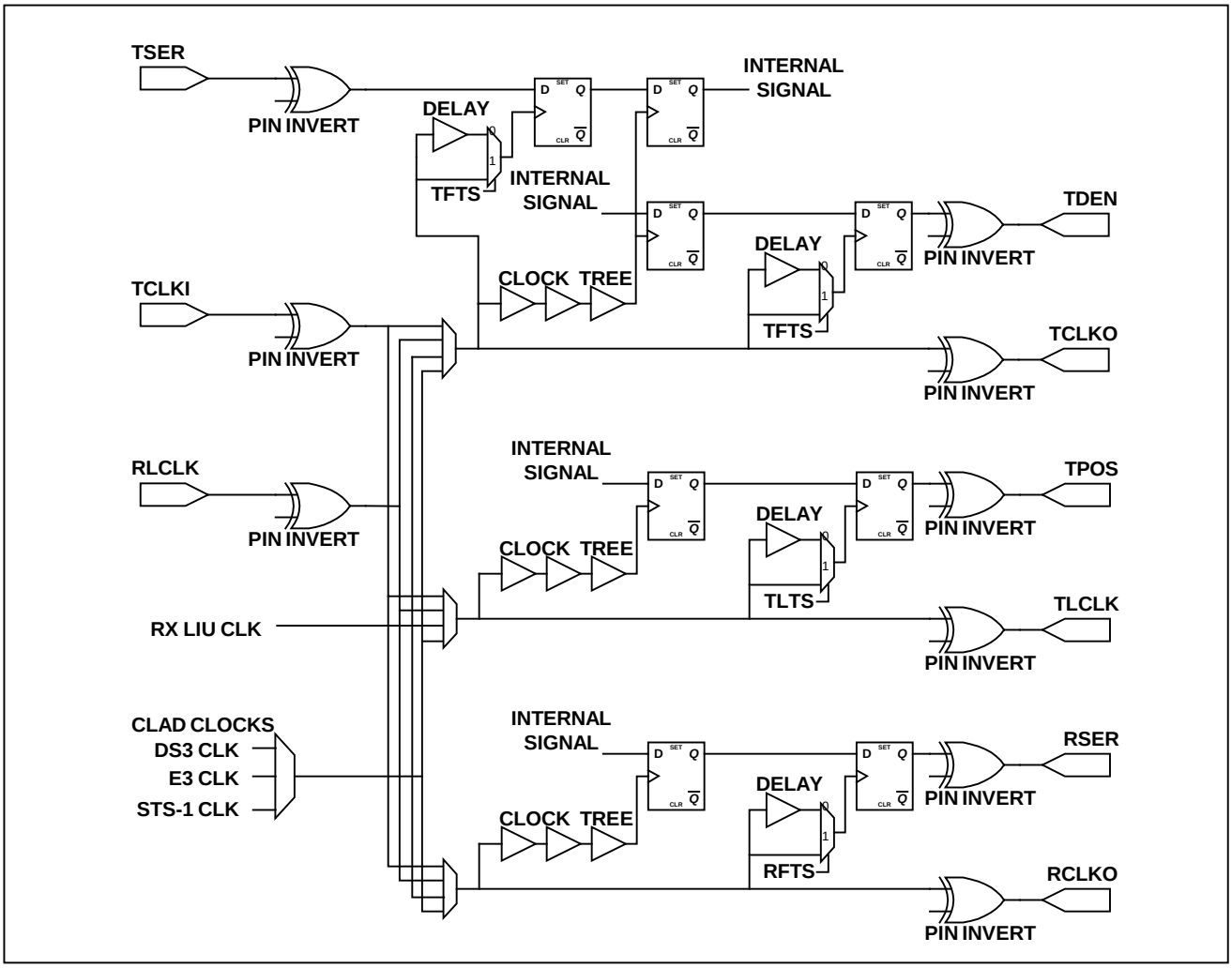
LOOPT	LBM[2:0]	LIUEN	CLADC	RFTS	VALID TIMING TO THESE CLOCK PINS
1	XXX	X	X	0	RCLKO, TLCLK, TCLKO
1	XXX	0	X	1	RLCLK
1	XXX	1	X	1	No valid timing to any input clock pin
0	PLB (011) or DLB (100) or ALB (001)	0	X	0	RCLKO, TLCLK, TCLKO
0	PLB (011) or DLB (100)	1	X	0	RCLKO, TLCLK, TCLKO
0	DLB&LLB (110)	X	X	0	RCLKO, TCLKO
0	LLB (010)	X	X	0	RCLKO, TLCLK
0	not LLB, DLB or PLB (00X)	X	X	0	RCLKO
0	DLB (100) or LLB & DLB (110)	X	0	1	No valid timing to any input clock pin
0	DLB (100) or LLB & DLB (110)	X	1	1	TCLKI
0	not DLB (100) and not LLB & DLB (110)	0	X	1	RLCLK
0	not DLB (100) and not LLB & DLB (110)	1	X	1	No valid timing to any input clock pin

10.2.4 Clock Structures On Signal IO Pins

The signals on the input pins (TSOFI, TSER) can be used with any of the clock pins for setup/hold timing on clock input and output pins. There will be a flop at each input whose clock is connected to the signal from the input or output clock source pins with as little delay as possible from the signal on the clock IO pins. This means using the input clock signal before the delays of the internal clock tree to clock the input signals, and using the output clock signals used to drive the output clock pins to clock the input signals.

The signals on the output pins (TPOS/TDAT, TNEG, TSOFO/TDEN, RSER, RSOFO/RDEN) can be with any of the clock sources for delay timing. There will be a flop at each output whose clock is connected to the signal from the input or output clock source pins with as little delay as possible from the signal on the clock IO pins. This means using the input clock signal before the delays of the internal clock tree to clock the input signals, and using the output clock signals used to drive the output clock pins to clock the input signals.

Figure 10-4. Example IO Pin Clock Muxing



10.2.5 Gapped Clocks

The transmit and receive output clocks can be gapped in certain configurations. See Table 10-22 and Table 10-24 for the configuration settings. The gapped clocks are active during DS3 or E3 framed payload bits overhead bits depending on which mode the device is configured for.

In the internal DS3 or E3 frame modes, the transmit gapped clock is created by the logical OR of the TCLKO and TDEN signals creating a positive or negative clock edge for each payload bit, the receive gapped clock is created by the logical OR of the RCLKO and RDEN signals.

When the output clock is disabled, the gapped output signal is high during clock periods if the pin is not inverted, otherwise it will be low.

The gapped clocks are very useful when the data being clocked does not need to be aligned with any frame structure. The data is simply clocked one bit at a time as a continuous data stream.

10.3 Reset and Power-Down

The device can be reset at a global level via the GL.CR1.RST bit or the $\overline{\text{RST}}$ pin and at the port level via the PORT.CR1.RST bit and the port can be explicitly powered down via the PORT.CR1.PD bit. The JTAG logic is reset using the power on reset signal from one of the LIUs as well as from the $\overline{\text{JTRST}}$ pin.

The external $\overline{\text{RST}}$ pin and the global reset bit in the global configuration register (GL.CR1.RST) are combined to create an internal global reset signal. The global reset signal resets all the status and control registers on the chip, except the GL.CR1.RST bit, to their default values and resets all the other flops in the global logic and port to their

reset values. The processor bus output signals are also forced to be HIZ when the $\overline{RST}$ pin is active (low). The global reset bit (GL.CR1.RST) stays set after a one is written to it, but is reset to zero when the external $\overline{RST}$ pin is active or when a zero is written to it.

At the port level, the global reset signal combines with the port reset bit in the port control register (PORT.CR1.RST) to create a port reset signal. The port reset signal resets all the status and control registers on the port to their default values and resets all the other flops, except PORT.CR1.RST, to their reset values. The port reset bit (PORT.CR1.RST) stays set after a one is written to it, but is reset to zero when the global reset signal is active or when a zero is written to it.

The data path reset function is a little different from the "general" reset function. The data path reset signal does not reset the control register bits, but it does reset all of the status registers, counters and flops, the "general" reset signal resets everything including the control register bits, excluding the reset bit. All clocks are functional, being controlled by configuration bits, while data path reset is active. The LIU and CLAD circuits will be operating normally during data path reset which allows the internal phase locked loops to settle as quickly as possible. The LIU will be sending all zeroes (LOS) since data path reset will be forcing the transmit TPOS and TNEG to logic zero. (NOTE: The BERT data path does not get reset when PORT.CR1.RSTDP is active.)

The global data path reset bit (GL.CR1.RSTDP) gets set to one when the global reset signal is active. The port data path reset bit (PORT.CR1.RSTDP) and the port power-down bit (PORT.CR1.PD) bit gets set to one when the port reset signal is active. These control bits will be cleared when a zero is written to them when the port reset signal is not active. The global data path reset signal is active when the global data path reset bit is set. The port data path reset signal is active when either the global data path reset bit or the port data path reset bit is set. The port power-down signal is active when the port power-down bit is set.

Figure 10-5. Reset Sources

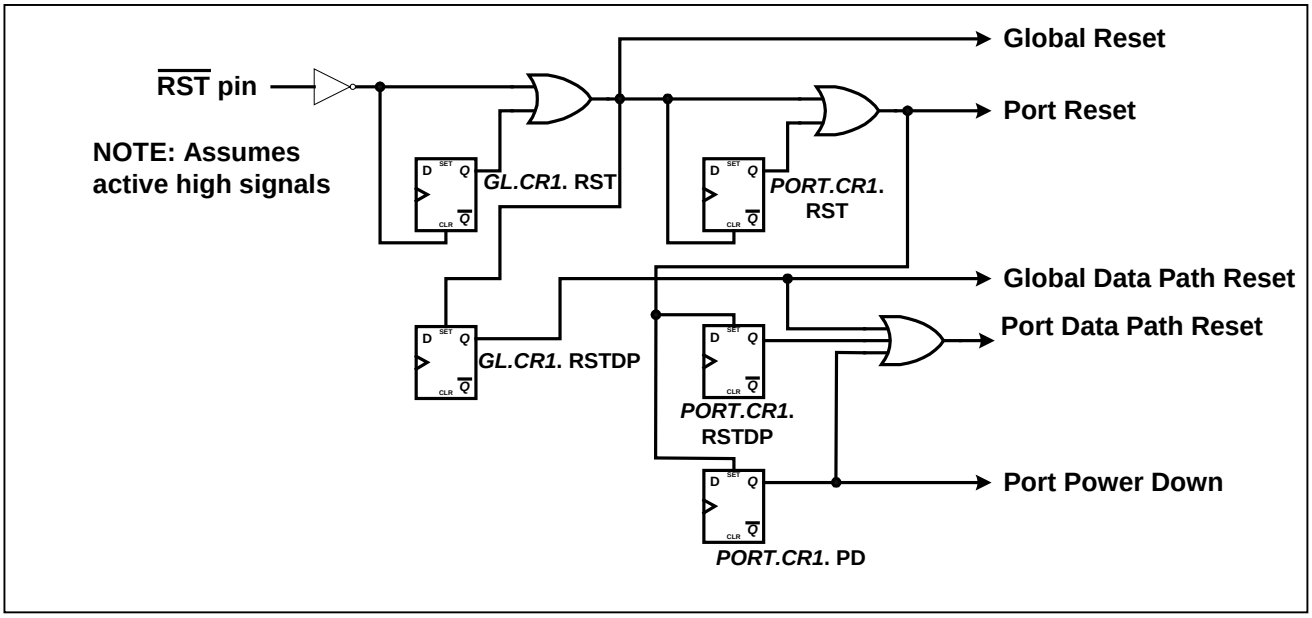


Table 10-10. Reset and Power-Down Sources

PIN	REGISTER BITS					INTERNAL SIGNALS				
$\overline{RST}$	G:RST	G:RSTDP	P:RST	P:RSTDP	P:PD	Global reset	Global dp reset	Port reset	Port dp reset	Port power dn
0	F0	F1	F0	F1	F1	1	1	1	1	1
1	1	F1	F0	F1	F1	1	1	1	1	1
1	0	1	1	F1	F1	0	1	1	1	1
1	0	1	0	X	1	0	1	0	1	1
1	0	1	0	X	0	0	1	0	1	0
1	0	0	1	F1	F1	0	0	1	1	1
1	0	0	0	1	1	0	0	0	1	1
1	0	0	0	1	0	0	0	0	1	0
1	0	0	0	0	1	0	0	0	1	1
1	0	0	0	0	0	0	0	0	0	0

Register Bit States—F0: Forced to 0; F1: Forced to 1; 0: Set to 0; 1: Set to 1; X: Don't care
Forced: Internally controlled; Set: User controlled

The reset signals in the device are asynchronous so they no not require a clock to put the logic into the reset state. Clock signals may be needed to make the logic come out of the reset state.

The power-down function disables the appropriate clocks to cause the logic to generate a minimum of power. It also puts the LIU circuits into the power-down mode. The 8KREF and ONESEC circuits can be powered down by disabling the 8KREF source. The CLAD can also be powered down by disabling it.

After a global reset, all of the control and status registers are set to their default values and all the other flops are reset to their reset values. The global register GL.CR1.RSTDP, and the port register PORT.CR1.RSTDP and PORT.CR1.PD bits, are set after the global reset. A valid initialization sequence would be to clear the PORT.CR1.PD bit, write to all of the configuration registers to set them in the desired modes, then clear the GL.CR1.RSTDP and PORT.CR1.RSTDP bits. This would cause the logic in the port to start up in a repeatable sequence. The device can also be initialized by clearing the GL.CR1.RSTDP, PORT.CR1.RSTDP and PORT.CR1.PD them writing to all of the configuration registers to set them in the desired modes, and clearing all of the latched status bits. The second initialization scheme could cause the device to temporarily go into modes of operation that were not requested, but will quickly go into the requested modes of operation.

Some of the IO pins are put in a known state at reset. The transmit LIU outputs TXP and TXN are quiet and will not drive positive or negative pulses. The global IO pins (GPIO[7:0]) are set as inputs at global reset. The port output pins (TLCLK, TPOS/TDAT, TNEG, TOHCLK, TOHSOF, TSOFO/TDEN, TCLKO/TGCLK, ROH, ROHCLK, ROHSOF, RSER, RSOFO/RDEN, RCLKO/RGCLK) are driven low at global or port reset and should stay low until after the port power-down PORT.CR1.PD and port data path reset PORT.CR1.RSTDP bits are cleared. The processor port three-state output pins (D[15:0], $\overline{RDY}$, $\overline{INT}$) are forced into the high impedance state when the $\overline{RST}$ pin is active, but not when the GL.CR1.RST bit is active.

After reset, the device will be in the default configuration:: The latched status bits are enabled to be cleared on write. The CLAD is disabled. The global 8KREF and one-second timers are disabled. The line interface is in B3ZS mode and the LIU is disabled and the transmit line pins are also disabled. The frame mode is DS3 C-bit with automatic downstream AIS on LOS or OOF is enabled and automatic RDI on LOF, LOS, SEF or AIS is enabled and automatic FEBE is enabled. Transmit clock comes from the REFCLK pin. The pin inversion on all pins is disabled.

Individual blocks are reset and powered down when not used determined by the settings in the line mode bits PORT.CR2.LM[2:0] and framer mode bits PORT.CR2.FM[2:0].

10.4 Global Resources

10.4.1 Clock Rate Adapter (CLAD)

The clock rate adapter is composed of a PLL block to create the internal clock which can be used for the transmit clock and/or LIU reference clock from a clock input on the reference input (REFCLK) pin. The device needs one of two (DS3 or E3) internal clock rates. The input reference clock frequency can be either 44.736, 34.368. 77.78, 51.84 or 19.44 MHz.

The receive LIU is supplied a reference clock from the CLAD. The receive LIU selects the clock frequency based upon the mode the user selects via the FM bits. The CLAD output is also available as a transmit clock source if selected via the PORT.CR2.CLADC register bit.

The user must supply at least one of the five rates (44.736, 34.368. 77.78, 51.84 or 19.4 MHz) to the REFCLK pin. The CLAD[2:0] bits informs the PLL of the frequency applied to the pins. Selection of the clock applied to the LIU and optionally the transmitter is controlled by the FM bits (located in PORT.CR2). The CLAD allows maximum flexibility to the user. The user may supply any of the five clock rates and use the CLAD to convert the rate to the particular clock rate needed for his application.

The CLAD PLL is enabled when the CLAD input reference clock is different from the clock required for the framing mode. The CLAD PLL is disabled and the CLAD output clock is connected directly to the CLAD input clock (REFCLK) when the framing mode requires the same clock as the CLAD input reference clock.

Table 10-11. CLAD Clock Source Settings

CLAD[2:0]	REFCLK (INPUT)
000	44.736 MHz
001	34.368 MHz
010	51.84 MHz
011	19.44 MHz
100	77.76 MHz
101	Undefined
11X	Undefined

10.4.2 8 kHz Reference Generation

The global 8KREF signal is used to generate the one second reference signal by dividing it by 8000. This signal can be derived from almost any clock source on the chip as well as the general purpose IO pin GPIO4. The port 8KREF signal can be sourced from the transmit or receive clocks. The minimum input frequency stability of the 8KREF input pin is +/- 500 ppm.

The global 8KREF signal can come from an external 8000 Hz reference connected to the GPIO4 general purpose IO pin by setting the GL.CR2.G8KIS bit. The global 8KREF signal can be output on the GPIO2 general purpose IO pin when the GL.CR2.G8KOS bit is set.

The global 8KREF signal can be derived from the CLAD PLL or pins or come from any of the port 8KREF signals by clearing GL.CR2.G8KIS bit and selecting the source using the GL.CR2.G8KRS[2:0] bits.

The port 8KREF signal can be derived from the transmit clock input pin or from the receive LIU or input clock pin. The PORT.CR3.P8KRS[1:0] bits are used to select which source.

The 8KREF 8.000 kHz signal is a simple divisor of 44736 kHz (DS3 divided by 5592) or 33368 kHz (E3 divided by 4296). The correct divisor for the port 8KREF source is selected by the mode the port is configured for. The CLAD clock chosen for the clock source selects the correct divisor for the global 8KREF. The 8KREF signal is only as accurate as the clock source chosen to generate it.

Table 10-12 lists the selectable sources for global 8 kHz reference.

Table 10-12. Global 8 kHz Reference Source Table

GL.CR2. G8KIS	GL.CR2. G8KRS[1:0]	SOURCE
0	00	None, the 8KHZ divider is disabled.
0	01	Derived from CLAD output clock
0	10	8KREF source selected by P8KRS[1:0]
0	11	Undefined
1	XX	GPIO4

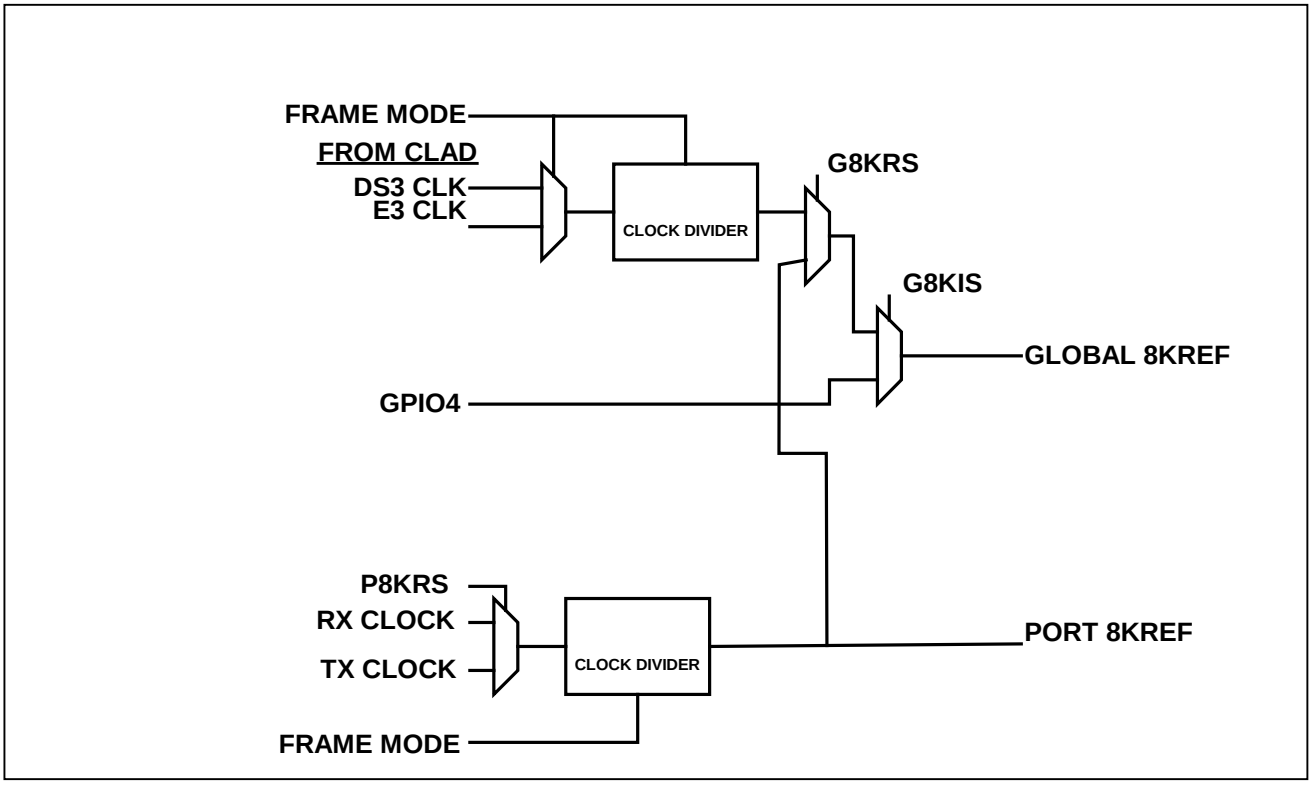
Table 10-13 lists the selectable sources for port 8 kHz reference sources.

Table 10-13. Port 8 kHz Reference Source Table

PORT.CR3.P8KRS[1:0]	SOURCE
0X	Undefined
10	Internal receive framer clock
11	Internal transmit framer clock

Figure 10-6 shows the 8 kHz reference logic tree.

Figure 10-6. 8KREF Logic



10.4.3 One Second Reference Generation

The one second reference signal is used as an option to update the performance registers on a precise one second interval. The generated internal signal should be about 50% duty cycle and it is derived from the Global 8 kHz reference signal by dividing it by 8000. The low to high edge on this signal will set the GL.SRL.ONESL latched one second detect bit which can generate an interrupt when the GL.SRIE.ONESIE interrupt enable bit is set. The low to high edge can also be used to generate performance monitor updates when GL.CR1.GPM[1:0]=1X.

10.4.4 General-Purpose IO Pins

There are eight general-purpose IO pins that can be used for general IO, global signals and framer alarm signals. Each pin is independently configurable to be a general-purpose input, general-purpose output, global signal or framer alarm. Two of the GPIO pins can be programmed to output one or two framer alarm statuses. One of the two pins assigned to framer alarms can be programmed as global input or output signals. When the port is powered down or reset and GL.GIOCR.GPIOx[1:0] = 01, the GPIO pin will be an output driving low. The 8KREFI, TMEI, and PMU signals that can be sourced by the GPIO pin will be driven low into the core logic when the GPIO pin is not selected for the source of the signal.

Table 10-14 lists the purpose and control thereof of the General-Purpose IO Pins.

Table 10-14. GPIO Global Signals

PIN	GLOBAL SIGNAL	CONTROL BIT
GPIO2	8KREFO output	GL.CR2.G8KOS
GPIO4	8KREFI input	GL.CR2.G8KIS
GPIO6	TMEI input	GL.CR1.MEIMS
GPIO8	PMU input	GL.CR1.GPM[1:0]

Table 10-15 describes the selection of mode for the GPIO Pins.

Table 10-15. GPIO Pin Global Mode Select Bits

GL.GIOCR.GPIOSx	GPIO PIN MODE
00	Input
01	Framer alarm status selected by port GPIO
10	Output logic 0
11	Output logic 1

x = A or B, valid when a GPIO pin is not selected for a global signal

Table 10-16 lists the various port alarm monitors that can be output on the GPIO pins. The GPIO(A/B)[3:0] bits are located in the PORT.CR4 Register.

Table 10-16. GPIO Port Alarm Monitor Select

PORT.CR4 GPIO(A/B)[3:0]	LINE LOS	DS3/E3 OOF	DS3/E3 LOF	DS3/E3 AIS	DS3/E3 RAI	DS3 IDLE
0000	X					
0001		X				
0010			X			
0011				X		
0100					X	
0101						X
0110						
0111						
1000						
1001						
1010						
1011	X		X	X		
1100						
1101	X		X	X		
1110					X	X
1111	X	X	X	X	X	X

10.4.5 Performance Monitor Counter Update Details

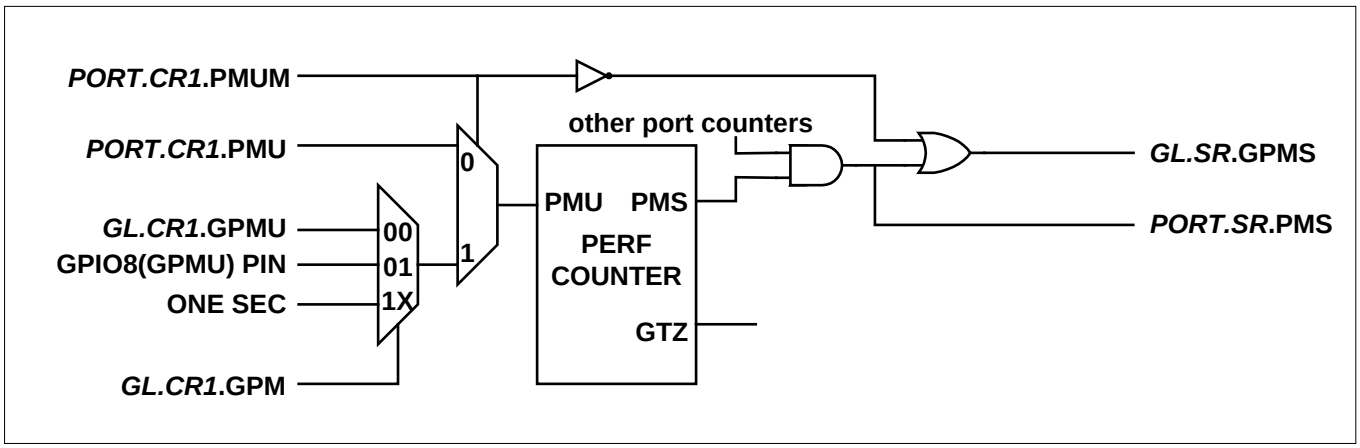
The performance monitor counters are designed to count at least one second of events before saturating to the maximum count. There is a status bit associated with some of the performance monitor counters that is set when the its counter is greater than zero, and a latched status bit that gets set when the counter changes from zero to one. There is also a latched status bit that gets set on every event that causes the error counter to increment.

There is a read register for each performance monitor counter. The count value of the counter gets loaded into this register and the counter is cleared when the update-clear operation is performed. If there is an event to be counted at the exact moment (clock cycle) that the counter is to be cleared then the counter will be set to a value of one so that that event will be counted.

The Performance Monitor Update signal affects the counter registers of the following blocks: the BERT, the DS3/E3 framer, the Line Encoder/Decoder.

The update-clear operation is controlled by the Performance Monitor Update signal (PMU). The update-clear operation will update the error counter registers with the value of the error counter and also reset each counter. The PMU signal can be created in hardware or software. The hardware sources can come from the one second counter or one of the general-purpose IO pins, which can be programmed to source this signal. The software sources can come from one of the port control register bits or one of the global control register bits. When using the software update method, the PMU control bit should be set to initiate the process and when the PMS status bit gets set, the PMU control bit should be cleared making it ready for the next update. When using the hardware update method, the PMS bit will be set shortly after the hardware signal goes high, and cleared shortly after the hardware signal goes low. The latched PMS signal can be used to generate an interrupt for reading the count registers. If the port is not configured for global PMU signals, the PMS signal from that port should be blocked from affecting the global PMS status.

Figure 10-7. Performance Monitor Update Logic

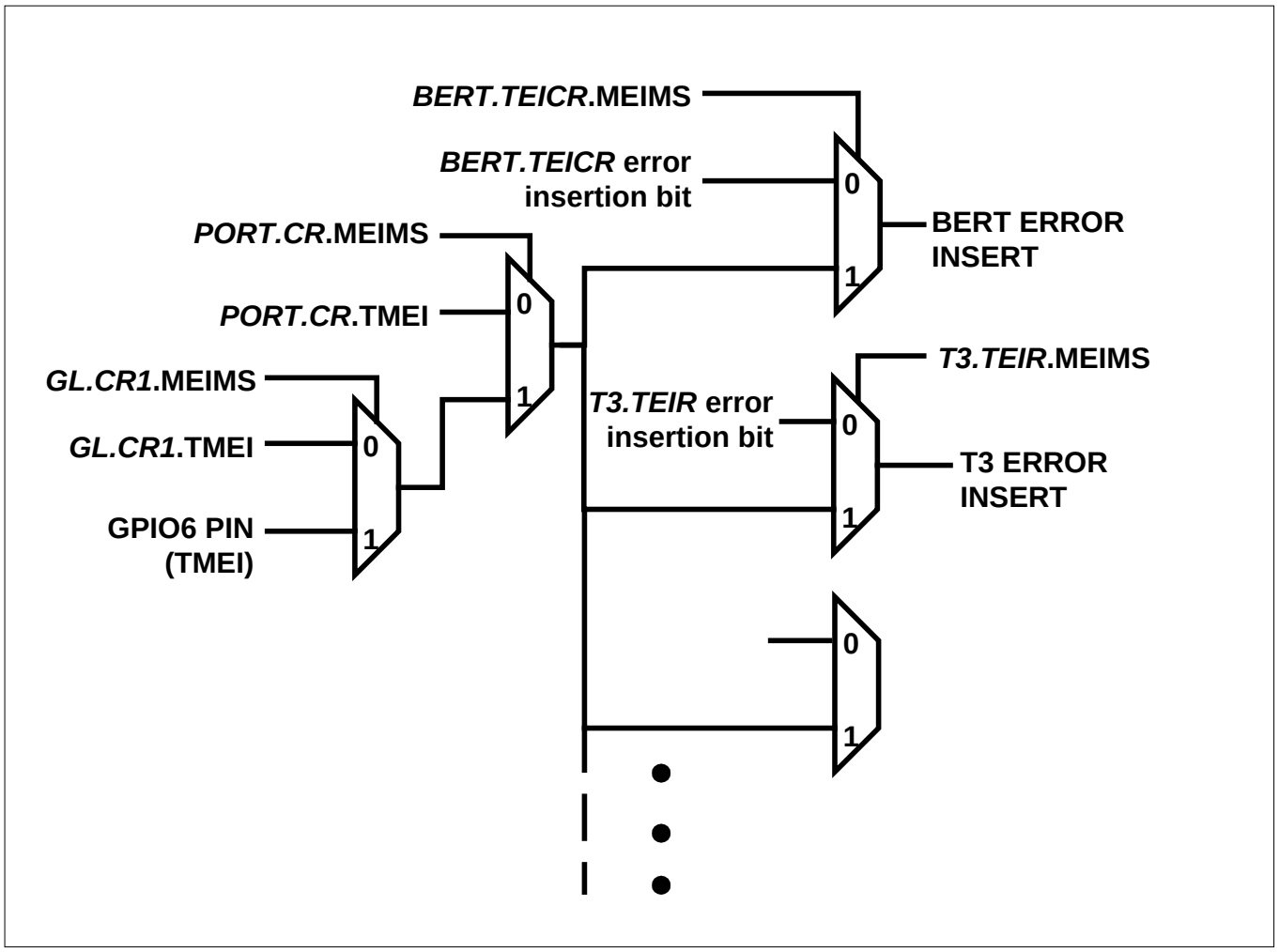


10.4.6 Transmit Manual Error Insertion

Transmit errors can be inserted in some of the functional blocks. These errors can be inserted using register bits in the functional blocks, using the global GL.CR1.TMEI bit, using the port PORT.CR1.TMEI bit, or by using the GPIO6 pin configured for TMEI mode.

There is a transmit error insertion register in the functional blocks that allow error insertion. The MEIMS bit controls whether the error is inserted using the bits in the error insertion register or using error insertion signals external to that block. When bit MEIMS=0, errors are inserted using other bits in the transmit error insertion register. When bit MEIMS=1, errors are inserted using a signal generated in the port or global control registers or using the external GPIO6 pin configured for TMEI operation.

Figure 10-8. Transmit Error Insert Logic



10.5 Port Resources

10.5.1 Loopbacks

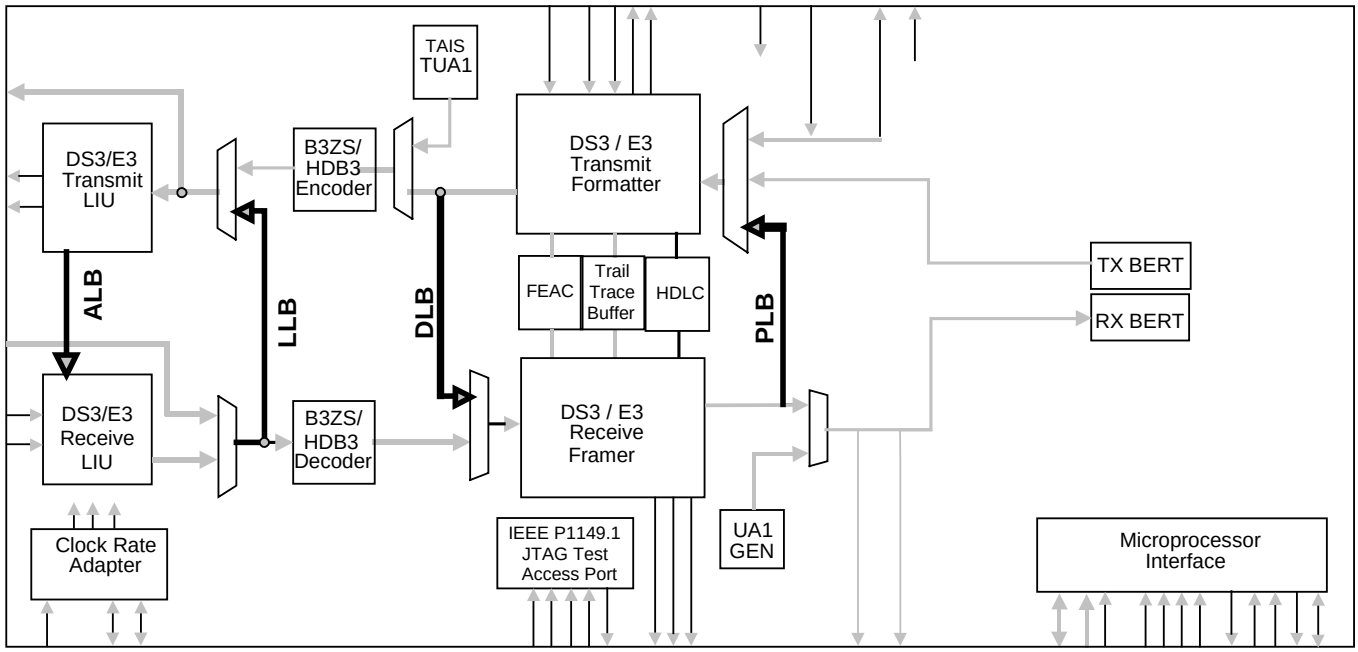
There are several loop back paths available. The following table lists the loopback modes available for analog loopback (ALB), line loopback (LLB), payload loopback (PLB) and diagnostic loopback (DLB). The LBM bits are located in PORT.CR4.

Table 10-17. Loopback Mode Selections

LBM[2:0]	ALB	LLB	PLB	DLB
000	0	0	0	0
001	1	0	0	0
010	0	1	0	0
011	0	0	1	0
10X	0	0	0	1
110	0	1	0	1
111	0	0	0	1

Figure 10-9 highlights where each loopback mode is located and gives an overall view of the various loopback paths available.

Figure 10-9. Loopback Modes

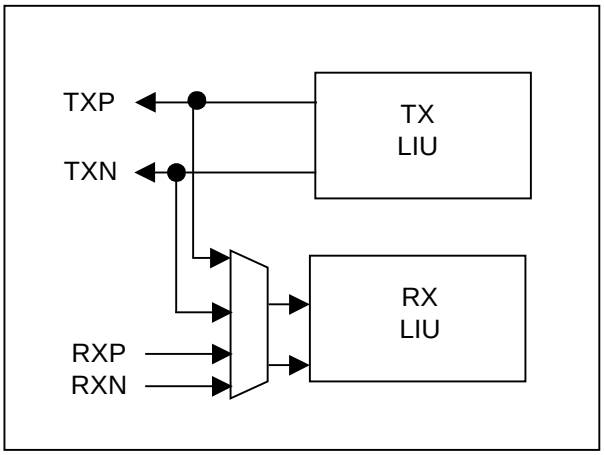


10.5.1.1 Analog Loopback (ALB)

Analog loopback is enabled by setting PORT.CR4.LBM[2:0] = 001. Analog loopback mode will not be enabled when the port is configured for loop timed mode (set via the PORT.CR3.LOOPT bit).

The analog loopback is a loopback as close to the pins as possible. When both the Tx and RX LIU is enabled, it loops back TXP and TXN to RXP and RXN, respectively. If the transmit signals on TXP and TXN are not terminated properly, this loopback path may have data errors or loss of signal. When the LIU is not enabled, it loops back TLCLK,TPOS / TDAT,TNEG to RLCLK, RPOS / RDAT , RNEG.

Figure 10-10. ALB Mux



10.5.1.2 Line Loopback (LLB)

Line loopback is enabled by setting PORT.CR4.LBM[2:0] = X10. DLB and LLB are enabled at the same time when LBM[2:0] = 110, and only LLB is enabled when LBM[2:0] = 010.

The clock from the receive LIU or the RLCLK pin will be output to the transmit LIU or TCLKO pin. The POS and NEG data from the receive LIU or the RPOS and RNEG pin will be sampled with the receive clock to time it to the LIU or pin interface.

When LLB is enabled, unframed all ones AIS can optionally be automatically enabled on the receive data path. This AIS signal will be output on the RSER pin in framed modes. When DLB and LLB is enabled, the AIS signal will not be transmitted. See Figure 10-9.

10.5.1.3 Payload Loopback (PLB)

Payload loopback is enabled by setting PORT.CR4.LBM[2:0] = 011.

The payload loopback copies the payload data from the receive framer to the transmit framer which then re-frames the payload before transmission. Payload loopback is operational in all framing modes.

When PLB is enabled, unframed all ones AIS transmission can optionally be automatically enabled on the receive data path. This AIS signal will be output on the RSER. In all PLB modes, the TSOFI input pin is ignored.

The external transmit output pins TDEN and TSOFO/TDEN can optionally be disabled by forcing a zero when PLB is enabled. See Figure 10-9.

10.5.1.4 Diagnostic Loopback (DLB)

Diagnostic loopback is enabled by setting PORT.CR4.LBM[2:0] = 1XX. DLB and LLB are enabled at the same time when LBM[2:0] = 110, only DLB is enabled when LBM[2:0] = 10X or 111.

The Diagnostic loopback sends the transmit data, before line encoding, back to the receive side.

Transmit AIS can still be enabled using PORT.CR1.LAIS[2:0] even when DLB is enabled. See Figure 10-9.

10.5.2 Loss Of Signal Propagation

The Loss Of Signal (LOS) is detected in the line decoder logic. In unipolar (UNI) line interface modes LOS is never detected. The LOS signal from the line decoder is sent to the DS3/E3 framer and the top level payload AIS logic except when DLB is activated. When DLB is activated the LOS signal to the framer and AIS logic is never active. The LOS status in the line decoder status register is valid in all frame and loop back modes, though it is always off in the line interface is in the UNI mode.

10.5.3 AIS Logic

There is AIS logic in both the framers and at the top level logic of the port. The framer AIS is enabled by setting the TAIS bit in the appropriate framer transmit control register (T3, E3-G.751, E3-G.832, or Clear Channel). The top level AIS is enabled by setting the PORT.CR1.LAIS[2:0] bits (see Table 10-18). The AIS signal is an unframed all ones pattern or a DS3 framed 101010… pattern depending on the FM[2:0] mode bits. The DS3 Framed Alarm Indication Signal (AIS) is a DS3 signal with valid F-bits, M-bits, and P-bits (P_1 and P_2). The X-bits (X_1 and X_2) are set to one, all C-bits (C_{XY}) are set to zero, and the payload bits are set to a 1010 pattern starting with a one immediately after each overhead bit. The DS3 framed AIS pattern is only available in DS3 modes. The unframed all ones pattern is available in all framing modes including the DS3 modes. The transmit line interface can send both unframed all ones AIS and DS3 framed AIS patterns from either the AIS generator in the framer or the AIS generator at the top level.

The AIS signal generated in the framer can be initiated and terminated without introducing any errors in the signal. When the unframed AIS signal is initiated or terminated, there will be no BPV or CV errors introduced, but there will be framing errors if a framed mode is enabled. When the DS3 framed AIS signal is initiated or terminated, in addition to no BPV or CV errors, there should be no framing or P-bit (parity) or CP-bit errors introduced.

The AIS signal generated at the top level will not generate BPV errors but may generate P-bit and CP-bit errors when the signal is initiated and terminated. The framed DS3 AIS signal will not cause the far end receiver to re-sync when the signal is initiated, but it may cause a re-sync when terminated if the DS3 frame position in the framer is changed while the DS3 AIS signal is being generated. A sequence of events can be executed which will enable the initiation and termination of DS3 AIS or unframed all ones at the top level without any errors introduced.

The sequence will only work when the automatic AIS generation is not enabled. CV and P-bit errors can occur when AIS is automatically generated and can not be avoided. This sequence to generate an error free DS# AIS at the top level is to have the DS3 AIS or unframed all ones signal initiate in the DS3 framer, and a few frames sent before initiating or terminating the DS3 AIS or unframed all ones at the top level. After the top level AIS signal is activated, the AIS signal in the framer can be terminated, DLB activated and diagnostic patterns generated. The DS3 AIS signal generated at the top level will not change frame alignment after starting even if the DS3 frame position in the framer is changed.

The transmit line AIS generator at the top level can generate AIS signals even when the framer is looped back using DLB, but not when the line is looped back using LLB. The AIS signal generated in the framer will be looped back to the receive side when DLB is activated.

The receive framer can detect both unframed all ones AIS and DS3 framed AIS patterns. When in DS3 framing modes, both framed DS3 AIS and unframed all ones can be detected. In E3 framing modes E3 AIS, which is unframed all ones, is detected.

The receive payload interface going to the RSER pin or the BERT logic can have an unframed all ones AIS signal replacing the receive signal, this is called Payload AIS. The all ones AIS signal is generated from either the DS3/E3 framer or the downstream top level unframed all ones AIS generator. The unframed all ones AIS signal generated in the framer will be looped back to the transmit side when PLB is activated. The unframed all ones AIS signal generated at the top level will be sent to the RSER pin and other receive logic, but not to the transmit side while PLB is activated. The top level AIS generator is used when a downstream AIS signal is desired while payload loop back is activated and is enabled by default after rest and must be cleared during configuration. Note that the downstream AIS circuit in the framer, when a DS3 mode is selected, enforces the OOF to be active for 2.5 msec before activating when automatic AIS in the framer is enabled. The top level downstream AIS will be generated with no delay when OOF is detected when automatic AIS at the top level is enabled.

There is no detection of any AIS signal on the transmit payload signal from the TSER pin or anywhere on the transmit data path.

The transmit AIS generator at the top level can also be activated with a software bit or automatically when DLB is activated. The receive AIS generator in the framer can be activated with a software bit, and automatically when AIS, LOS or OOF are detected. The receive payload AIS generator at the top level can be activated with a software bit or automatically when LOS, DS3/E3 OOF, LLB, or PLB is activated.

Figure 10-11 shows the AIS signal flow through the device.

Figure 10-11. AIS Signal Flow

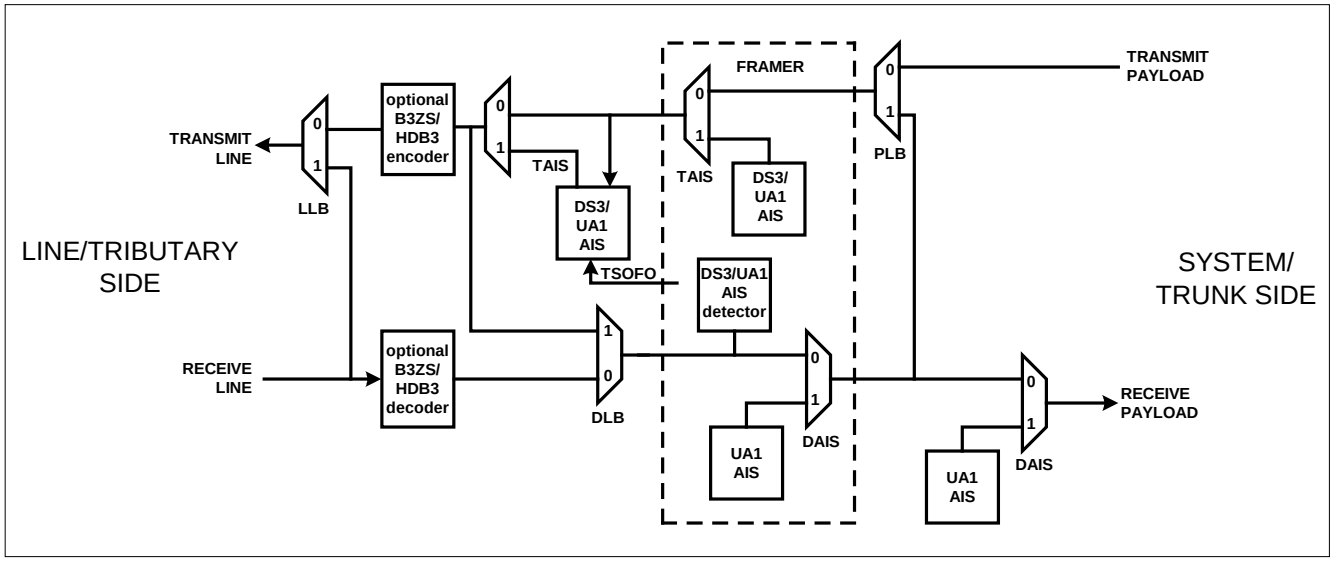


Table 10-18 lists the LAIS decodes for various line AIS enable modes.

Table 10-18. Line AIS Enable Modes

LAIS[1:0] PORT.CR1	FRAME MODE	DESCRIPTION	AIS CODE
00	DS3	Automatic AIS when DLB is enabled (PORT.CR4.LBM = 1XX)	DS3AIS
00	E3	Automatic AIS when DLB is enabled	UA1
01	Any	Send UA1	UA1
10	DS3	Send AIS	DS3AIS
10	E3	Send AIS	UA1
11	Any	Disable	none

Table 10-19 lists the PAIS decodes for various payload AIS enable modes.

Table 10-19. Payload (Downstream) AIS Enable Modes

PAIS[2:0] PORT.CR1	WHEN AIS IS SENT	AIS CODE
000	Always	UA1
001	When LLB (no DLB) active	UA1
010	When PLB active	UA1
011	When LLB(no DLB) or PLB active	UA1
100	When LOS (no DLB) active	UA1
101	When OOF active	UA1
110	When OOF, LOS. LLB (no DLB), or PLB active	UA1
111	Never	none

10.5.4 Loop Timing Mode

Loop timing mode is enabled by setting the *PORT.CR3*.LOOPT bit. This mode replaces the clock from the TCLKI pin with the internal receive clock from either the RLCLK pin if the RX LIU is disabled, or the recovered clock from the RX LIU if it is enabled. The loop timing mode can be activated in any framing or line interface mode.

10.5.5 HDLC Overhead Controller

The data signal to the receive HDLC controller will be forced to a one while still being clocked when the framer (DS3, E3), to which the HDLC is connected, detects LOF or AIS. Forcing the data signal to all ones will cause an HDLC packet abort if the data started to look like a packet instead of allowing a bad, and possibly very long, HDLC packet.

10.5.6 Trail Trace

There is a single Trail Trace controller for use in line maintenance protocols. The E3-G.832 framer has access to the trail trace controller.

10.5.7 BERT

There is a Bit Error Rate Test (BERT) circuit for use in generating and detecting test signals in the payload bits. The BERT can generate and detect PRBS patterns up to 2^32-1 bits as well as repeating patterns up to 32 bits

long. The generated BERT signal replaces the data on the TSER pin in framed modes when the BERT is enabled by setting the PORT.CR1.BENA.

When the BERT is enabled The TDEN and RDEN pins will still be active but the data on the TSER pin will be discarded.

10.5.8 System Port Pins

The system port pins have multiple functions based on the framing mode the device is in as well as other pin mode select bits.

10.5.8.1 Transmit System Port Pins

The transmit system pins are TSOFI, TSER, TSOFO / TDEN, and TCLKO / TGCLK. They have different functions based on the framing mode and other pin mode bits. Unused input pin functions should drive a logic zero into the device circuits expecting a signal from that pin. The control bits that configure the pins' modes are PORT.CR2.FM[2:0], PORT.CR3.TPFPE, PORT.CR3.TSOFOS and PORT.CR3.TCLKS.

Table 10-20 to Table 10-22 describe the function selected by the FM bits and other pin mode bits for the multiplexed pins.

Table 10-20. TSOFI Input Pin Functions

FM[2:0] PORT.CR2	PIN FUNCTION
0XX (FRM)	TSOFI
1XX (UFRM)	Not used

Table 10-21. TSOFO/TDEN/Output Pin Functions

FM[2:0] PORT.CR2	TSOFOS PORT.CR3	PIN FUNCTION
0XX (FRM)	0	TDEN
0XX (FRM)	1	TSOFO
1XX (UFRM)	X	High

Table 10-22 TCLKO/TGCLK Output Pin Functions

FM[2:0] PORT.CR2	TCLKS PORT.CR3	PIN FUNCTION	GAP SOURCE
0XX (FRM)	0	TGCLK	TDEN
0XX (FRM)	1	TCLKO	none
1XX (UFRM)	X	TCLKO	none

10.5.8.2 Receive System Port Pins

The receive system pins are RSER, RSOFO / RDEN and RCLKO / RGCLK. They have different functions based on the framing mode and other pin mode bits. Unused input pin functions should drive a logic zero into the device circuits expecting a signal from that pin. The control bits that configure these pins are PORT.CR2.FM[2:0], PORT.CR3.RPFPE, PORT.CR3.RSOFOS and PORT.CR3.RCLKS.

Table 10-23 to Table 10-24 describe the function selected by the FM bits and other pin mode bits for the multiplexed pins.

Table 10-23. RSOFO/RDEN Output Pin Functions

FM[2:0] PORT.CR2	RSOFOS PORT.CR3	PIN FUNCTION
0XX (FRM)	0	RDEN
0XX (FRM)	1	RSOFO
1XX (UFRM)	X	High

Table 10-24. RCLKO/RGCLK Output Pin Functions

FM[2:0] PORT.CR2	RCLKS PORT.CR3	PIN FUNCTION	GAP SOURCE
0XX (FRM)	0	RGCLK	RDEN
0XX (FRM)	1	RCLKO	none
1XX (UFRM)	X	RCLKO	none

10.5.9 Framing Modes

The framing modes are selected independently of the line interface modes using the *PORT.CR2*.FM[2:0] control bits. Different blocks are used in different framing modes. The bit error test (BERT) function can be enabled in any mode. The LIU, JA and line encoder/decoder blocks are selected by the line mode (LM[2:0]) code.

Table 10-25. Framing Mode Select Bits FM[2:0]

FM[2:0]	DESCRIPTION	LINE CODE	FIGURE
0 00	DS3 C-bit Framed	B3ZS/AMI/UNI	Figure 7-1
0 01	DS3 M23 Framed	B3ZS/AMI/UNI	Figure 7-1
0 10	E3 G.751 Famed	HDB3/AMI/UNI	Figure 7-1
0 11	E3 G.832 Framed	HDB3/AMI/UNI	Figure 7-1
1 00	DS3 Unframed	B3ZS/AMI/UNI	Figure 7-2
1 01	Undefined	---	
1 10	E3 Unframed	HDB3/AMI/UNI	Figure 7-2
1 11	Undefined	---	

10.5.10 Line Interface Modes

The line interface modes can be selected semi-independently of the framing modes using the *PORT.CR2*.LM[2:0] control bits. The major blocks controlled are the transmit LIU (Tx LIU), receive LIU (RX LIU), jitter attenuator (JA) and the line encoder/decoder. The line encoder/decoder is used for B3ZS, HDB3 and AMI line interface encoding modes. The line encoder-decoder block is not used for line encoding or decoding in the UNI mode but the BPV counter in it can be used to count external pulses on the RNEG / RCLV pin. The jitter attenuator (JA) can be off (OFF) or put in either the transmit (Tx) or receive (RX) path with the Tx LIU or RX LIU. Both Tx LIU and RX LIU can be enabled (ON) or disabled (OFF).

The “Analog Loop Back” (ALB) is available when the LIU is enabled or disabled. It is an actual loop back of the analog positive and negative pulses from the TX LIU to the RX LIU when the LIU is enabled. If the LIU is disabled, It is a digital loop back of the TLCLK, TPOS, TNEG signals to the RLCLK, RPOS and RNEG signals.

When the line is configured for B3ZS/HDB3/AMI line codes, the line codes are determined by the framing mode and the AMI line mode selection is controlled by the TZCDS and RZCDS bits in the line encoder/decoder blocks. The DS3 modes select the B3ZS line coding, the E3 modes select the HDB3 line codes. Refer to Table 10-26 for configuration.

Table 10-26. Line Mode Select Bits LM[2:0]

LINE.TCR.**TZSD** & LINE.RCR.**RZSD**	**LM[2:0]** (PORT.CR2)	**Line Code**	**LIU**	**JA**
0	000	B3ZS/HDB3	OFF	OFF
0	001	B3ZS/HDB3	ON	OFF
0	010	B3ZS/HDB3	ON	TX
0	011	B3ZS/HDB3	ON	RX
1	000	AMI	OFF	OFF
1	001	AMI	ON	OFF
1	010	AMI	ON	TX
1	011	AMI	ON	RX
X	1XX	UNI	OFF	OFF

10.6 DS3/E3 Framer / Formatter

10.6.1 General Description

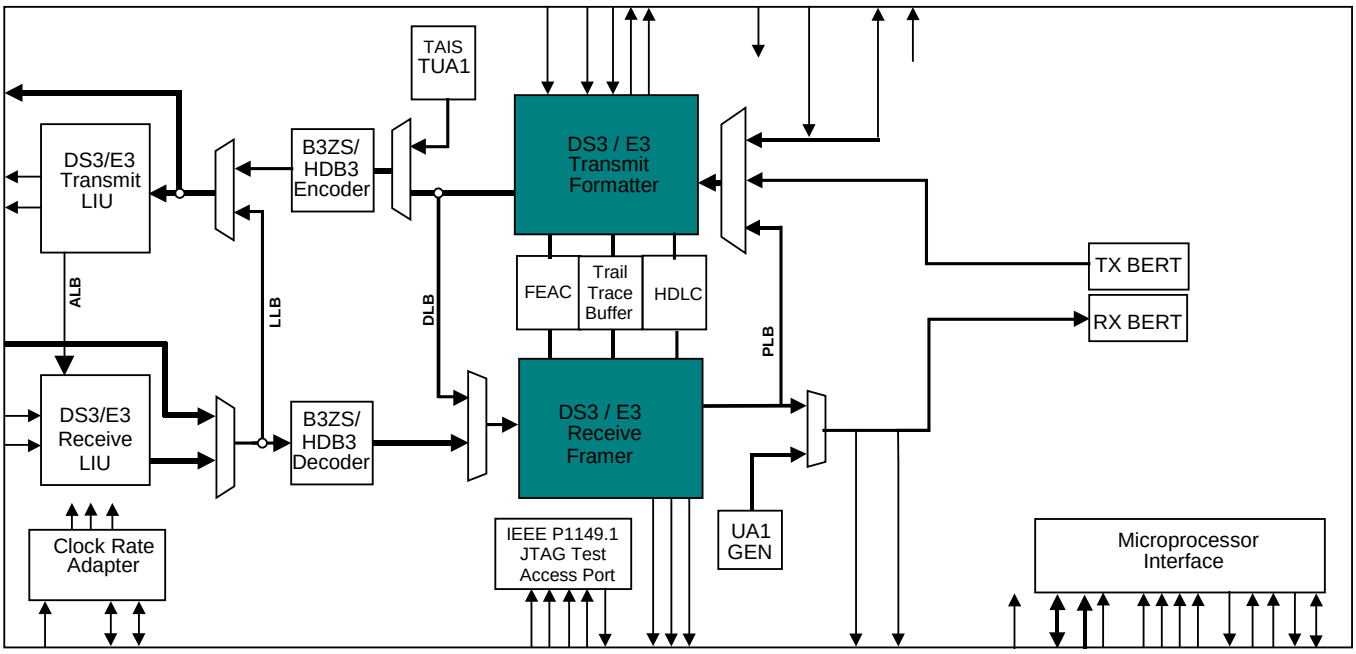
The Receive DS3/E3 Framer receives a unipolar DS3/E3 signal, determines frame alignment and extracts the DS3/E3 overhead in the receive direction. The Transmit DS3/E3 Formatter receives a DS3/E3 payload, generates framing, inserts DS3/E3 overhead, and outputs a unipolar DS3/E3 signal in the transmit direction.

The Receive DS3/E3 Framer receives a DS3/E3 signal from the Receive LIU or RDAT (or RPOS and RNEG), determines the frame alignment, extracts the DS3/E3 overhead, and outputs the payload with frame and overhead

The Transmit DS3/E3 Formatter receives a DS3/E3 payload on TSER, generates a DS3/E3 frame, optionally inserts DS3/E3 overhead, and transmits the DS3/E3 signal.

Refer to Figure 10-12 for the location of the DS3/E3 Framer/Formatter blocks in the DS3170.

Figure 10-12. Framer Detailed Block Diagram



10.6.2 Features

10.6.2.1 Transmit Formatter

- **Programmable DS3 or E3 formatter** – Accepts a DS3 (M23 or C-bit) or E3 (G.751 or G.832) signal and performs DS3/E3 overhead generation.
- **Arbitrary framing format support** – Generates a signal with an arbitrary framing format. The line overhead/stuff periods are added into the data stream using an overhead mask signal.
- **Generates alarms and errors** – DS3 alarm conditions (AIS, RDI, and Idle) and errors (framing, parity, and FEBE), or E3 alarm conditions (AIS and RDI/RAI) and errors (framing, parity, and REI) can be inserted into the outgoing data stream.
- **Externally controlled serial DS3/E3 overhead insertion port** – Can insert all DS3 or E3 overhead via a serial interface. DS3/E3 overhead insertion is fully controlled via the serial overhead interface.
- **HDLC overhead insertion** – An HDLC channel can be inserted into the DS3 or E3 data stream.
- **FEAC insertion** – A FEAC channel can be inserted into the DS3 or E3 data stream.
- **Trail Trace insertion** – Inputs and inserts the G.832 E3 TR byte.

10.6.2.2 Receive Framer

- **Programmable DS3 or E3 framer** – Accepts a DS3 (M23 or C-bit) or E3 (G.751 or G.832) signal and performs DS3/E3 overhead termination.

- **Arbitrary framing format support** – Accepts a signal with an arbitrary framing format. The Line overhead/stuff periods are removed from the data stream using an overhead mask signal.
- **Detects alarms and errors** – Detects DS3 alarm conditions (SEF, OOMF, OOF, LOF, COFA, AIS, AIC, RDI, and Idle) and errors (framing, parity, and FEBE), or E3 alarm conditions (OOF, LOF, COFA, AIS, and RDI/RAI) and errors (framing, parity, and REI).
- **Serial DS3/E3 overhead extraction port** – Extracts all DS3 or E3 overhead and outputs it on a serial interface.
- **HDLC overhead extraction** – An HDLC channel can be extracted from the DS3 or E3 data stream.
- **FEAC extraction** – A FEAC channel can be extracted from the DS3 or E3 data stream.
- **Trail Trace extraction** – Extracts and outputs the G.832 E3 TR byte.

10.6.3 Transmit Formatter

The Transmit Formatter receives a DS3 or E3 data stream and performs framing generation, error insertion, overhead insertion, and AIS/Idle generation for C-bit DS3, M23 DS3, G.751 E3, or G.832 E3 framing protocols.

The bits in a byte are transmitted MSB first, LSB last. When they are input serially, they are input in the order they are to be transmitted. The bits in a byte in an outgoing signal are numbered in the order they are transmitted, 1 (MSB) to 8 (LSB). However, when a byte is stored in a register, the MSB is stored in the highest numbered bit (7), and the LSB is stored in the lowest numbered bit (0). This is to differentiate between a byte in a register and the corresponding byte in a signal.

10.6.4 Receive Framer

The Receive Framer receives the incoming DS3,or E3, ine/tributary data stream, performs appropriate framing, and terminates and extracts the associated overhead bytes.

The Receive Framer processes a C-bit format DS3, M23 format DS3, G.751 format E3, or G.832 format E3 data stream, performing framing, performance monitoring, overhead extraction, and generates downstream AIS, if necessary.

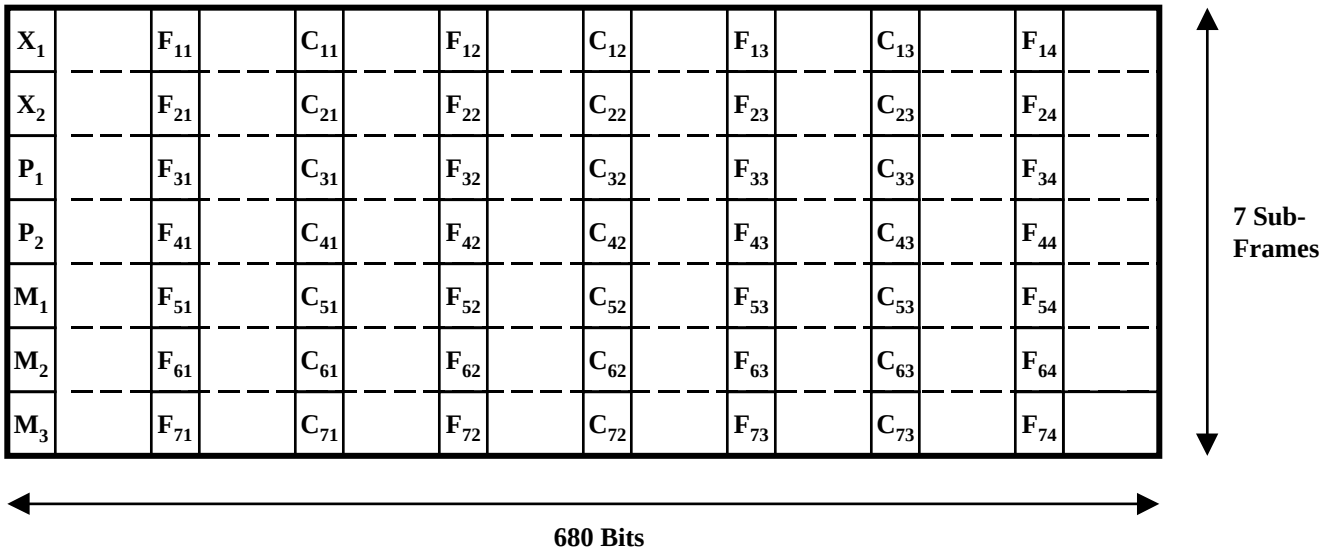
The bits in a byte are received MSB first, LSB last. When they are output serially, they are output MSB first, LSB last. The bits in a byte in an incoming signal are numbered in the order they are received, 1 (MSB) to 8 (LSB). However, when a byte is stored in a register, the MSB is stored in the highest numbered bit (7), and the LSB is stored in the lowest numbered bit (0). This is to differentiate between a byte in a register and the corresponding byte in a signal.

Some bits, bit groups, or bytes (data) are integrated before being stored in a register. Integration requires the data to have the same new data value for five consecutive occurrences before the new data value will be stored in the data register. Unless stated otherwise, integrated data may have an associated unstable indication. Integrated data is considered unstable if the received data value does not match the currently stored (integrated) data value or the previously received data value for eight consecutive occurrences. The unstable condition is terminated when the same value is received for five consecutive occurrences.

10.6.4.1.1 Receive DS3 Framing

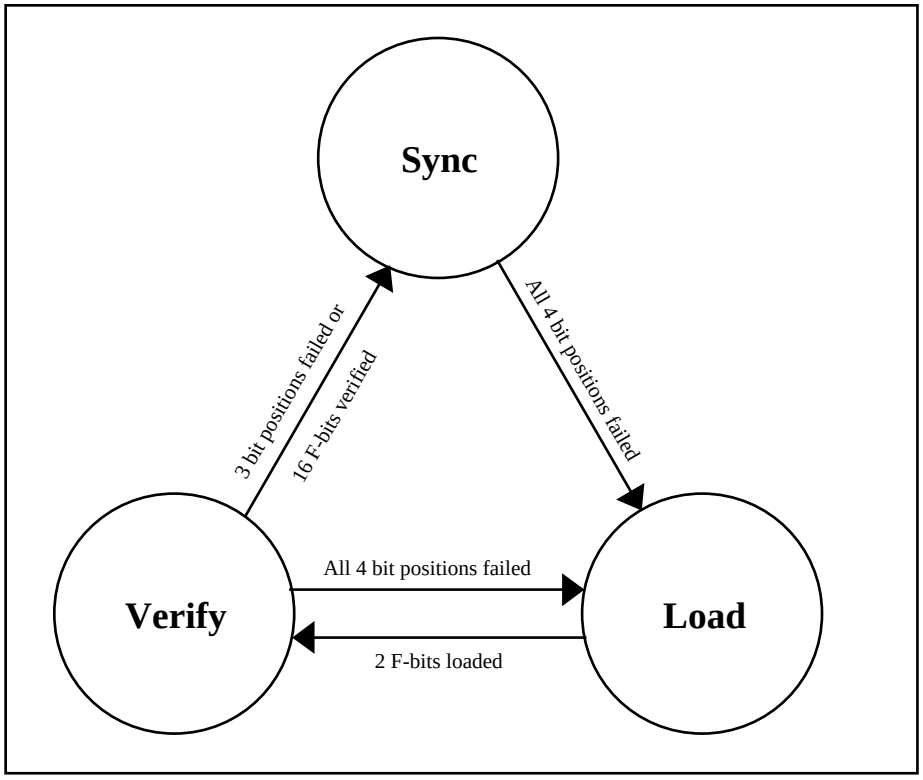
DS3 framing determines the DS3 frame boundary. In order to identify the DS3 frame boundary, first the subframe boundary must be found. The subframe boundary is found by identifying the subframe alignment bits F_{X1}, F_{X2}, F_{X3}, and F_{X4}, which have a value of one, zero, zero, and one respectively. See Figure 10-13. Once the subframe boundary is found, the multiframe frame boundary can be found. The multiframe boundary is found by identifying the multiframe alignment bits M_1, M_2, and M_3, which have a value of zero, one, and zero respectively. The DS3 framer is an off-line framer that only updates the data path frame counters when either an out of frame (OOF) or an out of multiframe (OOMF) condition is present. The use of an off-line framer reduces the average time required to reframe, and reduces data loss caused by burst error. The DS3 framer has a Maximum Average Reframe Time (MART) of approximately 1.0 ms.

Figure 10-13. DS3 Frame Format



The subframe framer continually searches four adjacent bit positions for a subframe boundary. A subframe alignment bit (F-bit) checker checks each bit position. All four bit positions must fail before any other bit positions are checked for a subframe boundary. There are 170 possible bit positions that must be checked, and four positions are checked simultaneously. Therefore up to 43 checks may be needed to identify the subframe boundary. The subframe framer enables the multiframe frame once it has identified a subframe boundary. Refer to Figure 10-14 for the subframe framer state diagram.

Figure 10-14. DS3 Subframe Framer State Diagram



The multiframe framer checks for a multiframe boundary. When the multiframe framer identifies a multiframe boundary, it updates the data path frame counters if either an OOF or OOMF condition is present. The multiframe framer waits until a subframe boundary has been identified. Then, each bit position is checked for the multiframe

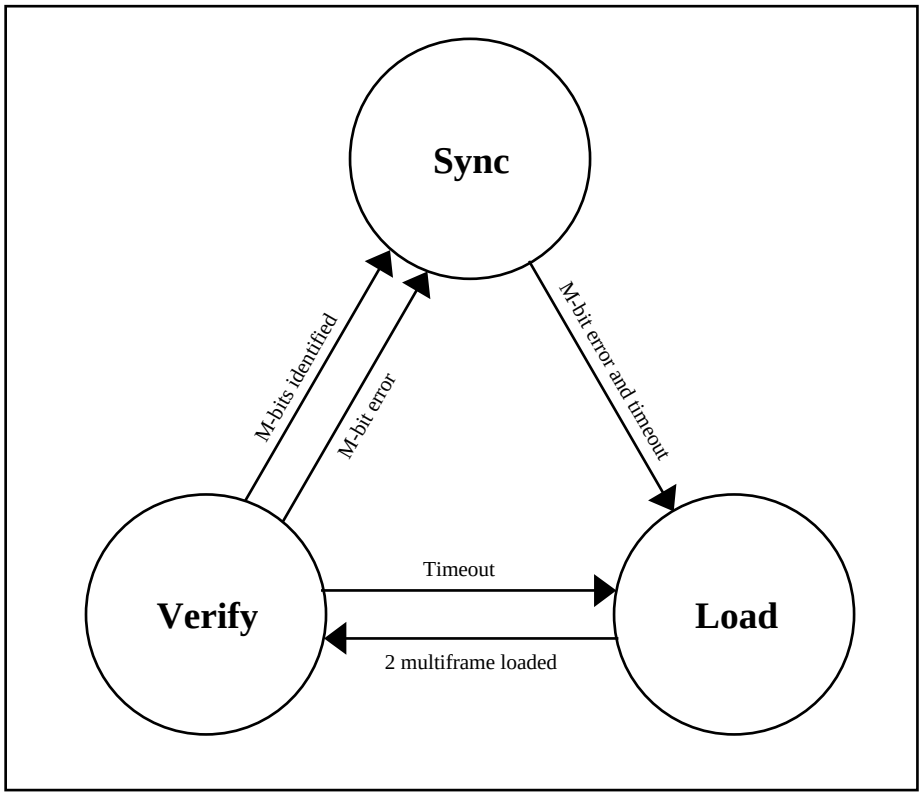
boundary. The multiframe boundary is found by identifying the three multiframe alignment bits (M-bits). Since there are seven multiframe bits and three bits are required to identify the multiframe boundary, up to 9 checks may be needed to find the multiframe boundary. Once the multiframe boundary is identified, it is checked in each subsequent frame. The data path frame counters are updated if the three multiframe alignment bits are error free, and an OOF or OOMF condition exists. If the multiframe framer checks more than fifteen multiframe bit (X-bits, P-bits, and M-bits) positions without identifying the multiframe boundary, the multiframe framer times out, and forces the subframe framer back into the load state. Refer to Figure 10-15 for the multiframe framer state diagram.

10.6.4.1.2 Receive DS3 Performance Monitoring

Performance monitoring checks the DS3 frame for alarm conditions and errors. The alarm conditions detected are OOMF, OOF, SEF, LOF, COFA, LOS, AIS, Idle, RUA1, and RDI. The errors accumulated are framing, P-bit parity, C-bit parity (C-bit format only), and Far-End Block Error (FEBE) (C-bit format only) errors.

An Out Of MultiFrame (OOMF) condition is declared when a multiframe alignment bit (M-bit) error has been detected in two or more of the last four consecutive DS3 frames, or when a manual resynchronization is requested. An OOMF condition is terminated when no M-bit errors have been detected in the last four consecutive DS3 frames, or when the DS3 framer updates the data path frame counters. Refer to Figure 10-15 for the multiframe framer state diagram.

Figure 10-15. DS3 Multiframe Framer State Diagram



If multiframe alignment OOF is disabled, an Out Of Frame (OOF) condition is declared when three or more out of the last sixteen consecutive subframe alignment bits (F-bits) have been errored, or a manual resynchronization is requested. If multiframe alignment OOF is enabled, an OOF condition is declared when three or more out of the last sixteen consecutive F-bits have been errored, when an OOMF condition is declared, or when a manual resynchronization is requested. If multiframe alignment OOF is disabled, an OOF condition is terminated when none of the last sixteen consecutive F-bits has been errored, or when the DS3 framer updates the data path frame counters. If multiframe alignment OOF is enabled, an OOF condition is terminated when an OOMF condition is not active and none of the last sixteen consecutive F-bits has been errored, or when the DS3 framer updates the data path frame counters. Multiframe alignment OOF is programmable (on or off).

A Severely Errored Frame (SEF) condition is declared when three or more out of the last sixteen consecutive F-bits have been errored, or when a manual resynchronization is requested. An SEF condition is terminated when an OOF condition is absent.

A Loss Of Frame (LOF) condition is declared by the LOF integration counter when it has been active for a total of *T* ms. The LOF integration counter is active (increments count) when an OOF condition is present, it is inactive (holds count) when an OOF condition is absent, and it is reset when an OOF condition is absent for *T* continuous ms. *T* is programmable (0, 1, 2, or 3). An LOF condition is terminated when an OOF condition is absent for *T* continuous ms.

A Change Of Frame Alignment (COFA) is declared when the DS3 framer updates the data path frame counters with a frame alignment that is different from the current data path DS3 frame alignment.

A Loss Of Signal (LOS) condition is declared when the B3ZS encoder is active, and it declares an LOS condition. An LOS condition is terminated when the B3ZS encoder is inactive, or it terminates an LOS condition.

An Alarm Indication Signal (AIS) is a DS3 signal with valid F-bits and M-bits. The X-bits (X_1 and X_2) are set to one, the P-bits (P_1 and P_2) are set to zero, all C-bits (C_{XY}) are set to zero, and the payload bits are set to a 1010 pattern starting with a one immediately after each DS3 overhead bit. An AIS signal is present when a DS3 frame is received with valid F-bits and M-bits, both X-bits set to one, both P-bits set to zero, all C-bits set to zero, and all but seven or fewer payload data bits matching the DS3 overhead aligned 1010 pattern. An AIS signal is absent when a DS3 frame is received that does not meet the aforementioned criteria for an AIS signal being present. The AIS integration counter declares an AIS condition when it has been active for a total of 10 to 17 DS3 frames. The AIS integration counter is active (increments count) when an AIS signal is present, it is inactive (holds count) when an AIS signal is absent, and it is reset when an AIS signal is absent for 10 to 17 consecutive DS3 frames. An AIS condition is terminated when an AIS signal is absent for 10 to 17 consecutive DS3 frames.

A Receive Unframed All 1's (RUA1) condition is declared if in each of 4 consecutive 2047 bit windows, five or less zeros are detected and an OOF condition is continuously present . A RUA1 condition is terminated if in each of 4 consecutive 2047 bit windows, six or more zeros are detected or an OOF condition is continuously absent.

An Idle Signal (Idle) is a DS3 signal with valid F-bits, M-bits, and P-bits (P_1 and P_2). The X-bits (X_1 and X_2) are set to one, C_{31}, C_{32}, and C_{33} are set to zero, and the payload bits are set to a 1100 pattern starting with 11 immediately after each overhead bit. In C-bit mode, an Idle signal is present when a DS3 frame is received with valid F-bits, M-bits, and P-bits, both X-bits set to one, C_{31}, C_{32}, and C_{33} set to zero, and all but seven or fewer payload data bits matching the T3 overhead aligned 1100 pattern. In M23 mode, an Idle signal is present when a T3 frame is received with valid F-bits, M-bits, and P-bits, both X-bits set to one, and all but seven or fewer payload data bits matching the overhead aligned 1100 pattern. An Idle signal is absent when a DS3 frame is received that does not meet aforementioned criteria for an Idle signal being present. The Idle integration counter declares an Idle condition when it has been active for a total of 10 to 17 DS3 frames. The Idle integration counter is active (increments count) when an Idle signal is present, it is inactive (holds count) when an Idle signal is absent, and it is reset when an Idle signal is absent for 10 to 17 consecutive DS3 frames. An Idle condition is terminated when an Idle signal is absent for 10 to 17 consecutive DS3 frames.

A Remote Defect Indication (RDI) condition (also called a far-end SEF/AIS defect condition) is declared when four consecutive DS3 frames are received with the X-bits (X_1 and X_2) set to zero. An RDI condition is terminated when four consecutive DS3 frames are received with the X-bits set to one.

A DS3 Framing Format Mismatch (DS3FM) condition is declared when the DS3 format programmed (M13, C-bit) does not match the incoming DS3 signal framing format. A DS3FM condition is terminated when the incoming DS3 signal framing format is the same format as programmed. Framing errors are determined by comparing F-bits and M-bits to their expected values. The type of framing errors accumulated is programmable (OOFs, F & M, F, or M). An OOF error increments the count whenever an OOF condition is first detected . An F & M error increments the count once for each F-bit or M-bit that does not match its expected value (up to 31 per DS3 frame). An F error increments the count once for each F-bit that does not match its expected value (up to 28 per DS3 frame). An M error increments the count once for each M-bit that does not match its expected value (up to 3 per DS3 frame).

P-bit parity errors are determined by calculating the parity of the current DS3 frame (payload bits only), and comparing the calculated parity to the P-bits (P_1 and P_2) in the next DS3 frame. If the calculated parity does not match P_1 or P_2, a single P-bit parity error is declared.

C-bit parity errors (C-bit format only) are determined by calculating the parity of the current DS3 frame (payload bits only), and comparing the calculated parity to the C-bits in subframe three (C_{31}, C_{32}, and C_{33}) in the next DS3 frame. If the calculated parity does not match C_{31}, C_{32}, or C_{33}, a single C-bit parity error is declared.

FEBE errors (C-bit format only) are determined by the C-bits in subframe four (C_{41}, C_{42}, and C_{43}). A value of 111 indicates no error and any other value indicates an error.

The receive alarm indication (RAI) bit will be set high in the transmitter when one or more of the indicated alarm conditions is present, and low when all of the indicated alarm conditions are absent. Setting the receive alarm indication on LOS, SEF, LOF, or AIS is individually programmable (on or off).

The Application Identification Channel (AIC) is stored in a register bit. It is determined from the C_{11} bit. The AIC is set to one (C-bit format) if the C_{11} bit is set to one in thirty-one consecutive multiframes. The AIC is set to zero (M23 format) if the C_{11} bit is set to zero in four of the last thirty-one consecutive multiframes. Note: The stored AIC bit must not change when an LOS, OOF, or AIS condition is present.

A FEBE is transmitted by default upon reception of a DS3 frame in which a C-bit parity error or a framing error is detected and counted.

10.6.5 C-bit DS3 Framer/Formatter

10.6.5.1 Transmit C-bit DS3 Frame Processor

The C-bit DS3 frame format is shown in Figure 10-13**.**

Figure 10-13. DS3 Frame Format

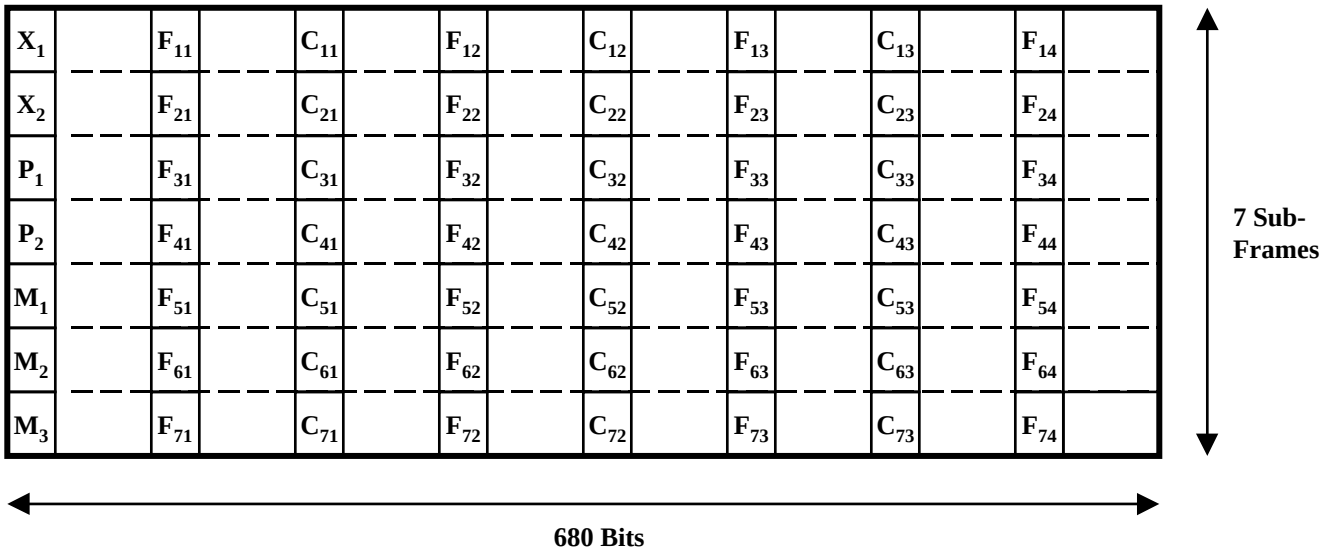


Table 10-27 shows the function of each overhead bit in the DS3 Frame

Table 10-27. C-Bit DS3 Frame Overhead Bit Definitions

BIT	DEFINITION
X_1, X_2	Remote Defect Indication (RDI)
P_1, P_2	Parity Bits
M_1, M_2, and M_3	Multiframe Alignment Bits
F_{XY}	Subframe Alignment Bits
C_{11}	Application Identification Channel (AIC)
C_{12}	Reserved
C_{13}	Far-End Alarm and Control (FEAC) signal
C_{21}, C_{22}, and C_{23}	Unused
C_{31}, C_{32}, and C_{33}	C-bit parity bits
C_{41}, C_{42}, and C_{43}	Far-End Block Error (FEBE) bits
C_{51}, C_{52}, and C_{53}	Path Maintenance Data Link (or HDLC) bits
C_{61}, C_{62}, and C_{63}	Unused
C_{71}, C_{72}, and C_{73}	Unused

X_1 and X_2 are the Remote Defect Indication (RDI) bits (also referred to as the far-end SEF/AIS bits). P_1 and P_2 are the parity bits used for line error monitoring. M_1, M_2, and M_3 are the multiframe alignment bits. F_{XY} are the subframe alignment bits. C_{11} is the Application Identification Channel (AIC). C_{12} is reserved for future network use, and has a value of one. C_{13} is the Far-End Alarm and Control (FEAC) signal. C_{21}, C_{22}, and C_{23} are unused, and have a value of one. C_{31}, C_{32}, and C_{33} are the C-bit parity bits used for path error monitoring. C_{41}, C_{42}, and C_{43} are the Far-End Block Error (FEBE) bits used for remote path error monitoring. C_{51}, C_{52}, and C_{53} are the path maintenance data link (or HDLC) bits. C_{61}, C_{62}, and C_{63} are unused, and have a value of one. C_{71}, C_{72}, and C_{73} are unused, and have a value of one. The X-bit, P-bit, M-bit, C-bit, and F-bit positions are overhead bits, and the other bit positions in the T3 frame are payload bits regardless of how they are marked by TDEN.

10.6.5.2 Transmit C-bit DS3 Frame Generation

C-bit DS3 frame generation receives the incoming payload data stream, and overwrites all of the overhead bit locations.

The multiframe alignment bits (M_1, M_2, and M_3) are overwritten with the values zero, one, and zero (010) respectively.

The subframe alignment bits (F_{X1}, F_{X2}, F_{X3}, and F_{X4}) are overwritten with the values one, zero, zero, and one (1001) respectively.

The X-bits (X_1 and X_2) are both overwritten with the Remote Defect Indicator (RDI). The RDI source is programmable (automatic, 1, or 0). If the RDI is generated automatically, the X-bits are set to zero when one or more of the indicated alarm conditions is present, and set to one when all of the indicated alarm conditions are absent. Automatically setting RDI on LOS, SEF, LOF, or AIS is individually programmable (on or off).

The P-bits (P_1 and P_2) are both overwritten with the calculated payload parity from the previous DS3 frame. The payload parity is calculated by performing modulo 2 addition of all of the payload bits after all frame processing has been completed. P-bit generation is programmable (on or off). The P-bits will be generated if either P-bit generation is enabled or frame generation is enabled.

The bits C_{11}, C_{12}, C_{21}, C_{22}, C_{23}, C_{61}, C_{62}, C_{63}, C_{71}, C_{72}, and C_{73} are all overwritten with a one.

The bit C_{13} is overwritten with the Far-End Alarm and Control (FEAC) data input from the transmit FEAC controller.

The bits C_{31}, C_{32}, and C_{33} are all overwritten with the calculated payload parity from the previous DS3 frame.

The bits C_{41}, C_{42}, and C_{43} are all overwritten with the Far-End Block Error (FEBE) bit. The FEBE bit can be generated automatically or inserted from a register bit. The FEBE bit source is programmable (automatic or register). If the FEBE bit is generated automatically, it is zero when at least one C-bit parity error has been detected during the previous frame.

The bits C_{51}, C_{52}, and C_{53} are overwritten with the path maintenance data link input from the HDLC controller.

Once all of the DS3 overhead bits have been overwritten, the data stream is passed on to error insertion. If frame generation is disabled, the incoming DS3 signal is passed on to error insertion. Frame generation is programmable (on or off). Note: P-bit generation may still be performed even if frame generation is disabled.

10.6.5.3 Transmit C-bit DS3 Error Insertion

Error insertion inserts various types of errors into the different DS3 overhead bits. The types of errors that can be inserted are framing errors, P-bit parity errors, C-bit parity errors, and Far-End Block Error (FEBE) errors.

The framing error insertion mode is programmable (F-bit, M-bit, SEF, or OOMF). An F-bit error is a single subframe alignment bit (F_{XY}) error. An M-bit error is a single multiframe alignment bit (M_1, M_2, or M_3) error. An SEF error is an error in all the subframe alignment bits in a subframe (F_{X1}, F_{X2}, F_{X3}, and F_{X4}). An OOMF error is a single multiframe alignment bit (M_1, M_2, or M_3) error in two consecutive DS3 frames.

A P-bit parity error is generated by is inverting the value of the P-bits (P_1 and P_2) in a single DS3 frame. P-bit parity error(s) can be inserted one error at a time, or continuously. The P-bit parity error insertion mode (single or continuous) is programmable.

A C-bit parity error is generated by is inverting the value of the C_{31}, C_{32}, and C_{33} bits in a single DS3 frame. C-bit parity error(s) can be inserted one error at a time, or continuously. The C-bit parity error insertion mode (single or continuous) is programmable.

A FEBE error is generated by forcing the C_{41}, C_{42}, and C_{43} bits in a single multiframe to zero. FEBE error(s) can be inserted one error at a time, or continuously. The FEBE error insertion rate (single or continuous) is programmable.

Each error type (framing, P-bit parity, C-bit parity, or FEBE) has a separate enable. Continuous error insertion mode inserts errors at every opportunity. Single error insertion mode inserts an error at the next opportunity when requested. the framing multi-error modes (SEF or OOMF) insert the indicated number of error(s) at the next opportunities when requested; i.e., a single request will cause multiple errors to be inserted. The requests can be initiated by a register bit(TSEI) or by the manual error insertion input (TMEI). The error insertion initiation type (register or input) is programmable. The insertion of each particular error type is individually enabled. Once all error insertion has been performed, the data stream is passed on to overhead insertion.

10.6.5.4 Transmit C-bit DS3 Overhead Insertion

Overhead insertion can insert any (or all) of the DS3 overhead bits into the DS3 frame. The DS3 overhead bits X_1, X_2, P_1, P_2, M_X, F_{XY}, and C_{XY} can be sourced from the transmit overhead interface (TOHCLK, TOH, TOHEN, and TOHSOF). The P-bits (P_1 and P_2) and C_{31}, C_{32}, and C_{33} bits are received as an error mask (modulo 2 addition of the input bit and the internally generated bit). The DS3 overhead insertion is fully controlled by the transmit overhead interface. If the transmit overhead data enable signal (TOHEN) is driven high, then the bit on the transmit overhead signal (TOH) is inserted into the output data stream. Insertion of bits using the TOH signal overwrites internal overhead insertion.

10.6.5.5 Transmit C-bit DS3 AIS/Idle Generation

C-bit DS3 AIS/Idle generation overwrites the data stream with AIS or an Idle signal. If transmit Idle is enabled, the data stream payload is forced to a 1100 pattern with two ones immediately following each DS3 overhead bit. M_1, M_2, and M_3 bits are overwritten with the values zero, one, and zero (010) respectively. F_{X1}, F_{X2}, F_{X3}, and F_{X4} bits are overwritten with the values one, zero, zero, and one (1001) respectively. X_1 and X_2 are overwritten with 11. And, P_1, P_2, C_{31}, C_{32}, and C_{33} are overwritten with the calculated payload parity from the previous output DS3 frame.

If transmit AIS is enabled, the data stream payload is forced to a 1010 pattern with a one immediately following each DS3 overhead bit. M_1, M_2, and M_3 bits are overwritten with the values zero, one, and zero (010) respectively. F_{X1}, F_{X2}, F_{X3}, and F_{X4} bits are overwritten with the values one, zero, zero, and one (1001) respectively. X_1 and X_2 are overwritten with 11. P_1, P_2, C_{31}, C_{32}, and C_{33} are overwritten with the calculated payload parity from the previous output DS3 frame. And, C_{X1}, C_{X2}, and C_{X3} ($X \neq 3$) are overwritten with 000. AIS will overwrite a transmit Idle signal.

10.6.5.5.1 Receive C-bit DS3 Frame Format

The DS3 frame format is shown in Figure 10-13. X_1 and X_2 are the Remote Defect Indication (RDI) bits (also referred to as the far-end SEF/AIS bits). P_1 and P_2 are the parity bits used for line error monitoring. M_1, M_2, and M_3 are the multiframe alignment bits that define the multiframe boundary. F_{XY} are the subframe alignment bits that define the subframe boundary. Note: Both the M-bits and F-bits define the DS3 frame boundary. C_{11} is the Application Identification Channel (AIC). C_{12} is reserved for future network use, and has a value of one. C_{13} is the Far-End Alarm and Control (FEAC) signal. C_{21}, C_{22}, and C_{23} are unused, and have a value of one. C_{31}, C_{32}, and C_{33} are the C-bit parity bits used for path error monitoring. C_{41}, C_{42}, and C_{43} are the Far-End Block Error (FEBE) bits used for remote path error monitoring. C_{51}, C_{52}, and C_{53} are the path maintenance data link (or HDLC) bits. C_{61}, C_{62}, and C_{63} are unused, and have a value of one. C_{71}, C_{72}, and C_{73} are unused, and have a value of one.

10.6.5.5.2 Receive C-bit DS3 Overhead Extraction

Overhead extraction extracts all of the DS3 overhead bits from the C-bit DS3 frame. All of the DS3 overhead bits X_1, X_2, P_1, P_2, M_X, F_{XY}, and C_{XY} are output on the receive overhead interface (ROH, ROHSOF, and ROHCLK). The P_1, P_2, C_{31}, C_{32}, and C_{33} bits are output as an error indication (modulo 2 addition of the calculated parity and the bit). The C_{13} bit is sent over to the receive FEAC controller. The C_{51}, C_{52}, and C_{53} bits are sent to the receive HDLC overhead controller.

10.6.6 M23 DS3 Framer/Formatter

10.6.6.1 Transmit M23 DS3 Frame Processor

The M23 DS3 frame format is shown in Figure 10-13. Table 10-28 defines the framing bits for M23 DS3. X_1 and X_2 are the Remote Defect Indication (RDI) bits (also referred to as the far-end SEF/AIS bits). P_1 and P_2 are the parity bits used for line error monitoring. M_1, M_2, and M_3 are the multiframe alignment bits. F_{XY} are the subframe alignment bits. C_{11} is the Application Identification Channel (AIC). C_{X1}, C_{X2}, and C_{X3} are the stuff control bits for tributary #X. The X-bit, P-bit, M-bit, C-bit, and F-bit positions are overhead bits, and the remainder of the bit positions in the T3 frame are payload bits regardless of how they are marked by TDEN.

Table 10-28. M23 DS3 Frame Overhead Bit Definitions

BIT	DEFINITION
X_1, X_2	Remote Defect Indication (RDI)
P_1, P_2	Parity Bits
M_1, M_2, and M_3	Multiframe Alignment Bits
F_{XY}	Subframe Alignment Bits
C_{11}	Application Identification Channel (AIC)
C_{X1}, C_{X2}, and C_{X3}	Stuff Control Bits for Tributary #X

10.6.6.2 Transmit M23 DS3 Frame Generation

M23 DS3 frame generation receives the incoming payload data stream, and overwrites all of the DS3 overhead bit locations.

The multiframe alignment bits (M_1, M_2, and M_3) are overwritten with the values zero, one, and zero (010) respectively.

The subframe alignment bits (F_{X1}, F_{X2}, F_{X3}, and F_{X4}) are overwritten with the values one, zero, zero, and one (1001) respectively.

The X-bits (X_1 and X_2) are both overwritten with the Remote Defect Indicator (RDI). The RDI source is programmable (automatic, 1, or 0). If the RDI is generated automatically, the X-bits are set to zero when one or

more of the indicated alarm conditions is present, and set to one when all of the indicated alarm conditions are absent. Automatically setting RDI on LOS, SEF, LOF, or AIS is individually programmable (on or off).

The P-bits (P_1 and P_2) are both overwritten with the calculated payload parity from the previous DS3 frame. The payload parity is calculated by performing modulo 2 addition of all of the payload bits after all frame processing has been completed. P-bit generation is programmable (on or off). The P-bits will be generated if either P-bit generation is enabled or frame generation is enabled.

If C-bit generation is enabled, the bit C_{11} is overwritten with an alternating one zero pattern, and all of the other C-bits (C_{XY}) are overwritten with zeros. If C-bit generation is disabled, then all of the C-bit timeslots (C_{XY}) will be treated as payload data, and passed through. C-bit generation is programmable (on or off). Note: Overhead insertion may still overwrite the C-bit time slots even if C-bit generation is disabled.

Once all of the DS3 overhead bits have been overwritten, the data stream is passed on to error insertion. If frame generation is disabled, the incoming DS3 signal is passed on directly to error insertion. Frame generation is programmable (on or off). Note: P-bit generation may still be performed even if frame generation is disabled.

10.6.6.3 Transmit M23 DS3 Error Insertion

Error insertion inserts various types of errors into the different DS3 overhead bits. The types of errors that can be inserted are framing errors and P-bit parity errors.

The framing error insertion mode is programmable (F-bit, M-bit, SEF, or OOMF). An F-bit error is a single subframe alignment bit (F_{XY}) error. An M-bit error is a single multiframe alignment bit (M_1, M_2, or M_3) error. An SEF error is an error in all the subframe alignment bits in a subframe (F_{X1}, F_{X2}, F_{X3}, and F_{X4}). An OOMF error is a single multiframe alignment bit (M_1, M_2, or M_3) error in each of two consecutive DS3 frames.

A P-bit parity error is generated by is inverting the value of the P-bits (P_1 and P_2) in a single DS3 frame. P-bit parity error(s) can be inserted one error at a time, or continuously. The P-bit parity error insertion mode (single or continuous) is programmable.

Each error type (framing or P-bit parity) has a separate enable. Continuous error insertion mode inserts errors at every opportunity. Single error insertion mode inserts an error at the next opportunity when requested. The framing multi-error insertion modes (SEF or OOMF) insert the indicated number of error(s) at the next opportunities when requested; i.e., a single request will cause multiple errors to be inserts. The requests can be initiated by a register bit(TSEI) or by the manual error insertion input (TMEI). The error insertion request source (register or input) is programmable. The insertion of each particular error type is individually enabled. Once all error insertion has been performed, the data stream is passed on to overhead insertion.

10.6.6.4 Transmit M23 DS3 Overhead Insertion

Overhead insertion can insert any (or all) of the DS3 overhead bits into the DS3 frame. The DS3 overhead bits X_1, X_2, P_1, P_2, M_X, F_{XY}, and C_{XY} can be sourced from the transmit overhead interface (TOHCLK, TOH, TOHEN, and TOHSOF). The P-bits (P_1 and P_2) are received as an error mask (modulo 2 addition of the input bit and the internally generated bit). The DS3 overhead insertion is fully controlled by the transmit overhead interface. If the transmit overhead data enable signal (TOHEN) is driven high, then the bit on the transmit overhead signal (TOH) is inserted into the output data stream. Insertion of bits using the TOH signal overwrites internal overhead insertion.

10.6.6.5 Transmit M23 DS3 AIS/Idle Generation

M23 DS3 AIS/Idle generation overwrites the data stream with AIS or an Idle signal. If transmit Idle is enabled, the data stream payload is forced to a 1100 pattern with two ones immediately following each DS3 overhead bit. M_1, M_2, and M_3 bits are overwritten with the values zero, one, and zero (010) respectively. F_{X1}, F_{X2}, F_{X3}, and F_{X4} bits are overwritten with the values one, zero, zero, and one (1001) respectively. X_1 and X_2 are overwritten with 11. P_1 and P_2 are overwritten with the calculated payload parity from the previous output DS3 frame. And, C_{31}, C_{32}, and C_{33} are overwritten with 000.

If transmit AIS is enabled, the data stream payload is forced to a 1010 pattern with a one immediately following each DS3 overhead bit. M_1, M_2, and M_3 bits are overwritten with the values zero, one, and zero (010) respectively. F_{X1}, F_{X2}, F_{X3}, and F_{X4} bits are overwritten with the values one, zero, zero, and one (1001) respectively. X_1 and X_2 are overwritten with 11. P_1 and P_2 are overwritten with the calculated payload parity from the previous DS3 frame. And, C_{X1}, C_{X2}, and C_{X3} are overwritten with 000. AIS will overwrite a transmit Idle signal.

10.6.6.5.1 Receive M23 DS3 Frame Format

The DS3 frame format is shown in Figure 10-13. The X_1 and X_2 are the Remote Defect Indication (RDI) bits (also referred to as the far-end SEF/AIS bits). P_1 and P_2 are the parity bits used for line error monitoring. M_1, M_2, and M_3 are the multiframe alignment bits that define the multiframe boundary. F_{XY} are the subframe alignment bits that define the subframe boundary. Note: Both the M-bits and F-bits define the DS3 frame boundary. C_{11} is the Application Identification Channel (AIC). C_{X1}, C_{X2}, and C_{X3} are the stuff control bits for tributary #X.

10.6.6.5.2 Receive M23 DS3 Overhead Extraction

Overhead extraction extracts all of the DS3 overhead bits from the M23 DS3 frame. All of the DS3 overhead bits X_1, X_2, P_1, P_2, M_X, F_{XY}, and C_{XY} are output on the receive overhead interface (ROH, ROHSOF, and ROHCLK). The P_1 and P_2 bits are output as an error indication (modulo 2 addition of the calculated parity and the bit).

10.6.6.5.3 Receive DS3 Downstream AIS Generation

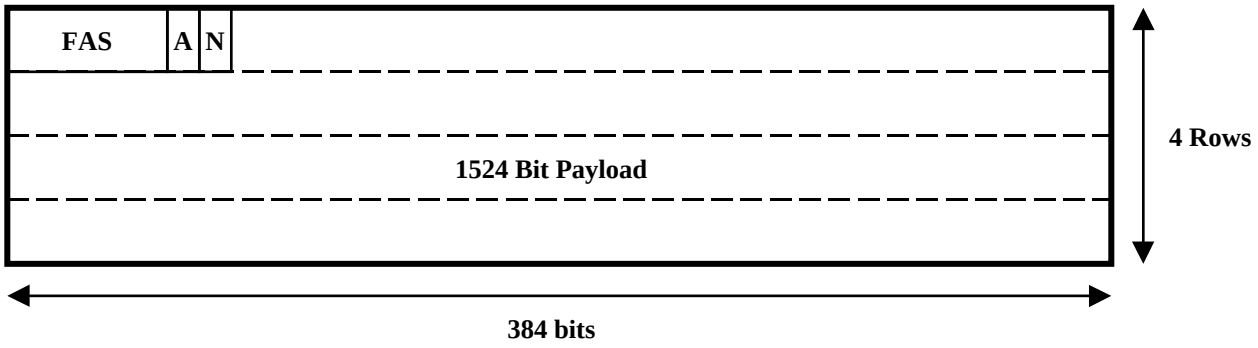
Downstream DS3 AIS (all '1's) can be automatically generated on an OOF, LOS, or AIS condition or manually inserted. If automatic downstream AIS is enabled, downstream AIS is inserted when an LOS or AIS condition is declared, or no earlier than 2.25 ms and no later than 2.75 ms after an OOF condition is declared. Automatic downstream AIS is programmable (on or off). If manual downstream AIS insertion is enabled, downstream AIS is inserted. Manual downstream AIS insertion is programmable (on or off). Downstream AIS is removed when all OOF, LOS, and AIS conditions are terminated and manual downstream AIS insertion is disabled.

10.6.7 G.751 E3 Framer/Formatter

10.6.7.1 Transmit G.751 E3 Frame Processor

The G.751 E3 frame format is shown in Figure 10-16. FAS is the Frame Alignment Signal. A is the Alarm indication bit used to indicate the presence of an alarm to the remote terminal equipment. N is the National use bit reserved for national use.

Figure 10-16. G.751 E3 Frame Format



10.6.7.2 Transmit G.751 E3 Frame Generation

G.751 E3 frame generation receives the incoming payload data stream, and overwrites all of the E3 overhead bit locations.

The first ten bits of the frame are overwritten with the frame alignment signal (FAS) which has a value of 1111010000b.

The eleventh bit of the frame is overwritten with the alarm indication (A) bit. The A bit can be generated automatically, sourced from the transmit FEAC controller, set to one, or set to zero. The A bit source is programmable (automatic, FEAC, 1, or 0). If the A bit is generated automatically, it is set to one when one or more of the indicated alarm conditions is present, and set to zero when all of the indicated alarm conditions are absent. Automatically setting RDI on LOS, LOF, or AIS is individually programmable (on or off).

The twelfth bit of the frame is overwritten with the national use (N) bit. The N bit can be sourced from the transmit FEAC controller, sourced from the transmit HDLC overhead controller, set to one, or set to zero. The N bit source is programmable (FEAC, HDLC, 1, or 0). Note: The FEAC controller will source one bit per frame regardless of whether the A bit only, the N bit only, or both are programmed to be sourced from the FEAC controller.

Once all of the E3 overhead bits have been overwritten, the data stream is passed on to error insertion. If frame generation is disabled, the incoming E3 signal is passed on directly to error insertion. Frame generation is programmable (on or off).

10.6.7.3 Transmit G.751 E3 Error Insertion

Error insertion inserts framing errors into the frame alignment signal (FAS). The type of error(s) inserted into the FAS is programmable (errored FAS bit or errored FAS). An errored FAS bit is a single bit error in the FAS. An errored FAS is an error in all ten bits of the FAS (a value of 0000101111b is inserted in the FAS). Framing error(s) can be inserted one error at a time, or in four consecutive frames. The framing error insertion number (single or four) is programmable.

Single error insertion mode inserts an error at the next opportunity when requested. The multi-error insertion mode inserts the indicated number of errors at the next opportunities when requested. I.e., a single request will cause multiple errors to be inserted. The requests can be initiated by a register bit(TSEI) or by the manual error insertion input (TMEI). The error insertion initiation type (register or input) is programmable. The insertion of each particular error type is individually enabled.

Once all error insertion has been performed, the data stream is passed on to overhead insertion.

10.6.7.4 Transmit G.751 E3 Overhead Insertion

Overhead insertion can insert any (or all) of the E3 overhead bits into the E3 frame. The FAS, A bit, and N bit can be sourced from the transmit overhead interface (TOHCLK, TOH, TOHEN, and TOHSOF). The E3 overhead insertion is fully controlled by the transmit overhead interface. If the transmit overhead data enable signal (TOHEN) is driven high, then the bit on the transmit overhead signal (TOH) is inserted into the output data stream. Insertion of bits using the TOH signal overwrites internal overhead insertion.

10.6.7.5 Transmit G.751 E3 AIS Generation

G.751 E3 AIS generation overwrites the data stream with AIS. If transmit AIS is enabled, the data stream (payload and E3 overhead) is forced to all ones.

10.6.7.6 Receive G.751 E3 Frame Processor

The G.751 E3 frame format is shown in Figure 10-16. FAS is the Frame Alignment Signal. A is the Alarm indication bit used to indicate the presence of an alarm to the remote terminal equipment. N is the National use bit reserved for national use.

10.6.7.6.1 Receive G.751 E3 Framing

G.751 E3 framing determines the G.751 E3 frame boundary. The frame boundary is found by identifying the frame alignment signal (FAS), which has a value of 1111010000b. The framer is an off-line framer that updates the data path frame counters when an out of frame (OOF) condition has been detected. The use of an off-line framer reduces the average time required to reframe, and reduces data loss caused by burst error. The G.751 E3 framer checks each bit position for the FAS. The frame boundary is set once the FAS is identified. Since, the FAS check is performed one bit at a time, up to 1536 checks may be needed to find the frame boundary. The data path frame counters are updated if an error free FAS is received for two additional frames, and an OOF condition is present, or if a manual frame resynchronization has been initiated.

10.6.7.6.2 Receive G.751 E3 Performance Monitoring

Performance monitoring checks the E3 frame for alarm conditions. The alarm conditions detected are OOF, LOF, COFA, LOS, AIS, RUA1, and RAI. An Out Of Frame (OOF) condition is declared when four consecutive frame alignment signals (FAS) contain one or more errors or at the next FAS check when a manual reframe is requested. An OOF condition is terminated when three consecutive FAS's are error free or the G.751 E3 framer updates the data path frame counters.

A Loss Of Frame (LOF) condition is declared by the LOF integration counter when it has been active for a total of *T* ms. The LOF integration counter is active (increments count) when an OOF condition is present, it is inactive (holds count) when an OOF condition is absent, and it is reset when an OOF condition is absent for *T* continuous ms. *T* is programmable (0, 1, 2, or 3). An LOF condition is terminated when an OOF condition is absent for *T* continuous ms.

A Change Of Frame Alignment (COFA) is declared when the G.751 E3 framer updates the data path frame counters with a frame alignment that is different from the current data path frame alignment.

A Loss Of Signal (LOS) condition is declared when the HDB3 encoder is active, and it declares an LOS condition. An LOS condition is terminated when the HDB3 encoder is inactive, or it terminates an LOS condition.

An Alarm Indication Signal (AIS) condition is declared when 4 or less zeros are detected in each of two consecutive frame periods. An AIS condition is terminated when 5 or more zeros are detected in each of two consecutive frame periods.

A Receive Unframed All 1's (RUA1) condition is declared if in each of 4 consecutive 2047 bit windows, five or less zeros are detected and an OOF condition is continuously present. A RUA1 condition is terminated if in each of 4 consecutive 2047 bit windows, six or more zeros are detected or an OOF condition is continuously absent.

A Remote Alarm Indication (RAI) condition is declared when four consecutive frames are received with the A bit (first bit after the FAS) set to one. An RAI condition is terminated when four consecutive frames are received with the A bit set to zero.

Only framing errors are accumulated. Framing errors are determined by comparing the FAS to its expected value. The type of framing errors accumulated is programmable (OOFs, bit, or word). An OOF error increments the count whenever an OOF condition is first detected. A bit error increments the count once for each bit in the FAS that does not match its expected value (up to 10 per frame. A word error increments the count once for each FAS that does not match its expected value (up to 1 per frame).

The receive alarm indication (RAI) signal is high when one or more of the indicated alarm conditions is present, and low when all of the indicated alarm conditions are absent. Setting the receive alarm indication on LOS, OOF, LOF, or AIS is individually programmable (on or off).

10.6.7.6.3 Receive G.751 E3 Overhead Extraction

Overhead extraction extracts all of the E3 overhead bits from the G.751 E3 frame. The FAS, A bit, and N bit are output on the receive overhead interface (ROH, ROHSOF, and ROHCLK). In addition, the A bit is integrated and stored in a register along with a change indication, and can be output over the receive FEAC controller. The N bit is integrated and stored in a register along with a change indication, is sent to the receive HDLC overhead controller, and can also be sent to the receive FEAC controller. The bit sent to the receive FEAC controller is programmable (A or N).

10.6.7.6.4 Receive G.751 Downstream AIS Generation

Downstream G.751 E3 AIS can be automatically generated on an OOF, LOS, or AIS condition or manually inserted. If automatic downstream AIS is enabled, downstream AIS is inserted when an LOS, OOF, or AIS condition is declared. Automatic downstream AIS is programmable (on or off). If manual downstream AIS insertion is enabled, downstream AIS is inserted. Manual downstream AIS insertion is programmable (on or off). Downstream AIS is removed when all OOF, LOS, and AIS conditions are terminated and manual downstream AIS insertion is disabled. RPDT will be forced to all ones during downstream AIS.

10.6.8 G.832 E3 Framer/Formatter

10.6.8.1 Transmit G.832 E3 Frame Processor

The G.832 E3 frame format is shown in Figure 10-17.

Figure 10-17. G.832 E3 Frame Format

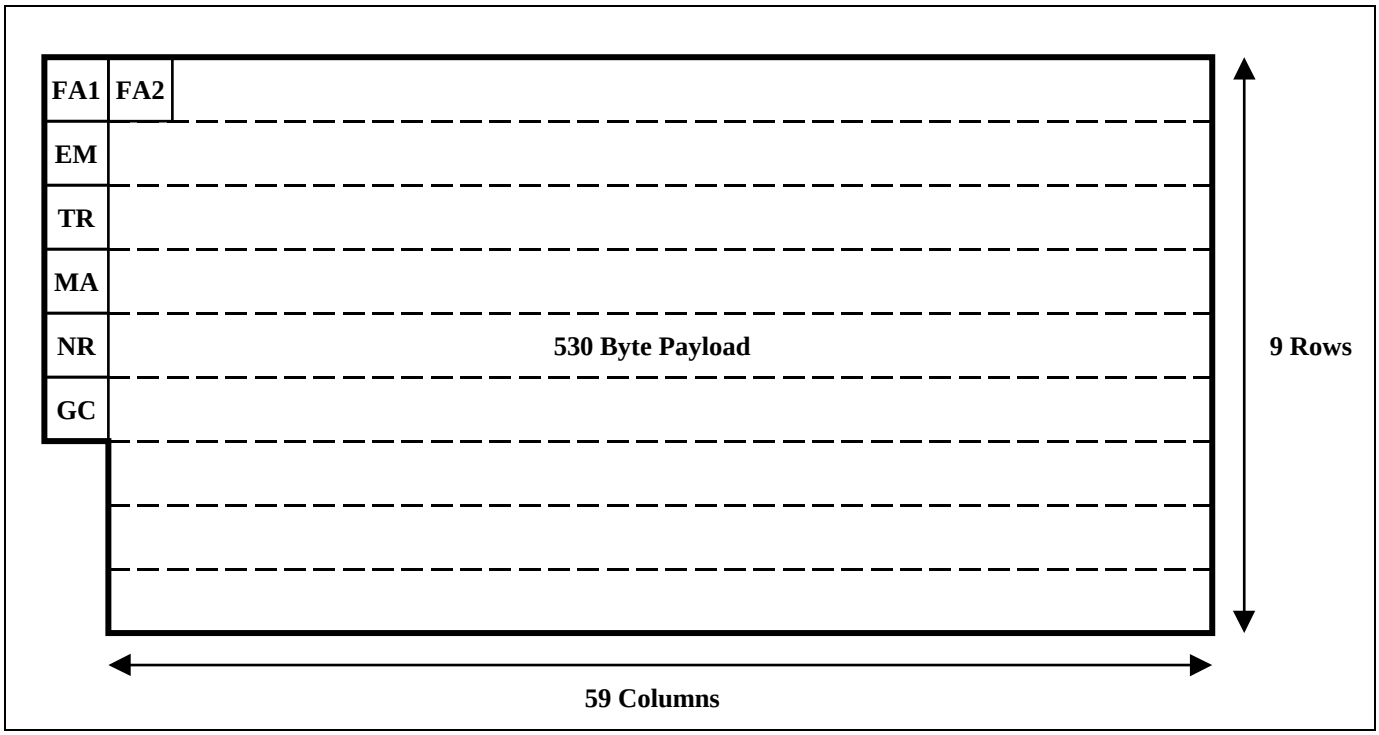


Figure 10-18. MA Byte Format

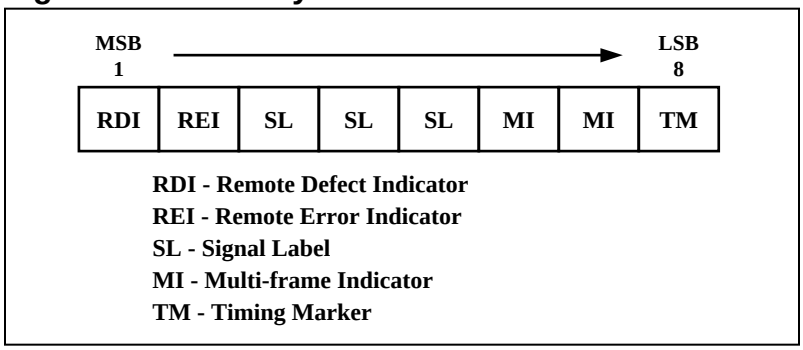


Table 10-29 shows the function of each overhead bit in the DS3 Frame.

Table 10-29. G.832 E3 Frame Overhead Bit Definitions

BYTE	DEFINITION
FA1, FA2	Frame Alignment bytes
EM	Error Monitoring byte
TR	Trail Trace byte
MA	Maintenance and Adaption byte
NR	Network Operator byte
GC	General Purpose Communication Channel byte

FA1 and FA2 are the Frame Alignment bytes. EM is the Error Monitoring byte used for path error monitoring. TR is the Trail Trace byte used for end-to-end connectivity verification. MA is the Maintenance and Adaptation byte used for far-end path status and performance monitoring.

NR is the Network Operator byte allocated for network operator maintenance purposes. GC is the General Purpose Communications Channel byte allocated for user communications purposes.

10.6.8.2 Transmit G.832 E3 Frame Generation

G.832 E3 frame generation receives the incoming payload data stream, and overwrites all of the E3 overhead byte locations.

The first two bytes of the first row in the frame are overwritten with the frame alignment bytes FA1 and FA2, which have a value of F6h and 28h respectively.

The first byte in the second row of the frame is overwritten with the EM byte which is a BIP-8 calculated over all of the bytes of the previous frame after all frame processing (frame generation, error insertion, overhead insertion, and AIS generation) has been performed. The first byte in the third row of the frame is overwritten with the TR byte which is input from the transmit trail trace controller.

The first byte in the fourth row of the frame is overwritten with the MA byte (see Figure 10-18), which consists of the RDI bit, REI bit, payload type, multiframe indicator, and timing source indicator.

The RDI bit can be generated automatically, set to one, or set to zero. The RDI source is programmable (automatic, 1, or 0). If the RDI is generated automatically, it is set to one when one or more of the indicated alarm conditions is present, and set to zero when all of the indicated alarm conditions are absent. Automatically setting RDI on LOS, LOF, or AIS is individually programmable (on or off).

The REI bit can be generated automatically or inserted from a register bit. The REI source is programmable (automatic or register). If REI is generated automatically, it is one when at least one parity error has been detected during the previous frame.

The payload type is sourced from a register. The three register bits are inserted in the third, fourth, and fifth bits of the MA byte in each frame.

The multiframe indicator and timing marker bits can be directly inserted from a 3-bit register or generated from a 4-bit register. The multiframe indicator and timing marker insertion type is programmable (direct or generated). When the multiframe indicator and timing marker bits are directly inserted, the three register bits are inserted in the last three bits of the MA byte in each frame. When the multiframe indicator and timing marker bits are generated, the four timing source indicator bits are transferred in a four-frame multiframe, MSB first. The multiframe indicator bits (sixth and seventh bits of the MA byte) identify the phase of the multiframe (00, 01, 10, or 11), and the timing marker bit (eighth bit of the MA byte) contains the corresponding timing source indicator bit (TMABR register bits TTI3, TTI2, TTI1, or TTI0 respectively). Note: The initial phase of the multiframe is arbitrarily chosen.

The first byte in the fifth row of the frame is overwritten with the NR byte which can be sourced from a register, from the transmit FEAC controller, or from the transmit HDLC controller. The NR byte source is programmable (register, FEAC, or HDLC). Note: The HDLC controller will source eight bits per frame period regardless of whether the NR byte only, GC byte only, or both are programmed to be sourced from the HDLC controller.

The first byte in the sixth row of the frame is overwritten with the GC byte which can be sourced from a register or from the transmit HDLC controller. The GC byte source is programmable (register or HDLC).

Once all of the E3 overhead bytes have been overwritten, the data stream is passed on to error insertion. If frame generation is disabled, the incoming E3 signal is passed on directly to error insertion. Frame generation is programmable (on or off).

10.6.8.3 Transmit G.832 E3 Error Insertion

Error insertion inserts various types of errors into the different E3 overhead bytes. The types of errors that can be inserted are framing errors, BIP-8 parity errors, and Remote Error Indication (REI) errors.

The type of framing error(s) inserted is programmable (errored frame alignment bit or errored frame alignment word). A frame alignment bit error is a single bit error in the frame alignment word (FA1 or FA2). A frame alignment word error is an error in all sixteen bits of the frame alignment word (the values 09h and D7h are inserted in the FA1 and FA2 bytes respectively). Framing error(s) can be inserted one error at a time, or four consecutive frames. The framing error insertion mode (single or four) is programmable.

The type of BIP-8 error(s) inserted is programmable (errored BIP-8 bit, or errored BIP-8 byte). An errored BIP-8 bit is inverting a single bit error in the EM byte. An errored BIP-8 byte is inverting all eight bits in the EM byte. BIP-8 error(s) can be inserted one error at a time, or continuously. The BIP-8 error insertion mode (single or continuous) is programmable.

An REI error is generated by forcing the second bit of the MA byte to a one. REI error(s) can be inserted one error at a time, or continuously. The REI error insertion mode (single or continuous) is programmable.

Each error type (framing, BIP-8, or REI) has a separate enable. Continuous error insertion mode inserts errors at every opportunity. Single error insertion mode inserts an error at the next opportunity when requested. The framing multi-error insertion mode inserts the indicated number of errors at the next opportunities when requested. i.e., a single request will cause multiple errors to be inserted. The requests can be initiated by a register bit(TSEI) or by the manual error insertion input (TMEI). The error insertion request source (register or input) is programmable. The insertion of each particular error type is individually enabled. Once all error insertion has been performed, the data stream is passed on to overhead insertion.

10.6.8.4 Transmit G.832 E3 Overhead Insertion

Overhead insertion can insert any (or all) of the E3 overhead bytes into the E3 frame. The E3 overhead bytes FA1, FA2, EM, TR, MA, NR, and GC can be sourced from the transmit overhead interface (TOHCLK, TOH, TOHEN, and TOHSOF). The EM byte is sourced as an error mask (modulo 2 addition of the input EM byte and the generated EM byte). The E3 overhead insertion is fully controlled by the transmit overhead interface. If the transmit overhead data enable signal (TOHEN) is driven high, then the bit on the transmit overhead signal (TOH) is inserted into the output data stream. Insertion of bits using the TOH signal overwrites internal overhead insertion.

10.6.8.5 Transmit G.832 E3 AIS Generation

G.832 E3 AIS generation overwrites the data stream with AIS. If transmit AIS is enabled, the data stream (payload and E3 overhead) is forced to all ones.

10.6.8.6 Receive G.832 E3 Frame Processor

The G.832 E3 frame format is shown in Figure 10-17. FA1 and FA2 are the Frame Alignment bytes. EM is the Error Monitoring byte used for path error monitoring. TR is the Trail Trace byte used for end-to-end connectivity verification. MA is the Maintenance and Adaptation byte used for far-end path status and performance monitoring (see Figure 10-18). NR is the Network Operator byte allocated for network operator maintenance purposes. GC is the General Purpose Communications Channel byte allocated for user communications purposes.

10.6.8.7 Receive G.832 E3 Framing

G.832 E3 framing determines the G.832 E3 frame boundary. The frame boundary is found by identifying the frame alignment bytes FA1 and FA2, which have a value of F6h and 28h respectively. The framer is an off-line framer that updates the data path frame counters when an out of frame (OOF) condition has been detected. The use of an off-line framer reduces the average time required to reframe, and reduces data loss caused by burst error. The G.832 E3 framer checks each bit position for the frame alignment word (FA1 and FA2). The frame boundary is set once the frame alignment word is identified. Since, the frame alignment word check is performed one bit at a time, up to 4296 checks may be needed to find the frame boundary. The data path frame counters are updated if an error free frame alignment word is received for two additional frames, and an OOF condition is present.

10.6.8.8 Receive G.832 E3 Performance Monitoring

Performance monitoring checks the E3 frame for alarm conditions and errors. The alarm conditions detected are OOF, LOF, COFA, LOS, AIS, RUA1, and RDI. The errors accumulated are framing, parity, and Remote Error Indication (REI) errors. An Out Of Frame (OOF) condition is declared when four consecutive frame alignment words (FA1 and FA2) contain one or more errors, when 986 or more frames out of 1,000 frames has a BIP-8 block error, or at the next framing word check when a manual reframe is requested. An OOF condition is terminated when three consecutive frame alignment words (FA1 and FA2) are error free or the G.832 E3 framer updates the data path frame counters.

A Loss Of Frame (LOF) condition is declared by the LOF integration counter when it has been active for a total of *T* ms. The LOF integration counter is active (increments count) when an OOF condition is present, it is inactive (holds count) when an OOF condition is absent, and it is reset when an OOF condition is absent for *T* continuous ms. *T* is programmable (0, 1, 2, or 3). An LOF condition is terminated when an OOF condition is absent for *T* continuous ms.

A Change Of Frame Alignment (COFA) is declared when the G.832 E3 framer updates the data path frame counters with a frame alignment that is different from the current data path frame alignment.

A Loss Of Signal (LOS) condition is declared when the HDB3 encoder is active, and it declares an LOS condition. An LOS condition is terminated when the HDB3 encoder is inactive, or it terminates an LOS condition.

An Alarm Indication Signal (AIS) condition is declared when 7 or less zeros are detected in each of two consecutive frame periods that do not contain a frame alignment word. An AIS condition is terminated when 8 or more zeros are detected in each of two consecutive frame periods.

A Receive Unframed All 1's (RUA1) condition is declared if in each of 4 consecutive 2047 bit windows, five or less zeros are detected and an OOF condition is continuously present. A RUA1 condition is terminated if in each of 4 consecutive 2047 bit windows, six or more zeros are detected or an OOF condition is continuously absent.

A Remote Defect Indication (RDI) condition is declared when four consecutive frames are received with the RDI bit (first bit of MA byte) set to one. An RDI condition is terminated when four consecutive frames are received with the RDI bit set to zero.

Three types of errors are accumulated, framing, parity, and Remote Error Indication (REI) errors. Framing errors are determined by comparing FA1 and FA2 to their expected values. The type of framing errors accumulated is programmable (OOFs, bit, byte, or word). An OOF error increments the count whenever an OOF condition is first detected. A bit error increments the count once for each bit in FA1 and each bit in FA2 that does not match its expected value (up to 16 per frame). A byte error increments the count once for each FA byte (FA1 or FA2) that does not match its expected value (up to 2 per frame). A word error increments the count once for each FA word (both FA1 and FA2) that does not match its expected value (up to 1 per frame).

Parity errors are determined by calculating the BIP-8 (8-Bit Interleaved Parity) of the current E3 frame (overhead and payload bytes), and comparing the calculated BIP-8 to the EM byte in the next frame. The type of parity errors accumulated is programmable (bit or block). A bit error increments the count once for each bit in the EM byte that does not match the corresponding bit in the calculated BIP-8 (up to 8 per frame). A block error increments the count if any bit in the EM byte does not match the corresponding bit in the calculated BIP-8 (up to 1 per frame).

REI errors are determined by the REI bit (second bit of MA byte). A one indicates an error and a zero indicates no errors.

The receive alarm indication (RAI) signal is high when one or more of the indicated alarm conditions is present, and low when all of the indicated alarm conditions are absent. Setting the receive alarm indication on LOS, OOF, LOF, or AIS is individually programmable (on or off).

The receive error indication (REI) signal will transition from low to high once for each frame in which a parity error is detected.

10.6.8.9 Receive G.832 E3 Overhead Extraction

Overhead extraction extracts all of the E3 overhead bytes from the G.832 E3 frame. All of the E3 overhead bytes FA1, FA2, EM, TR, MA, NR, and GC are output on the receive overhead interface (ROH, ROHSOF, and ROHCLK).

The EM byte is output as an error indication (modulo 2 addition of the calculated BIP-8 and the EM byte.

The TR byte is sent to the receive trail trace controller.

The payload type (third, fourth, and fifth bits of the MA byte) is integrated and stored in a register with change and unstable indications. The integrated received payload type is also compared against an expected payload type. If the received and expected payload types do not match (see Table 10-30), a mismatch indication is set.

Table 10-30. Payload Label Match Status

EXPECTED	RECEIVED	STATUS
000	000	Match
000	001	Mismatch
000	XXX	Mismatch
001	000	Mismatch
001	001	Match
001	XXX	Match
XXX	000	Mismatch
XXX	001	Match
XXX	XXX	Match
XXX	YYY	Mismatch

XXX and YYY equal any value other than 000 or 001; XXX ≠ YYY.

The multiframe indicator and timing marker bits (sixth, seventh, and eighth bits of the MA byte) can be integrated and stored in three register bits or extracted, integrated, and stored in four register bits. The bits (three or four) are stored with a change indication. The multiframe indicator and timing marker storage type is programmable (integrated or extracted). When the multiframe indicator and timing marker bits are integrated, the last three bits of the MA byte are integrated and stored in three register bits. When the multiframe indicator and timing marker bits are extracted, four timing source indicator bits are transferred in a four-frame multiframe, MSB first. The multiframe indicator bits (sixth and seventh bits of the MA byte) identify the phase of the multiframe (00, 01, 10, or 11). The timing marker bit (eighth bit of the MA byte) contains the timing source indicator bit indicated by the multiframe indicator bits (first, second, third, or fourth bit respectively). The four timing source indicator bits are extracted from the multiframe, integrated, and stored in four register bits with unstable and change indications.

The NR byte is integrated and stored in a register along with a change indication, it is sent to the receive FEAC controller, and it can be sent to the receive HDLC controller. The byte sent to the receive HDLC controller is programmable (NR or GC).

The GC byte is integrated and stored in a register along with a change indication, and can be sent to the receive HDLC controller. The byte sent to the receive HDLC controller is programmable (NR or GC).

10.6.8.10 Receive G.832 Downstream AIS Generation

Downstream G.832 E3 AIS can be automatically generated on an OOF, LOS, or AIS condition or manually inserted. If automatic downstream AIS is enabled, downstream AIS is inserted when an LOS, OOF, or AIS condition is declared. Automatic downstream AIS is programmable (on or off). If manual downstream AIS insertion is enabled, downstream AIS is inserted. Manual downstream AIS insertion is programmable (on or off). Downstream AIS is removed when all OOF, LOS, and AIS conditions are terminated and manual downstream AIS insertion is disabled. RPDT will be forced to all ones during downstream AIS.

10.7 HDLC Overhead Controller

10.7.1 General Description

The DS3170 device contains a built-in HDLC controller with 256 byte FIFOs for insertion/extraction of DS3 PMDL, G.751 Sn bit and G.832 NR/GC bytes.

The HDLC Overhead Controller demaps HDLC overhead packets from the DS3/E3 data stream in the receive direction and maps HDLC packets into the DS3/E3 data stream in the transmit direction.

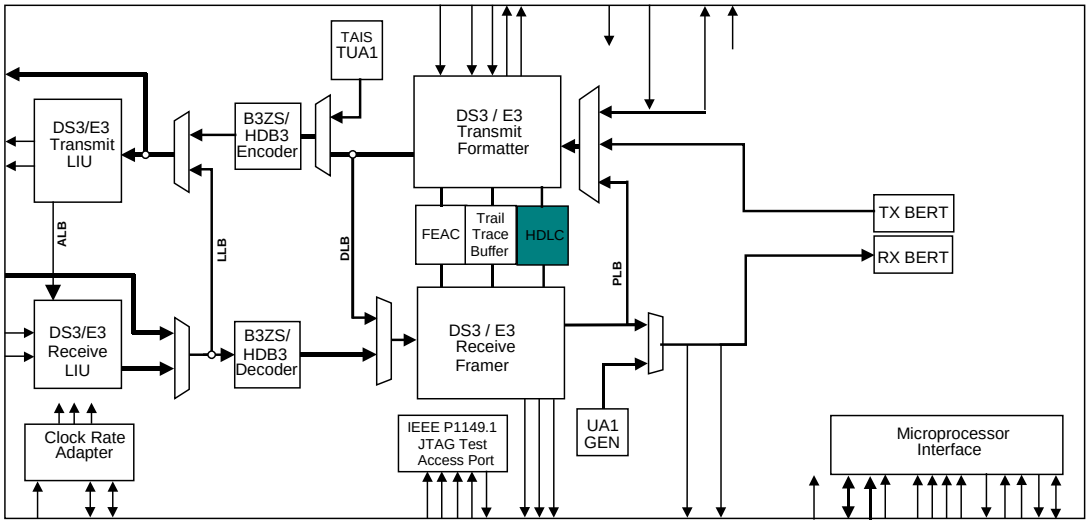
The receive direction performs packet processing and stores the packet data in the FIFO. It removes packet data from the FIFO and outputs the packet data to the microprocessor via the register interface.

The transmit direction inputs the packet data from the microprocessor via the register interface and stores the packet data in the FIFO. It removes the packet data from the FIFO and performs packet processing.

The bits in a byte are received MSB first, LSB last. When they are output serially, they are output MSB first, LSB last. The bits in a byte in an incoming signal are numbered in the order they are received, 1 (MSB) to 8 (LSB). However, when a byte is stored in a register, the MSB is stored in the lowest numbered bit (0), and the LSB is stored in the highest numbered bit (7). This is to differentiate between a byte in a register and the corresponding byte in a signal.

See Figure 10-19 for the location of HDLC controllers within the DS3170 device.

Figure 10-19. HDLC Controller Block Diagram



10.7.2 Features

- **Programmable inter-frame fill** – The inter-frame fill between packets can be all 1's or flags.
- **Programmable FCS generation/monitoring** – An FCS-16 can be generated and appended to the end of the packet, and the FCS can be checked and removed from the end of the packet.
- **Programmable bit reordering** – The packet data can be can be output MSB first or LSB first from the FIFO.
- **Programmable data inversion** – The packet data can be inverted immediately after packet processing on the transmit, and immediately before packet processing on the receive.
- **Fully independent transmit and receive paths**
- **Fully independent Line side and register interface timing** – The data storage can be read from or written to via the microprocessor interface while all line side clocks and signals are inactive, and read from or written to via the line side while all microprocessor interface clocks and signals are inactive.

10.7.3 Transmit FIFO

The Transmit FIFO block contains memory for 256 bytes of data with data status information and controller circuitry for reading and writing the memory. The Transmit FIFO controller functions include filling the memory, tracking the memory fill level, maintaining the memory read and write pointers, and detecting memory overflow and underflow conditions. The Transmit FIFO receives data and status from the microprocessor interface, and stores the data along with the data status information in memory. The Transmit Packet Processor reads the data and data status information from the Transmit FIFO. The Transmit FIFO also outputs FIFO fill status (empty/data storage available/full) via the microprocessor interface. All operations are byte based. The Transmit FIFO is considered empty when its memory does not contain any data. The Transmit FIFO is considered to have data storage available when its memory has a programmable number of bytes or more available for storage. The Transmit FIFO is considered full when it does not have any space available for storage. The Transmit FIFO accepts data from the register interface until full. If the Transmit FIFO is written to while the FIFO is full, the write is ignored, and a FIFO overflow condition is declared. The Transmit Packet Processor reads the Transmit FIFO. If the Transmit Packet Processor attempts to read the Transmit FIFO while it is empty, a FIFO underflow condition is declared.

10.7.4 Transmit HDLC Overhead Processor

The Transmit HDLC Overhead Processor accepts data from the Transmit FIFO, performs bit reordering, FCS processing, stuffing, packet abort sequence insertion, and inter-frame padding.

A byte is read from the Transmit FIFO with a packet end status. When a byte is marked with a packet end indication, the output data stream will be padded with FFh and marked with a FIFO empty indication if the Transmit FIFO contains less than two bytes or transmit packet start is disabled. Transmit packet start is programmable (on or off). When the Transmit Packet Processor reads the Transmit FIFO while it is empty, the output data stream is marked with an abort indication. Once the Transmit FIFO is empty, the output data stream will be padded with interframe fill until the Transmit FIFO contains two or more bytes of data and transmit packet start is enabled.

Bit reordering changes the bit order of each byte. If bit reordering is disabled, the outgoing 8-bit data stream DT[1:8] with DT[1] being the MSB and DT[8] being the LSB is input from the Transmit FIFO with the MSB in TFD[0] and the LSB in TFD[7] of the transmit FIFO data TFD[7:0]. If bit reordering is enabled, the outgoing 8-bit data stream DT[1:8] is input from the Transmit FIFO with the MSB in TFD[7] and the LSB in TFD[0] of the transmit FIFO data TFD[7:0]. DT[1] is the first bit transmitted on the outgoing data stream.

FCS processing calculates an FCS and appends it to the packet. FCS calculation is a CRC-16 calculation over the entire packet. The polynomial used for the CRC-16 is $x^{16} + x^{12} + x^5 + 1$. The CRC-16 is inverted after calculation, and appended to the packet. For diagnostic purposes, an FCS error can be inserted. This is accomplished by appending the calculated CRC-16 without inverting it. FCS error insertion is programmable (on or off). When FCS processing is disabled, the packet is output without appending an FCS. FCS processing is programmable (on or off).

Stuffing inserts control data into the packet to prevent packet data from mimicking flags. Stuffing is halted during FIFO empty periods. The 8-bit parallel data stream is multiplexed into a serial data stream, and bit stuffing is performed. Bit stuffing consists of inserting a '0' directly following any five contiguous '1's. Stuffing is performed from a packet start until a packet end.

Inter-frame padding inserts inter-frame fill between the packet start and end flags when the FIFO is empty. The inter-frame fill can be flags or '1's. If the inter-frame fill is flags, flags (minimum two) are inserted until a packet start is received. If the inter-frame fill is all '1's, an end flag is inserted, ‘1’s are inserted until a packet start is received, and a start flag is inserted after the ‘1’s. The number of '1's between the end flag and start flag may not be an integer number of bytes, however, the inter-frame fill will be at least 15 consecutive '1's. If the FIFO is not empty between a packet end and a packet start, then two flags are inserted between the packet end and packet start. The inter-frame padding type is programmable (flags or ‘1’s).

Packet abort insertion inserts a packet abort sequences as necessary. If a packet abort indication is detected, a packet abort sequence is inserted and inter-frame padding is done until a packet start is detected. The abort sequence is FFh.

Once all packet processing has been completed, the datastream is inserted into the DS3/E3 datastream at the proper locations. If transmit data inversion is enabled, the outgoing data is inverted after packet processing is performed. Transmit data inversion is programmable (on or off).

10.7.5 Receive HDLC Overhead Processor

The Receive HDLC Overhead Packet Processor accepts data from the DS3/E3 Framer and performs packet delineation, inter-frame fill filtering, packet abort detection, destuffing, FCS processing, and bit reordering. If receive data inversion is enabled, the incoming data is inverted before packet processing is performed. Receive data inversion is programmable (on or off).

Packet delineation determines the packet boundary by identifying a packet start flag. Each time slot is checked for a flag sequence (7Eh). Once a flag is found, if it is identified as a start or end flag, and the packet boundary is set. There may be a single flag (both end and start) between packets, there may be an end flag and a start flag with a shared zero (011111101111110) between packets, there may be an end flag and a start flag (two flags) between packets, or there may be an end flag, inter-frame fill, and a start flag between packets. The flag check is performed one bit at a time.

Inter-frame fill filtering removes the inter-frame fill between a start flag and an end flag. All inter-frame fill is discarded. The inter-frame fill can be flags (01111110) or all '1's. When inter-frame fill is all ‘1’s, the number of '1's between the end flag and the start flag may not be an integer number of bytes. When inter-frame fill is flags, the

number of bits between the end flag and the start flag will be an integer number of bytes (flags). Any time there is less than 16 bits between two flags, the data will be discarded.

Packet abort detection searches for a packet abort sequence. Between a packet start flag and a packet end flag, if an abort sequence is detected, the packet is marked with an abort indication, and all subsequent data is discarded until a packet start flag is detected. The abort sequence is seven consecutive ones.

Packet abort detection searches for a packet abort sequence. Between a packet start flag and a packet end flag, if an abort sequence is detected, the packet is marked with an abort indication, and all subsequent data is discarded until a packet start flag is detected. The abort sequence is seven consecutive ones.

Destuffing removes the extra data inserted to prevent data from mimicking a flag or an abort sequence. After a start flag is detected, destuffing is performed until an end flag is detected. Destuffing consists of discarding any '0' that directly follows five contiguous '1's. After destuffing is completed, the serial bit stream is demultiplexed into an 8-bit parallel data stream and passed on with packet start, packet end, and packet abort indications. If there is less than eight bits in the last byte, an invalid packet status is set, and the packet is tagged with an abort indication. If a packet ends with five contiguous '1's, the packet will be processed as a normal packet regardless of whether or not the five contiguous '1's are followed by a '0'.

FCS processing checks the FCS, discards the FCS bytes, and marks FCS erred packets. The FCS is checked for errors, and the last two bytes are removed from the end of the packet. If an FCS error is detected, the packet is marked with an FCS error indication. The HDLC CONTROLLER performs FCS-16 checking. FCS processing is programmable (on or off). If FCS processing is disabled, FCS checking is not performed, and all of the packet data is passed on.

Bit reordering changes the bit order of each byte. If bit reordering is disabled, the incoming 8-bit data stream DT[1:8] with DT[1] being the MSB and DT[8] being the LSB is output to the Receive FIFO with the MSB in RFD[0] and the LSB in RFD[7] of the receive FIFO data RFD[7:0]. If bit reordering is enabled, the incoming 8-bit data stream DT[1:8] is output to the Receive FIFO with the MSB in RFD[7] and the LSB in RFD[0] of the receive FIFO data RFD[7:0]. DT[1] is the first bit received from the incoming data stream.

Once all of the packet processing has been completed, The 8-bit parallel data stream is passed on to the Receive FIFO with packet start, packet end, and packet error indications.

10.7.6 Receive FIFO

The Receive FIFO block contains memory for 256 bytes of data with data status information and controller circuitry for reading and writing the memory. The Receive FIFO Controller controls filling the memory, tracking the memory fill level, maintaining the memory read and write pointers, and detecting memory overflow and underflow conditions. The Receive FIFO accepts data and data status from the Receive Packet Processor and stores the data along with data status information in memory. The data is read from the receive FIFO via the microprocessor interface. The Receive FIFO also outputs FIFO fill status (empty/data available/full) via the microprocessor interface. All operations are byte based. The Receive FIFO is considered empty when it does not contain any data. The Receive FIFO is considered to have data available when there is a programmable number of bytes or more stored in the memory. The Receive FIFO is considered full when it does not have any space available for storage.

The Receive FIFO accepts data from the Receive Packet Processor until full. If a packet start is received while full, the data is discarded and a FIFO overflow condition is declared. If any other packet data is received while full, the current packet being transferred is marked with an abort indication, and a FIFO overflow condition is declared. Once a FIFO overflow condition is declared, the Receive FIFO will discard incoming data until a packet start is received while the Receive FIFO has sixteen or more bytes available for storage. If the Receive FIFO is read while the FIFO is empty, the read is ignored, and an invalid data indication given.

10.8 Trail Trace Controller

10.8.1 General Description

The DS3170 has a dedicated Trail Trace Buffer for E3-G.832 link management

The Trail Trace Controller performs extraction and storage of the incoming G.832 trail access point identifier in a 16-byte receive register.

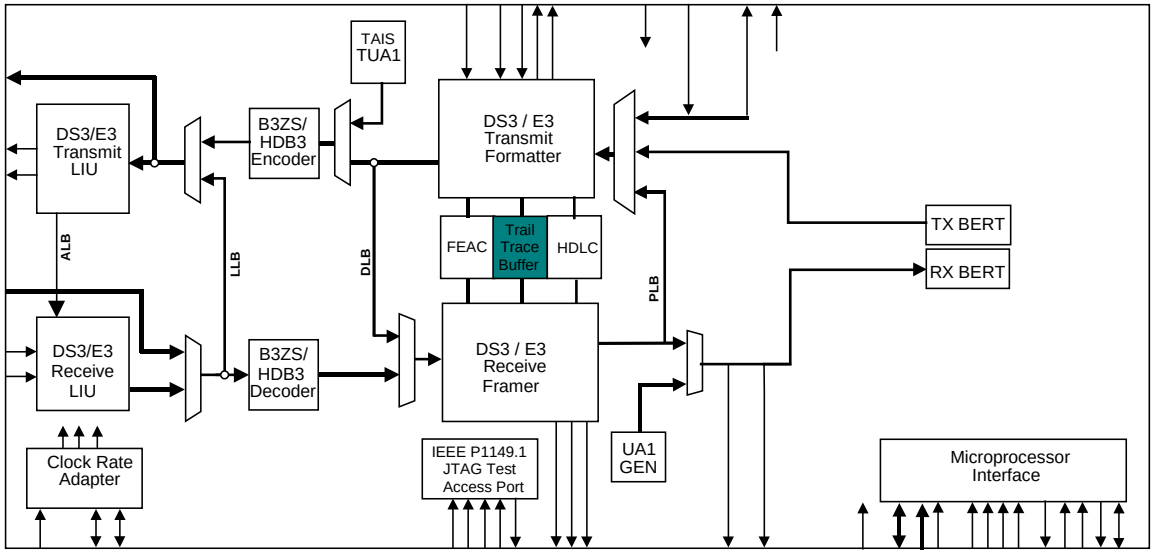
The Trail Trace Controller extracts/inserts E3-G.832 trail access point identifiers using a 16-byte register(one for transmit, one for receive).

The Trail Trace Controller demaps a 16-byte trail trace identifier from the E3-G.832 datastream in the receive direction and maps a trace identifier into the E3-G.832 datastream in the transmit direction.

The receive direction inputs the trace ID data stream, performs trace ID processing, and stores the trace identifier data in the data storage using line timing. It removes trace identifier data from the data storage and outputs the trace identifier data to the microprocessor via the microprocessor interface using register timing. The data is forced to all ones during LOS, LOF and AIS detection to eliminate false messages

The transmit direction inputs the trace identifier data from the microprocessor via the microprocessor interface and stores the trace identifier data in the data storage using register timing. It removes the trace identifier data from the data storage, performs trace ID processing, and outputs the trace ID data stream. Refer to Figure 10-20 for the location of the Trail Trace Controller with the DS3170 device.

Figure 10-20. Trail Trace Controller Block Diagram



10.8.2 Features

- **Programmable trail trace ID** – The trail trace ID controller can be programmed to handle a 16-byte trail trace identifier (trail trace mode).
- **Programmable transmit trace ID** – All sixteen bytes of the transmit trail trace identifier are programmable.
- **Programmable receive expected trace ID** – A 16-byte expected trail trace identifier can be programmed. Both a mismatch and unstable indication are provided.
- **Programmable trace ID multiframe alignment** – The transmit side can be programmed to perform trail trace multiframe alignment insertion. The receive side can be programmed to perform trail trace multiframe synchronization.
- **Programmable bit reordering** – The trace identifier data can be output MSB first or LSB first from the data storage.
- **Programmable data inversion** – The trace identifier data can be inverted immediately after trace ID processing on the transmit side, and immediately before trail ID processing on the receive side.
- **Fully independent transmit and receive sides**
- **Fully independent Line side and register interface timing** – The data storage can be read from or written to via the microprocessor interface while all line side clocks and signals are inactive, and read from or written to via the line side while all microprocessor interface clocks and signals are inactive.

10.8.3 Functional Description

The bits in a byte are received most significant bit (MSB) first and least significant bit (LSB) last. When they are output serially, they are output MSB first and LSB last. The bits in a byte in an incoming signal are numbered in the

order they are received, 1 (MSB) to 8 (LSB). However, when a byte is stored in a register, the MSB is stored in the highest numbered bit (7), and the LSB is stored in the lowest numbered bit (0). This is to differentiate between a byte in a register and the corresponding byte in a signal.

10.8.4 Transmit Data Storage

The Transmit Data Storage block contains memory for 16 bytes of data and controller circuitry for reading and writing the memory. The Transmit Data Storage controller functions include filling the memory and maintaining the memory read and write pointers. The Transmit Data Storage receives data from the microprocessor interface, and stores the data in memory. The Transmit Trace ID Processor reads the data from the Transmit Data Storage. The Transmit Data Storage contains the transmit trail trace identifier. Note: The contents of the transmit trail (path) trace identifier memory will be random data immediately after power-up, and will not change during a reset ($\overline{RST}$ or $\overline{DRST}$ low).

10.8.5 Transmit Trace ID Processor

The Transmit Trace ID Processor accepts data from Transmit Data Storage, processes the data according to the Transmit Trace ID mode, and outputs the serial trace ID data stream.

10.8.6 Transmit Trail Trace Processing

The Transmit Trail Trace Processing accepts data from the Transmit Data Storage performs bit reordering and multiframe alignment insertion.

Bit reordering changes the bit order of each byte. If bit reordering is disabled, the outgoing 8-bit data stream DT[1:8] with DT[1] being the MSB and DT[8] being the LSB is input from the Transmit Data Storage with the MSB in TTD[7] and the LSB in TTD[0] of the transmit trace ID data TTD[7:0]. If bit reordering is enabled, the outgoing 8-bit data stream DT[1:8] is input from the Transmit Data Storage with the MSB is in TTD[0] and the LSB is in TTD[7] of the transmit trace ID data TTD[7:0]. DT[1] is the first bit transmitted on the outgoing data stream.

Multiframe alignment insertion overwrites the MSB of each trail trace byte with the multiframe alignment signal. The MSB of the first byte in the trail trace identifier is overwritten with a one, the MSB of the other fifteen bytes in the trail trace identifier are overwritten with a zero. Multiframe alignment insertion is programmable (on or off).

If transmit data inversion is enabled, the outgoing data is inverted after trail trace processing is performed. Transmit data inversion is programmable (on or off). If transmit trail trace identifier idle (Idle) is enabled, the trail trace data is overwritten with all zeros. Transmit Idle is programmable (on or off).

10.8.7 Receive Trace ID Processor

The Receive Trace ID Processor receives the incoming serial trace ID data stream and processes the incoming data according to the Receive Trace ID mode, and passes the trace ID data on to Receive Data Storage.

The bits in a byte are received MSB first, LSB last. The bits in a byte in an incoming signal are numbered in the order they are received, 1 (MSB) to 8 (LSB). However, when a byte is stored in a register, the MSB is stored in the highest numbered bit (7), and the LSB is stored in the lowest numbered bit (0). This is to differentiate between a byte in a register and the corresponding byte in a signal.

10.8.8 Receive Trail Trace Processing

The Receive Trail Trace Processing accepts an incoming data line and performs trail trace alignment, trail trace extraction, expected trail trace comparison, and bit reordering. If receive data inversion is enabled, the incoming data is inverted before trail trace processing is performed. Receive data inversion is programmable (on or off).

Trail trace alignment determines the trail trace identifier boundary by identifying the multiframe alignment signal. The multiframe alignment signal (MAS) is located in the MSB of each byte (Figure 10-21). The MAS bits are each checked for the multiframe alignment start bit, which is a one. Once a multiframe alignment start bit is found, the remaining fifteen bits of the MAS are verified as being zero. The MAS check is performed one byte at a time. Multiframe alignment is programmable (on or off). When multiframe alignment is disabled, the incoming bytes are sequentially stored starting with a random byte.

Figure 10-21. Trail Trace Byte (DT = Trail Trace Data)

Bit 1 MSB	Bit 2	Bit 3	Bit 4	Bit 5	Bit 6	Bit 7	Bit 8 LSB
MAS or DT[1]	DT[2]	DT[3]	DT[4]	DT[5]	DT[6]	DT[7]	DT[8]

Trail trace extraction extracts the trail trace identifier from the incoming trail trace data stream, generates a trail trace identifier change indication, detects a trail trace identifier idle (Idle) condition, and detects a trail trace identifier unstable (TIU) condition. The trail trace identifier bytes are stored sequentially with the first byte (MAS equals 1 if trail trace alignment is enabled) being stored in the first byte of memory. If the exact same nonzero trail trace identifier is received five consecutive times and it is different from the receive trail trace identifier, a receive trail trace identifier update is performed, and the receive trail trace identifier change indication is set.

An Idle condition is declared when an all zeros trail trace identifier is received five consecutive times. An Idle condition is terminated when a nonzero trail trace identifier is received five consecutive times or a TIU condition is declared. A TIU condition is declared if eight consecutive trail trace identifiers are received that do not match either the receive trail trace identifier or the previously stored current trail trace identifier. The TIU condition is terminated when a nonzero trail trace identifier is received five consecutive times or an Idle condition is declared.

Expected trail trace comparison compares the received and expected trail trace identifiers. The comparison is a 7-bit comparison of the seven least significant bits (DT[2:8] (see Figure 10-21) of each trail trace identifier byte (The multiframe alignment signal is ignored). If the received and expected trail trace identifiers do not match, a trail trace identifier mismatch (TIM) condition is declared. If they do match the TIM condition is terminated. The 16-byte expected trail trace identifier is programmable. Expected trail trace comparison is programmable (on or off). If multiframe alignment is disabled, expected trail trace comparison is disabled. Immediately after a reset, the receive trail trace identifier is invalid. All comparisons between the receive trail trace identifier and expected trail trace identifier will match (a TIM condition cannot occur) until after the first receive trail trace identifier update occurs.

Bit reordering changes the bit order of each byte. If bit reordering is disabled, the incoming 8-bit data stream DT[1:8] with DT[1] being the MSB and DT[8] being the LSB is output to the Receive Data Storage with the MSB in RTD[7] and the LSB in RTD[0] of the receive trace ID data RTD[7:0]. If bit reordering is enabled, the incoming 8-bit data stream DT[1:8] is output to the Receive Data Storage with the MSB in RTD[0] and the LSB in RTD[7] of the receive trace ID data RTD[7:0]. DT[1] is the first bit received from the incoming data stream.

Once all of the trail trace processing has been completed, The 8-bit parallel data stream is passed on to the Receive Data Storage.

10.8.9 Receive Data Storage

The Receive Data Storage block contains memory for 48 bytes of data, maintains data status information, and has controller circuitry for reading and writing the memory. The Receive Data Storage controller functions include filling the memory and maintaining the memory read and write pointers. The Receive Data Storage accepts data and data status from the Receive Trace ID Processor, stores the data in memory, and maintains data status information. The data is read from the Receive Data Storage via the microprocessor interface. The Receive Data Storage contains the current trail trace identifier, the receive trail trace identifier, and the expected trail trace identifier.

10.9 FEAC Controller

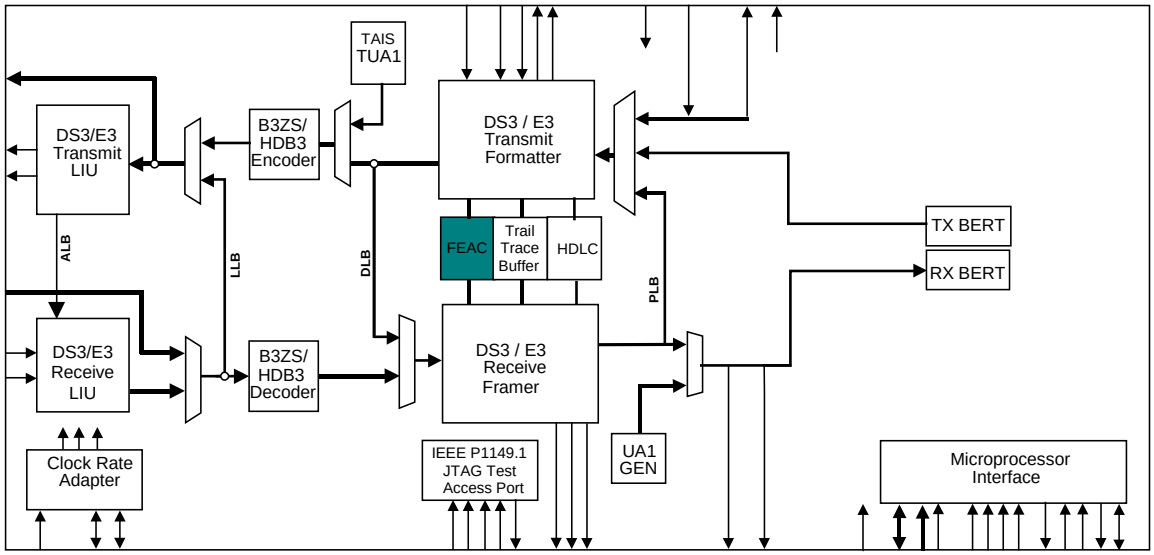
10.9.1 General Description

The FEAC Controller demaps FEAC codewords from a DS3/E3 data stream in the receive direction and maps FEAC codewords into a DS3/E3 data stream in the transmit direction. The transmit direction demaps FEAC codewords from a DS3/E3 data stream.

The receive direction performs FEAC processing, and stores the codewords in the FIFO using line timing. It removes the codewords from the FIFO and outputs them to the microprocessor via the register interface.

The transmit direction inputs codewords from the microprocessor via the register interface and stores the codewords. It removes the codewords and performs FEAC processing. See Figure 10-22 for the location of the FEAC Controller in the block diagram

Figure 10-22. FEAC Controller Block Diagram



10.9.2 Features

- **Programmable dual codeword output** – The transmit side can be programmed to output a single codeword ten times, one codeword ten times followed by a second codeword ten times, or a single codeword continuously.
- **Four codeword receive FIFO**
- **Fully independent transmit and receive paths**
- **Fully independent Line side and register side timing** – The FIFO can be read from or written to at the register interface side while all line side clocks and signals are inactive, and read from or written to at the line side while all register interface side clocks and signals are inactive.

10.9.3 Functional Description

The bits in a code are received MSB first, LSB last. When they are output serially, they are output MSB first, LSB last. The bits in a code in an incoming signal are numbered in the order they are received, 1 (MSB) to 6 (LSB). However, when a code is stored in a register, the MSB is stored in the lowest numbered bit (0), and the LSB is stored in the highest numbered bit (5). This is to differentiate between a code in a register and the corresponding code in a signal.

10.9.3.1 Transmit Data Storage

The Transmit Data Storage block contains the registers for two FEAC codes (C{1:6]) and controller circuitry for reading and writing the memory. The Transmit Data Storage receives data from the microprocessor interface, and stores the data in memory. The Transmit FEAC Processor reads the data from the Transmit Data Storage.

10.9.3.2 Transmit FEAC Processor

The Transmit FEAC Processor accepts data from the Transmit Data Storage performs FEAC processing. The FEAC codes are read from Transmit Data Storage with the MSB (C[1]) in TFCA[0] or TFCB[0], and the LSB (C[6]) in TFCA[5] or TFCB[5].

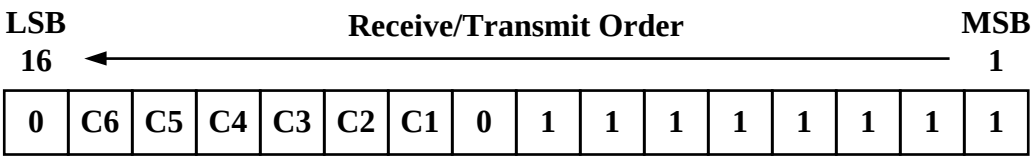
FEAC processing has four modes of operation (Idle, single code, dual code, and continuous code). In Idle mode, all ones are output on the outgoing FEAC data stream. In single code mode, the code from TFCA[5:0] is inserted into a codeword (Figure 10-23), and sent ten consecutive times. Once the ten codewords have been sent, all ones are output. In dual code mode, the code from TFCA[5:0] is inserted into a codeword, and sent ten consecutive times. Then the code from TFCB[5:0] is inserted into a codeword, and sent ten consecutive times. Once both codewords

have both been sent ten times, all ones are output. In continuous mode, the code from TFCA[5:0] is inserted into a codeword, and sent until the mode is changed

10.9.3.3 Receive FEAC Processor

The Receive FEAC Processor accepts an incoming data line and extracts all overhead and performs FEAC code extraction , and Idle detection.

Figure 10-23. FEAC Codeword Format



Cx - FEAC Code

FEAC code extraction determines the codeword boundary by identifying the codeword sequence and extracts the FEAC code. A FEAC codeword is a repeating 16-bit pattern (see Figure 10-23). The codeword sequence is the pattern (0xxxxxx011111111) that contains each FEAC code (C[6:1]). Each time slot is checked for a codeword sequence. Once a codeword sequence is found, the FEAC code is checked. If the same FEAC code is received in three consecutive codewords without errors, the FEAC code detection indication is set, and the FEAC code is stored in the Receive FIFO with the MSB (C[1]) in RFF[0], and the LSB (C[6]) in RFF[5]. The FEAC code detection indication is cleared if two consecutively received FEAC codewords differ from the current FEAC codeword, or a FEAC Idle condition is detected.

Idle detection detects a FEAC Idle condition. A FEAC idle condition is declared if sixteen consecutive ones are received. The FEAC Idle condition is terminated when the FEAC code detection indication is set.

10.9.3.4 Receive FEAC FIFO

The Receive FIFO block contains memory for four FEAC codes (C{1:6]) and controller circuitry for reading and writing the memory. The Receive FIFO controller functions include filling the memory, tracking the memory fill level, maintaining the memory read and write pointers, and detecting memory overflow and underflow conditions. The Receive FIFO accepts data from the Receive FEAC Processor and stores the data in memory. The data is read from the receive FIFO via the microprocessor interface. The Receive FIFO also outputs FIFO fill status (empty) via the microprocessor interface. All operations are code based (six bits). The Receive FIFO is considered empty when it does not contain any data. The Receive FIFO accepts data from the Receive FEAC Processor until full. If a FEAC code is received while full, the data is discarded and a FIFO overflow condition is declared. If the Receive FIFO is read while the FIFO is empty, the read is ignored.

10.10 Line Encoder/Decoder

10.10.1 General Description

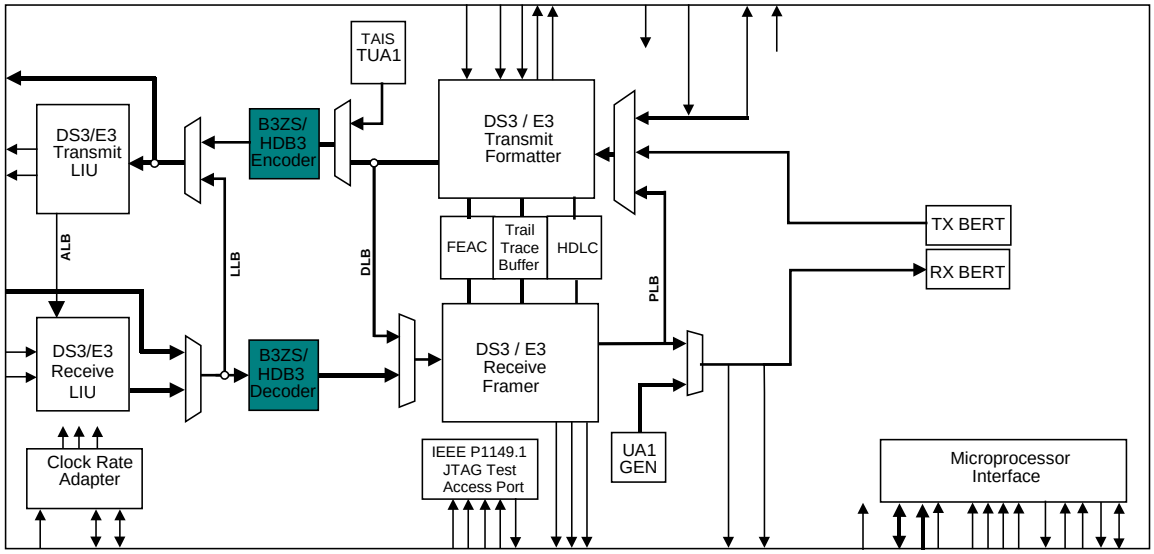
The B3ZS/HDB3 Decoder converts a bipolar signal to a unipolar signal in the receive direction. B3ZS/HDB3 Encoder converts a unipolar signal to a bipolar signal in the transmit direction.

In the transmit direction, the Encoder receives a unipolar signal, converts it to a bipolar signal, optionally performs zero suppression encoding, optionally inserts errors, and outputs the bipolar signals.

In the receive direction, the Decoder receives a bipolar signal, monitors it for alarms and errors, optionally performs zero suppression decoding, and converts it to a unipolar signal.

If the port line interface is configured for a Unipolar mode, the BPV detector will count pulses on the RLCV pin. See Figure 10-24 for the locations of the Line Encoder/ Decorder block in the DS3170 device.

Figure 10-24. Line Encoder/Decoder Block Diagram



10.10.2 Features

- **Performs bipolar to unipolar encoding and decoding** – Converts a unipolar signal into an AMI bipolar signal (POS data, and NEG data) and vice versa.
- **Programmable zero suppression** – B3ZS or HDB3 zero suppression encoding and decoding can be performed, or the bipolar data stream can be left as an AMI encoded data stream.
- **Programmable receive zero suppression code format –** The signature of B3ZS or HDB3 is selectable**.**
- **Generates and detects alarms and errors** – In the receive direction, detects LOS alarm condition BPV errors, and EXZ errors. In the transmit direction, errors can be inserted into the outgoing data stream.

10.10.3 B3ZS/HDB3 Encoder

B3ZS/HDB3 Encoder performs unipolar to bipolar conversion and zero suppression encoding.

Unipolar to bipolar conversion converts the unipolar data stream into an AMI bipolar data stream (POS and NEG). In an AMI bipolar data stream a zero is represented by a zero on both the POS and NEG signals, and a one is represented by a one on a bipolar signal (POS or NEG), and a zero on the other bipolar signal (NEG or POS). Successive ones are represented by ones that are alternately output on the POS and NEG signals. i.e., if a one is represented by a one on POS and a zero on NEG, the next one will be represented by a one on NEG and a zero on POS.

Zero suppression encoding converts an AMI bipolar data stream into a B3ZS or HDB3 encoded bipolar data stream. A B3ZS encoded bipolar signal is generated by inserting a B3ZS signature into the bipolar data stream if both the POS and NEG signals are zero for three consecutive clock periods. An HDB3 encoded bipolar signal is generated by inserting an HDB3 signature into the bipolar data stream if both the POS and NEG signals are zero for four consecutive clock periods. Zero suppression encoding can be disabled which will result in AMI-coded data.

Error insertion is also performed. Error insertion inserts bipolar violation (BPV) or excessive zero (EXZ) errors onto the bipolar signal. A BPV error will be inserted when three consecutive ones occur. An EXZ error will be inserted when three (or four) consecutive zeros on the bipolar signal occur by inhibiting the insertion of a B3ZS (HDB3) signature. There will be at least one intervening pulse between consecutive BPV or EXZ errors. A single BPV or EXZ error inserted will be detected as a single BPV/EXZ error at the far-end, and will not cause any other type of error to be detected. For example, if a BPV error is inserted, the far-end should not also detect a data error.

10.10.4 Transmit Line Interface

The Transmit Line Interface accepts a bipolar data stream from the B3ZS/HDB3 Encoder, performs error insertion, and transmits the bipolar data stream.

Error insertion inserts BPV or EXZ errors into the bipolar signal. When a BPV error is to be inserted, the Transmit Line Interface waits for the next occurrence of three consecutive ones. The first bipolar one is generated according to the normal AMI rules. The second bipolar one is generated by transmitting the same values on TPOS and TNEG

as the values for the first one. The third bipolar one is generated according to the normal AMI rules. When an EXZ error is to be inserted, the Transmit Line Interface waits for the next occurrence of three (four) consecutive zeros on the bipolar signal, and inhibits the insertion of a B3ZS (HDB3) signature. There must be at least one intervening one between consecutive BPV or EXZ errors. A single BPV or EXZ error inserted must be detected as a single BPV/EXZ error at the far-end, and not cause any other type of error to be detected. For example, if a BPV error is inserted, the far-end should not also detect a data error. If a second error insertion request of a given type (BPV or EXZ) is initiated before a previous request has been completed, the second request will be ignored.

The outgoing bipolar data stream consists of positive pulse data (TPOS) and negative pulse data (TNEG). TPOS and TNEG are updated on the rising edge of TLCLK.

10.10.5 Receive Line Interface

The Receive Line Interface receives a bipolar signal. The incoming bipolar data line consists of positive pulse data (RPOS), negative pulse data (RNEG), and clock (RLCLK) signals. RPOS and RNEG are sampled on the rising edge of RLCLK. The incoming bipolar signal is checked for a Loss Of Signal (LOS) condition, and passed on to B3ZS/HDB3 Decoder. An LOS condition is declared if both RPOS and RNEG do not have any transitions for 192 clock cycles. The LOS condition is terminated after 192 clock cycles without any EXZ errors. Note: When zero suppression (B3ZS or HDB3) decoding is disabled, the LOS condition is cleared, and cannot be detected.

10.10.6 B3ZS/HDB3 Decoder

The B3ZS/HDB3 Decoder receives a bipolar signal from the LIU (or the RPOS/RNEG pins). The incoming bipolar signal is checked for a Loss of Signal (LOS) condition. An LOS condition is declared if both the positive pulse data and negative pulse data signals do not have any transitions for 192 clock cycles. The LOS condition is terminated after 192 clock cycles without any EXZ errors.

B3ZS/HDB3 Decoder performs EXZ detection, zero suppression decoding, BPV detection, and bipolar to unipolar conversion.

EXZ detection checks the bipolar data stream for excessive zeros (EXZ) errors. In B3ZS mode, an EXZ error is declared whenever there is an occurrence of 3 or more zeros. In HDB3 mode, an EXZ error is declared whenever there is an occurrence of 4 or more zeros. EXZ errors are accumulated in the EXZ counter (*LINE.REXZCR* register).

Zero-suppression decoding converts B3ZS or HDB3 encoded bipolar data into an AMI bipolar signal. In B3ZS mode, the encoded bipolar signal is checked for a B3ZS signature. If a B3ZS signature is found, it is replaced with three zeros. In HDB3 mode, the encoded bipolar signal is checked for an HDB3 signature. If an HDB3 signature is found, it is replaced with four zeros. The format of both an HDB3 signature and a B3ZS signature is programmable. When LINE.RCR.RZSF = 0, the decoder will search for a zero followed by a BPV in B3ZS mode, and in HDB3 mode it will search for two zeros followed by a BPV. If LINE.RCR.RZSF = 1, the same criteria is applied with an additional requirement that the BPV must be the opposite polarity of the previous BPV. Please refer to Figure 10-25 and Figure 10-26. Zero suppression decoding is also programmable (on or off). Note: Immediately after a reset or a LOS condition, the first B3ZS/HDB3 signature to be detected will not depend upon the polarity of any BPV contained within the signature.

Figure 10-25. B3ZS Signatures

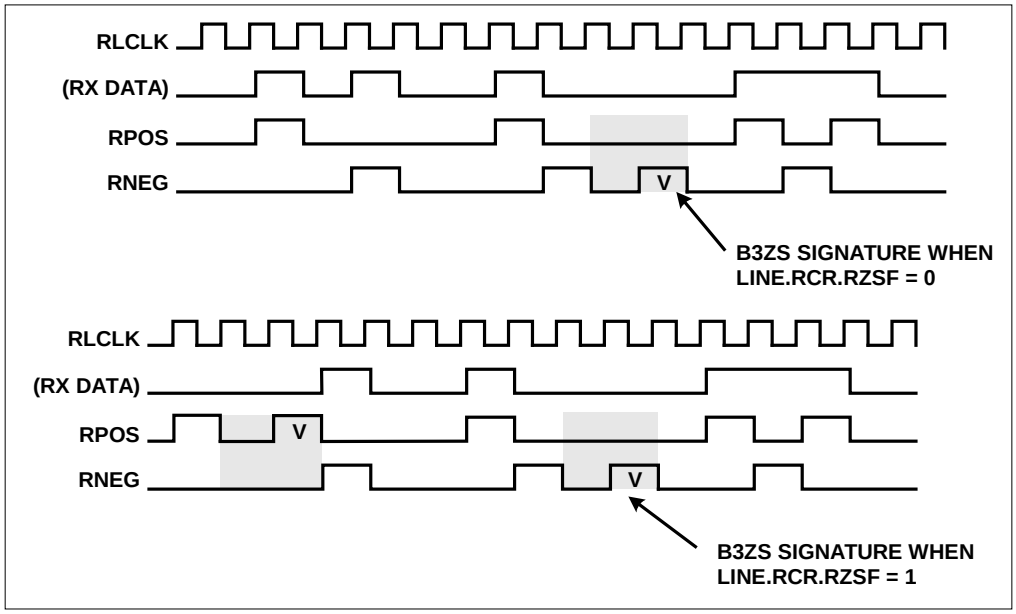
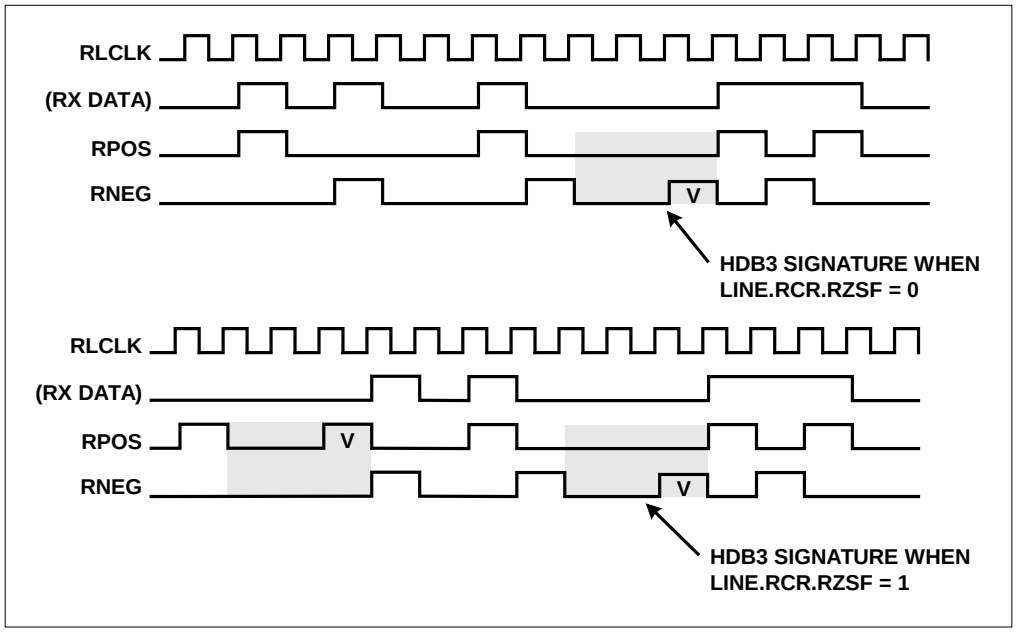


Figure 10-26. HDB3 Signatures



BPV detection checks the bipolar signal for bipolar violation (BPV) errors and E3 code violation (CV) errors. A BPV error is declared if two 1's are detected on RXP or RXN without an intervening 1 on RXN or RXP, and the 1's are not part of a B3ZS/HDB3 signature, or when both RXP and RXN are a one. An E3 coding violation is declared if consecutive BPVs of the same polarity are detected (ITU O.161 definition). E3 CVs are accumulated in the BPV counter (*LINE.RBPVCR* register) if E3 CV detection has been enabled (applicable only in HDB3 mode), otherwise, BPVs are accumulated in the BPV counter. If zero code suppression is disabled, the BPV counter will count all bipolar violations. The BPV counter will count pulses on the RLCV pin when the device is configured for unipolar mode.

Immediately after a reset (or datapath reset) or a LOS condition, a BPV will not be declared when the first valid one (RPOS high and RNEG low, or RPOS low and RNEG high) is received. Bipolar to unipolar conversion converts the AMI bipolar data into a unipolar signal by OR'ing together the RXP and RXN signals.

10.11 BERT

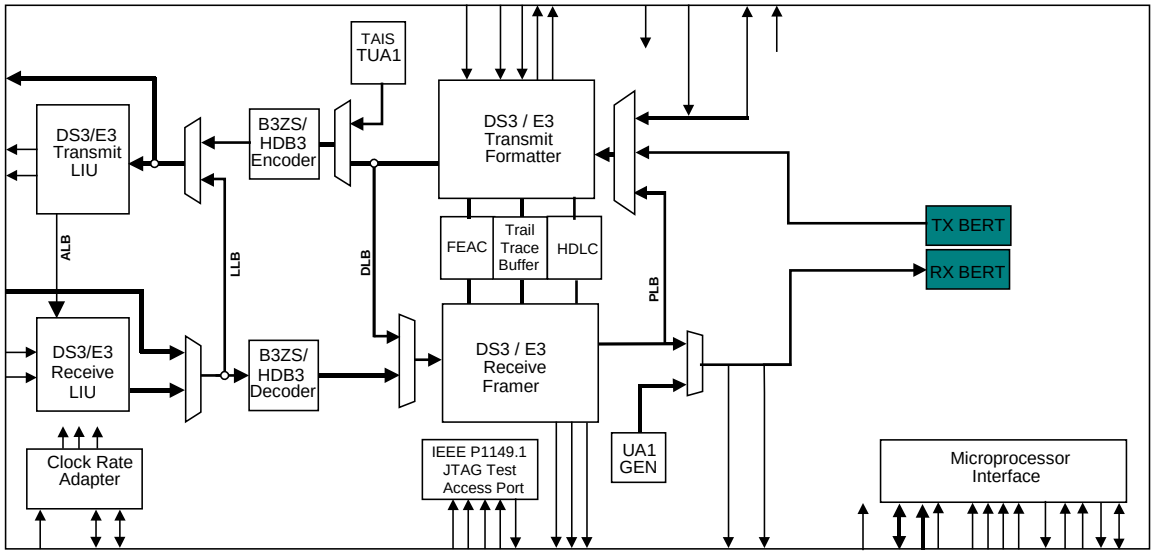
10.11.1 General Description

The BERT is a software programmable test pattern generator and monitor capable of meeting most error performance requirements for digital transmission equipment. It will generate and synchronize to pseudo-random patterns with a generation polynomial of the form $x^n + x^y + 1$, where n and y can take on values from 1 to 32 and to repetitive patterns of any length up to 32 bits.

The transmit direction generates the programmable test pattern, and inserts the test pattern payload into the data stream.

The receive direction extracts the test pattern payload from the receive data stream, and monitors the test pattern payload for the programmable test pattern. See Figure 10-27 for the location of the BERT Block within the DS3170 device.

Figure 10-27. BERT Block Diagram



10.11.2 Features

- **Programmable PRBS pattern** – The Pseudo Random Bit Sequence (PRBS) polynomial ($x^n + x^y + 1$) and seed are programmable (length n = 1 to 32, tap y = 1 to n - 1, and seed = 0 to $2^n - 1$).
- **Programmable repetitive pattern** – The repetitive pattern length and pattern are programmable (the length n = 1 to 32 and pattern = 0 to $2^n - 1$).
- **24-bit error count and 32-bit bit count registers**
- **Programmable bit error insertion** – Errors can be inserted individually, on a pin transition, or at a specific rate. The rate $1/10^n$ is programmable (n = 1 to 7).
- **Pattern synchronization at a 10^{-3} BER** – Pattern synchronization will be achieved even in the presence of a random Bit Error Rate (BER) of 10^{-3}.

10.11.3 Configuration and Monitoring

Set *PORT.CR1*.BENA = 1 to enable the BERT. The BERT must be enabled before the pattern is loaded for the pattern load operation to take affect.

The following tables show how to configure the on-board BERT to send and receive common patterns.

Table 10-31. Pseudo-Random Pattern Generation

PATTERN TYPE	BERT.PCR Register				BERT. PCR	BERT. SPR2	BERT. SPR1	BERT.CR
	PTF[4:0] (hex)	PLF[4:0] (hex)	PTS	QRSS				TPIC, RPIC
2^9-1 O.153 (511 type)	04	08	0	0	0x0408	0xFFFF	0xFFFF	0
2^{11}-1 O.152 and O.153 (2047 type)	08	0A	0	0	0x080A	0xFFFF	0xFFFF	0
2^{15}-1 O.151	0D	0E	0	0	0x0D0E	0xFFFF	0xFFFF	1
2^{20}-1 O.153	10	13	0	0	0x1013	0xFFFF	0xFFFF	0
2^{20}-1 O.151 QRSS	02	13	0	1	0x0253	0xFFFF	0xFFFF	0
2^{23}-1 O.151	11	16	0	0	0x1116	0xFFFF	0xFFFF	1

Table 10-32. Repetitive Pattern Generation

PATTERN TYPE	BERT.PCR Register				BERT. PCR	BERT. SPR2	BERT. SPR1
	PTF[4:0] (hex)	PLF[4:0] (hex)	PTS	QRSS			
all 1s	NA	00	1	0	0x0020	0xFFFF	0xFFFF
all 0s	NA	00	1	0	0x0020	0xFFFF	0xFFFE
alternating 1s and 0s	NA	01	1	0	0x0021	0xFFFF	0xFFFE
double alternating and 0s	NA	03	1	0	0x0023	0xFFFF	0xFFFC
3 in 24	NA	17	1	0	0x0037	0xFF20	0x0022
1 in 16	NA	0F	1	0	0x002F	0xFFFF	0x0001
1 in 8	NA	07	1	0	0x0027	0xFFFF	0xFF01
1 in 4	NA	03	1	0	0x0023	0xFFFF	0xFFF1

After configuring these bits, the pattern must be loaded into the BERT. This is accomplished via a zero-to-one transition on BERT.CR.TNPL and BERT.CR.RNPL

Monitoring the BERT requires reading the BERT.SR Register which contains the Bit Error Count (BEC) bit and the Out of Synchronization (OOS) bit. The BEC bit will be one when the bit error counter is one or more. The OOS will be one when the receive pattern generator is not synchronized to the incoming pattern, which will occur when it receives a minimum 6 bit errors within a 64 bit window. The Receive BERT Bit Count Register (BERT.RBCR1) and the Receive BERT Bit Error Count Register (BERT.RBECR1) will be updated upon the reception of a Performance Monitor Update signal (e.g. BERT.CR.LPMU). This signal will update the registers with the values of the counter since the last update and will reset the counters. Please see section 10.4.5 for more details of the PMU.

10.11.4 Receive Pattern Detection

Since the Receive BERT is always enabled, it can be used as an off-line monitor. The Receive BERT receives only the payload data and synchronizes the receive pattern generator to the incoming pattern. The receive pattern generator is a 32-bit shift register that shifts data from the least significant bit (LSB) or bit 1 to the most significant bit (MSB) or bit 32. The input to bit 1 is the feedback. For a PRBS pattern (generating polynomial $x^n + x^y + 1$), the feedback is an XOR of bit n and bit y. For a repetitive pattern (length n), the feedback is bit n. The values for n and y are individually programmable (1 to 32). The output of the receive pattern generator is the feedback. If QRSS is enabled, the feedback is an XOR of bits 17 and 20, and the output will be forced to one if the next 14 bits are all zeros. QRSS is programmable (on or off). For PRBS and QRSS patterns, the feedback will be forced to one if bits 1 through 31 are all zeros. Depending on the type of pattern programmed, pattern detection performs either PRBS synchronization or repetitive pattern synchronization.

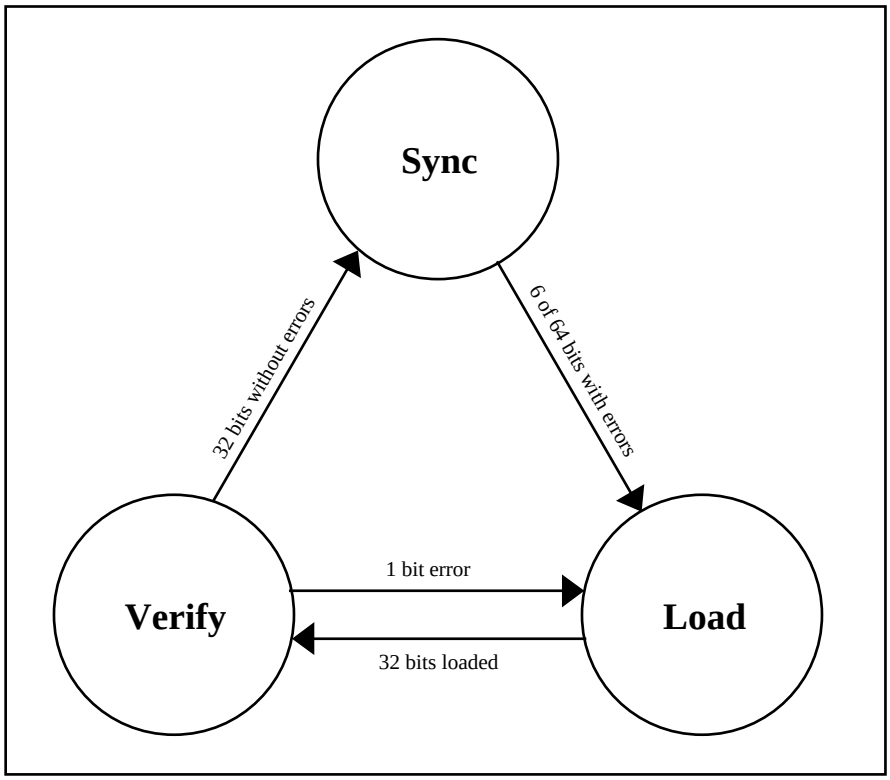
10.11.4.1 Receive PRBS Synchronization

PRBS synchronization synchronizes the receive pattern generator to the incoming PRBS or QRSS pattern. The receive pattern generator is synchronized by loading 32 data stream bits into the receive pattern generator, and

then checking the next 32 data stream bits. Synchronization is achieved if all 32 bits match the incoming pattern. If at least six incoming bits in the current 64-bit window do not match the receive pattern generator, automatic pattern resynchronization is initiated. Automatic pattern resynchronization can be disabled.

Refer to Figure 10-28 for the PRBS synchronization diagram.

Figure 10-28. PRBS Synchronization State Diagram

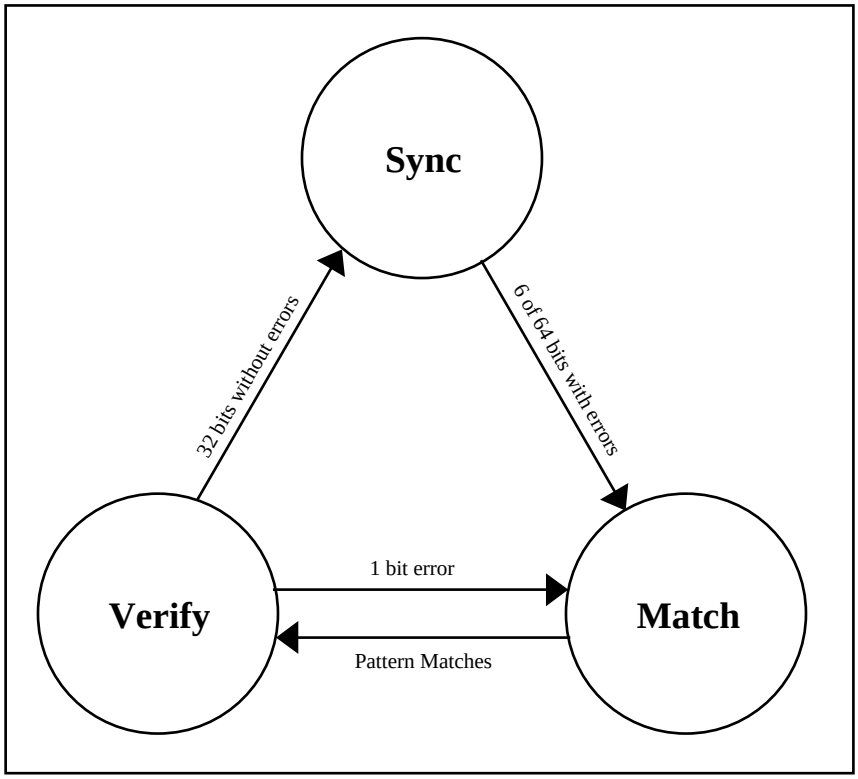


10.11.4.2 Receive Repetitive Pattern Synchronization

Repetitive pattern synchronization synchronizes the receive pattern generator to the incoming repetitive pattern. The receive pattern generator is synchronized by searching each incoming data stream bit position for the repetitive pattern, and then checking the next 32 data stream bits. Synchronization is achieved if all 32 bits match the incoming pattern. If at least six incoming bits in the current 64-bit window do not match the receive PRBS pattern generator, automatic pattern resynchronization is initiated. Automatic pattern resynchronization can be disabled.

Refer to Figure 10-29 for the repetitive pattern synchronization state diagram.

Figure 10-29. Repetitive Pattern Synchronization State Diagram



10.11.4.3 Receive Pattern Monitoring

Receive pattern monitoring monitors the incoming data stream for both an OOS condition and bit errors and counts the incoming bits. An Out Of Synchronization (OOS) condition is declared when the synchronization state machine is not in the “Sync” state. An OOS condition is terminated when the synchronization state machine is in the “Sync” state.

Bit errors are determined by comparing the incoming data stream bit to the receive pattern generator output. If they do not match, a bit error is declared, and the bit error and bit counts are incremented. If they match, only the bit count is incremented. The bit count and bit error count are not incremented when an OOS condition exists.

10.11.5 Transmit Pattern Generation

Pattern Generation generates the outgoing test pattern, and passes it onto Error Insertion. The transmit pattern generator is a 32-bit shift register that shifts data from the least significant bit (LSB) or bit 1 to the most significant bit (MSB) or bit 32. The input to bit 1 is the feedback. For a PRBS pattern (generating polynomial $x^n + x^y + 1$), the feedback is an XOR of bit n and bit y. For a repetitive pattern (length n), the feedback is bit n. The values for n and y are individually programmable (1 to 32). The output of the receive pattern generator is the feedback. If QRSS is enabled, the feedback is an XOR of bits 17 and 20, and the output will be forced to one if the next 14 bits are all zeros. QRSS is programmable (on or off). For PRBS and QRSS patterns, the feedback will be forced to one if bits 1 through 31 are all zeros. When a new pattern is loaded, the pattern generator is loaded with a seed/pattern value before pattern generation starts. The seed/pattern value is programmable ($0 – 2^n - 1$).

10.11.5.1 Transmit Error Insertion

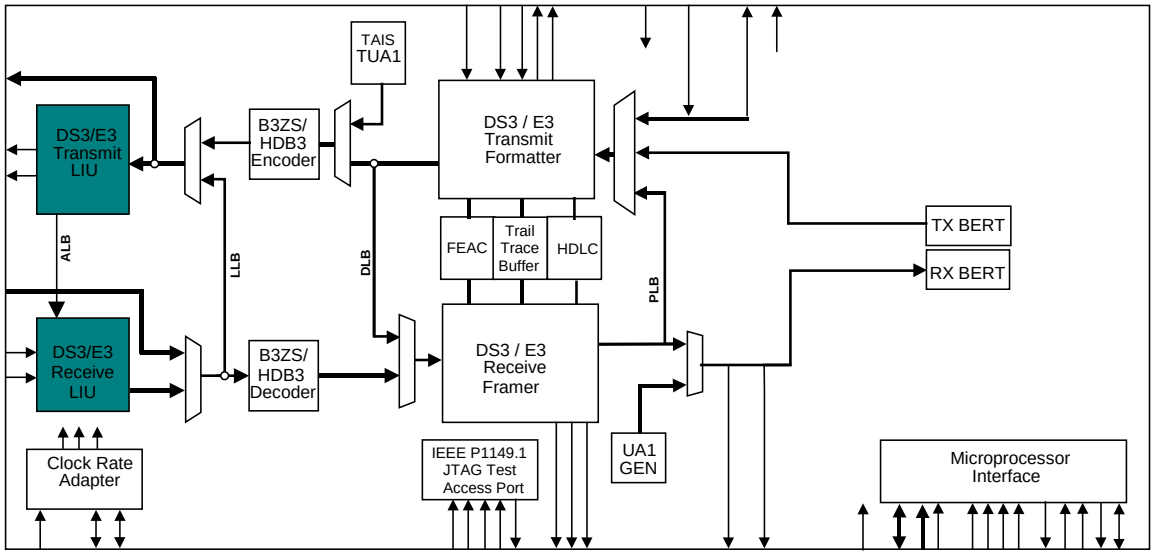
Error insertion inserts errors into the outgoing pattern data stream. Errors are inserted one at a time or at a rate of one out of every 10^n bits. The value of n is programmable (1 to 7 or off). Single bit error insertion can be initiated from the microprocessor interface, or by the manual error insertion input (TMEI). The method of single error insertion is programmable (register or input). If pattern inversion is enabled, the data stream is inverted before the overhead/stuff bits are inserted. Pattern inversion is programmable (on or off).

10.12 LIU – Line Interface Unit

10.12.1 General Description

The line interface units (LIUs) perform the functions necessary for interfacing at the physical layer to DS3 or E3 lines. The LIU has independent receive and transmit paths and a built-in jitter attenuator. See Figure 10-30 for the location within the DS3170 device of the LIU.

Figure 10-30. LIU Functional Diagram



10.12.2 Features

- Performs Receive Clock/Data Recovery and Transmit Waveshaping
- Jitter Attenuators can be Placed in Either the Receive or Transmit Paths
- Interfaces to 75Ω Coaxial Cable at Lengths Up to 380 meters (DS3), 440 meters (E3)
- Use 1:2 Transformers on Tx and RX
- Requires Minimal External Components
- Local and Remote Loopbacks

10.12.2.1 Transmitter

- Gapped clock capable up to 52MHz
- Wide 50 ±20% transmit clock duty cycle
- Clock inversion for glueless interfacing
- Unframed all-ones generator (E3 AIS)
- Line build-out (LBO) control
- Tri-state line driver outputs support protection switching applications
- Per-channel power-down control
- Output driver monitor

10.12.2.2 Receiver

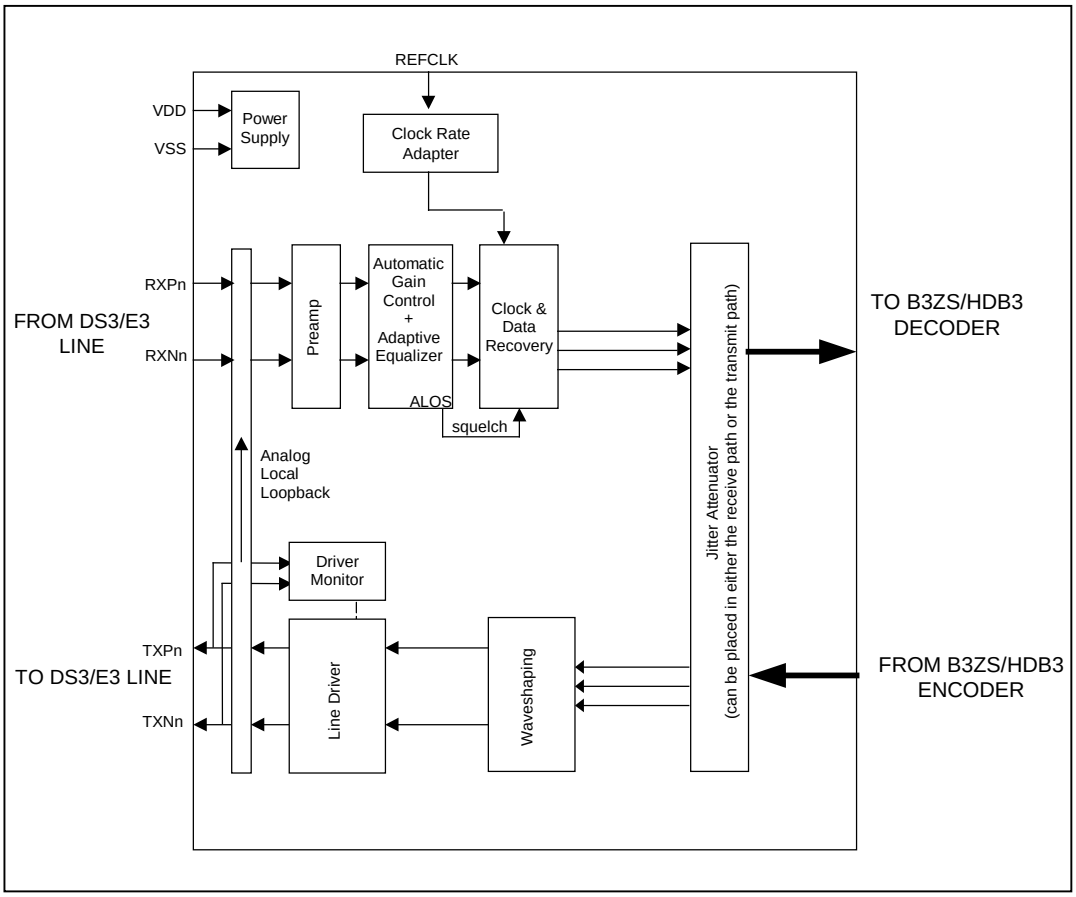
- AGC/equalizer block handles from 0 to 15dB of cable loss
- Loss-of-lock (LOL) PLL status indication
- Interfaces directly to a DSX monitor signal (~20dB flat loss) using built-in preamp
- Digital and analog loss-of-signal (LOS) detectors (ANSI T1.231 and ITU G.775)
- Clock inversion for glueless interfacing
- Per-channel power-down control

10.12.3 Detailed Description

The receiver performs clock and data recovery from an alternate mark inversion (AMI) coded signal or a B3ZS- or HDB3-coded AMI signal and monitors for loss of the incoming signal. The transmitter drives standard pulse-shape

waveforms onto 75Ω coaxial cable. Refer to Figure 10-31 for a detailed functional block diagram of the DS3/E3 LIU. The jitter attenuator can be mapped into the receiver data path, mapped into the transmitter data path, or be disabled. The DS3/E3 LIU conforms to the telecommunications standards listed in Table 5-1. Figure 2-1 shows the external components required for proper operation.

Figure 10-31. DS3/E3 LIU Block Diagram



10.12.4 Transmitter

10.12.4.1 Transmit Clock

The clock used in the LIU Transmitter is typically based on either the CLAD clock or TCLKI, selected by the CLADC bit in *PORT.CR3*.

10.12.4.2 Waveshaping, Line Build-Out, Line Driver

The waveshaping block converts the transmit clock, positive data, and negative data signals into a single AMI signal with the waveshape required for interfacing to DS3/E3 lines. Table 16-7 through Table 16-9 and Figure 16-11 (AC Timing Section) show the waveform template specifications and test parameters.

Because DS3 signals must meet the waveform templates at the cross-connect through any cable length from 0 to 450ft, the waveshaping circuitry includes a selectable LBO feature. For cable lengths of 225ft or greater, the TLBO configuration bit (*PORT.CR2*.TLBO) should be low. When TLBO is low, output pulses are driven onto the coaxial cable without any preattenuation. For cable lengths less than 225ft, TLBO should be high to enable the LBO circuitry. When TLBO is high, pulses are preattenuated by the LBO circuitry before being driven onto the coaxial cable. The LBO circuitry provides attenuation that mimics the attenuation of 225ft of coaxial cable.

The transmitter line driver can be disabled and the TXP and TXN outputs tri-stated by asserting the LTS configuration bit (*PORT.CR2*.LTS). Powering down the transmitter through the TPD configuration bit (CPU bus mode) also tri-states the TXP and TXN outputs.

10.12.4.3 Interfacing to the Line

The transmitter interfaces to the outgoing DS3/E3 coaxial cable (75Ω) through a 2:1 step-down transformer connected to the TXP and TXN pins. Figure 2-1 shows the arrangement of the transformer and other recommended interface components. Table 10-33 specifies the required characteristics of the transformer.

10.12.4.4 Transmit Driver Monitor

If the transmit driver monitor detects a faulty transmitter, it sets the *PORT.SR*.TDM status bit. When the transmitter is tri-stated, the transmit driver monitor is also disabled. The transmitter is declared to be faulty when the transmitter outputs see a load of less than ~25Ω.

10.12.4.5 Transmitter Power-Down

To minimize power consumption when the transmitter is not being used, assert the *PORT.CR1*.PD configuration bit. When the transmitter is powered down, the TXP and TXN pins are put in a high-impedance state and the transmit amplifiers are powered down.

10.12.4.6 Transmitter Jitter Generation (Intrinsic)

The transmitter meets the jitter generation requirements of all applicable standards, with or without the jitter attenuator enabled.

10.12.4.7 Transmitter Jitter Transfer

Without the jitter attenuator enabled in the transmit side, the transmitter passes jitter through unchanged. With the jitter attenuator enabled in the transmit side, the transmitter meets the jitter transfer requirements of all applicable telecommunication standards. See Table 5-1.

10.12.5 Receiver

10.12.5.1 Interfacing to the Line

The receiver can be transformer-coupled or capacitor-coupled to the line. Typically, the receiver interfaces to the incoming coaxial cable (75Ω) through a 1:2 step-up transformer. Figure 2-1 shows the arrangement of the transformer and other recommended interface components. Table 10-33 specifies the required characteristics of the transformer. Figure 10-31 shows a general overview of the LIU block. The receiver expects the incoming signal to be in B3ZS- or HDB3-coded AMI format.

Table 10-33. Transformer Characteristics

PARAMETER	VALUE
Turns Ratio	1:2ct ±2%
Bandwidth 75Ω	0.250MHz to 500MHz (typ)
Primary Inductance	19µH (min)
Leakage Inductance	0.12µH (max)
Interwinding Capacitance	10pF (max)
Isolation Voltage	$1500V_{RMS}$ (min)

Table 10-34. Recommended Transformers

MANUFACTURER	PART	TEMP RANGE	PIN-PACKAGE/ SCHEMATIC	OCL PRIMARY (µH) (min)	L_L (µH) (max)	BANDWIDTH 75Ω (MHz)
Pulse Engineering	PE-65968	0°C to +70°C	6 SMT LS-1/C	19	0.06	0.250 to 500
Pulse Engineering	PE-65969	0°C to +70°C	6 Thru-Hole LC-1/C	19	0.06	0.250 to 500
Halo Electronics	TG07-0206NS	0°C to +70°C	6 SMT SMD/B	19	0.06	0.250 to 500
Halo Electronics	TD07-0206NE	0°C to +70°C	6 DIP DIP/B	19	0.06	0.250 to 500

Note: *Table subject to change. Industrial temperature range and multiport transformers are also available. Contact the manufacturers for details at www.pulseeng.com and www.haloelectronics.com.*

10.12.5.2 Optional Preamp

The receiver can be used in monitoring applications, which typically have series resistors with a resistive loss of approximately 20dB. When the PORT.CR2.RMON bit is high, the receiver compensates for this resistive loss by applying flat gain to the incoming signal before sending the signal to the AGC/equalizer block.

10.12.5.3 Automatic Gain Control (AGC) and Adaptive Equalizer.

The AGC circuitry applies flat (frequency independent) gain to the incoming signal to compensate for flat losses in the transmission channel and variations in transmission power. Since the incoming signal also experiences frequency-dependent losses as it passes through the coaxial cable, the adaptive equalizer circuitry applies frequency-dependent gain to offset line losses and restore the signal. The AGC/equalizer circuitry automatically adapts to coaxial cable losses from 0 to 15dB, which translates into 0 to 380 meters (DS3) or 0 to 440 meters (E3) of coaxial cable (AT&T 734A or equivalent). The AGC and the equalizer work simultaneously but independently to supply a signal of nominal amplitude and pulse shape to the clock and data recovery block. The AGC/equalizer block automatically handles direct (0 meters) monitoring of the transmitter output signal.

10.12.5.4 Clock and Data Recovery (CDR)

The CDR block takes the amplified, equalized signal from the AGC/equalizer block and produces a separate clock, positive data, and negative data signals. The CDR requires a master clock. The master clock is derived from REFCLK.

The receive clock is locked using a clock recovery PLL. The status of the PLL lock is indicated in the RLOL (PORT.SR) status bit. The receive loss-of-lock status bit (RLOL) is set when the difference between the recovered clock frequency and the master clock frequency is greater than 7900ppm and cleared when the difference is less than 7700ppm. A change of state of the *PORT.SR*.RLOL status bit can cause an interrupt on the $\overline{INT}$ pin if enabled to do so by the *PORT.SRIE*.RLOLIE interrupt-enable bit. Note that if the master clock is not present, or the master clock is high and TCLK is not present, RLOL is not set.

10.12.5.5 Loss-of-Signal (LOS) Detector

The receiver contains analog and digital LOS detectors. The analog LOS detector resides in the AGC/equalizer block. If the incoming signal level is less than a signal level approximately 24dB below nominal, analog LOS (ALOS) is declared. The ALOS signal cannot be directly examined, but when ALOS occurs the AGC/equalizer mutes the recovered data, forcing all zeros out of the data recovery circuitry and causing digital LOS (DLOS). DLOS is determined by the Line Decoder block (see Section 10.10.4) and indicated by the LOS status bit (LINE.RSR.LOS).

ALOS clears when the incoming signal level is greater than or equal to a signal level approximately 18dB below nominal.

For E3 LOS Assertion:

The ALOS detector in the AGC/equalizer block detects that the incoming signal is less than or equal to a signal level approximately 24dB below nominal, and mutes the data coming out of the clock and data recovery block. (24dB below nominal in the “tolerance range” of G.775, where LOS may or may not be declared.)

For E3 LOS Clear:

The ALOS detector in the AGC/equalizer block detects that the incoming signal is greater than or equal to a signal level approximately 18dB below nominal, and enables data to come out of the CDR block. (18dB is in the “tolerance range” of G.775, where LOS may or may not be declared.)

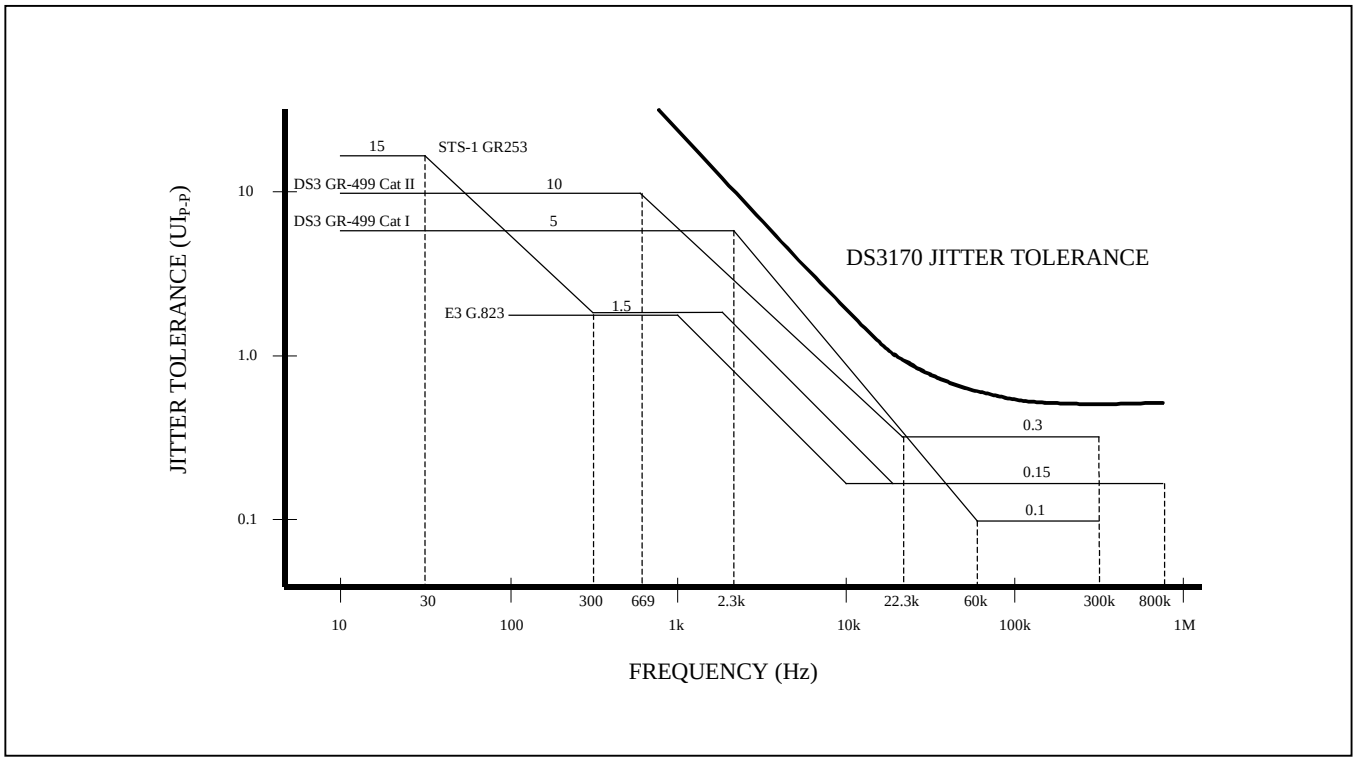
10.12.5.6 Receiver Power-Down

To minimize power consumption when the receiver is not being used, write a one to the *PORT.CR1*.PD bit. When the receiver is powered down, the RCLKO pin is tri-stated. In addition, the RXP and RXN pins become high impedance.

10.12.5.7 Receiver Jitter Tolerance.

The receiver exceeds the input jitter tolerance requirements of all applicable telecommunication standards in Table 5-1. See Figure 10-32.

Figure 10-32. Receiver Jitter Tolerance



11 OVERALL REGISTER MAP

The register addresses of the global, test and the port are concatenated to cover the address range of 000 to 7FF. The address map requires 9 bits of address, ADR[8:0].

The register banks that are not marked with an "X" are not writeable and read back all zeroes. Bits that are underlined are read-only; all other bits are read-write.

Unused bits and registers marked with "—" are ignored when written to, and return zero when read.

Configuration registers can be written to and read from during a data path reset ($\overline{DRST}$ low, and $\overline{RST}$ high). However, all changes to these registers will be ignored during the data path reset. As a result, all initiating action requiring a "0 to 1" transition must be re-initiated after the data path reset is released.

All counters saturate at their maximum count. A counter register is updated by asserting (low to high transition) the performance monitoring update signal (PMU). During the counter register update process, the performance monitoring status signal (PMS) will be deasserted. The counter register update process consists of loading the counter register with the current count, resetting the counter, forcing the zero count status indication low for one clock period, and then asserting PMS. No events shall be missed during an update procedure.

A latched bit is set when the associated event occurs, and remains set until it is cleared. Once cleared, a latched bit will not be set again until the associated event reoccurs (goes away and comes back). A latched on change bit is a latched bit that is set when the event occurs, and when it goes away. A latched status bit can be cleared using clear on read or clear on write techniques, selectable by the GL.CR1.LSBCRE bit. When clear on write is selected, the latched bits in a latched status register will be cleared after the register is read from. If the device is configured for 16-bit mode, all 16 latched status bits will be cleared. If the device is configured for 8-bit mode, only the 8 bits being accessed will be cleared. When clear on write is selected, the latched bits in a latched status register will be cleared when a logic 1 is written to that bit position. For example, writing a FFFFh to a 16-bit latched status register will clear any latched status bit, whereas writing a 0001h will only clear latched bit 0 of the latched status register.

Reserved bits and registers are implemented in a different mode. Reserved configuration bits and registers can be written and read, however they will not affect the operation of the current mode. Reserved status bits will be zero. Reserved latched status bits cannot be set, however, they may remain set or get set during a mode change. Reserved interrupt enable bits can be written and read, and can cause an interrupt if the associated latched status bit is set. Reserved counter registers and the associated counter will retain the values held before a mode change, however, the associated counter cannot be incremented. A performance monitor update will operate normally. If the data path reset is set during or after a mode change, the latched status bits and counter registers (with the associated counters) will be automatically cleared. If the data path reset is not used, then the latched status bits must be cleared via the register interface in the normal manner. And, the counter registers must be cleared by performing two performance monitor updates. The first to clear the associated counter, and load the current count into the counter register, and the second to clear the counter register.

The term "global" is used to make the register names compatible with the mult-port versions (DS3174, DS3173, DS3172, DS3171) of this device.

NOTE: The $\overline{RDY}$ signal will not go active if the user attempts to read or write unused registers not assigned to any design blocks. The $\overline{RDY}$ signal will go active if the user writes or reads reserved registers or unused registers within design blocks.

Table 11-1. Register Address Map

Address offset	Description
000 - 01F	Global registers
020 – 03F	Unused
040 - 05F	Port control registers
060 – 07F	BERT
080 – 08B	Unused

Address offset	Description
08C – 08F	B3ZS/HDB3 transmit line encoder
090 – 09F	B3ZS/HDB3 receive line decoder
0A0 – 0AF	HDLC Transmit
0B0 – 0BF	HDLC Receive
0C0 – 0CF	FEAC Transmit
0D0 – 0DF	FEAC Receive
0E0 – 0E7	Unused
0E8 – 0EF	Trail Trace Transmit
0F0 – 0FF	Trail Trace Receive
100 – 117	Unused
118 – 11F	DS3/E3 Framer Transmit
120 – 13F	DS3/E3 Framer Receive
140 – 17F	Unused
180 – 19F	Test Registers
1A0 – 1FF	Unused

12 REGISTER MAPS AND DESCRIPTIONS

12.1 Registers Bit Maps

Note: In 8-bit mode, register bits[15:8] correspond to the upper byte, and register bits[7:0] correspond to the lower byte. For example, address 001h is the upper byte (bits [15:8]) and address 000h is the lower byte (bits [7:0]) for register GL.IDR in 8-bit mode.

All registers listed, including those designated Unused and Reserved, will cause the $\overline{RDY}$ signal to go low when written to or read from. The "—" designation indicates that the bit is not assigned.

12.1.1 Global Register Bit Map

Table 12-1. Global Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
000	000	GL.IDR	R	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
	001			ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8
002	002	GL.CR1	RW	TMEI	MEIMS	GPM1	GPM0	PMU	LSBCRE	RSTDP	RST
	003			--	INTM	--	--	--	--	--	--
004	004	GL.CR2	RW	--	--	--	--	CLAD2	CLAD1	CLAD0	--
	005			--	--	--	--	G8KRS1	G8KRS0	G8K0S	G8KIS
006-008	006-009	UNUSED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--
00A	00A	GL.GIOCR	RW	GPIO4S1	GPIO4S0	GPIO3S1	GPIO3S0	GPIO2S1	GPIO2S0	GPIO1S1	GPIO1S0
	00B			GPIO8S1	GPIO8S0	GPIO7S1	GPIO7S0	GPIO6S1	GPIO6S0	GPIO5S1	GPIO5S0
00C	00C	UNUSED		--	--	--	--	--	--	--	--
	00D			--	--	--	--	--	--	--	--
010	010	GL.ISR	R				PISR	--	--	--	GSR
	011			--	--	--	--	--	--	--	--
012	012	GL.ISRIE	RW				PISRIE	--	--	--	GSRIE
	013										
014	014	GL.SR	R	--	--	--	--	--	--	CLOL	GPMS
	015			--	--	--	--	--	--	--	--
016	016	GL.SRL	RL	--	--	--	8KREFL	CLADL	ONESL	CLOLL	GPMSL
	017			--	--	--	--	--	--	--	--
018	018	GL.SRIE	R	--	--	--	--	--	ONESIE	CLOLIE	GPMSIE
	019			--	--	--	--	--	--	--	--
01A	01A	UNUSED		--	--	--	--	--	--	--	--
	01B			--	--	--	--	--	--	--	--
01C	01C	**GL.GIORR**	R	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1
	01D			--	--	--	--	--	--	--	--
01E	01E	UNUSED		--	--	--	--	--	--	--	--
	01F			--	--	--	--	--	--	--	--

Table 12-2. Port Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
040	040	PORT.CR1	RW	TMEI	MEIM	--	PMUM	PMU	PD	RSTDP	RST
	041			RES	PAIS2	PAIS1	PAIS0	LAIS1	LAIS0	BENA	RES
042	042	PORT.CR2	RW	RES	RES	FM2	FM1	FM0	RES	RES	RES
	043			TLEN	TTS	RMON	TLBO	RES	LM2	LM1	LM0
044	044	PORT.CR3	RW	P8KRS1	P8KRS0	P8KREF	LOOPT	CLADC	RFTS	TFTS	TLTS
	045			--	--	RCLKS	RSOFOS	RES	TCLKS	TSOFOS	RES
046	046	PORT.CR4	RW	GPIOB3	GPIOB2	GPIOB1	GPIOB0	GPIOA3	GPIOA2	GPIOA1	GPIOA0
	047			--	--	--	--	RES	LBM2	LBM1	LBM0
048	048	UNUSED		--	--	--	--	--	--	--	--
	049			--	--	--	--	--	--	--	--
04A	04A	PORT.INV1	RW	TOHI	TOHCKI	TSOFII	TNEGI	TDATI	TLCKI	TCKOI	TCKII
	04B			RES	RES	--	TSOFOI	RES	TSERI	TOHSI	TOHEI
04C	04C	PORT.INV2	RW	ROHI	ROHCKI	--	RNEGI	RPOSI	RLCKI	RCLKOI	--
	04D			--	RES	RES	RSOFOI	--	RSERI	ROHSI	--
04E	04E	UNUSED		--	--	--	--	--	--	--	--
	04F			--	--	--	--	--	--	--	--
050	050	PORT.ISR	R	TTSR	FSR	HSR	BSR	RES	RES	RES	FMSR
	051			--	--	--	--	--	--	PSR	LCSR
052	052	PORT.SR	R	--	--	--	--	--	TDM	RLOL	PMS
	053			--	--	--	--	--	--	--	--
054	054	PORT.SRL	RL	RLCLKL	TCLKIL	--	--	--	TDML	RLOLL	PMSL
	055			--	--	--	--	--	--	--	--
056	056	PORT.SRIE	RW	--	--	--	--	--	TDMIE	RLOLIE	PMSIE
	057			--	--	--	--	--	--	--	--
058-05E	058-05F	UNUSED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--

Table 12-3. BERT Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
060	060	BERT.CR	RW	PMUM	LPMU	RNPL	RPIC	MPR	APRD	TNPL	TPIC
	061			--	--	--	--	--	--	--	--
062	062	BERT.PCR	RW	--	QRSS	PTS	PLF4	PLF3	PLF2	PLF1	PLF0
	063			--	--	--	PTF4	PTF3	PTF2	PTF1	PTF0
064	064	BERT.SPR1	RW	BSP7	BSP6	BSP5	BSP4	BSP3	BSP2	BSP1	BSP0
	065			BSP15	BSP14	BSP13	BSP12	BSP11	BSP10	BSP9	BSP8
066	066	BERT.SPR2	RW	BSP23	BSP22	BSP21	BSP20	BSP19	BSP18	BSP17	BSP16
	067			BSP31	BSP30	BSP29	BSP28	BSP27	BSP26	BSP25	BSP24
068	068	BERT.TEICR	RW	--	--	TEIR2	TEIR1	TEIR0	BEI	TSEI	MEIMS
	069			--	--	--	--	--	--	--	--
06A	06A	UNUSED		--	--	--	--	--	--	--	--
	06B			--	--	--	--	--	--	--	--
06C	06C	BERT.SR	R	--	--	--	--	PMS	--	BEC	OOS
	06D			--	--	--	--	--	--	--	--
06E	06E	BERT.SRL	RL	--	--	--	--	PMSL	BEL	BECL	OOSL
	06F			--	--	--	--	--	--	--	--
070	070	BERT.SRIE	RW	--	--	--	--	PMSIE	BEIE	BECIE	OOSIE
	071			--	--	--	--	--	--	--	--
072	072	UNUSED		--	--	--	--	--	--	--	--
	073			--	--	--	--	--	--	--	--

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
074	074	BERT.RBECR1	R	BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
	075			BEC15	BEC14	BEC13	BEC12	BEC11	BEC10	BEC9	BEC8
076	076	BERT.RBECR2	R	BEC23	BEC22	BEC21	BEC20	BEC19	BEC18	BEC17	BEC16
	077			--	--	--	--	--	--	--	--
078	078	BERT.RBCR1	R	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
	079			BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8
07A	07A	BERT.RBCR2	R	BC23	BC22	BC21	BC20	BC19	BC18	BC17	BC16
	07B			BC31	BC30	BC29	BC28	BC27	BC26	BC25	BC24
07C-07E	07C	UNUSED		--	--	--	--	--	--	--	--
	07F			--	--	--	--	--	--	--	--

Table 12-4. Line Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
08C	08C	LINE.TCR	RW	--	--	--	TZSD	EXZI	BPVI	TSEI	MEIMS
	08D			--	--	--	--	--	--	--	--
08E	08E	UNUSED		--	--	--	--	--	--	--	--
	08F			--	--	--	--	--	--	--	--
090	090	LINE.RCR	RW	--	--	--	--	E3CVE	REZSF	RDZSF	RZSD
	091			--	--	--	--	--	--	--	--
092	092	UNUSED		--	--	--	--	--	--	--	--
	093			--	--	--	--	--	--	--	--
094	094	LINE.RSR	R	--	--	--	--	EXZC	--	BPVC	LOS
	095			--	--	--	--	--	--	--	--
096	096	LINE.RSRL	RL	--	--	ZSCDL	EXZL	EXZCL	BPVL	BPVCL	LOSL
	097			--	--	--	--	--	--	--	--
098	098	LINE.RSRIE	RW	--	--	ZSCDIE	EXZIE	EXZCIE	BPVIE	BPVCIE	LOSIE
	099			--	--	--	--	--	--	--	--
09A	09A	UNUSED		--	--	--	--	--	--	--	--
	09B			--	--	--	--	--	--	--	--
09C	09C	LINE.RBPVCR	R	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	BPV0
	09D			BPV15	BPV14	BPV13	BPV12	BPV11	BPV10	BPV9	BPV8
09E	09E	LINE.REXZCR	R	EXZ7	EXZ6	EXZ5	EXZ4	EXZ3	EXZ2	EXZ1	EXZ0
	09F			EXZ15	EXZ14	EXZ13	EXZ12	EXZ11	EXZ10	EXZ9	EXZ8

12.1.2 HDLC Register Bit Map

Table 12-5. HDLC Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
0A0	0A0	HDLC.TCR	RW	--	TPSD	TFEI	TIFV	TBRE	TDIE	TFPD	TFRST
	0A1			--	--	--	TDAL4	TDAL3	TDAL2	TDAL1	TDAL0
0A2	0A2	HDLC.TFDR	RW	--	--	--	--	--	--	--	TDPE
	0A3			TFD7	TFD6	TFD5	TFD4	TFD3	TFD2	TFD1	TFD0
0A4	0A4	HDLC.TSR	R	--	--	--	--	--	TFF	TFE	THDA
	0A5			--	--	TFFL5	TFFL4	TFFL3	TFFL2	TFFL1	TFFL0
0A6	0A6	HDLC.TSRL	RL	--	--	TFOL	TFUL	TPEL	--	TFEL	THDAL
	0A7			--	--	--	--	--	--	--	--
0A8	0A8	HDLC.TSRIE	RW	--	--	TFOIE	TFUIE	TPEIE	--	TFEIE	THDAIE
	0A9			--	--	--	--	--	--	--	--

Address 16-bit	8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
0AA-0AE	0AA	UNUSED		--	--	--	--	--	--	--	--
	0AF			--	--	--	--	--	--	--	--
0B0	0B0	HDLC.RCR	RW	--	--	--	--	RBRE	RDIE	RFPD	RFRST
	0B1			--	--	--	RDAL4	RDAL3	RDAL2	RDAL1	RDAL0
0B2	0B2	UNUSED		--	--	--	--	--	--	--	--
	0B3			--	--	--	--	--	--	--	--
0B4	0B4	HDLC.RSR	R	--	--	--	--	--	RFF	RFE	RHDA
	0B5			--	--	--	--	--	--	--	--
0B6	0B6	HDLC.RSRL	RL	RFOL	--	--	RPEL	RPSL	RFFL	--	RHDAL
	0B7			--	--	--	--	--	--	--	--
0B8	0B8	HDLC.RSRIE	RW	RFOIE	--	--	RPEIE	RPSIE	RFFIE	--	RHDAIE
	0B9			--	--	--	--	--	--	--	--
0BA	0BA	UNUSED		--	--	--	--	--	--	--	--
	0BB			--	--	--	--	--	--	--	--
0BC	0BC	HDLC.RFDR	R	--	--	--	--	RPS2	RPS1	RPS0	RFDV
	0BD			RFD7	RFD6	RFD5	RFD4	RFD3	RFD2	RFD1	RFD0
0BE	0BE	UNUSED		--	--	--	--	--	--	--	--
	0BF			--	--	--	--	--	--	--	--

Table 12-6. FEAC Register Bit Map

Address 16-bit	8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
0C0	0C0	FEAC.TCR	RW	--	--	--	--	--	TFCL	TFS1	TFS0
	0C1			--	--	--	--	--	--	--	--
0C2	0C2	FEAC.TFDR	RW	--	--	TFCA5	TFCA4	TFCA3	TFCA2	TFCA1	TFCA0
	0C3			--	--	TFCB5	TFCB4	TFCB3	TFCB2	TFCB1	TFCB0
0C4	0C4	FEAC.TSR	R	--	--	--	--	--	--	--	TFI
	0C5			--	--	--	--	--	--	--	--
0C6	0C6	FEAC.TSRL	RL	--	--	--	--	--	--	--	TFIL
	0C7			--	--	--	--	--	--	--	--
0C8	0C8	FEAC.TSRIE	RW	--	--	--	--	--	--	--	TFIIE
	0C9			--	--	--	--	--	--	--	--
0CA-0CE	0CA	UNUSED		--	--	--	--	--	--	--	--
	0CF			--	--	--	--	--	--	--	--
0D0	0D0	FEAC.RCR	RW	--	--	--	--	--	--	--	RFR
	0D1			--	--	--	--	--	--	--	--
0D2	0D2	UNUSED		--	--	--	--	--	--	--	--
	0D3			--	--	--	--	--	--	--	--
0D4	0D4	FEAC.RSR	R	--	--	--	--	RFFE	--	RFCD	RFI
	0D5			--	--	--	--	--	--	--	--
0D6	0D6	FEAC.RSRL	RL	--	--	--	--	--	RFFOL	RFCDL	RFIL
	0D7			--	--	--	--	--	--	--	--
0D8	0D8	FEAC.RSRIE	RW	--	--	--	--	--	RFFOIE	RFCDIE	RFIIE
	0D9			--	--	--	--	--	--	--	--
0DA	0DA	UNUSED		--	--	--	--	--	--	--	--
	0DB			--	--	--	--	--	--	--	--
0DC	0DC	FEAC.RFDR	R	RFFI	--	RFF5	RFF4	RFF3	RFF2	RFF1	RFF0
	0DD			--	--	--	--	--	--	--	--
0DE	0DE	UNUSED		--	--	--	--	--	--	--	--
	0DF			--	--	--	--	--	--	--	--

Table 12-7. Trail Trace Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
0E8	0E8	TT.TCR	RW	--	--	--	Reserved	TMAD	TIDLE	TDIE	TBRE
	0E9			--	--	--	--	--	--	--	--
0EA	0EA	TT.TTIAR	R	--	--	Reserved	Reserved	TTIA3	TTIA2	TTIA1	TTIA0
	0EB			--	--	--	--	--	--	--	--
0EC	0EC	TT.TIR	R	TTD7	TTD6	TTD5	TTD4	TTD3	TTD2	TTD1	TTD0
	0ED			--	--	--	--	--	--	--	--
0EE	0EE	UNUSED		--	--	--	--	--	--	--	--
	0EF			--	--	--	--	--	--	--	--
0F0	0F0	TT.RCR	RW	--	--	Reserved	Reserved	RMAD	RETCD	RDIE	RBRE
	0F1			--	--	--	--	--	--	--	--
0F2	0F2	TT.RTIAR	R	--	--	Reserved	Reserved	RTIA3	RTIA2	RTIA1	RTIA0
	0F3			--	--	Reserved	Reserved	ETIA3	ETIA2	ETIA1	ETIA0
0F4	0F4	TT.RSR	R	--	--	--	--	--	RTIM	RTIU	RIDL
	0F5			--	--	--	--	--	--	--	--
0F6	0F6	TT.RSRL	RL	--	--	--	--	RTICL	RTIML	RTIUL	RIDLL
	0F7			--	--	--	--	--	--	--	--
0F8	0F8	TT.RSRIE	RW	--	--	--	--	RTICIE	RTIMIE	RTIUIE	RIDLIE
	0F9			--	--	--	--	--	--	--	--
0FA	0FA	UNUSED		--	--	--	--	--	--	--	--
	0FB			--	--	--	--	--	--	--	--
0FC	0FC	TT.RIR	R	RTD7	RTD6	RTD5	RTD4	RTD3	RTD2	RTD1	RTD0
	0FD			--	--	--	--	--	--	--	--
0FE	0FE	TT.EIR	R	ETD7	ETD6	ETD5	ETD4	ETD3	ETD2	ETD1	ETD0
	0FF			--	--	--	--	--	--	--	--
100-116	100-1117	RESERVED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--

12.1.3 T3 Register Bit Map

Table 12-8. T3 Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
118	118	T3.TCR	RW	--	--	TFEBE	AFEBED	TRDI	ARDID	TFGD	TAIS
	119			--	--	--	PBGE	TIDLE	CBGE	--	--
11A	11A	T3.TEIR	RW	Reserved	CPEIE	PEI	FEIC1	FEIC0	FEI	TSEI	MEIMS
	11B			--	--	--	--	CCPEIE	CPEI	CFBEIE	FBEI
11C-11E	11C	RESERVED		--	--	--	--	--	--	--	--
	11F			--	--	--	--	--	--	--	--
120	120	T3.RCR	RW	RAILE	RAILD	RAIOD	RAIAD	ROMD	LIP1	LIP0	FRSYNC
	121			Reserved	COVHD	MAOD	MDAISI	AAISD	ECC	FECC1	FECC0
122	122	RESERVED		--	--	--	--	--	--	--	--
	123			--	--	--	--	--	--	--	--
124	124	T3.RSR1	R	OOMF	SEF	--	LOF	RAI	AIS	OOF	LOS
	125			Reserved	Reserved	--	Reserved	T3FM	AIC	IDLE	RUA1
126	126	T3.RSR2	R	--	--	--	--	CPEC	FBEC	PEC	FEC
	127			--	--	--	--	--	--	--	--
128	128	T3.RSRL1	RL	OOMFL	SEFL	COFAL	LOFL	RAIL	AISL	OOFL	LOSL
	129			Reserved	Reserved	Reserved	Reserved	T3FML	AICL	IDLEL	RUA1L

Address 16-bit	8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
12A	12A	T3.RSRL2	RL	--	--	--	--	CPECL	FBECL	PECL	FECL
	12B			--	--	--	--	CPEL	FBEL	PEL	FEL
12C	12C	T3.RSRIE1	RW	OOMFIE	SEFIE	COFAIE	LOFIE	RAIIE	AISIE	OOFIE	LOSIE
	12D			Reserved	Reserved	Reserved	Reserved	T3FMIE	AICIE	IDLEIE	RUA1IE
12E	12E	T3.RSRIE2	RW	--	--	--	--	CPECIE	FBECIE	PECIE	FECIE
	12F			--	--	--	--	CPEIE	FBEIE	PEIE	FEIE
130-132	130	RESERVED		--	--	--	--	--	--	--	--
	133			--	--	--	--	--	--	--	--
134	134	T3.RFECR	R	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
	135			FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
136	136	T3.RPECR	R	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
	137			PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
138	138	T3.RFBECR	R	FBE7	FBE6	FBE5	FBE4	FBE3	FBE2	FBE1	FBE0
	139			FBE15	FBE14	FBE13	FBE12	FBE11	FBE10	FBE9	FBE8
13A	13A	T3.RCPECR	R	CPE7	CPE6	CPE5	CPE4	CPE3	CPE2	CPE1	CPE0
	13B			CPE15	CPE14	CPE13	CPE12	CPE11	CPE10	CPE9	CPE8
13C-13E	13C	UNUSED		--	--	--	--	--	--	--	--
	13F			--	--	--	--	--	--	--	--

12.1.4 E3 G.751 Register Bit Map

Table 12-9. E3 G.751 Register Bit Map

Address 16-bit	8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
118	118	E3G751.TCR	RW	--	--	Reserved	Reserved	TABC1	TABC0	TFGD	TAIS
	119			Reserved	--	--	Reserved	Reserved	Reserved	TNBC1	TNBC0
11A	11A	E3G751.TEIR	RW	Reserved	Reserved	Reserved	FEIC1	FEIC0	FEI	TSEI	MEIMS
	11B			--	--	--	--	Reserved	Reserved	Reserved	Reserved
11C-11E	11C	RESERVED		--	--	--	--	--	--	--	--
	11F			--	--	--	--	--	--	--	--
120	120	E3G751.RCR	RW	RAILE	RAILD	RAIOD	RAIAD	ROMD	LIP1	LIP0	FRSYNC
	121			Reserved	Reserved	DLS	MDAISI	AAISD	ECC	FECC1	FECC0
122	122	RESERVED		--	--	--	--	--	--	--	--
	123			--	--	--	--	--	--	--	--
124	124	E3G751.RSR1	R	RAB	RNB	--	LOF	RAI	AIS	OOF	LOS
	125			Reserved	Reserved	--	Reserved	Reserved	Reserved	Reserved	RUA1
126	126	E3G751.RSR2	R	--	--	--	--	Reserved	Reserved	Reserved	FEC
	127			--	--	--	--	--	--	--	--
128	128	E3G751.RSRL1	RL	ACL	NCL	COFAL	LOFL	RAIL	AISL	OOFL	LOSL
	129			Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RUA1L
12A	12A	E3G751.RSRL2	RL	--	--	--	--	Reserved	Reserved	Reserved	FECL
	12B			--	--	--	--	Reserved	Reserved	Reserved	FEL
12C	12C	E3G751.RSRIE1	RW	ACIE	NCIE	COFAIE	LOFIE	RAIIE	AISIE	OOFIE	LOSIE
	12D			Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RUA1IE
12E	12E	E3G751.RSRIE2	RW	--	--	--	--	Reserved	Reserved	Reserved	FECIE
	12F			--	--	--	--	Reserved	Reserved	Reserved	FEIE
130-132	130	RESERVED		--	--	--	--	--	--	--	--
	133			--	--	--	--	--	--	--	--
134	134	E3G751.RFECR	R	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
	135			FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
136-13A	136-13B	RESERVED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--
13C-13E	13C-13F	UNUSED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--

12.1.5 E3 G.832 Register Bit Map

Table 12-10. E3 G.832 Register Bit Map

Address 16-bit	Address 8-bit	Register	Type	Bit 7 Bit 15	Bit 6 Bit 14	Bit 5 Bit 13	Bit 4 Bit 12	Bit 3 Bit 11	Bit 2 Bit 10	Bit 1 Bit 9	Bit 0 Bit 8
118	118	E3G832.TCR	RW	--	--	TFEBE	AFEBED	TRDI	ARDID	TFGD	TAIS
	119			Reserved	--	--	Reserved	Reserved	TGCC	TNRC1	TNRC0
11A	11A	E3G832.TEIR	RW	PBEE	CPEIE	PEI	FEIC1	FEIC0	FEI	TSEI	MEIMS
	11B			--	--	--	--	Reserved	Reserved	CFBEIE	FBEI
11C	11C	E3G832.TMABR	RW	TPT2	TPT1	TPT0	TTIGD	TTI3	TTI2	TTI1	TTI0
	11D			--	--	--	--	--	--	--	--
11E	11E	E3G832.TNGBR	RW	TNR7	TNR6	TNR5	TNR4	TNR3	TNR2	TNR1	TNR0
	11F			TGC7	TGC6	TGC5	TGC4	TGC3	TGC2	TGC1	TGC0
120	120	E3G832.RCR	RW	RAILE	RAILD	RAIOD	RAIAD	ROMD	LIP1	LIP0	FRSYNC
	121			Reserved	PEC	DLS	MDAISI	AAISD	ECC	FECC1	FECC0
122	122	E3G832.RMACR	RW	--	--	--	--	EPT2	EPT1	EPT0	TIED
	123			--	--	--	--	--	--	--	--
124	124	E3G832.RSR1	R	Reserved	Reserved	--	LOF	RAI	AIS	OOF	LOS
	125			Reserved	--	--	RPTU	RPTM	Reserved	Reserved	RUA1
126	126	E3G832.RSR2	R	--	--	--	--	Reserved	FBEC	PEC	FEC
	127			--	--	--	--	--	--	--	--
128	128	E3G832.RSRL1	RL	GCL	NRL	COFAL	LOFL	RAIL	AISL	OOFL	LOSL
	129			Reserved	--	TIL	RPTUL	RPTML	RPTL	Reserved	RUA1L
12A	12A	E3G832.RSRL2	RL	--	--	--	--	Reserved	FBECL	PECL	FECL
	12B			--	--	--	--	Reserved	FBEL	PEL	FEL
12C	12C	E3G832.RSRIE1	RW	GCIE	NRIE	COFAIE	LOFIE	RAIIE	AISIE	OOFIE	LOSIE
	12D			Reserved	--	TIIE	RPTUIE	RPTMIE	RPTIE	Reserved	RUA1IE
12E	12E	E3G832.RSRIE2	RW	--	--	--	--	Reserved	FBECIE	PECIE	FECIE
	12F			--	--	--	--	Reserved	FBEIE	PEIE	FEIE
130	130	E3G832.RMABR	R	--	RPT2	RPT1	RPT0	TI3	TI2	TI1	TI0
	131			--	--	--	--	--	--	--	--
132	132	E3G832.RNGBR	R	RNR7	RNR6	RNR5	RNR4	RNR3	RNR2	RNR1	RNR0
	133			RGC7	RGC6	RGC5	RGC4	RGC3	RGC2	RGC1	RGC0
134	134	E3G832.RFECR	R	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
	135			FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
136	136	E3G832.RPECR	R	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
	137			PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
138	138	E3G832.RFBER	R	FBE7	FBE6	FBE5	FBE4	FBE3	FBE2	FBE1	FBE0
	139			FBE15	FBE14	FBE13	FBE12	FBE11	FBE10	FBE9	FBE8
13A	13A	RESERVED		--	--	--	--	--	--	--	--
	13B			--	--	--	--	--	--	--	--
13C-13E	13C-13F	UNUSED		--	--	--	--	--	--	--	--
				--	--	--	--	--	--	--	--

Bits that are underlined are read-only; all other bits are read-write.

12.2 Global Registers

Table 12-11. Global Register Map

Address	Register	Register Description
000h	GL.IDR	Global ID Register
002h	GL.CR1	Global Control Register 1
004h	GL.CR2	Global Control Register 2
006h	--	Unused
008h	--	Unused
00Ah	GL.GIOCR	Global General Purpose IO Control Register
00Ch	--	Unused
00Eh	--	Unused
010h	GL.ISR	Global Interrupt Status Register
012h	GL.ISRIE	Global Interrupt Enable Register
014h	GL.SR	Global Status Register
016h	GL.SRL	Global Status Register Latched
018h	GL.SRIE	Global Status Register Interrupt Enable
01Ah	--	Unused
01Ch	GL.GIORR	Global General Purpose IO read register
01Eh	--	Unused

12.2.1 Register Bit Descriptions

Register Name: **GL.IDR**
Register Description: **Global ID Register**
Register Address: **000h**

Bit #	15	14	13	12	11	10	9	8
Name	ID15	ID14	ID13	ID12	ID11	ID10	ID9	ID8

Bit #	7	6	5	4	3	2	1	0
Name	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0

Bits 15 to 12: Device REV ID Bits 15 to 12 (ID15 to ID12). These bits of the device ID register has same information as the four bits of JTAG REV ID portion of the JTAG ID register. JTAG ID[31:28].

Bits 11 to 0: Device CODE ID Bits 11 to 0 (ID11 to ID0). These bits of the device code ID register has same information as the lower 12 bits of JTAG CODE ID portion of the JTAG ID register. JTAG ID[23:12].

Register Name: **GL.CR1**
Register Description: **Global Control Register 1**
Register Address: **002h**

Bit #	15	14	13	12	11	10	9	8
Name	--	INTM	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TMEI	MEIMS	GPM1	GPM0	PMU	LSBCRE	RSTDP	RST
Default	0	0	0	0	0	0	1	0

Bit 14: $\overline{\text{INT}}$ pin mode (INTM) This bit determines the inactive mode of the $\overline{\text{INT}}$ pin. The $\overline{\text{INT}}$ pin always drives low when active.

0 = Pin is high impedance when not active
1 = Pin drives high when not active

Bit 7: Transmit Manual Error Insert (TMEI) This bit is used insert an error if the port is configured for global error insertion. An error(s) is inserted at the next opportunity when this bit transitions from low to high. The GL.CR1.MEIMS bit must be clear for this bit to operate.

Bit 6: Transmit Manual Error Insert Select (MEIMS) This bit is used to select the source of the global manual error insertion signal

0 = Global error insertion using TMEI bit
1 = Global error insertion using the GPIO6 pin

Bits 5 and 4: Global Performance Monitor Update Mode (GPM[1:0]) These bits select the global performance monitor register update mode.

00 = Global PM update using the PMU bit
01 = Global PM update using the GPIO8 pin
1x = One second PM update using the internal one second counter

Bit 3: Global Performance Monitor Update Register (PMU) This bit is used to update all of the performance monitor registers configured to use this bit. When this bit is toggled from low to high the performance registers configured to use this signal will be updated with the latest count value from the counters, and the counters will be reset. The bit should remain high until the performance register update status bit (GL.SR.PMS) goes high, then it should be brought back low which clears the PMS status bit.

Bit 2: Latched Status Bit Clear on Read Enable (LSBCRE). This signal determines when latched status register bits are cleared.

0 = Latched status register bits are cleared on a write
1 = Latched status register bits are cleared on a read

Bit 1: Reset Data Path (RSTDP). When this bit is set, it will force all of the internal data path registers to their default state. This bit must be set high for a minimum of 100ns. See the Reset and Power-Down section 10.3. Note: The default state is a 1 (after a general reset, this bit will be set to one).

0 = Normal operation
1 = Force all data path registers to their default values

Bit 0: Reset (RST). When this bit is set, all of the internal data path and status and control registers (except this RST bit), will be reset to their default state. This bit must be set high for a minimum of 100ns. See the Reset and Power-Down section 10.3.

0 = Normal operation
1 = Force all internal registers to their default values

Register Name: **GL.CR2**
Register Description: **Global Control Register 2**
Register Address: **004h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	G8KRS1	G8KRS0	G8K0S	G8KIS
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	CLAD2	CLAD1	CLAD0	--
Default	0	0	0	0	0	0	0	0

Bits 11 to 10: Global 8KHz Reference Source [1:0] (G8KRS[1:0]). These bits determine the source for the internally generated 8 kHz reference as well as the internal one second reference, which is derived from the Global 8 kHz reference. The source is selected from the CLAD clock or from the port 8KREF clock source. See Table 10-12. Global 8 kHz Reference Source Table

These bits are ignored when the G8KIS bit = 1.

Table 10-12. Global 8 kHz Reference Source Table

GL.CR2. G8KIS	GL.CR2. G8KRS[1:0]	SOURCE
0	00	None, the 8KHZ divider is disabled.
0	01	Derived from CLAD output clock
0	10	8KREF source selected by P8KRS[1:0]
0	11	Undefined
1	XX	GPIO4

Bit 9: Global 8KHz Reference Output Select (G8KOS). This bit determines whether GPIO2 pin is used for the global 8KREFO output signal, or is used as specified by GL.GIOCR.GPIO2S[1:0].

0 = GPIO2 pin mode selected by GL.GIOCR.GPIO2S[1:0]
1 = GPIO2 is the global 8KREFO output signal selected by GL.CR2.8KRS[2:0]

Bit 8: Global 8KHz Reference Input Select (G8KIS). This bit determines whether GPIO4 pin is used for the global 8KREFI input signal, or is used as specified by GL.GIOCR.GPIO4S[1:0]. G8KREFI signal will be low if not selected. Global 8KREF pin signal will be low if not selected.

0 = GPIO4 pin mode selected by GL.GIOCR.GPIO4S[1:0]
1 = GPIO4 is the global 8KREFI input signal for one second timer and port to use

Bits 3 to 1: CLAD IO Mode [2:0] (CLAD[2:0]). These bits control the CLAD. See Table 10-11.

Table 10-11. CLAD Clock Source Settings

CLAD[2:0]	REFCLK (INPUT)
000	44.736 MHz
001	34.368 MHz
010	51.84 MHz
011	19.44 MHz
100	77.76 MHz
101	Undefined
11X	Undefined

Register Name: **GL.GIOCR**
Register Description: **Global General Purpose IO Control Register**
Register Address: **00Ah**

Bit #	15	14	13	12	11	10	9	8
Name	GPIO8S1	GPIO8S0	GPIO7S1	GPIO7S0	GPIO6S1	GPIO6S0	GPIO5S1	GPIO5S0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	GPIO4S1	GPIO4S0	GPIO3S1	GPIO3S0	GPIO2S1	GPIO2S0	GPIO1S1	GPIO1S0
Default	0	0	0	0	0	0	0	0

Bits 15 to 14: General Purpose IO 8 Select [1:0] (GPIO8S[1:0]). These bits determine the function of the GPIO8 pin. These selections are only valid if GL.CR1.GPM[1:0] is not set to 01.

00 = Input
01 = Reserved
10 = Output logic 0
11 = Output logic 1

Bits 13 to 12: General Purpose IO 7 Select [1:0] (GPIO7S[1:0]). These bits determine the function of the GPIO7 pin.

00 = Input
01 = Reserved
10 = Output logic 0
11 = Output logic 1

Bits 11 to 10 : General Purpose IO 6 Select [1:0] (GPIO6S[1:0]). These bits determine the function of the GPIO6 pin. These selections are only valid if GL.CR1.MEIMS=0.

00 = Input
01 = Reserved
10 = Output logic 0
11 = Output logic 1

Bits 9 to 8: General Purpose IO 5 Select [1:0] (GPIO5S[1:0]). These bits determine the function of the GPIO5 pin.

00 = Input
01 = Reserved
10 = Output logic 0
11 = Output logic 1

Bits 7 to 6: General Purpose IO 4 Select [1:0] (GPIO4S[1:0]). These bits determine the function of the GPIO4 pin. These selections are only valid if GL.CR2 .G8KRIS=0.

00 = Input
01 = Reserved
10 = Output logic 0
11 = Output logic 1

Bits 5 to 4: General Purpose IO 3 Select [1:0] (GPIO3S[1:0]). These bits determine the function of the GPIO3 pin.

00 = Input
01 = Reserved
10 = Output logic 0
11 = Output logic 1

Bits 3 to 2: General Purpose IO 2 Select [1:0] (GPIO2S[1:0]). These bits determine the function of the GPIO2 pin. These selections are only valid if GL.CR2.GKROS=0.

00 = Input
01 = Port B status output selected by PORT.CR4:GPIOB[3:0] in port control registers
10 = Output logic 0
11 = Output logic 1

Bits 1 to 0: General Purpose IO 1 Select [1:0] (GPIO1S[1:0]). These bits determine the function of the GPIO1 pin.

00 = Input
01 = Port A status output selected by PORT.CR4:GPIOA[3:0] in port control registers
10 = Output logic 0
11 = Output logic 1

Register Name: **GL.ISR**
Register Description: **Global Interrupt Status Register**
Register Address: **010h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	PISR	--	--	--	GSR

Bit 4: Port Interrupt Status Register (PISR) This bit is set when any of the bits in the port interrupt status registers (PORT.ISR) are set. The $\overline{INT}$ interrupt pin will be driven low when this bit is set and the GL.ISRIE.PISRIE interrupt enable bit is enabled.

Bit 0: Global Status Register Interrupt Status (GSR) This bit is set when any of the latched status register bits in the global latched status register (GL.SRL) are set and enabled for interrupt. The $\overline{INT}$ interrupt pin will be driven low when this bit is set and the *GL.ISRIE*.GSRIE interrupt enable bit is enabled.

Register Name: **GL.ISRIE**
Register Description: **Global Interrupt Status Register Interrupt Enable**
Register Address: **012h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	PISRIE	--	--	RESERVED	GSRIE
Default	0	0	0	0	0	0	0	0

Bit 4: Port Interrupt Status Register Interrupt Enable (PISRIE) When this is enabled and the GL.ISR.PISR status bit is set, the $\overline{INT}$ pin will be driven low.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Global Status Register Interrupt Status Interrupt Enable (GSRIE) When this interrupt enable bit is enabled, and the *GL.ISR*.GSR status bit is set, the $\overline{INT}$ pin will be driven low.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **GL.SR**
Register Description: **Global Status Register**
Register Address: **014h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	CLOL	GPMS

Bit 1 : CLAD Loss of Lock (CLOL) – This bit is set when any of the PLLs in the CLAD are not locked to the reference frequency.

Bit 0: Global Performance Monitoring Update Status (GPMS) This bit is set when all of the port performance register update status bits (*PORT.SR.*PMU), that are enabled for global update control (*PORT.CR2.*PMUM=1), are set. It is an "AND" of all the globally enabled port PMU status bits. In global software update mode, the global update request bit (*GL.CR.*GPMU) should be held high until this status bit goes high.

0 = The associated update request signal is low or not all register updates are completed
1 = The requested performance register updates are all completed

Register Name: **GL.SRL**
Register Description: **Global Status Register Latched**
Register Address: **016h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	8KREFL	CLADL	ONESL	CLOLL	GPMSL

Bit 4: 8kHz Reference Activity Status Latched (8KREFL) This bit will be set when the 8 kHz reference signal on the GPIO4 pin is active. The GL.CR2.G8KIS bit must be set for the activity to be monitored.

Bit 3: CLAD Reference Clock Activity Status Latched (CLADL) This bit will be set when the CLAD PLL reference clock signal on the REFCLK pin is active.

Bit 2: One Second Status Latched (ONESL) This bit will be set once a second. The GL.ISR.GSR status bit will be set when this bit is set and the GL.SRIE.ONESIE bit is enabled. The $\overline{INT}$ pin will be driven low if this bit is set and the GL.SRIE.ONESIE bit and the GL.ISRIE.GSRIE bit are enabled.

Bit 1: CLAD Loss Of Lock Latched (CLOLL) This bit will be set when the *GL.SR*.CLOL status bit changes from low to high. The *GL.ISR*.GSR bit will be set when this bit is set and the *GL.SRIE*.CLOLIE bit is set and the $\overline{INT}$ pin will be driven low if the *GL.ISRIE*.GSRIE bit is also enabled.

Bit 0: Global Performance Monitoring Update Status Latched (GPMSL) This bit will be set when the GL.SR.GPMS status bit changes from low to high. This bit will set the GL.ISR.GSR status bit if the GL.SRIE.GPMSIE is enabled. This bit will drive the interrupt pin low if the GL.SRIE.GPMSIE bit and the GL.ISRIE.GSRIE bit are enabled.

Register Name: **GL.SRIE**
Register Description: **Global Status Register Interrupt Enable**
Register Address: **018h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	ONESIE	CLOLIE	GPMSIE
Default	0	0	0	0	0	0	0	0

Bit 2: One Second Interrupt Enable (ONESIE) This bit will drive the interrupt pin low if the GL.SRL.ONESL bit is set, and the GL.ISRIE.GSRIE bit is enabled.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: CLAD Loss Of Lock Interrupt Enable (CLOLIE) The interrupt pin will be driven when this bit is enabled, the *GL.SRL*.CLOLL is set, and *GL.ISRIE*.GSRIE bit is enabled.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Global Performance Monitoring Update Status Interrupt Enable (GPMSIE) The interrupt pin will be driven when this bit is enabled and the GL.SRL.GPMSL bit is set and the GL.ISRIE.GSRIE bit is enabled.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **GL.GIORR**
Register Description: **Global General Purpose IO Read Register**
Register Address: **01Ch**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	GPIO8	GPIO7	GPIO6	GPIO5	GPIO4	GPIO3	GPIO2	GPIO1

Bits 7 to 0: General Purpose IO Status [8:1]] (GPIO[8:1]) These bits reflect the input or output signal on the 8 general purpose IO pins.

12.3 Port Register

12.3.1 Register Bit Descriptions

Table 12-12. Port Register Map

Address	Register	Register Description
040h	PORT.CR1	Port Control Register 1
042h	PORT.CR2	Port Control Register 2
044h	PORT.CR3	Port Control Register 3
046h	PORT.CR4	Port Control Register 4
048h	--	Unused
04Ah	PORT.INV1	Port IO Invert Control Register 1
04Ch	PORT.INV2	Port IO Invert Control Register 2
04Eh	--	Unused
050h	PORT.ISR	Port Interrupt Status Register
052h	PORT.SR	Port Status Register
054h	PORT.SRL	Port Status Register Latched
056h	PORT.SRIE	Port Status Register Interrupt Enable
058h	--	Unused
05Ah	--	Unused
05Ch	--	Unused
05Eh	--	Unused

Register Name: **PORT.CR1**
Register Description: **Port Control Register 1**
Register Address: **040h**

Bit #	15	14	13	12	11	10	9	8
Name	RESERVED	PAIS2	PAIS1	PAIS0	LAIS1	LAIS0	BENA	RESERVED
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TMEI	MEIM	--	PMUM	PMU	PD	RSTDP	RST
Default	0	0	--	0	0	1	1	0

Bits 14 to 12: Payload AIS Select [2:0] (PAIS[2:0]). This bit controls when an unframed all ones signal is forced on the receive data path after the receive framer and payload loopback mux. Default: Payload AIS always sent.

PAIS[2:0] PORT.CR1	WHEN AIS IS SENT	AIS CODE
000	Always	UA1
001	When LLB (no DLB) active	UA1
010	When PLB active	UA1
011	When LLB(no DLB) or PLB active	UA1
100	When LOS (no DLB) active	UA1
101	When OOF active	UA1
110	When OOF, LOS. LLB (no DLB), or PLB active	UA1
111	Never	none

Bits 11 to 10: Line AIS Select [1:0] (LAIS[1:0). These bits control when a DS3 framed AIS or an unframed all ones signal is to be transmitted on TPOS/TNEG and/or TXP/TXN. The signal on TPOS/TNEG can be AMI or unipolar. This signal is sent even when in diagnostic loopback and always over-rides signals from the framers. Default: AIS sent if DLB is enabled.

LAIS[1:0] PORT.CR1	FRAME MODE	DESCRIPTION	AIS CODE
00	DS3	Automatic AIS when DLB is enabled (PORT.CR4.LBM = 1XX)	DS3AIS
00	E3	Automatic AIS when DLB is enabled	UA1
01	Any	Send UA1	UA1
10	DS3	Send AIS	DS3AIS
10	E3	Send AIS	UA1
11	Any	Disable	none

Bit 9: BERT Enable (BENA). This bit is used to enable the transmit BERT logic; the receive BERT is always enabled. The BERT pattern will replace the the system interface datastream (TSER) into the payload datastream.

0 = Tranmit BERT logic disabled and powered down

1 = Transmit BERT logic enabled

Bit 7: Transmit Manual Error Insert (TMEI) This bit is used to insert errors in all error insertion logic configured to use this bit when *PORT.CR1*.MEIM=0. The error(s) will be inserted when this bit is toggled low to high.

Bit 6 : Transmit Manual Error Insert Mode (MEIM). These bits select the method transmit manual error insertion for this port for error generators configured to use the external TMEI signal. The global updates are controlled by the GL.CR1.MEIMS bit.

0 = Port software update via *PORT.CR1*.TMEI
1 = Global update source

Bit 4: Performance Monitor Update Mode (PMUM). These bits select the method of updating the performance monitor registers. The global updates are controlled by the *GL.CR1*.GPMU bits.

0 = Port software update
1 = Global update

Bit 3: Performance Monitor Register Update (PMU) This bit is used to update all of the performance monitor registers configured to use this bit when *PORT.CR1*.PMUM=0. The performance registers configured to use this signal will be updated with the latest count value and the counters reset when this bit is toggled low to high. The bit should remain high until the performance register update status bit (*PORT.SR*.PMS) goes high, then it should be brought back low which clears the PMS status bit.

Bit 2: Power-Down (PD). When this bit is set, the LIU and digital logic for this port are powered down and considered "out of service". The logic is powered down by stopping the clocks. See the Reset and Power-Down section 10.3.

0 = Normal operation
1 = Power-down port circuits (default state)

Bit 1: Reset Data Path (RSTDP). When this bit is set, it will force all of the internal data path registers to their default state. This bit must be set high for a minimum of 100ns and then set back low. See the Reset and Power-Down section 10.3. Note: The Default State of this bit is 1 (after a general reset (port or global), this bit will be set to one).

0 = Normal operation
1 = Force all data path registers to their default values

Bit 0: Reset (RST). When this bit is set, it will force all the internal data path and status and control registers (except this RST bit) of this port to their default state. See the Reset and Power-Down section 10.3. This bit must be set high for a minimum of 100ns and then set back low. This software bit is logically OR'ed with the inverted hardware signal $\overline{RST}$ and the GL.CR1.RST bit.

0 = Normal operation
1 = Force all internal registers to their default values

Register Name: **PORT.CR2**
Register Description: **Port Control Register 2**
Register Address: **042h**

Bit #	15	14	13	12	11	10	9	8
Name	TLEN	TTS	RMON	TLBO	RESERVED	LM2	LM1	LM0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RESERVED	RESERVED	FM2	FM1	FM0	RESERVED	RESERVED	RESERVED
Default	0	0	0	0	0	0	0	0

Bit 15: Transmit Line IO Signal Enable (TLEN). This bit is used to enable to transmit line interface output pins TLCLK, TPOS/TDAT and TNEG.

0 = Disable, force outputs low
1 = Enable normal operation

Bit 14: Transmit LIU Tri-State (TTS) This bit is used to tri-state the transmit TXP and TXN pins. The LIU is still powered up when the pins are tri-stated. It has no effect when the LIU is disabled and powered down.

0 = TXP and TXN driven
1 = TXP and TXN tri-stated

Bit 13: Receive LIU Monitor Mode (RMON) This bit is used to enable the receive LIU monitor mode pre-amplifier. Enabling the pre-amplifier adds about 20 dB of linear amplification for use in monitor applications where the signal has been reduced 20 dB using resistive attenuator circuits.

0 = Disable the 20 dB pre-amp
1 = Enable the 20 dB pre-amp

Bit 12: Transmit LIU LBO (TLBO) This bit is used enable the transmit LBO circuit which causes the transmit signal to have a wave shape that approximates about 225 feet of cable. This is used to reduce near end crosstalk when the cable lengths are short. This signal is only valid in DS3 LIU mode.

0 = TXP and TXN have full amplitude signals
1 = TXP and TXN signals approximate 225 feet of cable

Bits 10 to 8 : Port Interface Mode (LM[2:0]). The **LM[2:0]** bits select main port interface operational modes. The default state disables the LIU and the JA.

Table 10-26. Line Mode Select Bits LM[2:0]

LINE.TCR.**TZSD** & LINE.RCR.**RZSD**	**LM[2:0]** (PORT.CR2)	**Line Code**	**LIU**	**JA**
0	000	B3ZS/HDB3	OFF	OFF
0	001	B3ZS/HDB3	ON	OFF
0	010	B3ZS/HDB3	ON	TX
0	011	B3ZS/HDB3	ON	RX
1	000	AMI	OFF	OFF
1	001	AMI	ON	OFF
1	010	AMI	ON	TX
1	011	AMI	ON	RX
X	1XX	UNI	OFF	OFF

Bits 5 to 3: Framing mode (FM[2:0]). The FM[2:0] bits select main framing operational modes. Default: DS3 C-bit.

FM[2:0]	DESCRIPTION	LINE CODE	FIGURE
0 00	DS3 C-bit Framed	B3ZS/AMI/UNI	Figure 7-1
0 01	DS3 M23 Framed	B3ZS/AMI/UNI	Figure 7-1
0 10	E3 G.751 Famed	HDB3/AMI/UNI	Figure 7-1
0 11	E3 G.832 Framed	HDB3/AMI/UNI	Figure 7-1
1 00	DS3 Unframed	B3ZS/AMI/UNI	Figure 7-2
1 01	Undefined	---	
1 10	E3 Unframed	HDB3/AMI/UNI	Figure 7-2
1 11	Undefined	---	

Register Name: **PORT.CR3**
Register Description: **Port Control Register 3**
Register Address: **044h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	RCLKS	RSOFOS	RESERVED	TCLKS	TSOFOS	RESERVED
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	P8KRS1	P8KRS0	P8KREF	LOOPT	CLADC	RFTS	TFTS	TLTS
Default	0	0	0	0	0	0	0	0

Bit 13: Receive Clock Output Select (RCLKS). This bit is used to select the function of the RGCLK / RCLKO pins. See Table 10-24.

0 = Selects the RGCLK signal, or the drive low pin function.
1 = Selects RCLKO signal.

Bit 12: Receive Start Of Frame Output Select (RSOFOS). This bit is to select the function of the RSOFO / RDEN pins. See Table 10-23.

0 = Selects RDEN signal.
1 = Selects RSOFO signal.

Bit 10: Transmit Clock Output Select (TCLKS). This bit is used to select the function of the TGCLK / TCLKO pins. See Table 10-22.

0 = Selects TGCLK signal.
1 = Selects TCLKO signal.

Bit 9: Transmit Start Of Frame Output Select (TSOFOS). This bit is used to select the function of the TSOFO / TDEN pins. See Table 10-21.

0 = Selects TDEN signal.
1 = Selects TSOFO signal.

Bits 7 to 6: Port 8 kHz Reference Source Select (P8KRS[1:0]). This bit selects the source of the 8 kHz reference from the port sources. The 8K reference for this port can be used as the global 8K reference source. See Table 10-13.

Table 10-13. Port 8 kHz Reference Source Table

PORT.CR3.P8KRS[1:0]	SOURCE
0X	Undefined
10	Internal receive framer clock
11	Internal transmit framer clock

Bit 5: PORT 8 kHz Reference Source (P8KREF). This bit selects the source of the 8 kHz reference for one second timer.

0 = 8 kHz reference from global source
1 = 8 kHz reference from port's selected source

Bit 4: LOOP Time Enable (LOOPT). When this bit is set, the port is in loop time mode. The transmit clock is set to the receive clock from the RLCLK pin or the recovered clock from the LIU or the CLAD clock and the TCLKI pin is not used. This function of this bit is conditional on other control bits. See Table 10-4 for more details.

0 = Normal transmit clock operation
1 = Transmit using the receive clock

Bit 3: CLAD Transmit Clock Source Control (CLADC). This bit is used to enable the CLAD clocks as the source of the internal transmit clock. This function of this bit is conditional on other control bits. See Table 10-4 for more details.

0 = Use CLAD clocks for the transmit clock as appropriate
1 = Do not use CLAD clocks for the transmit clock – (if no loopback is enabled, TCLKI is the source)

Bit 2: Receive Framer IO Signal Timing Select (RFTS). This bit controls the timing reference for the signals on the receive framer interface IO pins. The pins controlled are RSER, RSOFO / RDEN. See Table 10-8 for more details.

0 = Use output clocks for timing reference
1 = Use input clocks for timing reference

Bit 1: Transmit Framer IO Signal Timing Select (TFTS). This bit controls the timing reference for the signals on the transmit framer interface IO pins. The pins controlled are TSOFIn, TSER, and TSOFO / TDEN. See Table 10-7 for more details.

0 = Use output clocks for timing reference
1 = Use input clocks for timing reference

Bit 0: Transmit Line IO Signal Timing Select (TLTS). This bit controls the timing reference for the signals on the transmit line interface IO pins. The pins controlled are TPOS / TDAT and TNEG. See Table 10-6 for more details.

0 = Use output clocks for timing reference
1 = Use input clocks for timing reference

Register Name: **PORT.CR4**
Register Description: **Port Control Register 4**
Register Address: **046h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	RESERVED	LBM2	LBM1	LBM0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	GPIOB3	GPIOB2	GPIOB1	GPIOB0	GPIOA3	GPIOA2	GPIOA1	GPIOA0
Default	0	0	0	0	0	0	0	0

Bits 10 to 8: Loopback Mode [2:0] (LBM[2:0]). These bits select the loopback modes for analog loopback (ALB), line loopback (LLB), payload loopback (PLB) and diagnostic loopback (DLB). See Table 10-17 for the loopback select codes. Default: No Loopback.

LBM[2:0]	ALB	LLB	PLB	DLB
000	0	0	0	0
001	1	0	0	0
010	0	1	0	0
011	0	0	1	0
10X	0	0	0	1
110	0	1	0	1
111	0	0	0	1

Bits 7 to 4: General Purpose IO B Output Select[3:0] (GPIOB[3:0]) These bits determine which alarm status signal to output on the GPIO2, pin. The GPIO pin must be enabled by setting the bits in the GL.GIOCR and GL.CR2 registers to output the selected alarm signal. See Table 10-15. See Table 10-16 for the alarm select codes.

Bits 3 to 0: General Purpose IO A Output Select[3:0] (GPIOA[3:0]) These bits determine which alarm status signal to output on the GPIO1 pin. The GPIO pin must be enabled for output by setting the bits in the GL.GIOCR register. See Table 10-15 for configuration settings. See Table 10-16 below for the alarm select codes.

Table 10-16. GPIO Port Alarm Monitor Select

PORT.CR4 GPIO(A/B)[3:0]	LINE LOS	DS3/E3 OOF	DS3/E3 LOF	DS3/E3 AIS	DS3/E3 RAI	DS3 IDLE
0000	X					
0001		X				
0010			X			
0011				X		
0100					X	
0101						X
0110						
0111						
1000						
1001						
1010						
1011	X		X	X		
1100						
1101	X		X	X		
1110					X	X
1111	X	X	X	X	X	X

Register Name: **PORT.INV1**
Register Description: **Port IO Invert Control Register 1**
Register Address: **04Ah**

Bit #	15	14	13	12	11	10	9	8
Name	RESERVED	RESERVED	--	TSOFOI	RESERVED	TSERI	TOHSI	TOHEI
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TOHI	TOHCKI	TSOFII	TNEGI	TDATI	TLCKI	TCKOI	TCKII
Default	0	0	0	0	0	0	0	0

Bit 12 : TSOFO / TDEN/ Invert (TSOFOI). This bit inverts the TSOFO / TDEN pin when set.

Bit 10 : TSER Invert (TSERI). This bit inverts the TSER pin when set.

Bit 9 : TOHSOF Invert (TOHSI). This bit inverts the TOHSOF pin when set.

Bit 8 : TOHEN Invert (TOHEI). This bit inverts the TOHEN pin when set.

Bit 7 : TOH Invert (TOHI). This bit inverts the TOH pin when set.

Bit 6 : TOHCLK Invert (TOHCKI). This bit inverts the TOHCLK pin when set.

Bit 5 : TSOFIn Invert (TSOFII). This bit inverts the TSOFIn pin when set.

Bit 4 : TNEG Invert (TNEGI). This bit inverts the TNEG pin when set.

Bit 3 : TDAT Invert (TDATI). This bit inverts the TDAT pin when set.

Bit 2 : TLCLK Invert (TLCKI). This bit inverts the TLCLK pin when set.

Bit 1 : TCLKO / TGCLK Invert (TCKOI). This bit inverts the TCLKO / TGCLK pin when set.

Bit 0 : TCLKI Invert (TCKII). This bit inverts the TCLKI pin when set.

Register Name: **PORT.INV2**
Register Description: **Port IO Invert Control Register 2**
Register Address: **04Ch**

Bit #	15	14	13	12	11	10	9	8
Name	--	RESERVED	RESERVED	RSOFOI	--	RSERI	ROHSI	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	ROHI	ROHCKI	--	RNEGI	RPOSI	RLCKI	RCLKOI	--
Default	0	0	0	0	0	0	0	0

Bit 12 : RSOFO / RDEN Invert (RSOFOI). This bit inverts the RSOFO / RDEN pin when set.

Bit 10 : RSER Invert (RSERI). This bit inverts the RSER pin when set.

Bit 9 : ROHSOF Invert (ROHSI). This bit inverts the ROHSOF pin when set.

Bit 7 : ROH Invert (ROHI). This bit inverts the ROH pin when set.

Bit 6 : ROHCLK Invert (ROHCKI). This bit inverts the ROHCLK pin when set.

Bit 4 : RNEG / RLCV Invert (RNEGI). This bit inverts the RNEG / RLCV when set.

Bit 3 : RPOS / RDAT Invert (RPOSI). This bit inverts the RPOS / RDAT pin when set.

Bit 2 : RLCLK Invert (RLCKI). This bit inverts the RLCLK pin when set.

Bit 1 : RCLKO / RGCLK Invert (RCLKOI). This bit inverts the RCLKO / RGCLK pin when set.

Register Name: **PORT.ISR**
Register Description: **Port Interrupt Status Register**
Register Address: **050h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	PSR	LCSR

Bit #	7	6	5	4	3	2	1	0
Name	TTSR	FSR	HSR	BSR	RESERVED	RESERVED	RESERVED	FMSR

Bit 9: Port Status Register Interrupt Status (PSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the *PORT.SRL* register are set. The interrupt pin will be driven when this bit is set and the GL.ISRIE.PISRIE bit is set.

Bit 8: Line Code Status Register Interrupt Status (LCSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the B3ZS/HDB3 Line Encoder/Decoder block are set. The interrupt pin will be driven when this bit is set and the GL.ISRIE.PISRIE bit is set.

Bit 7: Trail Trace Status Register Interrupt Status (TTSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the trail trace block are set. The interrupt pin will be driven when this bit is set and the GL.ISRIE.PISRIE bit is set.

Bit 6: FEAC Status Register Interrupt Status (FSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the FEAC block are set. The interrupt pin will be driven when this bit is set and the GL.ISRIE.PISRIE bit is set.

Bit 5: HDLC Status Register Interrupt Status (HSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the HDLC block are set. The interrupt pin will be driven when this bit is set and the GL.ISRIE.PISRIE bit is set.

Bit 4: BERT Status Register Interrupt Status (BSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the BERT block are set. The interrupt pin will be driven when this bit is set and the GL.ISRIE.PISRIE bit is set.

Bit 0: Framer Status Register Interrupt Status (FMSR) This bit is set when any of the latched status register bits, that are enabled for interrupt, in the active DS3 or E3 framer block are set. The interrupt pin will be driven when this bit is set and the GL.ISRIE.PISRIE bit is set.

Register Name: **PORT.SR**
Register Description: **Port Status Register**
Register Address: **052h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	TDM	RLOL	PMS

Bit 2: Transmit Driver Monitor Status (TDM) This bits indicates the status of the transmit monitor circuit in the transmit LIU.

0 = Transmit output not over loaded
1 = Transmit signal is overloaded

Bit 1: Receive Loss Of Lock Status (RLOL) This bits indicates the status of the receive LIU clock recovery PLL circuit.

0 = Locked to the incoming signal
1 = Not locked to the incoming signal

Bit 0: Performance Monitoring Update Status (PMS) This bits indicates the status of all active performance monitoring register and counter update signals in this port. It is an "AND" of all update status bits and is not set until all performance registers are updated and the counters reset. In software update modes, the update request bit PORT.CR1.PMU should be held high until this status bit goes high.

0 = The associated update request signal is low
1 = The requested performance register updates are all completed

Register Name: **PORT.SRL**
Register Description: **Port Status Register Latched**
Register Address: **054h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	RLCLKL	TCLKIL	--	--	--	TDML	RLOLL	PMSL

Bit 7: Receive Line Clock Activity Status Latched (RLCLKL) This bit will be set when the signal on the RLCLK pin or the recovered clock from the LIU for this port is active.

Bit 6: Transmit Input Clock Activity Status Latched (TCLKIL) This bit will be set when the signal on the TCLKI pin for this port is active.

Bit 2: Transmit Driver Monitor Status Latched (TDML) This bit will be set when the *PORT.SR.*TDM status bit changes from low to high. This bit will also set the *PORT.ISR.*PSR status bit if the *PORT.SRIE.*TDMIE bit is enabled. The interrupt pin will be driven when this bit is set, the *PORT.SRIE.*TDMIE bit is set, and the corresponding *GL.ISRIE.*PISRIE bit is also set.

Bit 1: Receive Loss Of Lock Status Latched (RLOLL) This bit will be set when the *PORT.SR*.RLOL status bit changes from low to high. This bit will also set the *PORT.ISR*.PSR status bit if the *PORT.SRIE*.RLOLIE bit is enabled. The interrupt pin will be driven when this bit is set, the *PORT.SRIE*.RLOLIE bit is set, and the corresponding *GL.ISRIE*.PISRIE bit is also set.

Bit 0: Performance Monitoring Update Status Latched (PMSL) This bit will be set when the *PORT.SR*.PMS status bit changes from low to high. This bit will also set the *PORT.ISR*.PSR status bit if the *PORT.SRIE*.PMUIE bit is enabled. The interrupt pin will be driven when this bit is set, the *PORT.SRIE*.PMUIE bit is set, and the *PORT.SRIE*.PMSIE bit are set.

Register Name: **PORT.SRIE**
Register Description: **Port Status Register Interrupt Enable**
Register Address: **056h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	TDMIE	RLOLIE	PMSIE
Default	0	0	0	0	0	0	0	0

Bit 2: Transmit Driver Monitor Latched Status Interrupt Enable (TDMIE) The interrupt pin will be driven when this bit is enabled and the *PORT.SRL*.TDML bit is set and the GL.ISRIE.PISRIE bit is enabled.

Bit 1: Receive Loss Of Lock Latched Status Interrupt Enable (RLOLIE) The interrupt pin will be driven when this bit is enabled and the *PORT.SRL*.RLOLL bit is set and the bit in GL.ISRIE.PISRIE bit is enabled.

Bit 0: Performance Monitoring Update Latched Status Interrupt Enable (PMSIE) The interrupt pin will be driven when this bit is enabled and the *PORT.SRL*.PMSL bit is set and the bit in GL.ISRIE.PISRIE bit is enabled.

12.4 BERT

12.4.1 BERT Register Map

The BERT utilizes twelve registers.

Table 12-13. BERT Register Map

Address	Register	Register Description
060h	BERT.CR	BERT Control Register
062h	BERT.PCR	BERT Pattern Configuration Register
064h	BERT.SPR1	BERT Seed/Pattern Register #1
066h	BERT.SPR2	BERT Seed/Pattern Register #2
068h	BERT.TEICR	BERT Transmit Error Insertion Control Register
06Ah	--	Unused
06Ch	BERT.SR	BERT Status Register
06Eh	BERT.SRL	BERT Status Register Latched
070h	BERT.SRIE	BERT Status Register Interrupt Enable
072h	--	Unused
074h	BERT.RBECR1	BERT Receive Bit Error Count Register #1
076h	BERT.RBECR2	BERT Receive Bit Error Count Register #2
078h	BERT.RBCR1	BERT Receive Bit Count Register #1
07Ah	BERT.RBCR2	BERT Receive Bit Count Register #2
07Ch	--	Unused
07Eh	--	Unused

12.4.2 BERT Register Bit Descriptions

Register Name: **BERT.CR**
Register Description: **BERT Control Register**
Register Address: **060h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	PMUM	LPMU	RNPL	RPIC	MPR	APRD	TNPL	TPIC
Default	0	0	0	0	0	0	0	0

Bit 7: Performance Monitoring Update Mode (PMUM) – When 0, a performance monitoring update is initiated by the LPMU register bit. When 1, a performance monitoring update is initiated by the global or port PMU register bit. Note: If the LPMU bit or the global or port PMU bit is one, changing the state of this bit may cause a performance monitoring update to occur.

Bit 6: Local Performance Monitoring Update (LPMU) – This bit causes a performance monitoring update to be initiated if local performance monitoring update is enabled (PMUM = 0). A 0 to 1 transition causes the performance monitoring registers to be updated with the latest data, and the counters reset (0 or 1). For a second performance monitoring update to be initiated, this bit must be set to 0, and back to 1. If LPMU goes low before the PMS bit goes high; an update might not be performed. This bit has no affect when PMUM=1.

Bit 5: Receive New Pattern Load (RNPL) – A zero to one transition of this bit will cause the programmed test pattern (QRSS, PTS, PLF[4:0}, PTF[4:0], and BSP[31:0]) to be loaded in to the receive pattern generator. This bit

must be changed to zero and back to one for another pattern to be loaded. Loading a new pattern will forces the receive pattern generator out of the "Sync" state which causes a resynchronization to be initiated. Note: QRSS, PTS, PLF[4:0}, PTF[4:0], and BSP[31:0] must not change from the time this bit transitions from 0 to 1 until four receive clock cycles after this bit transitions from 0 to 1.

Bit 4: Receive Pattern Inversion Control (RPIC) – When 0, the receive incoming data stream is not altered. When 1, the receive incoming data stream is inverted.

Bit 3: Manual Pattern Resynchronization (MPR) – A zero to one transition of this bit will cause the receive pattern generator to resynchronize to the incoming pattern. This bit must be changed to zero and back to one for another resynchronization to be initiated. Note: A manual resynchronization forces the receive pattern generator out of the "Sync" state.

Bit 2: Automatic Pattern Resynchronization Disable (APRD) – When 0, the receive pattern generator will automatically resynchronize to the incoming pattern if six or more times during the current 64-bit window the incoming data stream bit and the receive pattern generator output bit did not match. When 1, the receive pattern generator will not automatically resynchronize to the incoming pattern.

Bit 1: Transmit New Pattern Load (TNPL) – A zero to one transition of this bit will cause the programmed test pattern (QRSS, PTS, PLF[4:0}, PTF[4:0], and BSP[31:0]) to be loaded in to the transmit pattern generator. This bit must be changed to zero and back to one for another pattern to be loaded. Note: QRSS, PTS, PLF[4:0}, PTF[4:0], and BSP[31:0] must not change from the time this bit transitions from 0 to 1 until four transmit clock cycles after this bit transitions from 0 to 1.

Bit 0: Transmit Pattern Inversion Control (TPIC) – When 0, the transmit outgoing data stream is not altered. When 1, the transmit outgoing data stream is inverted.

Register Name: **BERT.PCR**
Register Description: **BERT Pattern Configuration Register**
Register Address: **062h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	PTF4	PTF3	PTF2	PTF1	PTF0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	QRSS	PTS	PLF4	PLF3	PLF2	PLF1	PLF0
Default	0	0	0	0	0	0	0	0

Bits 12 to 8: Pattern Tap Feedback (PTF[4:0]) – These five bits control the PRBS "tap" feedback of the pattern generator. The "tap" feedback will be from bit y of the pattern generator (y = PTF[4:0] +1). These bits are ignored when programmed for a repetitive pattern. For a PRBS signal, the feedback is an XOR of bit n and bit y.

Bit 6: QRSS Enable (QRSS) – When 0, the pattern generator configuration is controlled by PTS, PLF[4:0], and PTF[4:0], and BSP[31:0]. When 1, the pattern generator configuration is forced to a PRBS pattern with a generating polynomial of $x^{20} + x^{17} + 1$. The output of the pattern generator will be forced to one if the next fourteen output bits are all zero.

Bit 5: Pattern Type Select (PTS) – When 0, the pattern is a PRBS pattern. When 1, the pattern is a repetitive pattern.

Bits 4 to 0: Pattern Length Feedback (PLF[4:0]) – These five bits control the "length" feedback of the pattern generator. The "length" feedback will be from bit n of the pattern generator (n = PLF[4:0] +1). For a PRBS signal, the feedback is an XOR of bit n and bit y. For a repetitive pattern the feedback is bit n.

Register Name: **BERT.SPR1**
Register Description: **BERT Seed/Pattern Register #1**
Register Address: **064h**

Bit #	15	14	13	12	11	10	9	8
Name	BSP15	BSP14	BSP13	BSP12	BSP11	BSP10	BSP9	BSP8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BSP7	BSP6	BSP5	BSP4	BSP3	BSP2	BSP1	BSP0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: BERT Seed/Pattern (BSP[15:0]) – Lower sixteen bits of 32 bits. Register description follows next register.

Register Name: **BERT.SPR2**
Register Description: **BERT Seed/Pattern Register #2**
Register Address: **066h**

Bit #	15	14	13	12	11	10	9	8
Name	BSP31	BSP30	BSP29	BSP28	BSP27	BSP26	BSP25	BSP24
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BSP23	BSP22	BSP21	BSP20	BSP19	BSP18	BSP17	BSP16
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: BERT Seed/Pattern (BSP[31:16]) - Upper 16 bits of 32 bits.

BERT Seed/Pattern (BSP[31:0]) – These 32 bits are the programmable seed for a transmit PRBS pattern, or the programmable pattern for a transmit or receive repetitive pattern. BSP(31) will be the first bit output on the transmit side for a 32-bit repetitive pattern or 32-bit length PRBS. BSP(31) will be the first bit input on the receive side for a 32-bit repetitive pattern.

Register Name: **BERT.TEICR**
Register Description: **BERT Transmit Error Insertion Control Register**
Register Address: **068h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TEIR2	TEIR1	TEIR0	BEI	TSEI	MEIMS
Default	0	0	0	0	0	0	0	0

Bits 5 to 3: Transmit Error Insertion Rate (TEIR[2:0]) – These three bits indicate the rate at which errors are inserted in the output data stream. One out of every 10^n bits is inverted. TEIR[2:0] is the value n. A TEIR[2:0] value of 0 disables error insertion at a specific rate. A TEIR[2:0] value of 1 result in every 10^{th} bit being inverted. A TEIR[2:0] value of 2 result in every 100^{th} bit being inverted. Error insertion starts when this register is written to with a TEIR[2:0] value that is nonzero. If this register is written to during the middle of an error insertion process, the new error rate will be started after the next error is inserted.

TEIR[2:0]	Error Rate
000	Disabled
001	$1*10^{-1}$
010	$1*10^{-2}$
011	$1*10^{-3}$
100	$1*10^{-4}$
101	$1*10^{-5}$
110	$1*10^{-6}$
111	$1*10^{-7}$

Bit 2: Bit Error Insertion Enable (BEI) – When 0, single bit error insertion is disabled. When 1, single bit error insertion is enabled.

Bit 1: Transmit Single Error Insert (TSEI) – This bit causes a bit error to be inserted in the transmit data stream if manual error insertion is disabled (MEIMS = 0) and single bit error insertion is enabled. A 0 to 1 transition causes a single bit error to be inserted. For a second bit error to be inserted, this bit must be set to 0, and back to 1. Note: If MEIMS is low, and this bit transitions more than once between error insertion opportunities, only one error will be inserted.

Bit 0: Manual Error Insert Mode Select (MEIMS) – When 0, error insertion is initiated by the TSEI register bit. When 1, error insertion is initiated by the transmit manual error insertion signal (TMEI). Note: If TMEI or TSEI is one, changing the state of this bit may cause a bit error to be inserted.

Register Name: **BERT.SR**
Register Description: **BERT Status Register**
Register Address: **06Ch**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	PMS	--	BEC	OOS

Bit 3: Performance Monitoring Update Status (PMS) – This bit indicates the status of the receive performance monitoring register (counters) update. This bit will transition from low to high when the update is completed. PMS will be forced low when the LPMU bit (PMUM = 0) or the global or port PMU bit (PMUM=1) goes low.

Bit 1: Bit Error Count (BEC) – When 0, the bit error count is zero. When 1, the bit error count is one or more. This bit is cleared when the user updates the BERT counters via the PMU bit (BERT.CR).

Bit 0: Out Of Synchronization (OOS) – When 0, the receive pattern generator is synchronized to the incoming pattern. When 1, the receive pattern generator is not synchronized to the incoming pattern.

Register Name: **BERT.SRL**
Register Description: **BERT Status Register Latched**
Register Address: **06Eh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	PMSL	BEL	BECL	OOSL

Bit 3: Performance Monitoring Update Status Latched (PMSL) – This bit is set when the PMS bit transitions from 0 to 1.

Bit 2: Bit Error Latched (BEL) – This bit is set when a bit error is detected.

Bit 1: Bit Error Count Latched (BECL) – This bit is set when the BEC bit transitions from 0 to 1.

Bit 0: Out Of Synchronization Latched (OOSL) – This bit is set when the OOS bit changes state.

Register Name: **BERT.SRIE**
Register Description: **BERT Status Register Interrupt Enable**
Register Address: **070h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	PMSIE	BEIE	BECIE	OOSIE
Default	0	0	0	0	0	0	0	0

Bit 3: Performance Monitoring Update Status Interrupt Enable (PMSIE) – This bit enables an interrupt if the PMSL bit is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Bit Error Interrupt Enable (BEIE) – This bit enables an interrupt if the BEL bit is set and the GL.ISRIE.PSRIE bit is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Bit Error Count Interrupt Enable (BECIE) – This bit enables an interrupt if the BECL bit is set and the GL.ISRIE.PSRIE bit is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Out Of Synchronization Interrupt Enable (OOSIE) – This bit enables an interrupt if the OOSL bit is set and the GL.ISRIE.PSRIE bit is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **BERT.RBECR1**
Register Description: **BERT Receive Bit Error Count Register #1**
Register Address: **074h**

Bit #	15	14	13	12	11	10	9	8
Name	BEC15	BEC14	BEC13	BEC12	BEC11	BEC10	BEC9	BEC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BEC7	BEC6	BEC5	BEC4	BEC3	BEC2	BEC1	BEC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Bit Error Count (BEC[15:0]) – Lower sixteen bits of 24 bits. Register description follows next register.

Register Name: **BERT.RBECR2**
Register Description: **BERT Receive Bit Error Count Register #2**
Register Address: **076h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BEC23	BEC22	BEC21	BEC20	BEC19	BEC18	BEC17	BEC16
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Bit Error Count (BEC[23:16]) - Upper 8-bits of Register.

Bit Error Count (BEC[23:0]) – These twenty-four bits indicate the number of bit errors detected in the incoming data stream. This count stops incrementing when it reaches a count of FF FFFFh. This bit error counter will not increment when an OOS condition exists. This register is updated via the PMU signal (see section 10.4.5)

Register Name: **BERT.RBCR1**
Register Description: **Receive Bit Count Register #1**
Register Address: **078h**

Bit #	15	14	13	12	11	10	9	8
Name	BC15	BC14	BC13	BC12	BC11	BC10	BC9	BC8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BC7	BC6	BC5	BC4	BC3	BC2	BC1	BC0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Bit Count (BC[15:0]) – Lower sixteen bits of 32 bits. Register description follows next register.

Register Name: **BERT.RBCR2**
Register Description: **Receive Bit Count Register #2**
Register Address: **07Ah**

Bit #	15	14	13	12	11	10	9	8
Name	BC31	BC30	BC29	BC28	BC27	BC26	BC25	BC24
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BC23	BC22	BC21	BC20	BC19	BC18	BC17	BC16
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Bit Count (BC[31:16]) - Upper 16 bits of 32 bits.

Bit Count (BC[31:0]) – These thirty-two bits indicate the number of bits in the incoming data stream. This count stops incrementing when it reaches a count of FFFF FFFFh. This bit counter will not increment when an OOS condition exists. This register is updated via the PMU signal (see section 10.4.5)

12.5 B3ZS/HDB3 Line Encoder/Decoder

12.5.1 Transmit Side Line Encoder/Decoder Register Map

The transmit side utilizes one register.

Table 12-14. Transmit Side B3ZS/HDB3 Line Encoder/Decoder Register Map

Address	Register	Register Description
08Ch	LINE.TCR	Line Transmit Control Register
08Eh	--	Unused

12.5.1.1 Register Bit Descriptions

Register Name: **LINE.TCR**
Register Description: **Line Transmit Control Register**
Register Address: **08Ch**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	TZSD	EXZI	BPVI	TSEI	MEIMS
Default	0	0	0	0	0	0	0	0

Bit 4: Transmit Zero Suppression Encoding Disable (TZSD) – When 0, the B3ZS/HDB3 Encoder performs zero suppression (B3ZS or HDB3) and AMI encoding. When 1, zero suppression (B3ZS or HDB3) encoding is disabled, and only AMI encoding is performed.

Bit 3: Excessive Zero Insert Enable (EXZI) – When 0, excessive zero (EXZ) event insertion is disabled. When 1, EXZ event insertion is enabled.

Bit 2: Bipolar Violation Insert Enable (BPVI) – When 0, bipolar violation (BPV) insertion is disabled. When 1, BPV insertion is enabled.

Bit 1: Transmit Single Error Insert (TSEI) – This bit causes an error of the enabled type(s) to be inserted in the transmit data stream if manual error insertion is disabled (MEIMS = 0). A 0 to 1 transition causes a single error to be inserted. For a second error to be inserted, this bit must be set to 0, and back to 1. Note: If MEIMS is low, and this bit transitions more than once between error insertion opportunities, only one error will be inserted.

Bit 0: Manual Error Insert Mode Select (MEIMS) – When 0, error insertion is initiated by the TSEI register bit. When 1, error insertion is initiated by the transmit manual error insertion signal (TMEI). Note: If TMEI or TSEI is one, changing the state of this bit may cause an error to be inserted.

12.5.2 Receive Side Line Encoder/Decoder Register Map

The receive side utilizes six registers.

Table 12-15. Receive Side B3ZS/HDB3 Line Encoder/Decoder Register Map

Address	Register	Register Description
090h	LINE.RCR	Line Receive Control Register
092h	--	Unused
094h	LINE.RSR	Line Receive Status Register
096h	LINE.RSRL	Line Receive Status Register Latched
098h	LINE.RSRIE	Line Receive Status Register Interrupt Enable
09Ah	--	Unused
09Ch	LINE.RBPVCR	Line Receive Bipolar Violation Count Register
09Eh	LINE.REXZCR	Line Receive Excessive Zero Count Register

12.5.2.1 Register Bit Descriptions

Register Name: **LINE.RCR**
Register Description: **Line Receive Control Register**
Register Address: **(0.2.4.6)90h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	E3CVE	REZSF	RDZSF	RZSD
Default	0	0	0	0	0	0	0	0

Bit 2: E3 Code Violation Enable (E3CVE) – When 0, the bipolar violation count will be a count of bipolar violations. When 1, the bipolar violation count will be a count of E3 line coding violations. Note: E3 line coding violations are defined as consecutive bipolar violations of the same polarity in ITU O.161. This bit is ignored in B3ZS mode.

Bit 2: Receive BPV Error Detection Zero Suppression Code Format (REZSF) – When 0, BPV error detection detects a B3ZS signature if a zero is followed by a bipolar violation (BPV), and an HDB3 signature if two zeros are followed by a BPV. When 1, BPV error detection detects a B3ZS signature if a zero is followed by a BPV that has the opposite polarity of the BPV in the previous B3ZS signature, and an HDB3 signature if two zeros are followed by a BPV that has the opposite polarity of the BPV in the previous HDB3 signature. Note: Immediately after a reset, this bit is ignored. The first B3ZS signature is defined as a zero followed by a BPV, and the first HDB3 signature is defined as two zeros followed by a BPV. All subsequent B3ZS/HDB3 signatures will be determined by the setting of this bit.

Note: The default setting (REZSF = 0) conforms to ITU O.162. The default setting may falsely decode actual BPVs that are not codewords. It is recommended that REZSF be set to one for most applications. This setting is more robust to accurately detect codewords.

Bit 1: Receive Zero Suppression Decoding Zero Suppression Code Format (RDZSF) – When 0, zero suppression decoding detects a B3ZS signature if a zero is followed by a bipolar violation (BPV), and an HDB3 signature if two zeros are followed by a BPV. When 1, zero suppression decoding detects a B3ZS signature if a zero is followed by a BPV that has the opposite polarity of the BPV in the previous B3ZS signature, and an HDB3 signature if two zeros are followed by a BPV that has the opposite polarity of the BPV in the previous HDB3 signature. Note: Immediately after a reset ($\overline{\text{DRST}}$ or $\overline{\text{RST}}$ low), this bit is ignored. The first B3ZS signature is defined as a zero followed by a BPV, and the first HDB3 signature is defined as two zeros followed by a BPV. All subsequent B3ZS/HDB3 signatures will be determined by the setting of this bit.

Bit 0: Receive Zero Suppression Decoding Disable (RZSD) – When 0, the B3ZS/HDB3 Decoder performs zero suppression (B3ZS or HDB3) and AMI decoding. When 1, zero suppression (B3ZS or HDB3) decoding is disabled, and only AMI decoding is performed.

Register Name: **LINE.RSR**
Register Description: **Line Receive Status Register**
Register Address: **(0.2.4.6)94h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	EXZC	--	BPVC	LOS

Bit 3: Excessive Zero Count (EXZC) – When 0, the excessive zero count is zero. When 1, the excessive zero count is one or more.

Bit 1: Bipolar Violation Count (BPVC) – When 0, the bipolar violation count is zero. When 1, the bipolar violation count is one or more.

Bit 0: Loss Of Signal (LOS) – When 0, the receive line is not in a loss of signal (LOS) condition. When 1, the receive line is in an LOS condition. See Section 10.10.4

Register Name: **LINE.RSRL**
Register Description: **Line Receive Status Register Latched**
Register Address: **(0.2.4.6)96h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	ZSCDL	EXZL	EXZCL	BPVL	BPVCL	LOSL

Bit 5: Zero Suppression Code Detect Latched (ZSCDL) – This bit is set when a B3ZS or HDB3 signature is detected.

Bit 4: Excessive Zero Latched (EXZL) – This bit is set when an excessive zero event is detected on the incoming bipolar data stream.

Bit 3: Excessive Zero Count Latched (EXZCL) – This bit is set when the LINE.RSR.EXZC bit transitions from zero to one.

Bit 2: Bipolar Violation Latched (BPVL) – This bit is set when a bipolar violation (or E3 LCV if enabled) is detected on the incoming bipolar data stream.

Bit 1: Bipolar Violation Count Latched (BPVCL) – This bit is set when the LINE.RSR.BPVC bit transitions from zero to one.

Bit 0: Loss of Signal Change Latched (LOSL) – This bit is set when the LINE.RSR.LOS bit changes state.

Note: When zero suppression (B3ZS or HDB3) decoding is disabled, the LOS condition is cleared, and cannot be detected.

Register Name: **LINE.RSRIE**
Register Description: **Line Receive Status Register Interrupt Enable**
Register Address: **(0.2.4.6)98h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	ZSCDIE	EXZIE	EXZCIE	BPVIE	BPVCIE	LOSIE
Default	0	0	0	0	0	0	0	0

Bit 5: Zero Suppression Code Detect Interrupt Enable (ZSCDIE) – This bit enables an interrupt if the *LINE.RSRL*.ZSCDL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Excessive Zero Interrupt Enable (EXZIE) – This bit enables an interrupt if the *LINE.RSRL*.EXZL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Excessive Zero Count Interrupt Enable (EXZCIE) – This bit enables an interrupt if the *LINE.RSRL*.EXZCL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Bipolar Violation Interrupt Enable (BPVIE) – This bit enables an interrupt if the *LINE.RSRL*.BPVL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Bipolar Violation Count Interrupt Enable (BPVCIE) – This bit enables an interrupt if the *LINE.RSRL*.BPVCL bit and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set. is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Loss Of Signal Interrupt Enable (LOSIE) – This bit enables an interrupt if the *LINE.RSRL*.LOSL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **LINE.RBPVCR**
Register Description: **Line Receive Bipolar Violation Count Register**
Register Address: **(0.2.4.6)9Ch**

Bit #	15	14	13	12	11	10	9	8
Name	BPV15	BPV14	BPV13	BPV12	BPV11	BPV10	BPV9	BPV8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	BPV7	BPV6	BPV5	BPV4	BPV3	BPV2	BPV1	BPV0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Bipolar Violation Count (BPV[15:0]) – These sixteen bits indicate the number of bipolar violations detected on the incoming bipolar data stream. This register is updated via the PMU signal (see section 10.4.5)

Register Name: **LINE.REXZCR**
Register Description: **Line Receive Excessive Zero Count Register**
Register Address: **(0.2.4.6)9Eh**

Bit #	15	14	13	12	11	10	9	8
Name	EXZ15	EXZ14	EXZ13	EXZ12	EXZ11	EXZ10	EXZ9	EXZ8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	EXZ7	EXZ6	EXZ5	EXZ4	EXZ3	EXZ2	EXZ1	EXZ0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Excessive Zero Count (EXZ[15:0]) – These sixteen bits indicate the number of excessive zero conditions detected on the incoming bipolar data stream. This register is updated via the PMU signal (see section 10.4.5)

12.6 HDLC

12.6.1 HDLC Transmit Side Register Map

The transmit side utilizes five registers.

Table 12-16. Transmit Side HDLC Register Map

Address	Register	Register Description
0A0h	HDLC.TCR	HDLC Transmit Control Register
0A2h	HDLC.TFDR	HDLC Transmit FIFO Data Register
0A4h	HDLC.TSR	HDLC Transmit Status Register
0A6h	HDLC.TSRL	HDLC Transmit Status Register Latched
0A8h	HDLC.TSRIE	HDLC Transmit Status Register Interrupt Enable
0AAh	--	Unused
0ACh	--	Unused
0AEh	--	Unused

12.6.1.1 Register Bit Descriptions

Register Name: **HDLC.TCR**
Register Description: **HDLC Transmit Control Register**
Register Address: **0A0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	TDAL4	TDAL3	TDAL2	TDAL1	TDAL0
Default	0	0	0	0	1	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	TPSD	TFEI	TIFV	TBRE	TDIE	TFPD	TFRST
Default	0	0	0	0	0	0	0	0

Bits 12 to 8: Transmit HDLC Data Storage Available Level (TDAL[4:0]) – These five bits indicate the minimum number of bytes ([TDAL*8}+1) that must be available for storage (do not contain data) in the Transmit FIFO for HDLC data storage to be available. For example, a value of 21 (15h) results in HDLC data storage being available (THDA=1) when the Transmit FIFO has 169 (A9h) bytes or more available for storage, and HDLC data storage not being available (THDA=0) when the Transmit FIFO has 168 (A8h) bytes or less available for storage.

Bit 6: Transmit Packet Start Disable (TPSD) – When 0, the Transmit Packet Processor will continue sending packets after the current packet end. When 1, the Transmit Packet Processor will stop sending packets after the current packet end.

Bit 5: Transmit FCS Error Insertion (TFEI) – When 0, the calculated FCS (inverted CRC-16) is appended to the packet. When 1, the inverse of the calculated FCS (noninverted CRC-16) is appended to the packet causing an FCS error. This bit is ignored if transmit FCS processing is disabled (TFPD = 1).

Bit 4: Transmit Inter-frame Fill Value (TIFV) – When 0, inter-frame fill is done with the flag sequence (7Eh). When 1, inter-frame fill is done with all ‘1’s.

Bit 3: Transmit Bit Reordering Enable (TBRE) – When 0, bit reordering is disabled (The first bit transmitted is the LSB of the Transmit FIFO Data byte TFD[0]). When 1, bit reordering is enabled (The first bit transmitted is the MSB of the Transmit FIFO Data byte TFD[7]).

Bit 2: Transmit Data Inversion Enable (TDIE) – When 0, the outgoing data is directly output from packet processing. When 1, the outgoing data is inverted before being output from packet processing.

Bit 1: Transmit FCS Processing Disable (TFPD) – This bit controls whether or not an FCS is calculated and appended to the end of each packet. When 0, the calculated FCS bytes are appended to the end of the packet. When 1, the packet is transmitted without an FCS.

Bit 0: Transmit FIFO Reset (TFRST) – When 0, the Transmit FIFO will resume normal operations, however, data is discarded until a start of packet is received after RAM power-up is completed. When 1, the Transmit FIFO is emptied, any transfer in progress is halted, the FIFO RAM is powered down, and all incoming data is discarded (all TFDR register writes are ignored).

Register Name: **HDLC.TFDR**
Register Description: **HDLC Transmit FIFO Data Register**
Register Address: **0A2h**

Bit #	15	14	13	12	11	10	9	8
Name	TFD7	TFD6	TFD5	TFD4	TFD3	TFD2	TFD1	TFD0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TDPE
Default	0	0	0	0	0	0	0	0

Note: The FIFO data and status are loaded into the Transmit FIFO when the Transmit FIFO Data (TFD[7:0]) is written (upper byte write). When read, the value of these bits is always zero.

Bits 15 to 8: Transmit FIFO Data (TFD[7:0]) – These eight bits are the packet data to be stored in the Transmit FIFO. TFD[7] is the MSB, and TFD[0] is the LSB. If bit reordering is disabled, TFD[0] is the first bit transmitted, and TFD[7] is the last bit transmitted. If bit reordering is enabled, TFD[7] is the first bit transmitted, and TFD[0] is the last bit transmitted.

Bit 0: Transmit FIFO Data Packet End (TDPE) – When 0, the Transmit FIFO data is not a packet end. When 1, the Transmit FIFO data is a packet end.

Register Name: **HDLC.TSR**
Register Description: **HDLC Transmit Status Register**
Register Address: **0A4h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	TFFL5	TFFL4	TFFL3	TFFL2	TFFL1	TFFL0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	TFF	TFE	THDA

Bits 13 to 8: Transmit FIFO Fill Level (TFFL[5:0]) – These six bits indicate the number of eight byte groups available for storage (do not contain data) in the Transmit FIFO. E.g., a value of 21 (15h) indicates the FIFO has 168 (A8h) to 175 (AFh) bytes are available for storage.

Bit 2: Transmit FIFO Full (TFF) – When 0, the Transmit FIFO contains 255 or less bytes of data. When 1, the Transmit FIFO is full.

Bit 1: Transmit FIFO Empty (TFE) – When 0, the Transmit FIFO contains at least one byte of data. When 1, the Transmit FIFO is empty.

Bit 0: Transmit HDLC Data Storage Available (THDA) – When 0, the Transmit FIFO has less storage space available in the Transmit FIFO than the Transmit HDLC data storage available level (TDAL[4:0]). When 1, the Transmit FIFO has the same or more storage space available than the Transmit FIFO HDLC data storage available level.

Register Name: **HDLC.TSRL**
Register Description: **HDLC Transmit Status Register Latched**
Register Address: **0A6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TFOL	TFUL	TPEL	--	TFEL	THDAL

Bit 5: Transmit FIFO Overflow Latched (TFOL) – This bit is set when a Transmit FIFO overflow condition occurs.

Bit 4: Transmit FIFO Underflow Latched (TFUL) – This bit is set when a Transmit FIFO underflow condition occurs. An underflow condition results in a loss of data.

Bit 3: Transmit Packet End Latched (TPEL) – This bit is set when an end of packet is read from the Transmit FIFO.

Bit 1: Transmit FIFO Empty Latched (TFEL) – This bit is set when the TFE bit transitions from 0 to 1.

Note: This bit is also set when HDLC.TCR.TFRST is deasserted.

Bit 0: Transmit HDLC Data Available Latched (THDAL) – This bit is set when the THDA bit transitions from 0 to 1.

Note: This bit is also set when HDLC.TCR.TFRST is deasserted.

Register Name: **HDLC.TSRIE**
Register Description: **HDLC Transmit Status Register Interrupt Enable**
Register Address: **0A8h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TFOIE	TFUIE	TPEIE	--	TFEIE	THDAIE
Default	0	0	0	0	0	0	0	0

Bit 5: Transmit FIFO Overflow Interrupt Enable (TFOIE) – This bit enables an interrupt if the TFOL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Transmit FIFO Underflow Interrupt Enable (TFUIE) – This bit enables an interrupt if the TFUL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Transmit Packet End Interrupt Enable (TPEIE) – This bit enables an interrupt if the TPEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Transmit FIFO Full Interrupt Enable (TFFIE) – This bit enables an interrupt if the TFFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Transmit FIFO Empty Interrupt Enable (TFEIE) – This bit enables an interrupt if the TFEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Transmit HDLC Data Available Interrupt Enable (THDAIE) – This bit enables an interrupt if the THDAL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled

1 = interrupt enabled

12.6.2 HDLC Receive Side Register Map

The receive side utilizes five registers.

Table 12-17. Receive Side HDLC Register Map

Address	Register	Register Description
0B0h	HDLC.RCR	HDLC Receive Control Register
0B2h	--	Unused
0B4h	HDLC.RSR	HDLC Receive Status Register
0B6h	HDLC.RSRL	HDLC Receive Status Register Latched
0B8h	HDLC.RSRIE	HDLC Receive Status Register Interrupt Enable
0BAh	--	Unused
0BCh	HDLC.RFDR	HDLC Receive FIFO Data Register
0BEh	--	Unused

12.6.2.1 Register Bit Descriptions

Register Name: **HDLC.RCR**
Register Description: **HDLC Receive Control Register**
Register Address: **0B0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	RDAL4	RDAL3	RDAL2	RDAL1	RDAL0
Default	0	0	0	0	1	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	RBRE	RDIE	RFPD	RFRST
Default	0	0	0	0	0	0	0	0

Bits 12 to 8: Receive HDLC Data Available Level (RDAL[4:0]) – These five bits indicate the minimum number of eight byte groups that must be stored (contain data) in the Receive FIFO before HDLC data is considered to be available (RHDA=1). For example, a value of 21 (15h) results in HDLC data being available when the Receive FIFO contains 168 (A8h) bytes or more.

Bit 3: Receive Bit Reordering Enable (RBRE) – When 0, bit reordering is disabled (The first bit received is in the LSB of the Receive FIFO Data byte RFD[0]). When 1, bit reordering is enabled (The first bit received is in the MSB of the Receive FIFO Data byte RFD[7]).

Bit 2: Receive Data Inversion Enable (RDIE) – When 0, the incoming data is directly passed on for packet processing. When 1, the incoming data is inverted before being passed on for packet processing.

Bit 1: Receive FCS Processing Disable (RFPD) – When 0, FCS processing is performed (the packets have an FCS appended). When 1, FCS processing is disabled (the packets do not have an FCS appended).

Bit 0: Receive FIFO Reset (RFRST) – When 0, the Receive FIFO will resume normal operations, however, data is discarded until a start of packet is received after RAM power-up is completed. When 1, the Receive FIFO is emptied, any transfer in progress is halted, the FIFO RAM is powered down, the RHDA bit is forced low, and all incoming data is discarded.

Register Name: **HDLC.RSR**
Register Description: **HDLC Receive Status Register**
Register Address: **0B4h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	RFF	RFE	RHDA

Bit 2: Receive FIFO Full (RFF) – When 0, the Receive FIFO contains 255 or less bytes of data. When 1, the Receive FIFO is full.

Bit 1: Receive FIFO Empty (RFE) – When 0, the Receive FIFO contains at least one byte of data. When 1, the Receive FIFO is empty.

Bit 0: Receive HDLC Data Available (RHDA) – When 0, the Receive FIFO contains less data than the Receive HDLC data available level (RDAL[4:0]). When 1, the Receive FIFO contains the same or more data than the Receive HDLC data available level.

Register Name: **HDLC.RSRL**
Register Description: **HDLC Receive Status Register Latched**
Register Address: **0B6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	RFOL	--	--	RPEL	RPSL	RFFL	--	RHDAL

Bit 7: Receive FIFO Overflow Latched (RFOL) – This bit is set when a Receive FIFO overflow condition occurs. An overflow condition results in a loss of data.

Bit 4: Receive Packet End Latched (RPEL) – This bit is set when an end of packet is stored in the Receive FIFO.

Bit 3: Receive Packet Start Latched (RPSL) – This bit is set when a start of packet is stored in the Receive FIFO.

Bit 2: Receive FIFO Full Latched (RFFL) – This bit is set when the RFF bit transitions from 0 to 1.

Bit 0: Receive HDLC Data Available Latched (RHDAL) – This bit is set when the RHDA bit transitions from 0 to 1.

Register Name: **HDLC.RSRIE**
Register Description: **HDLC Receive Status Register Interrupt Enable**
Register Address: **0B8h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RFOIE	--	--	RPEIE	RPSIE	RFFIE	--	RHDAIE
Default	0	0	0	0	0	0	0	0

Bit 7: Receive FIFO Overflow Interrupt Enable (RFOIE) – This bit enables an interrupt if the RFOL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Receive Packet End Interrupt Enable (RPEIE) – This bit enables an interrupt if the RPEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Receive Packet Start Interrupt Enable (RPSIE) – This bit enables an interrupt if the RPSL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Receive FIFO Full Interrupt Enable (RFFIE) – This bit enables an interrupt if the RFFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Receive HDLC Data Available Interrupt Enable (RHDAIE) – This bit enables an interrupt if the RHDAL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **HDLC.RFDR**
Register Description: **HDLC Receive FIFO Data Register**
Register Address: **0BCh**

Bit #	15	14	13	12	11	10	9	8
Name	RFD7	RFD6	RFD5	RFD4	RFD3	RFD2	RFD1	RFD0
Default	X	X	X	X	X	X	X	X

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	RPS2	RPS1	RPS0	RFDV
Default	0	0	0	0	X	X	X	0

Note: The FIFO data and status are updated when the Receive FIFO Data (RFD[7:0]) is read (upper byte read). When this register is read eight bits at a time, a read of the lower byte will reflect the status of the next read of the upper byte, and reading the upper byte when RFDV=0 may result in a loss of data.

Bits 15 to 8: Receive FIFO Data (RFD[7:0]) – These eight bits are the packet data stored in the Receive FIFO. RFD[7] is the MSB, and RFD[0] is the LSB. If bit reordering is disabled, RFD[0] is the first bit received, and RFD[7] is the last bit received. If bit reordering is enabled, RFD[7] is the first bit received, and RFD[0] is the last bit received.

Bits 3 to 1: Receive Packet Status (RPS[2:0]) – These three bits indicate the status of the received packet and packet data.

000 = packet middle
001 = packet start.
010 = reserved
011 = reserved
100 = packet end: good packet
101 = packet end: FCS errored packet.
110 = packet end: invalid packet (a noninteger number of bytes).
111 = packet end: aborted packet.

Bit 0: Receive FIFO Data Valid (RFDV) – When 0, the Receive FIFO data (RFD[7:0]) is invalid (the Receive FIFO is empty). When 1, the Receive FIFO data (RFD[7:0]) is valid.

12.7 FEAC Controller

12.7.1 FEAC Transmit Side Register Map

The transmit side utilizes five registers.

Table 12-18. FEAC Transmit Side Register Map

Address	Register	Register Description
0C0h	FEAC.TCR	FEAC Transmit Control Register
0C2h	FEAC.TFDR	FEAC Transmit Data Register
0C4h	FEAC.TSR	FEAC Transmit Status Register
0C6h	FEAC.TSRL	FEAC Transmit Status Register Latched
0C8h	FEAC.TSRIE	FEAC Transmit Status Register Interrupt Enable
0CAh	--	Unused
0CCh	--	Unused
0CEh	--	Unused

12.7.1.1 Register Bit Descriptions

Register Name: **FEAC.TCR**
Register Description: **FEAC Transmit Control Register**
Register Address: **0C0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	1	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	TFCL	TFS1	TFS0
Default	0	0	0	0	0	0	0	0

Bit 2: Transmit FEAC Codeword Load (TFCL) – A 0 to 1 transition on this bit loads the transmit FEAC processor mode select bits (TFS[1:0]), and transmit FEAC codes (TFCA[5:0] and TFCB[5:0]). Note: Whenever a FEAC codeword is loaded, any current FEAC codeword transmission in progress will be immediately halted, and the new FEAC codeword transmission will be started based on the new values for TFS[1:0], TFCA[5:0], and TFCB[5:0]..

Bits 1 to 0: Transmit FEAC Codeword Select (TFS[1:0]) – These two bits control the transmit FEAC processor mode. The TFCL bit loads the mode set by this bit.

00 = Idle (all ones)
01 = single code (send code TFCA ten times and send all ones)
10 = dual code (send code TFCA ten times, send code TFCB ten times, and send all ones)
11 = continuous code (send code TFCA continuously)

Register Name: **FEAC.TFDR**
Register Description: **Transmit FEAC Data Register**
Register Address: **0C2h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	TFCB5	TFCB4	TFCB3	TFCB2	TFCB1	TFCB0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TFCA5	TFCA4	TFCA3	TFCA2	TFCA1	TFCA0
Default	0	0	0	0	0	0	0	0

Bits 13 to 8: Transmit FEAC Code B (TFCB[5:0]) – These six bits are the transmit FEAC code B data to be stored inserted into codeword B. TFCB[5] is the LSB (last bit transmitted) of the FEAC code (C[6]), and TFCB[0] is the MSB (first bit transmitted) of the FEAC code (C[1]).

Bits 5 to 0: Transmit FEAC Code A (TFCA[5:0]) – These six bits are the transmit FEAC code A data to be stored inserted into codeword A. TFCA[5] is the LSB (last bit transmitted) of the FEAC code (C[6]), and TFCA[0] is the MSB (first bit transmitted) of the FEAC code (C[1]).

Register Name: **FEAC.TSR**
Register Description: **FEAC Transmit Status Register**
Register Address: **0C4h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TFI

Bit 0: Transmit FEAC Idle (TFI) – When 0, the Transmit FEAC processor is sending a FEAC codeword. When 1, the Transmit FEAC processor is sending an Idle signal (all ones).

Register Name: **FEAC.TSRL**
Register Description: **FEAC Transmit Status Register Latched**
Register Address: **0C6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TFIL

Bit 0: Transmit FEAC Idle Latched (TFIL) – This bit is set when the TFI bit transitions from 0 to 1. Note: Immediately after a reset, this bit will be set to one.

Register Name: **FEAC.TSRIE**
Register Description: **FEAC Transmit Status Register Interrupt Enable**
Register Address: **0C8h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	TFIIE
Default	0	0	0	0	0	0	0	0

Bit 0: Transmit FEAC Idle Interrupt Enable (TFIIE) – This bit enables an interrupt if the TFIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

12.7.2 FEAC Receive Side Register Map

The receive side utilizes five registers.

Table 12-19. FEAC Receive Side Register Map

Address	Register	Register Description
0D0h	FEAC.RCR	FEAC Receive Control Register
0D2h	--	Unused
0D4h	FEAC.RSR	FEAC Receive Status Register
0D6h	FEAC.RSRL	FEAC Receive Status Register Latched
0D8h	FEAC.RSRIE	FEAC Receive Status Register Interrupt Enable
0DAh	--	Unused
0DCh	FEAC.RFDR	FEAC Receive FIFO Data Register
0DEh	--	Unused

12.7.2.1 Register Bit Descriptions

Register Name: **FEAC.RCR**
Register Description: **FEAC Receive Control Register**
Register Address: **0D0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	1	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	--	--	RFR
Default	0	0	0	0	0	0	0	0

Bit 0: Receive FEAC Reset (RFR) –When 0, the Receive FEAC Processor and Receive FEAC FIFO will resume normal operations. When 1, the Receive FEAC controller is reset. The FEAC FIFO is emptied, any transfer in progress is halted, and all incoming data is discarded.

Register Name: **FEAC.RSR**
Register Description: **FEAC Receive Status Register**
Register Address: **0D4h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	RFFE	--	RFCD	RFI

Bit 3: Receive FEAC FIFO Empty (RFFE) – When 0, the Receive FIFO contains at least one code. When 1, the Receive FIFO is empty.

Bit 1: Receive FEAC Codeword Detect (RFCD) – When 0, the Receive FEAC Processor is not currently receiving a FEAC codeword. When 1, the Receive FEAC Processor is currently receiving a FEAC codeword.

Bit 0: Receive FEAC Idle (RFI) – When 0, the Receive FEAC processor is not receiving a FEAC Idle signal (all ones). When 1, the Receive FEAC processor is receiving a FEAC Idle signal.

Register Name: **FEAC.RSRL**
Register Description: **FEAC Receive Status Register Latched**
Register Address: **0D6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	RFFOL	RFCDL	RFIL

Bit 2: Receive FEAC FIFO Overflow Latched (RFFOL) – This bit is set when a Receive FIFO overflow condition occurs. An overflow condition results in a loss of data.

Bit 1: Receive FEAC Codeword Detect Latched (RFCDL) – This bit is set when the RFCD bit transitions from 0 to 1.

Bit 0: Receive FEAC Idle Latched (RFIL) – This bit is set when the RFI bit transitions from 0 to 1. Note: Immediately after a reset, this bit will be set to one.

Register Name: **FEAC.RSRIE**
Register Description: **FEAC Receive Status Register Interrupt Enable**
Register Address: **0D8h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	RFFOIE	RFCDIE	RFIIE
Default	0	0	0	0	0	0	0	0

Bit 2: Receive FEAC FIFO Overflow Interrupt Enable (RFFOIE) – This bit enables an interrupt if the RFFOL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Receive FEAC Codeword Detect Interrupt Enable (RFCDIE) – This bit enables an interrupt if the RFCDL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Receive FEAC Idle Interrupt Enable (RFIIE) – This bit enables an interrupt if the RFIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **FEAC.RFDR**
Register Description: **FEAC Receive FIFO Data Register**
Register Address: **0DCh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RFFI	--	RFF5	RFF4	RFF3	RFF2	RFF1	RFF0
Default	0	0	0	0	0	0	0	0

Bit 7: Receive FEAC FIFO Data Invalid (RFFI) – When 0, the Receive FIFO data (RFF[5:0]) is valid. When 1, the Receive FIFO data is invalid (Receive FIFO is empty).

Bits 5 to 0: Receive FEAC FIFO Data (RFF[5:0]) – These six bits are the FEAC code data stored in the Receive FIFO. RFF[5] is the LSB (last bit received) of the FEAC code (C[6]), and RFF[0] is the MSB (first bit received) of the FEAC code (C[1]). The Receive FEAC FIFO data (RFF[5:0]) is updated when it is read (lower byte read).

12.8 Trail Trace

12.8.1 Trail Trace Transmit Side

The transmit side utilizes three registers.

Table 12-20. Transmit Side Trail Trace Register Map

Address	Register	Register Description
0E8h	TT.TCR	Trail Trace Transmit Control Register
0EAh	TT.TTIAR	Trail Trace Transmit Identifier Address Register
0ECh	TT.TIR	Trail Trace Transmit Identifier Register
0EEh	--	Unused

12.8.1.1 Register Bit Descriptions

Register Name: **TT.TCR**
Register Description: **Trail Trace Transmit Control Register**
Register Address: **0E8h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	Reserved	TMAD	TIDLE	TDIE	TBRE
Default	0	0	0	0	0	0	0	0

Bit 3: Transmit Multiframe Alignment Insertion Disable (TMAD) – When 0, multiframe alignment signal (MAS) insertion is enabled, and the first bit transmitted of each trail trace byte is overwritten with an MAS bit. When 1, MAS insertion is disabled, and the trail trace bytes from the Transmit Data Storage are output without being modified.

Bit 2: Transmit Trail Trace Identifier Idle (TIDLE) – When 0, the programmed transmit trail trace identifier will be transmitted. When 1, all zeros will be transmitted.

Bit 1: Transmit Data Inversion Enable (TDIE) – When 0, the outgoing data from trail trace processing is output directly. When 1, the outgoing data from trail trace processing is inverted before being output.

Bit 0: Transmit Bit Reordering Enable (TBRE) – When 0, bit reordering is disabled (The first bit transmitted is the MSB *TT.TIR*.TTD[7] of the byte). When 1, bit reordering is enabled (The first bit transmitted is the LSB *TT.TIR*.TTD[0] of the byte).

Register Name: **TT.TTIAR**
Register Description: **Trail Trace Transmit Identifier Address Register**
Register Address: **0EAh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	Reserved	Reserved	TTIA3	TTIA2	TTIA1	TTIA0
Default	0	0	0	0	0	0	0	0

Bits 3 to 0: Transmit Trail Trace Identifier Address (TTIA[3:0]) – These four bits indicate the transmit trail trace identifier byte to be read/written by the next memory access. Address 0h indicates the first byte of the transmit trail trace identifier. Note: The value of these bits increments with each transmit trail trace identifier memory access (when these bits are Fh, a memory access will return them to 0h).

Register Name: **TT.TIR**
Register Description: **Trail Trace Transmit Identifier Register**
Register Address: **0ECh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TTD7	TTD6	TTD5	TTD4	TTD3	TTD2	TTD1	TTD0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Transmit Trail Trace Identifier Data (TTD[7:0]) – These eight bits are the transmit trail trace identifier data. The transmit trail trace identifier address will be incremented whenever these bits are read or written (when address location Fh is read or written, the address will return to 0h).

12.8.2 Trail Trace Receive Side Register Map

The receive side utilizes seven registers.

Table 12-21. Trail Trace Receive Side Register Map

Address	Register	Register Description
0F0h	TT.RCR	Trail Trace Receive Control Register
0F2h	TT.RTIAR	Trail Trace Receive Identifier Address Register
0F4h	TT.RSR	Trail Trace Receive Status Register
0F6h	TT.RSRL	Trail Trace Receive Status Register Latched
0F8h	TT.RSRIE	Trail Trace Receive Status Register Interrupt Enable
0FAh	--	Unused
0FCh	TT.RIR	Trail Trace Receive Identifier Register
0FEh	TT.EIR	Trail Trace Expected Identifier Register

12.8.2.1 Register Bit Descriptions

Register Name: **TT.RCR**
Register Description: **Trail Trace Receive Control Register**
Register Address: **0F0h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	Reserved	Reserved	RMAD	RETCE	RDIE	RBRE
Default	0	0	0	0	0	0	0	0

Bit 3: Receive Multiframe Alignment Disable (RMAD) – When 0, multiframe alignment is performed. When 1, multiframe alignment is disabled and the trail trace bytes are stored starting with a random byte.

Bit 2: Receive Expected Trail Trace Comparison Enable (RETCE) – When 0, expected trail trace comparison is disabled. When 1, expected trail trace comparison is performed. Note: When the RMAD bit is one, expected trail trace comparison is disabled regardless of the setting of this bit.

Bit 1: Receive Data Inversion Enable (RDIE) – When 0, the incoming data is directly passed on for trail trace processing. When 1, the incoming data is inverted before being passed on for trail trace processing.

Bit 0: Receive Bit Reordering Enable (RBRE) – When 0, bit reordering is disabled (The first bit received is the MSB *TT.RIR*.RTD[7] of the byte). When 1, bit reordering is enabled (The first bit received is the LSB *TT.RIR*.RTD[0] of the byte).

Register Name: **TT.RTIAR**
Register Description: **Trail Trace Receive Identifier Address Register**
Register Address: **0F2h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	Reserved	Reserved	ETIA3	ETIA2	ETIA1	ETIA0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	Reserved	Reserved	RTIA3	RTIA2	RTIA1	RTIA0
Default	0	0	0	0	0	0	0	0

Bits 11 to 8: Expected Trail Trace Identifier Address (ETIA[3:0]) – These four bits indicate the expected trail trace identifier byte to be read/written by the next memory access. Address 0h indicates the first byte of the expected trail trace identifier. Note: The value of these bits increments with each expected trail trace identifier memory access (when these bits are Fh, a memory access will return them to 0h).

Bits 3 to 0: Receive Trail Trace Identifier Address (RTIA[3:0]) – These four bits indicate the receive trail trace identifier byte to be read by the next memory access. Address 0h indicates the first byte of the receive trail trace identifier. Note: The value of these bits increments with each received trail trace identifier memory access (when these bits are Fh, a memory access will return them to 0h).

Register Name: **TT.RSR**
Register Description: **Trail Trace Receive Status Register**
Register Address: **0F4h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	--	RTIM	RTIU	RIDL

Bit 2: Receive Trail Trace Identifier Mismatch (RTIM)

0 = Received and expected trail trace identifiers match.
1 = Received and expected trail trace identifiers do not match; trail trace identifier mismatch (TIM) declared.

Bit 1: Receive Trail Trace Identifier Unstable (RTIU)

0 = Received trail trace identifier is not unstable
1 = Received trail trace identifier is in an unstable condition (TIU); TIU is declared when eight consecutive trail trace identifiers are received that do not match either the receive trail trace identifier or the previously stored current trail trace identifier.

Bit 0: Receive Trail Trace Identifier Idle (RIDL)

0 = Received trail trace identifier is not in idle condition.
1 = Received trail trace identifier is in idle condition. Idle condition is declared upon the reception of an all zeros trail trace identifier five consecutive times.

Register Name: **TT.RSRL**
Register Description: **Trail Trace Receive Status Register Latched**
Register Address: **0F6h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	RTICL	RTIML	RTIUL	RIDLL

Bit 3: Receive Trail Trace Identifier Change Latched (RTICL) – This bit is set when the receive trail trace identifier is updated.

Bit 2: Receive Trail Trace Identifier Mismatch Latched (RTIML) – This bit is set when the *TT.RSR*.RTIM bit transitions from 0 to 1.

Bit 1: Receive Trail Trace Identifier Unstable Latched (RTIUL) – This bit is set when the *TT.RSR*.RTIU bit transitions from 0 to 1.

Bit 0: Receive Trail Trace Identifier Idle Latched (RIDLL) – This bit is set when the *TT.RSR*.RIDL bit transitions from 0 to 1.

Register Name: **TT.RSRIE**
Register Description: **Trail Trace Receive Status Register Interrupt Enable**
Register Address: **0F8h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	RTICIE	RTIMIE	RTIUIE	RIDLIE
Default	0	0	0	0	0	0	0	0

Bit 3: Receive Trail Trace Identifier Change Interrupt Enable (RTICIE) – This bit enables an interrupt if the *TT.RSRL*.RTICL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Receive Trail Trace Identifier Mismatch Interrupt Enable (RTIMIE) – This bit enables an interrupt if the *TT.RSRL*.RTIML bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Receive Trail Trace Identifier Unstable Interrupt Enable (RTIUIE) – This bit enables an interrupt if the *TT.RSRL*.RTIUL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Receive Trail Trace Identifier Idle Interrupt Enable (RIDLIE) – This bit enables an interrupt if the *TT.RSRL*.RIDLL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **TT.RIR**
Register Description: **Trail Trace Receive Identifier Register**
Register Address: **0FCh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RTD7	RTD6	RTD5	RTD4	RTD3	RTD2	RTD1	RTD0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Receive Trail Trace Identifier Data (RTD[7:0]) – These eight bits are the receive trail trace identifier data. The receive trail trace identifier address will be incremented whenever these bits are read (when byte Fh is read, the address will return to 0h).

Register Name: **TT.EIR**
Register Description: **Trail Trace Expected Identifier Register**
Register Address: **0FEh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	ETD7	ETD6	ETD5	ETD4	ETD3	ETD2	ETD1	ETD0
Default	0	0	0	0	0	0	0	0

Bits 7 to 0: Expected Trail Trace Identifier Data (ETD[7:0]) – These eight bits are the expected trail trace identifier data. The expected trail trace identifier address will be incremented whenever these bits are read or written (when byte Fh is read or written, the address will return to 0h).

12.9 DS3/E3 framer

12.9.1 Transmit DS3

The transmit DS3 utilizes two registers.

Table 12-22. Transmit DS3 Framer Register Map

Address	Register	Register Description
118h	T3.TCR	T3 Transmit Control Register
11Ah	T3.TEIR	T3 Transmit Error Insertion Register
11Ch	--	Reserved
11Eh	--	Reserved

12.9.1.1 Register Bit Descriptions

Register Name: **T3.TCR**
Register Description: **T3 Transmit Control Register**
Register Address: **118h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	PBGE	TIDLE	CBGD	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TFEBE	AFEBED	TRDI	ARDID	TFGD	TAIS
Default	0	0	0	0	0	0	0	0

Bit 12: P-bit Generation Enable (PBGE) – When 0, if transmit frame generation is disabled, Transmit Frame Processor P-bit generation is disabled. The P-bit overhead periods in the incoming T3 signal will be passed through to error insertion. When 1, Transmit Frame Processor P-bit generation is enabled. The P-bit overhead periods in the incoming T3 signal will be overwritten even if transmit frame generation is disabled.

Bit 11: Transmit DS3 Idle Signal (TIDLE) –

0 = Transmit DS3 Idle signal is not inserted
1 = Transmit DS3 Idle signal is inserted into the DS3 frame.

Bit 10: C-bit Generation Disable (CBGD) (M23 mode only) – When 0, Transmit Frame Processor C-bit generation is enabled. The C-bit overhead periods in the incoming M23 DS3 signal will be overwritten with zeros. When 1, Transmit Frame Processor C-bit generation is disabled. The C-bit overhead periods in the incoming M23 DS3 signal will be treated as payload, and passed through to overhead insertion. This bit is ignored in C-bit DS3 mode.

Bit 5: Transmit FEBE Error (TFEBE) – When automatic far-end block error generation is defeated (AFEBED = 1), the inverse of this bit is inserted into the bits C_{41}, C_{42}, and C_{43}. Note: a far-end block error value of zero (TFEBE=1) indicates a far-end block error. This bit is ignored in M23 DS3 mode.

Bit 4: Automatic FEBE Defeat (AFEBED) – When 0, a far-end block error is automatically generated based upon the receive C-bit parity errors or framing errors. When 1, a far-end block error is inserted from the register bit TFEBE. This bit is ignored in M23 DS3 mode.

Bit 3: Transmit RDI Alarm (TRDI) – When automatic RDI generation is defeated (ARDID = 1), the inverse of this bit is inserted into the X-bits (X_1 and X_2). Note: an RDI value of zero (TRDI=1) indicates an alarm.

Bit 2: Automatic RDI Defeat (ARDID) – When 0, the RDI is automatically generated based received DS3 alarms. When 1, the RDI is inserted from the register bit TRDI.

Bit 1: Transmit Frame Generation Disabled (TFGD) –

0 = Transmit Frame Generation is enabled
1 = Transmit Frame Generation is disabled; DS3 overhead positions in the incoming DS3 payload will be passed through to error insertion. Note: Frame generation will still overwrite the P-bits if PBGE = 1. Also, the DS3 overhead periods can still be overwritten by error insertion, overhead insertion, or AIS/Idle generation.

Bit 0: Transmit Alarm Indication Signal (TAIS) –

0 = Transmit Alarm Indication Signal is not inserted
1 = Transmit Alarm Indication Signal is inserted into data stream payload

Register Name: **T3.TEIR**
Register Description: **T3 Transmit Error Insertion Register**
Register Address: **11Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	CCPEIE	CPEI	CFBEIE	FBEI
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	Reserved	CPEIE	PEI	FEIC1	FEIC0	FEI	TSEI	MEIMS
Default	0	0	0	0	0	0	0	0

Bit 11: Continuous C-bit Parity Error Insertion Enable (CCPEIE) – When 0, single C-bit parity error insertion is enabled. When 1, continuous C-bit parity error insertion is enabled, and C-bit parity errors will be transmitted continuously if CPEI is high.

Bit 10: C-bit Parity Error Insertion Enable (CPEI) – When 0, C-bit parity error insertion is disabled. When 1, C-bit parity error insertion is enabled.

Bit 9: Continuous Far-End Block Error Insertion Enable (CFBEIE) – When 0, single far-end block error insertion is enabled. When 1, continuous far-end block error insertion is enabled, and far-end block errors will be transmitted continuously if FBEI is high.

Bit 8: Far-End Block Error Insertion Enable (FBEI) – When 0, far-end block error insertion is disabled. When 1, far-end block error insertion is enabled.

Bit 6: Continuous P-bit Parity Error Insertion Enable (CPEIE) – When 0, single P-bit parity error insertion is enabled. When 1, continuous P-bit parity error insertion is enabled, and P-bit parity errors will be transmitted continuously if PEI is high.

Bit 5: P-bit Parity Error Insertion Enable (PEI) – When 0, P-bit parity error insertion is disabled. When 1, P-bit parity error insertion is enabled.

Bits 4 to 3: Framing Error Insertion Control (FEIC[1:0]) – These two bits control the framing error event to be inserted.

00 = F-bit error.
01 = M-bit error.
10 = SEF error.
11 = OOMF error.

Bit 2: Framing Error Insertion Enable (FEI) – When 0, framing error insertion is disabled. When 1, framing error insertion is enabled.

Bit 1: Transmit Single Error Insert (TSEI) – This bit causes an error of the enabled type(s) to be inserted in the transmit data stream if manual error insertion is disabled (MEIMS = 0). A 0 to 1 transition causes a single error to be inserted. For a second error to be inserted, this bit must be set to 0, and back to 1. Note: If MEIMS is low, and this bit transitions more than once between error insertion opportunities, only one error will be inserted.

Bit 0: Manual Error Insert Mode Select (MEIMS) – When 0, error insertion is initiated by the TSEI register bit. When 1, error insertion is initiated by the transmit manual error insertion signal (TMEI). Note: If TMEI or TSEI is one, changing the state of this bit may cause an error to be inserted.

12.9.2 Receive DS3 Register Map

The receive DS3 utilizes eleven registers. Two registers are shared for C-Bit and M23 DS3 modes. The M23 DS3 mode does not use the RFEBER or RCPECR count registers.

Table 12-23. Receive DS3 Framer Register Map

Address	Register	Register Description
120h	T3.RCR	T3 Receive Control Register
122h	--	Reserved
124h	T3.RSR1	T3 Receive Status Register #1
126h	T3.RSR2	T3 Receive Status Register #2
128h	T3.RSRL1	T3 Receive Status Register Latched #1
12Ah	T3.RSRL2	T3 Receive Status Register Latched #2
12Ch	T3.RSRIE1	T3 Receive Status Register Interrupt Enable #1
12Eh	T3.RSRIE2	T3 Receive Status Register Interrupt Enable #2
130h	--	Reserved
132h	--	Reserved
134h	T3.RFECR	T3 Receive Framing Error Count Register
136h	T3.RPECR	T3 Receive P-bit Parity Error Count Register
138h	T3.RFBECR	T3 Receive Far-End Block Error Count Register
13Ah	T3.RCPECR	T3 Receive C-bit Parity Error Count Register
13Ch	--	Unused
13Eh	--	Unused

12.9.2.1 Register Bit Descriptions

Register Name: **T3.RCR**
Register Description: **T3 Receive Control Register**
Register Address: **120h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	COVHD	MAOD	MDAISI	AAISD	ECC	FECC1	FECC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RAILE	RAILD	RAIOD	RAIAD	ROMD	LIP1	LIP0	FRSYNC
Default	0	0	0	0	0	0	0	0

Bit 14: C-bit Overhead Masking Disable (COVHD) – When 0, the C-bit positions will be marked as overhead (RDEN=0). When 1, the C-bit positions will be marked as data (RDEN=1). This bit is ignored in C-bit DS3 mode or when the ROMD bit is set to one.

Bit 13: Multiframe Alignment OOF Disable (MAOD) – When 0, an OOF condition is declared whenever an OOMF or SEF condition is declared. When 1, an OOF condition is declared only when an SEF condition is declared.

Bit 12: Manual Downstream AIS Insertion (MDAISI) – When 0, manual downstream AIS insertion is disabled. When 1, manual downstream AIS insertion is enabled.

Bit 11: Automatic Downstream AIS Disable (AAISD) – When 0, the presence of an LOS, OOF, or AIS condition will cause downstream AIS to be inserted. When 1, the presence of an LOS, OOF, or AIS condition will not cause downstream AIS to be inserted.

Bit 10: Error Count Control (ECC) – When 0, framing errors, P-bit parity errors, C-bit parity errors, and far-end block errors will not be counted if an OOF or AIS condition is present. P-bit parity errors, C-bit parity errors, and far-end block errors will also not be counted during the DS3 frame in which an OOF condition is terminated, and the next DS3 frame. When 1, framing errors, P-bit parity errors, C-bit parity errors, and far-end block errors will be counted regardless of the presence of an OOF or AIS condition.

Bits 9 to 8: Framing Error Count Control (FECC[1:0]) – These two bits control the type of framing error events that are counted.

00 = count OOF occurrences (counted regardless of the setting of the ECC bit).
01 = count M bit and F bit errors.
10 = count only F bit errors.
11 = count only M bit errors.

Bit 7: Receive Alarm Indication on LOF Enable (RAILE) – When 0, an LOF condition does not affect the receive alarm indication signal (RAI). When 1, an LOF condition will cause the transmit DS3 X-bits to be set to zero if transmit automatic RDI is enabled.

Bit 6: Receive Alarm Indication on LOS Disable (RAILD) – When 0, an LOS condition will cause the transmit DS3 X-bits to be set to zero if transmit automatic RDI is enabled. When 1, an LOS condition does not affect the RAI signal.

Bit 5: Receive Alarm Indication on SEF Disable (RAIOD) – When 0, an SEF condition will cause the transmit DS3 X-bits to be set to zero if transmit automatic RDI is enabled. When 1, an SEF condition does not affect the RAI signal.

Bit 4: Receive Alarm Indication on AIS Disable (RAIAD) – When 0, an AIS condition will cause the transmit DS3 X-bits to be set to zero if transmit automatic RDI is enabled. When 1, an AIS condition does not affect the RAI signal.

Bit 3: Receive Overhead Masking Disable (ROMD) – When 0, the DS3 overhead positions in the outgoing DS3 payload will be marked as overhead by RDEN. When 1, the DS3 overhead positions in the outgoing DS3 payload will be marked as data by RDEN. When this bit is set to one, the COVHD bit is ignored.

Bits 2 to 1: LOF Integration Period (LIP[1:0]) – These two bits determine the OOF integration period for declaring LOF.

00 = OOF is integrated for 3 ms before declaring LOF
01 = OOF is integrated for 2 ms before declaring LOF
10 = OOF is integrated for 1 ms before declaring LOF.
11 = LOF is declared at the same time as OOF.

Bit 0: Force Framer Resynchronization (FRSYNC) – A 0 to 1 transition forces an OOF, SEF, and OOMF condition. The bit must be cleared and set to one again to force another resynchronization Note: The OOMF condition is created by failing the most recent four data path M-bit checks.

Register Name: **T3.RSR1**
Register Description: **T3 Receive Status Register #1**
Register Address: **124h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	--	Reserved	T3FM	AIC	IDLE	RUA1

Bit #	7	6	5	4	3	2	1	0
Name	OOMF	SEF	--	LOF	RDI	AIS	OOF	LOS

Bit 11: T3 Framing Format Mismatch (T3FM) – This bit indicates the DS3 framer is programmed for a framing format (C-bit or M23) that is different than the format indicated by the AIC bit in the incoming DS3 signal.

Bit 10: Application Identification Channel (AIC) – This bit indicates the current state of the Application Identification Channel (AIC) from the C_{11} bit. A one indicates C-bit format and a zero indicates M23 format.

Bit 9: DS3 Idle Signal (IDLE) – When 0, the receive frame processor is not in a DS3 idle signal (Idle) condition. When 1, the receive frame processor is in an Idle condition.

Bit 8: Receive Unframed All 1's (RUA1) – When 0, the receive frame processor is not in a receive unframed all 1's (RUA1) condition. When 1, the receive frame processor is in an RUA1 condition.

Bit 7: Out Of MultiFrame (OOMF) – When 0, the receive frame processor is not in an out of multiframe (OOMF) condition. When 1, the receive frame processor is in an OOMF condition.

Bit 6: Severely Errored Frame (SEF) – When 0, the receive frame processor is not in a severely errored frame (SEF) condition. When 1, the receive frame processor is in an SEF condition.

Bit 4: Loss Of Frame (LOF) – When 0, the receive framer is not in a loss of frame (LOF) condition. When 1, the receive frame processor is in an LOF condition.

Bit 3: Remote Defect Indication (RDI) – This bit indicates the current state of the remote defect indication (RDI)
Bit 2: Alarm Indication Signal (AIS) – When 0, the receive frame processor is not in an alarm indication signal (AIS) condition. When 1, the receive frame processor is in an AIS condition.

Bit 1: Out Of Frame (OOF) – When 0, the receive framer is not in an out of frame (OOF) condition. When 1, the receive frame processor is in an OOF condition.

Bit 0: Loss Of Signal (LOS) – When 0, the receive framer is not in a loss of signal (LOS) condition. When 1, the receive framer is in an LOS condition.

Register Name: **T3.RSR2**
Register Description: **T3 Receive Status Register #2**
Register Address: **126h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	CPEC	FBEC	PEC	FEC

Bit 3: C-bit Parity Error Count (CPEC) – When 0, the C-bit parity error count is zero. When 1, the C-bit parity error count is one or more. This bit is set to zero in M23 DS3 mode.

Bit 2: Remote Error Indication Count (FBEC) – When 0, the remote error indication count is zero. When 1, the remote error indication count is one or more. This bit is set to zero in M23 DS3 mode.

Bit 1: P-bit Parity Error Count (PEC) – When 0, the P-bit parity error count is zero. When 1, the P-bit parity error count is one or more.

Bit 0: Framing Error Count (FEC) – When 0, the framing error count is zero. When 1, the framing error count is one or more. The type of framing error event counted is determined by T3.RCR.FECC[1:0]

Register Name: **T3.RSRL1**
Register Description: **T3 Receive Status Register Latched #1**
Register Address: **128h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	Reserved	Reserved	T3FML	AICL	IDLEL	RUA1L

Bit #	7	6	5	4	3	2	1	0
Name	OOMFL	SEFL	COFAL	LOFL	RAIL	AISL	OOFL	LOSL

Bit 11: T3 Framing Format Mismatch Latched (T3FML) – This bit is set when the T3FM bit transitions from zero to one.

Bit 10: Application Identification Channel Change Latched (AICL) – This bit is set when the AIC bit changes state.

Bit 9: DS3 Idle Signal Change Latched (IDLEL) – This bit is set when the IDLE bit changes state.

Bit 8: Receive Unframed All 1's Change Latched (RUA1L) – This bit is set when the RUA1 bit changes state.

Bit 7: Out Of MultiFrame Change Latched (OOMFL) – This bit is set when the OOMF bit changes state.

Bit 6: Severely Errored Frame Change Latched (SEFL) – This bit is set when the SEF bit changes state.

Bit 5: Change Of Frame Alignment Latched (COFAL) – This bit is set when the data path frame counters are updated with a new DS3 frame alignment that is different from the previous DS3 frame alignment.

Bit 4: Loss Of Frame Change Latched (LOFL) – This bit is set when the LOF bit changes state.

Bit 3: Remote Defect Indication Change Latched (RDIL) – This bit is set when the RDI bit changes state.

Bit 2: Alarm Indication Signal Change Latched (AISL) – This bit is set when the AIS bit changes state.

Bit 1: Out Of Frame Change Latched (OOFL) – This bit is set when the OOF bit changes state.

Bit 0: Loss Of Signal Change Latched (LOSL) – This bit is set when the LOS bit changes state.

Register Name: **T3.RSRL2**
Register Description: **T3 Receive Status Register Latched #2**
Register Address: **12Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	CPEL	FBEL	PEL	FEL

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	CPECL	FBECL	PECL	FECL

Bit 11: C-bit Parity Error Latched (CPEL) – This bit is set when a C-bit parity error is detected. This bit is set to zero in M23 DS3 mode.

Bit 10: Remote Error Indication Latched (FBEL) – This bit is set when a far-end block error is detected. This bit is set to zero in M23 DS3 mode.

Bit 9: P-bit Parity Error Latched (PEL) – This bit is set when a P-bit parity error is detected.

Bit 8: Framing Error Latched (FEL) – This bit is set when a framing error is detected. The type of framing error event that causes this bit to be set is determined by T3.RCR.FECC[1:0]

Bit 3: C-bit Parity Error Count Latched (CPECL) – This bit is set when the CPEC bit transitions from zero to one. This bit is set to zero in M23 DS3 mode.

Bit 2: Remote Error Indication Count Latched (FBECL) – This bit is set when the FBEC bit transitions from zero to one. This bit is set to zero in M23 DS3 mode.

Bit 1: P-bit Parity Error Count Latched (PECL) – This bit is set when the PEC bit transitions from zero to one.

Bit 0: Framing Error Count Latched (FECL) – This bit is set when the FEC bit transitions from zero to one.

Register Name: **T3.RSRIE1**
Register Description: **T3 Receive Status Register Interrupt Enable #1**
Register Address: **12Ch**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	Reserved	Reserved	T3FMIE	AICIE	IDLEIE	RUA1IE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	OOMFIE	SEFIE	COFAIE	LOFIE	RAIIE	AISIE	OOFIE	LOSIE
Default	0	0	0	0	0	0	0	0

Bit 11: T3 Framing Format Mismatch Interrupt Enable (T3FMIE) – This bit enables an interrupt if the T3FML bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 10: Application Identification Channel Interrupt Enable (AICIE) – This bit enables an interrupt if the AICL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 9: DS3 Idle Signal Change Interrupt Enable (IDLEIE) – This bit enables an interrupt if the IDLEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 8: Receive Unframed All 1's Interrupt Enable (RUA1IE) – This bit enables an interrupt if the RUA1L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 7: Out Of Multiframe Interrupt Enable (OOMFIE) – This bit enables an interrupt if the OOMFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 6: Severely Errored Frame Interrupt Enable (SEFIE) – This bit enables an interrupt if the SEFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 5: Change Of Frame Alignment Interrupt Enable (COFAIE) – This bit enables an interrupt if the COFAL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Loss Of Frame Interrupt Enable (LOFIE) – This bit enables an interrupt if the LOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Remote Defect Indication Interrupt Enable (RDIIE) – This bit enables an interrupt if the RDIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Alarm Indication Signal Interrupt Enable (AISIE) – This bit enables an interrupt if the AISL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Out Of Frame Interrupt Enable (OOFIE) – This bit enables an interrupt if the OOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Loss Of Signal Interrupt Enable (LOSIE) – This bit enables an interrupt if the LOSL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **T3.RSRIE2**
Register Description: **T3 Receive Status Register Interrupt Enable #2**
Register Address: **12Eh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	CPEIE	FBEIE	PEIE	FEIE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	CPECIE	FBECIE	PECIE	FECIE
Default	0	0	0	0	0	0	0	0

Bit 11: C-bit Parity Error Interrupt Enable (CPEIE) – This bit enables an interrupt if the CPEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 10: Remote Error Interrupt Enable (FBEIE) – This bit enables an interrupt if the FBEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 9: P-bit Parity Error Interrupt Enable (PEIE) – This bit enables an interrupt if the PEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 8: Framing Error Interrupt Enable (FEIE) – This bit enables an interrupt if the FEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: C-bit Parity Error Count Interrupt Enable (CPECIE) – This bit enables an interrupt if the CPECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Far-End Block Error Count Interrupt Enable (FBECIE) – This bit enables an interrupt if the FBECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: P-bit Parity Error Count Interrupt Enable (PECIE) – This bit enables an interrupt if the PECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Framing Error Count Interrupt Enable (FECIE) – This bit enables an interrupt if the FECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **T3.RFECR**
Register Description: **T3 Receive Framing Error Count Register**
Register Address: **134h**

Bit #	15	14	13	12	11	10	9	8
Name	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Framing Error Count (FE[15:0]) – These sixteen bits indicate the number of framing error events on the incoming **DS3** data stream. This register is updated via the PMU signal (see section 10.4.5)

Register Name: **T3.RPECR**
Register Description: **T3 Receive P-bit Parity Error Count Register**
Register Address: **136h**

Bit #	15	14	13	12	11	10	9	8
Name	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: P-bit Parity Error Count (PE[15:0]) – These sixteen bits indicate the number of P-bit parity errors detected on the incoming **DS3** data stream. This register is updated via the PMU signal (see section 10.4.5)

Register Name: **T3.RFBECR**
Register Description: **T3 Receive Far-End Block Error Count Register**
Register Address: **138h**

Bit #	15	14	13	12	11	10	9	8
Name	FBE15	FBE14	FBE13	FBE12	FBE11	FBE10	FBE9	FBE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	FBE7	FBE6	FBE5	FBE4	FBE3	FBE2	FBE1	FBE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Far-End Block Error Count (FBE[15:0]) – These sixteen bits indicate the number of far-end block errors detected on the incoming DS3 data stream. The associated counter will not increment in M23 DS3 mode. This register is updated via the PMU signal (see section 10.4.5)

Register Name: **T3.RCPECR**
Register Description: **T3 Receive C-bit Parity Error Count Register**
Register Address: **13Ah**

Bit #	15	14	13	12	11	10	9	8
Name	CPE15	CPE14	CPE13	CPE12	CPE11	CPE10	CPE9	CPE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	CPE7	CPE6	CPE5	CPE4	CPE3	CPE2	CPE1	CPE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: C-bit Parity Error Count (CPE[15:0]) – These sixteen bits indicate the number of C-bit parity errors detected on the incoming DS3 data stream. The associated counter will not increment in M23 DS3 mode. This register is updated via the PMU signal (see section 10.4.5)

12.9.3 Transmit G.751 E3

The transmit G.751 E3 utilizes two registers.

12.9.3.1 Register Map

Table 12-24. Transmit G.751 E3 Framer Register Map

Address	Register	Register Description
118h	E3G751.TCR	E3 G.751 Transmit Control Register
11Ah	E3G751.TEIR	E3 G.751 Transmit Error Insertion Register
11Ch	--	Reserved
11Eh	--	Reserved

12.9.3.2 Register Bit Descriptions

Register Name: **E3G751.TCR**
Register Description: **E3 G.751 Transmit Control Register**
Register Address: **118h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	--	--	Reserved	Reserved	Reserved	TNBC1	TNBC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	Reserved	Reserved	TABC1	TABC0	TFGD	TAIS
Default	0	0	0	0	0	0	0	0

Bits 9 to 8: Transmit N Bit Control (TNBC[1:0]) – These two bits control the source of the N bit.

00 = 1
01 = transmit data from HDLC controller.
10 = transmit data from FEAC controller.
11 = 0

Note: If TNBC[1:0] is 10 and TABC[1:0] is 01, both the N bit and A bit will carry the same transmit FEAC controller (one bit per frame period), however, the N bit and A bit in the same frame may or may not be equal.

Bits 3 to 2: Transmit A Bit Control (TABC[1:0]) – These two bits control the source of the A bit.

00 = automatically generated based upon received E3 alarms.
01 = transmit from the FEAC controller.
10 = 0
11 = 1

Note: If TABC[1:0] is 01 and TNBC[1:0] is 10, both the A bit and N bit will carry the same transmit FEAC controller (one bit per frame period), however, the A bit and N bit in the same frame may or may not be equal.

Bit 1: Transmit Frame Generation Disable (TFGD) –

0 = Transmit Frame Generation is enabled
1 = Transmit Frame Generation is disabled; E3 overhead positions in the incoming E3 payload will be passed through to error insertion. Note: The E3 overhead periods can still be overwritten by by error insertion, overhead insertion, or AIS generation.

Bit 0: Transmit Alarm Indication Signal (TAIS) – When 0, the normal signal is transmitted. When 1, the output E3 data stream is forced to all ones (AIS).

Register Name: **E3G751.TEIR**
Register Description: **E3 G.751 Transmit Error Insertion Register**
Register Address: **11Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	Reserved	Reserved	Reserved
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	Reserved	FEIC1	FEIC0	FEI	TSEI	MEIMS
Default	0	0	0	0	0	0	0	0

Bits 4 to 3: Framing Error Insert Control (FEIC[1:0]) – These two bits control the framing error event to be inserted.

00 = single bit error in one frame.
01 = word error in one frame.
10 = single bit error in four consecutive frames.
11 = word error in four consecutive frames.

Bit 2: Framing Error Insertion Enable (FEI) – When 0, framing error insertion is disabled. When 1, framing error insertion is enabled.

Bit 1: Transmit Single Error Insert (TSEI) – This bit causes an error of the enabled type(s) to be inserted in the transmit data stream if manual error insertion is disabled (MEIMS = 0). A 0 to 1 transition causes a single error to be inserted. For a second error to be inserted, this bit must be set to 0, and back to 1. Note: If MEIMS is low, and this bit transitions more than once between error insertion opportunities, only one error will be inserted.

Bit 0: Manual Error Insert Mode Select (MEIMS) – When 0, error insertion is initiated by the TSEI register bit. When 1, error insertion is initiated by the transmit manual error insertion signal (TMEI). Note: If TMEI or TSEI is one, changing the state of this bit may cause an error to be inserted.

12.9.4 Receive G.751 E3 Register Map

The receive G.751 E3 utilizes eight registers.

Table 12-25. Receive G.751 E3 Framer Register Map

Address	Register	Register Description
120h	E3G751.RCR	E3 G.751 Receive Control Register
122h	--	Reserved
124h	E3G751.RSR1	E3 G.751 Receive Status Register #1
126h	E3G751.RSR2	E3 G.751 Receive Status Register #2
128h	E3G751.RSRL1	E3 G.751 Receive Status Register Latched #1
12Ah	E3G751.RSRL2	E3 G.751 Receive Status Register Latched #2
12Ch	E3G751.RSRIE1	E3 G.751 Receive Status Register Interrupt Enable #1
12Eh	E3G751.RSRIE2	E3 G.751 Receive Status Register Interrupt Enable #2
130h	--	Reserved
132h	--	Reserved
134h	E3G751.RFECR	E3 G.751 Receive Framing Error Count Register
136h	--	Reserved
138h	--	Reserved
13Ah	--	Reserved
13Ch	--	Unused
13Eh	--	Unused

12.9.4.1 Register Bit Descriptions

Register Name: **E3G751.RCR**
Register Description: **E3 G.751 Receive Control Register**
Register Address: **120h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	DLS	MDAISI	AAISD	ECC	FECC1	FECC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RAILE	RAILD	RAIOD	RAIAD	ROMD	LIP1	LIP0	FRSYNC
Default	0	0	0	0	0	0	0	0

Bit 13: Receive FEAC Data Link Source (DLS) – When 0, the receive FEAC controller will be sourced from the N bit. When 1, the receive FEAC controller will be sourced from the A bit.

Bit 12: Manual Downstream AIS Insertion (MDAISI) – When 0, manual downstream AIS insertion is disabled. When 1, manual downstream AIS insertion is enabled.

Bit 11: Automatic Downstream AIS Disable (AAISD) – When 0, the presence of an LOS, OOF, or AIS condition will cause downstream AIS to be inserted. When 1, the presence of an LOS, OOF, or AIS condition will not cause downstream AIS to be inserted.

Bit 10: Error Count Control (ECC) – When 0, framing errors will not be counted if an OOF or AIS condition is present. When 1, framing errors will be counted regardless of the presence of an OOF or AIS condition.

Bits 9 to 8: Framing Error Count Control (FECC[1:0]) – These two bits control the type of framing error events that are counted.

00 = count OOF occurrences (counted regardless of the setting of the ECC bit)..
01 = count each bit error in the FAS (up to 10 per frame).
10 = count frame alignment signal (FAS) errors (up to one per frame).
11 = reserved

Bit 7: Receive Alarm Indication on LOF Enable (RAILE) – When 0, an LOF condition does not affect the receive alarm indication signal (RAI). When 1, an LOF condition will cause the transmit E3 A bit to be set to one if transmit automatic RAI is enabled.

Bit 6: Receive Alarm Indication on LOS Disable (RAILD) – When 0, an LOS condition will cause the transmit E3 A bit to be set to one if transmit automatic RAI is enabled. When 1, an LOS condition does not affect the RAI signal.

Bit 5: Receive Alarm Indication on OOF Disable (RAIOD) – When 0, an OOF condition will cause the transmit E3 A bit to be set to one if transmit automatic RAI is enabled. When 1, an OOF condition does not affect the RAI signal.

Bit 4: Receive Alarm Indication on AIS Disable (RAIAD) – When 0, an AIS condition will cause the transmit E3 A bit to be set to one if transmit automatic RAI is enabled. When 1, an AIS condition does not affect the RAI signal.

Bit 3: Receive Overhead Masking Disable (ROMD) – When 0, the E3 overhead positions in the outgoing E3 payload will be marked as overhead by RDEN. When 1, the E3 overhead positions in the outgoing E3 payload will be marked as data by RDEN.

Bits 2 to 1: LOF Integration Period (LIP[1:0]) – These two bits determine the OOF integration period for declaring LOF.

00 = OOF is integrated for 3 ms before declaring LOF
01 = OOF is integrated for 2 ms before declaring LOF.
10 = OOF is integrated for 1 ms before declaring LOF
11 = LOF is declared at the same time as OOF

Bit 0: Force Framer Resynchronization (FRSYNC) – A 0 to 1 transition forces an OOF condition at the FAS check. This bit must be cleared and set to one again to force another resynchronization. Note: The OOF condition is created by failing the most recent four data path FAS checks.

Register Name: **E3G751.RSR1**
Register Description: **E3 G.751 Receive Status Register #1**
Register Address: **124h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	--	Reserved	Reserved	Reserved	Reserved	RUA1

Bit #	7	6	5	4	3	2	1	0
Name	RAB	RNB	--	LOF	RDI	AIS	OOF	LOS

Bit 8: Receive Unframed All 1's (RUA1) – When 0, the receive frame processor is not in a receive unframed all 1's (RUA1) condition. When 1, the receive frame processor is in an RUA1 condition.

Bit 7: Receive A Bit (RAB) – This bit is the integrated A bit extracted from the E3 frame.

Bit 6: Receive N Bit (RNB) – This bit is the integrated N bit extracted from the E3 frame.

Bit 4: Loss Of Frame (LOF) – When 0, the receive frame processor is not in a loss of frame (LOF) condition. When 1, the receive frame processor is in an LOF condition.

Bit 3: Remote Alarm Indication (RDI) – This bit indicates the current state of the remote alarm indication (RDI).

Bit 2: Alarm Indication Signal (AIS) – When 0, the receive frame processor is not in an alarm indication signal (AIS) condition. When 1, the receive frame processor is in an AIS condition.

Bit 1: Out Of Frame (OOF) – When 0, the receive frame processor is not in an out of frame (OOF) condition. When 1, the receive frame processor is in an OOF condition.

Bit 0: Loss Of Signal (LOS) – When 0, the receive loss of signal (LOS) input (RLOS) is low. When 1, RLOS is high.

Register Name: **E3G751.RSR2**
Register Description: **E3 G.751 Receive Status Register #2**
Register Address: **126h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	Reserved	Reserved	Reserved	FEC

Bit 0: Framing Error Count (FEC) – When 0, the framing error count is zero. When 1, the framing error count is one or more.

Register Name: **E3G751.RSRL1**
Register Description: **E3 G.751 Receive Status Register Latched #1**
Register Address: **128h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RUA1L

Bit #	7	6	5	4	3	2	1	0
Name	ACL	NCL	COFAL	LOFL	RDIL	AISL	OOFL	LOSL

Bit 8: Receive Unframed All 1's Change Latched (RUA1L) – This bit is set when the RUA1 bit changes state.

Bit 7: A Bit Change Latched (ACL) – This bit is set when the RAB bit changes state.

Bit 6: N Bit Change Latched (NCL) – This bit is set when the RNB bit changes state.

Bit 5: Change Of Frame Alignment Latched (COFAL) – This bit is set when the data path frame counters are updated with a new frame alignment that is different from the previous frame alignment.

Bit 4: Loss Of Frame Change Latched (LOFL) – This bit is set when the LOF bit changes state.

Bit 3: Remote Alarm Indication Change Latched (RDIL) – This bit is set when the RDI bit changes state.

Bit 2: Alarm Indication Signal Change Latched (AISL) – This bit is set when the AIS bit changes state.

Bit 1: Out Of Frame Change Latched (OOFL) – This bit is set when the OOF bit changes state.

Bit 0: Loss Of Signal Change Latched (LOSL) – This bit is set when the LOS bit changes state.

Register Name: **E3G751.RSRL2**
Register Description: **E3 G.751 Receive Status Register Latched #2**
Register Address: **12Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	Reserved	Reserved	FEL

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	Reserved	Reserved	Reserved	FECL

Bit 8: Framing Error Latched (FEL) – This bit is set when a framing error is detected.

Bit 0: Framing Error Count Latched (FECL) – This bit is set when the FEC bit transitions from zero to one.

Register Name: **E3G751.RSRIE1**
Register Description: **E3 G.751 Receive Status Register Interrupt Enable #1**
Register Address: **12Ch**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	RUA1IE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	ACIE	NCIE	COFAIE	LOFIE	RDIIE	AISIE	OOFIE	LOSIE
Default	0	0	0	0	0	0	0	0

Bit 8: Receive Unframed All 1's Interrupt Enable (RUA1IE) – This bit enables an interrupt if the RUA1L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 7: A Bit Change Interrupt Enable (ACIE) – This bit enables an interrupt if the ACL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 6: N Bit Change Interrupt Enable (NCIE) – This bit enables an interrupt if the NCL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 5: Change Of Frame Alignment Interrupt Enable (COFAIE) – This bit enables an interrupt if the COFAL bit and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set. set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Loss Of Frame Interrupt Enable (LOFIE) – This bit enables an interrupt if the LOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Remote Alarm Indication Interrupt Enable (RDIIE) – This bit enables an interrupt if the RDIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Alarm Indication Signal Interrupt Enable (AISIE) – This bit enables an interrupt if the AISL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Out Of Frame Interrupt Enable (OOFIE) – This bit enables an interrupt if the OOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Loss Of Signal Interrupt Enable (LOSIE) – This bit enables an interrupt if the LOSL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **E3G751.RSRIE2**
Register Description: **E3 G.751 Receive Status Register Interrupt Enable #2**
Register Address: **12Eh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	Reserved	Reserved	FEIE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	Reserved	Reserved	Reserved	FECIE
Default	0	0	0	0	0	0	0	0

Bit 8: Framing Error Interrupt Enable (FEIE) – This bit enables an interrupt if the FEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Framing Error Count Interrupt Enable (FECIE) – This bit enables an interrupt if the FECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **E3G751.RFECR**
Register Description: **E3 G.751 Receive Framing Error Count Register**
Register Address: **134h**

Bit #	15	14	13	12	11	10	9	8
Name	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Framing Error Count (FE[15:0]) – These sixteen bits indicate the number of framing error events on the incoming E3 data stream. This register is updated via the PMU signal (see section 10.4.5)

12.9.5 Transmit G.832 E3 Register Map

The transmit G.832 E3 utilizes four registers.

Table 12-26. Transmit G.832 E3 Framer Register Map

Address	Register	Register Description
118h	E3G832.TCR	E3 G.832 Transmit Control Register
11Ah	E3G832.TEIR	E3 G.832 Transmit Error Insertion Register
11Ch	E3G832.TMABR	E3 G.832 Transmit MA Byte Register
11Eh	E3G832.TNGBR	E3 G.832 Transmit NR and GC Byte Register

12.9.5.1 Register Bit Descriptions

Register Name: **E3G832.TCR**
Register Description: **E3 G.832 Transmit Control Register**
Register Address: **118h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	--	--	Reserved	Reserved	TGCC	TNRC1	TNRC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	TFEBE	AFEBED	TRDI	ARDID	TFGD	TAIS
Default	0	0	0	0	0	0	0	0

Bit 10: Transmit GC Byte Control (TGCC) – When 0, the GC byte is inserted from the transmit HDLC controller . When 1, the GC byte is inserted from the GC byte register.

Note: If bit TGCC is 0 and TNRC[1:0] is 01, both the GC byte and NR byte will carry the same transmit HDLC controller (eight bits per frame period), however, the GC byte and NR byte in the same frame may or may not be equal.

Bits 9 to 8: Transmit NR Byte Control (TNRC[1:0]) – These two bits control the source of the NR byte.

00 = all ones.
01 = transmit from the HDLC controller.
10 = transmit from the FEAC controller.
11 = NR byte register.

Note: If TNRC[1:0] is 01 and TGCC is 0, both the NR byte and GC byte will carry the same transmit HDLC controller (eight bits per frame period), however, the NR byte and GC byte in the same frame may or may not be equal.

Bit 5: Transmit REI Error (TFEBE) – When automatic REI generation is defeated (AFEBED = 1), this bit is inserted into the second bit of the MA byte.

Bit 4: Automatic REI Defeat (AFEBED) – When 0, the REI is automatically generated based upon the transmit remote error indication (TREI) signal. When 1, the REI is inserted from the register bit TFEBE.

Bit 3: Transmit RDI Alarm (TRDI) – When automatic RDI generation is defeated (ARDID = 1), this bit is inserted into the first bit of the MA byte.

Bit 2: Automatic RDI Defeat (ARDID) – When 0, the RDI is automatically generated based upon the received E3 alarms. When 1, the RDI is inserted from the register bit TRDI.

Bit 1: Transmit Frame Generation Disabled (TFGD) –

0 = Transmit Frame Generation is enabled

1 = Transmit Frame Generation is disabled; E3 overhead positions in the incoming E3 payload will be passed through to error insertion. Note: The E3 overhead periods can still be overwritten by by error insertion, overhead insertion, or AIS generation.

Bit 0: Transmit Alarm Indication Signal (TAIS) – When 0, the normal signal is transmitted. When 1, the E3 output data stream is forced to all ones (AIS).

Register Name: **E3G832.TEIR**
Register Description: **E3 G.832 Transmit Error Insertion Register**
Register Address: **11Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	Reserved	CFBEIE	FBEI
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	PBEE	CPEIE	PEI	FEIC1	FEIC0	FEI	TSEI	MEIMS
Default	0	0	0	0	0	0	0	0

Bit 9: Continuous Remote Error Indication Error Insertion Enable (CFBEIE) – When 0, single remote error indication (REI) error insertion is enabled. When 1, continuous REI error insertion is enabled, and REI errors will be transmitted continuously if FBEI is high.

Bit 8: Remote Error Indication Error Insertion Enable (FBEI) – When 0, REI error insertion is disabled. When 1, REI error insertion is enabled.

Bit 7: Parity Block Error Enable (PBEE) – When 0, a parity error is generated by inverting a single bit in the EM byte. When 1, a parity error is generated by inverting all eight bits in the EM byte.

Bit 6: Continuous Parity Error Insertion Enable (CPEIE) – When 0, single parity (BIP-8) error insertion is enabled. When 1, continuous parity error insertion is enabled, and parity errors will be transmitted continuously if PEI is high.

Bit 5: Parity Error Insertion Enable (PEI) – When 0, parity error insertion is disabled. When 1, parity error insertion is enabled.

Bits 4 to 3: Framing Error Control (FEIC[1:0]) – These two bits control the framing error event to be inserted.

00 = single bit error in one frame.
01 = word error in one frame.
10 = single bit error in four consecutive frames.
11 = word error in four consecutive frames.

Bit 2: Framing Error Insertion Enable (FEI) – When 0, framing error insertion is disabled. When 1, framing error insertion is enabled.

Bit 1: Transmit Single Error Insert (TSEI) – This bit causes an error of the enabled type(s) to be inserted in the transmit data stream if manual error insertion is disabled (MEIMS = 0). A 0 to 1 transition causes a single error to be inserted. For a second error to be inserted, this bit must be set to 0, and back to 1. Note: If MEIMS is low, and this bit transitions more than once between error insertion opportunities, only one error will be inserted.

Bit 0: Manual Error Insert Mode Select (MEIMS) – When 0, error insertion is initiated by the TSEI register bit. When 1, error insertion is initiated by the transmit manual error insertion signal (TMEI). Note: If TMEI or TSEI is one, changing the state of this bit may cause an error to be inserted.

Register Name: **E3G832.TMABR**
Register Description: **E3 G.832 Transmit MA Byte Register**
Register Address: **11Ch**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TPT2	TPT1	TPT0	TTIGD	TTI3	TTI2	TTI1	TTI0
Default	0	0	0	0	0	0	0	0

Bits 7 to 5: Transmit Payload Type (TPT[2:0]) – These bits determines the value transmitted in the payload type (third, fourth, and fifth bits in the MA byte).

Bit 4: Transmit Timing Source Indicator Bit Generation Disable (TTIGD) – When 0, the last three bits of the MA byte (MA[6:8]) are generated from the four timing source indicator bits TTI[3:0]. When 1, TTI[3] is ignored and TTI[2:0] are directly inserted into the last three bits of the MA byte.

Bits 3 to 0: Transmit Timing Source Indication (TTI[3:0]) – These four bits make up the timing source indicator bits.

Register Name: **E3G832.TNGBR**
Register Description: **E3 G.832 Transmit NR and GC Byte Register**
Register Address: **11Eh**

Bit #	15	14	13	12	11	10	9	8
Name	TGC7	TGC6	TGC5	TGC4	TGC3	TGC2	TGC1	TGC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	TNR7	TNR6	TNR5	TNR4	TNR3	TNR2	TNR1	TNR0
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Transmit GC Byte (TGC[7:0]) – These eight bits are the GC byte to be inserted into the E3 frame.

Bits 7 to 0: Transmit NR Byte (TNR[7:0]) – These eight bits are the NR byte to be inserted into the E3 frame.

12.9.6 Receive G.832 E3 Register Map

The receive G.832 E3 utilizes thirteen registers.

Table 12-27. Receive G.832 E3 Framer Register Map

Address	Register	Register Description
120h	E3G832.RCR	E3 G.832 Receive Control Register
122h	E3G832.RMACR	E3 G.832 Receive MA Byte Control Register
124h	E3G832.RSR1	E3 G.832 Receive Status Register #1
126h	E3G832.RSR2	E3 G.832 Receive Status Register #2
128h	E3G832.RSRL1	E3 G.832 Receive Status Register Latched #1
12Ah	E3G832.RSRL2	E3 G.832 Receive Status Register Latched #2
12Ch	E3G832.RSRIE1	E3 G.832 Receive Status Register Interrupt Enable #1
12Eh	E3G832.RSRIE2	E3 G.832 Receive Status Register Interrupt Enable #2
130h	E3G832.RMABR	E3 G.832 Receive MA Byte Register
132h	E3G832.RNGBR	E3 G.832 Receive NR and GC Byte Register
134h	E3G832.RFECR	E3 G.832 Receive Framing Error Count Register
136h	E3G832.RPECR	E3 G.832 Receive Parity Error Count Register
138h	E3G832.RFBER	E3 G.832 Receive Remote Error Indication Count Register
13Ah	--	Reserved
13Ch	--	Unused
13Eh	--	Unused

12.9.6.1 Register Bit Descriptions

Register Name: **E3G832.RCR**
Register Description: **E3 G.832 Receive Control Register**
Register Address: **120h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	PEC	DLS	MDAISI	AAISD	ECC	FECC1	FECC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RAILE	RAILD	RAIOD	RAIAD	ROMD	LIP1	LIP0	FRSYNC
Default	0	0	0	0	0	0	0	0

Bit 14: Parity Error Count (PEC) – When 0, BIP-8 block errors (EM byte) are detected (no more than one per frame). When 1, BIP-8-bit errors are detected (up to 8 per frame).

Bit 13: Receive HDLC Data Link Source (DLS) – When 0, the receive HDLC data link will be sourced from the GC byte. When 1, the receive HDLC data link will be sourced from the NR byte.

Bit 12: Manual Downstream AIS Insertion (MDAISI) – When 0, manual downstream AIS insertion is disabled. When 1, manual downstream AIS insertion is enabled.

Bit 11: Automatic Downstream AIS Disable (AAISD) – When 0, the presence of an LOS, OOF, or AIS condition will cause downstream AIS to be inserted. When 1, the presence of an LOS, OOF, or AIS condition will not cause downstream AIS to be inserted.

Bit 10: Error Count Control (ECC) – When 0, framing errors, parity errors, and REI errors will not be counted if an OOF or AIS condition is present. Parity errors and REI errors will also not be counted during the E3 frame in which an OOF or AIS condition is terminated, and the next E3 frame. When 1, framing errors, parity errors, and REI errors will be counted regardless of the presence of an OOF or AIS condition.

Bits 9 to 8: Framing Error Count Control (FECC[1:0]) – These two bits control the type of framing error events that are counted.

00 = count OOF occurrences (counted regardless of the setting of the ECC bit)..
01 = count each bit error in FA1 and FA2 (up to 16 per frame).
10 = count frame alignment word (FA1 and FA2) errors (up to one per frame).
11 = count FA1 byte errors and FA2 byte errors (up to 2 per frame).

Bit 7: Receive Alarm Indication on LOF Enable (RAILE) – When 0, an LOF condition does not affect the receive alarm indication signal (RAI). When 1, an LOF condition will cause the transmit E3 RDI bit to be set to one if transmit automatic RDI is enabled.

Bit 6: Receive Alarm Indication on LOS Disable (RAILD) – When 0, an LOS condition will cause the transmit E3 RDI bit to be set to one if transmit automatic RDI is enabled. When 1, an LOS condition does not affect the RAI signal.

Bit 5: Receive Alarm Indication on OOF Disable (RAIOD) – When 0, an OOF condition will cause the transmit E3 RDI bit to be set to one if transmit automatic RDI is enabled. When 1, an OOF condition does not affect the RAI signal.

Bit 4: Receive Alarm Indication on AIS Disable (RAIAD) – When 0, an AIS condition will cause the transmit E3 RDI bit to be set to one if transmit automatic RDI is enabled. When 1, an AIS condition does not affect the RAI signal.

Bit 3: Receive Overhead Masking Disable (ROMD) – When 0, the E3 overhead positions in the outgoing E3 payload will be marked as overhead by RDEN. When 1, the E3 overhead positions in the outgoing E3 payload will be marked as data by RDEN.

Bits 2 to 1: LOF Integration Period (LIP[1:0]) – These two bits determine the OOF integration period for declaring LOF.

00 = OOF is integrated for 3 ms before declaring LOF.
01 = OOF is integrated for 2 ms before declaring LOF.
10 = OOF is integrated for 1 ms before declaring LOF.
11 = LOF is declared at the same time as OOF.

Bit 0: Force Framer Resynchronization (FRSYNC) – A 0 to 1 transition forces. an OOF condition at the next framing word check. This bit must be cleared and set to one again to force another resynchronization. Note: The OOF condition is created by failing the most recent four data path frame alignment word checks.

Register Name: **E3G832.RMACR**
Register Description: **E3 G.832 Receive MA Byte Control Register**
Register Address: **122h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	EPT2	EPT1	EPT0	TIED
Default	0	0	0	0	0	0	0	0

Bits 3 to 1: Expected Payload Type (EPT[2:0]) – These three bits contain the expected value of the payload type.

Bit 0: Timing Source Indicator Bit Extraction Disable (TIED) – When 0, the four timing source indications bits are extracted from the last three bits of the MA byte (MA[6:8]), and stored in a register. When 1, timing source indicator bit extraction is disabled, and the last three bits of the MA byte are integrated and stored in a register.

Register Name: **E3G832.RSR1**
Register Description: **E3 G.832 Receive Status Register #1**
Register Address: **124h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	--	--	RPTU	RPTM	Reserved	Reserved	RUA1

Bit #	7	6	5	4	3	2	1	0
Name	Reserved	Reserved	--	LOF	RAI	AIS	OOF	LOS

Bit 12: Receive Payload Type Unstable (RPTU) – When 0, the receive payload type is stable. When 1, the receive payload type is unstable.

Bit 11: Receive Payload Type Mismatch (RPTM) – When 0, the receive payload type and expected payload type match. When 1, the receive payload type and expected payload type do not match.

Bit 8: Receive Unframed All 1's (RUA1) – When 0, the receive frame processor is not in a receive unframed all 1's (RUA1) condition. When 1, the receive frame processor is in an RUA1 condition.

Bit 4: Loss Of Frame (LOF) – When 0, the receive frame processor is not in a loss of frame (LOF) condition. When 1, the receive frame processor is in an LOF condition.

Bit 3: Remote Defect Indication (RDI) – This bit indicates the current state of the remote defect indication (RDI).

Bit 2: Alarm Indication Signal (AIS) – When 0, the receive frame processor is not in an alarm indication signal (AIS) condition. When 1, the receive frame processor is in an AIS condition.

Bit 1: Out Of Frame (OOF) – When 0, the receive frame processor is not in an out of frame (OOF) condition. When 1, the receive frame processor is in an OOF condition.

Bit 0: Loss Of Signal (LOS) – When 0, the receive loss of signal (LOS) input (RLOS) is low. When 1, RLOS is high.

Register Name: **E3G832.RSR2**
Register Description: **E3 G.832 Receive Status Register #2**
Register Address: **126h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	Reserved	FBEC	PEC	FEC

Bit 2: Remote Error Indication Count (FBEC) – When 0, the remote error indication count is zero. When 1, the remote error indication count is one or more.

Bit 1: Parity Error Count (PEC) – When 0, the parity error count is zero. When 1, the parity error count is one or more.

Bit 0: Framing Error Count (FEC) – When 0, the framing error count is zero. When 1, the framing error count is one or more.

Register Name: **E3G832.RSRL1**
Register Description: **E3 G.832 Receive Status Register Latched #1**
Register Address: **128h**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	--	TIL	RPTUL	RPTML	RPTL	Reserved	RUA1L

Bit #	7	6	5	4	3	2	1	0
Name	GCL	NRL	COFAL	LOFL	RDIL	AISL	OOFL	LOSL

Bit 13: Timing Source Indication Change Latched (TIL) – This bit is set when the TI[3:0] bits change state.

Bit 12: Receive Payload Type Unstable Latched (RPTUL) – This bit is set when the RPTU bit transitions from zero to one.

Bit 11: Receive Payload Type Mismatch Latched (RPTML) – This bit is set when the RPTM bit transitions from zero to one.

Bit 10: Receive Payload Type Change Latched (RPTL) – This bit is set when the RPT[2:0] bits change state.

Bit 8: Receive Unframed All 1's Change Latched (RUA1L) – This bit is set when the RUA1 bit changes state.

Bit 7: GC Byte Change Latched (GCL) – This bit is set when the RGC byte changes state.

Bit 6: NR Byte Change Latched (NRL) – This bit is set when the RNR byte changes state.

Bit 5: Change Of Frame Alignment Latched (COFAL) – This bit is set when the data path frame counters are updated with a new frame alignment that is different from the previous frame alignment.

Bit 4: Loss Of Frame Change Latched (LOFL) – This bit is set when the LOF bit changes state.

Bit 3: Remote Defect Indication Change Latched (RDIL) – This bit is set when the RDI bit changes state.

Bit 2: Alarm Indication Signal Change Latched (AISL) – This bit is set when the AIS bit changes state.

Bit 1: Out Of Frame Change Latched (OOFL) – This bit is set when the OOF bit changes state.

Bit 0: Loss Of Signal Change Latched (LOSL) – This bit is set when the LOS bit changes state.

Register Name: **E3G832.RSRL2**
Register Description: **E3 G.832 Receive Status Register Latched #2**
Register Address: **12Ah**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	FBEL	PEL	FEL

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	Reserved	FBECL	PECL	FECL

Bit 10: Remote Error Indication Latched (FBEL) – This bit is set when a remote error indication is detected.

Bit 9: Parity Error Latched (PEL) – This bit is set when a BIP-8 parity error is detected.

Bit 8: Framing Error Latched (FEL) – This bit is set when a framing error is detected.

Bit 2: Remote Error Indication Count Latched (FBECL) – This bit is set when the FBEC bit transitions from zero to one.

Bit 1: Parity Error Count Latched (PECL) – This bit is set when the PEC bit transitions from zero to one.

Bit 0: Framing Error Count Latched (FECL) – This bit is set when the FEC bit transitions from zero to one.

Register Name: **E3G832.RSRIE1**
Register Description: **E3 G.832 Receive Status Register Interrupt Enable #1**
Register Address: **12Ch**

Bit #	15	14	13	12	11	10	9	8
Name	Reserved	--	TIIE	RPTUIE	RPTMIE	RPTIE	Reserved	RUA1IE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	GCIE	NRIE	COFAIE	LOFIE	RAIIE	AISIE	OOFIE	LOSIE
Default	0	0	0	0	0	0	0	0

Bit 13: Timing Indication Interrupt Enable (TIIE) – This bit enables an interrupt if the TIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 12: Receive Payload Type Unstable Interrupt Enable (RPTUIE) – This bit enables an interrupt if the RPTUL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 11: Receive Payload Type Mismatch Interrupt Enable (RPTMIE) – This bit enables an interrupt if the RPTML bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 10: Receive Payload Type Interrupt Enable (RPTIE) – This bit enables an interrupt if the RPTL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 8: Receive Unframed All 1's Interrupt Enable (RUA1IE) – This bit enables an interrupt if the RUA1L bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 7: GC Byte Interrupt Enable (GCIE) – This bit enables an interrupt if the GCL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 6: NR Byte Interrupt Enable (NRIE) – This bit enables an interrupt if the NRL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 5: Change Of Frame Alignment Interrupt Enable (COFAIE) – This bit enables an interrupt if the COFAL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 4: Loss Of Frame Interrupt Enable (LOFIE) – This bit enables an interrupt if the LOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 3: Remote Defect Indication Interrupt Enable (RDIIE) – This bit enables an interrupt if the RDIL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Alarm Indication Signal Interrupt Enable (AISIE) – This bit enables an interrupt if the AISL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Out Of Frame Interrupt Enable (OOFIE) – This bit enables an interrupt if the OOFL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Loss Of Signal Interrupt Enable (LOSIE) – This bit enables an interrupt if the LOSL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **E3G832.RSRIE2**
Register Description: **E3 G.832 Receive Status Register Interrupt Enable #2**
Register Address: **12Eh**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	Reserved	FBEIE	PEIE	FEIE
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	--	--	--	Reserved	FBECIE	PECIE	FECIE
Default	0	0	0	0	0	0	0	0

Bit 10: Remote Error Indication Interrupt Enable (FBEIE) – This bit enables an interrupt if the FBEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 9: Parity Error Interrupt Enable (PEIE) – This bit enables an interrupt if the PEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 8: Framing Error Interrupt Enable (FEIE) – This bit enables an interrupt if the FEL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 2: Remote Error Indication Count Interrupt Enable (FBECIE) – This bit enables an interrupt if the FBECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 1: Parity Error Count Interrupt Enable (PECIE) – This bit enables an interrupt if the PECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Bit 0: Framing Error Count Interrupt Enable (FECIE) – This bit enables an interrupt if the FECL bit is set and the bit in GL.ISRIE.PSRIE[4:1] that corresponds to this port is set.

0 = interrupt disabled
1 = interrupt enabled

Register Name: **E3G832.RMABR**
Register Description: **E3 G.832 Receive MA Byte Register**
Register Address: **130h**

Bit #	15	14	13	12	11	10	9	8
Name	--	--	--	--	--	--	--	--
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	--	RPT2	RPT1	RPT0	TI3	TI2	TI1	TI0
Default	0	0	0	0	0	0	0	0

Bits 6 to 4: Receive Payload Type (RPT[2:0]) – These three bits are the integrated version of the payload type (MA[3:5]) from the MA byte.

Bits 3 to 0: Receive Timing Source Indication (TI[3:0]) – When timing source indicator extraction is enabled, these four bits are the integrated version of the four timing source indicator bits extracted from the last three bits of the MA byte (MA[6:8]). When timing source indicator bit extraction is disabled, TI[3] is zero, and TI[2:0] contain the integrated version of the last three bits of the MA byte.

Register Name: **E3G832.RNGBR**
Register Description: **E3 G.832 Receive NR and GC Byte Register**
Register Address: **132h**

Bit #	15	14	13	12	11	10	9	8
Name	RGC7	RGC6	RGC5	RGC4	RGC3	RGC2	RGC1	RGC0
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	RNR7	RNR6	RNR5	RNR4	RNR3	RNR2	RNR1	RNR0
Default	0	0	0	0	0	0	0	0

Bits 15 to 8: Receive GC Byte (RGC[7:0]) – These eight bits are the integrated version of the GC byte as extracted from the E3 frame.

Bits 7 to 0: Receive NR Byte (RNR[7:0]) – These eight bits are the integrated version of the NR byte as extracted from the E3 frame.

Register Name: **E3G832.RFECR**
Register Description: **E3 G.832 Receive Framing Error Count Register**
Register Address: **134h**

Bit #	15	14	13	12	11	10	9	8
Name	FE15	FE14	FE13	FE12	FE11	FE10	FE9	FE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	FE7	FE6	FE5	FE4	FE3	FE2	FE1	FE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Framing Error Count (FE[15:0]) – These sixteen bits indicate the number of framing error events on the incoming E3 data stream. This register is updated via the PMU signal (see section 10.4.5)

Register Name: **E3G832.RPECR**
Register Description: **E3 G.832 Receive Parity Error Count Register**
Register Address: **136h**

Bit #	15	14	13	12	11	10	9	8
Name	PE15	PE14	PE13	PE12	PE11	PE10	PE9	PE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	PE7	PE6	PE5	PE4	PE3	PE2	PE1	PE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Parity Error Count (PE[15:0]) – These sixteen bits indicate the number of parity (BIP-8) errors detected on the incoming E3 data stream. This register is updated via the PMU signal (see section 10.4.5)

Register Name: **E3G832.RFBER**
Register Description: **E3 G.832 Receive Remote Error Indication Count Register**
Register Address: **138h**

Bit #	15	14	13	12	11	10	9	8
Name	FBE15	FBE14	FBE13	FBE12	FBE11	FBE10	FBE9	FBE8
Default	0	0	0	0	0	0	0	0

Bit #	7	6	5	4	3	2	1	0
Name	FBE7	FBE6	FBE5	FBE4	FBE3	FBE2	FBE1	FBE0
Default	0	0	0	0	0	0	0	0

Bits 15 to 0: Remote Error Indication Count (FBE[15:0]) – These sixteen bits indicate the number of remote error indications detected on the incoming E3 data stream. This register is updated via the PMU signal (see section 10.4.5)

13 JTAG INFORMATION

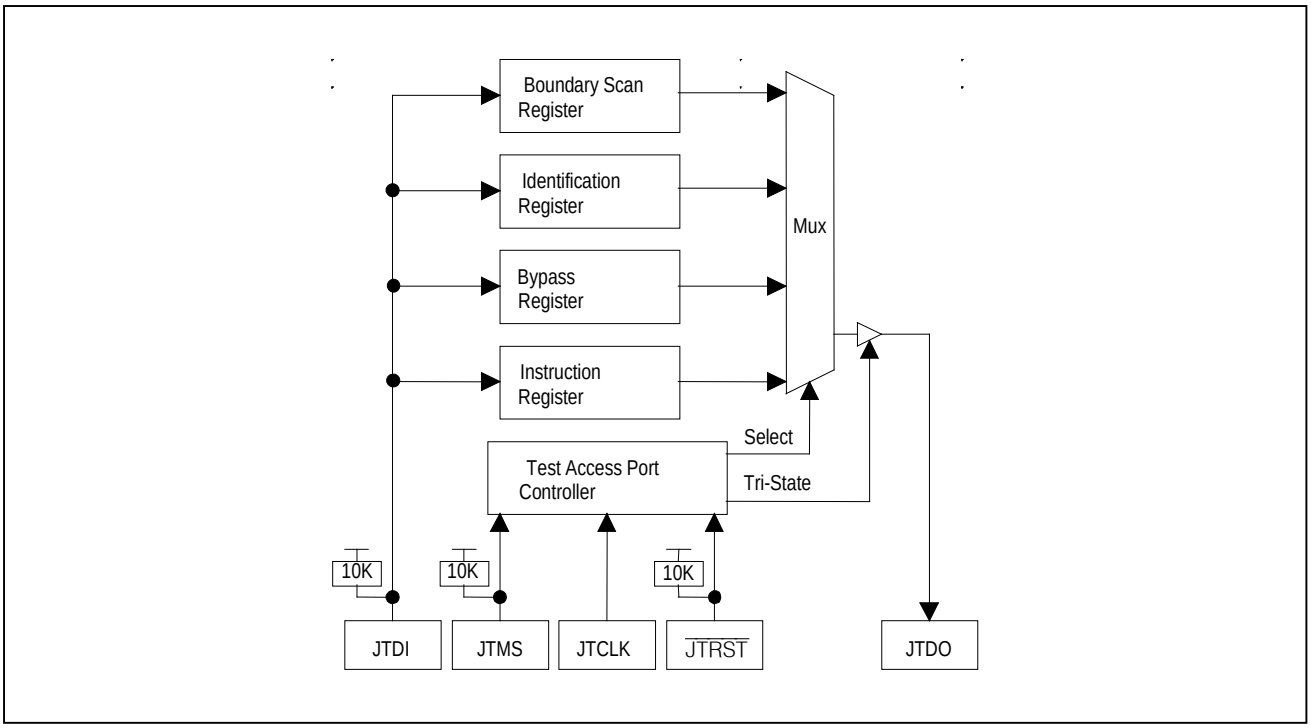
13.1 JTAG Description

This device supports the standard instruction codes SAMPLE/PRELOAD, BYPASS, and EXTEST. Optional public instructions included are HIGHZ, CLAMP, and IDCODE. The device contains the following items, which meet the requirements set by the IEEE 1149.1 Standard Test Access Port (TAP) and Boundary Scan Architecture:

Test Access Port (TAP)
TAP Controller
Instruction Register
Bypass Register
Boundary Scan Register
Device Identification Register

The Test Access Port has the necessary interface pins, namely JTCLK, JTDI, JTDO, and JTMS, and the optional $\overline{\text{JTRST}}$ input. Details on these pins can be found in Section 8. Refer to IEEE 1149.1-1990, IEEE 1149.1a-1993, and IEEE 1149.1b-1994 for details about the Boundary Scan Architecture and the Test Access Port.

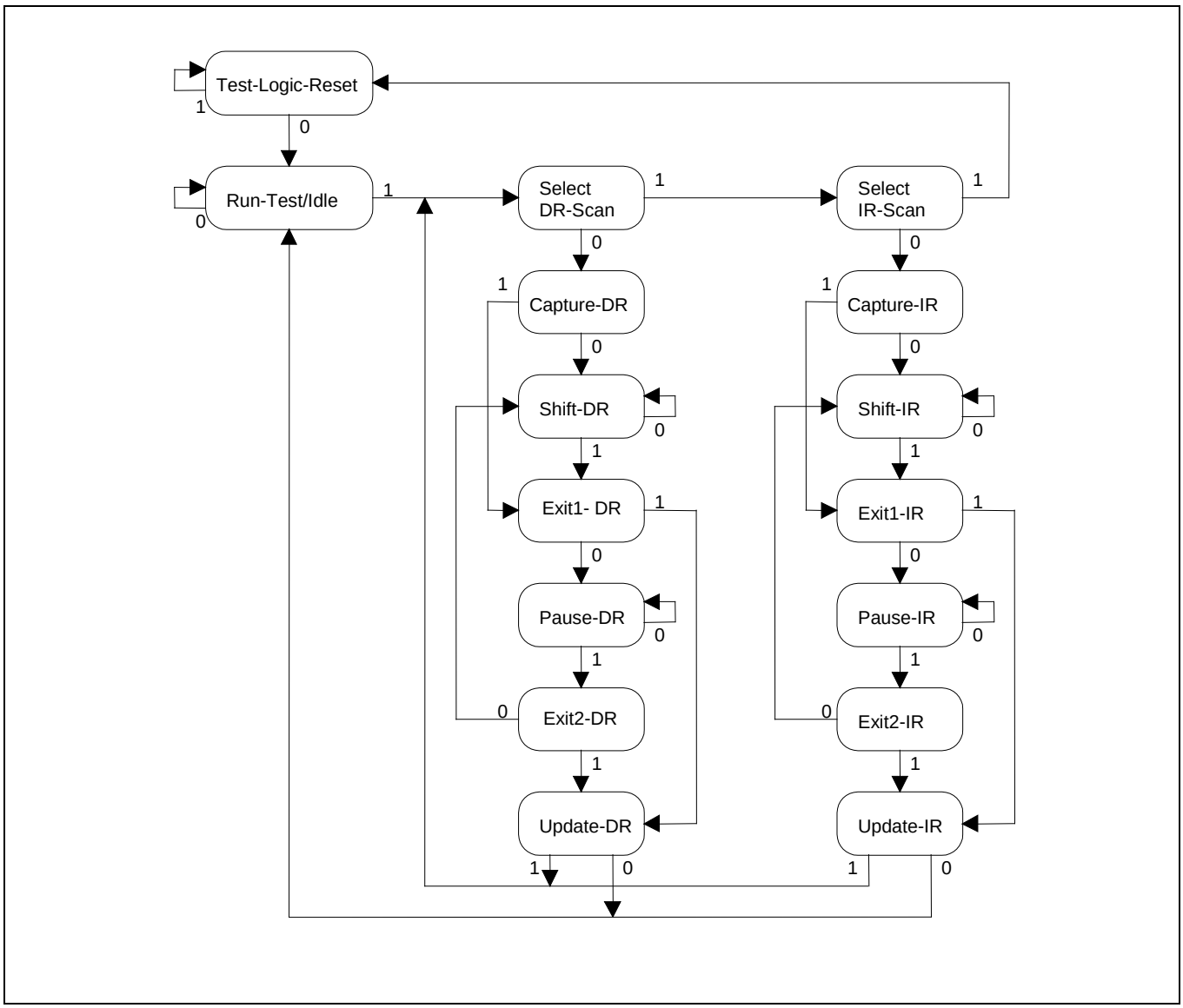
Figure 13-1. JTAG Block Diagram



13.2 JTAG TAP Controller State Machine Description

This section covers the details on the operation of the Test Access Port (TAP) Controller State Machine. See Figure 13-2 for details on each of the states described below. The TAP controller is a finite state machine that responds to the logic level at JTMS on the rising edge of JTCLK.

Figure 13-2. JTAG TAP Controller State Machine



Test-Logic-Reset. When $\overline{\text{JTRST}}$ is changed from low to high, the TAP controller starts in the Test-Logic-Reset state, and the Instruction Register is loaded with the **IDCODE** instruction. All system logic and I/O pads on the device operate normally. This state can also be reached from any other state by holding JTMS high and clocking JTCLK five times.

Run-Test-Idle. Run-Test-Idle is used between scan operations or during specific tests. The Instruction Register and Test Register remain idle.

Select-DR-Scan. All test registers retain their previous state. With JTMS low, a rising edge of JTCLK moves the controller into the Capture-DR state and initiates a scan sequence. JTMS high moves the controller to the Select-IR-Scan state.

Capture-DR. Data may be parallel loaded into the Test Data register selected by the current instruction. If the instruction does not call for a parallel load or the selected register does not allow parallel loads, the Test Register remains at its current value. On the rising edge of JTCLK, the controller goes to the Shift-DR state if JTMS is low or to the Exit1-DR state if JTMS is high.

Shift-DR. The Test Data Register selected by the current instruction is connected between JTDI and JTDO and shifts data one stage towards its serial output on each rising edge of JTCLK. If a Test Register selected by the current instruction is not placed in the serial path, it maintains its previous state.

Exit1-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state that terminates the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Pause-DR state.

Pause-DR. Shifting of the Test registers is halted while in this state. All Test registers selected by the current instruction retain their previous state. The controller remains in this state while JTMS is low. A rising edge on JTCLK with JTMS high puts the controller in the Exit2-DR state.

Exit2-DR. While in this state, a rising edge on JTCLK with JTMS high puts the controller in the Update-DR state and terminate the scanning process. A rising edge on JTCLK with JTMS low puts the controller in the Shift-DR state.

Update-DR. A falling edge on JTCLK while in the Update-DR state latches the data from the shift register path of the Test registers into the data output latches. This prevents changes at the parallel output due to changes in the shift register. A rising edge on JTCLK with JTMS low, puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

Select-IR-Scan. All Test registers retain their previous state. The Instruction register remains unchanged during this state. With JTMS low, a rising edge on JTCLK moves the controller into the Capture-IR state and initiates a scan sequence for the Instruction register. JTMS high during a rising edge on JTCLK puts the controller back into the Test-Logic-Reset state.

Capture-IR. The Capture-IR state is used to load the shift register in the Instruction register with a fixed value of 001. This value is loaded on the rising edge of JTCLK. If JTMS is high on the rising edge of JTCLK, the controller enters the Exit1-IR state. If JTMS is low on the rising edge of JTCLK, the controller enters the Shift-IR state.

Shift-IR. In this state, the shift register in the Instruction register is connected between JTDI and JTDO and shifts data one stage for every rising edge of JTCLK towards the serial output. The parallel registers, as well as all Test registers, remain at their previous states. A rising edge on JTCLK with JTMS high moves the controller to the Exit1-IR state. A rising edge on JTCLK with JTMS low keeps the controller in the Shift-IR state while moving data one stage through the Instruction shift register.

Exit1-IR. A rising edge on JTCLK with JTMS low puts the controller in the Pause-IR state. If JTMS is high on the rising edge of JTCLK, the controller enters the Update-IR state and terminate the scanning process.

Pause-IR. Shifting of the Instruction register is halted temporarily. With JTMS high, a rising edge on JTCLK puts the controller in the Exit2-IR state. The controller remains in the Pause-IR state if JTMS is low during a rising edge on JTCLK.

Exit2-IR. A rising edge on JTCLK with JTMS high put the controller in the Update-IR state. The controller loops back to the Shift-IR state if JTMS is low during a rising edge of JTCLK in this state.

Update-IR. The instruction shifted into the Instruction shift register is latched into the parallel output on the falling edge of JTCLK as the controller enters this state. Once latched, this instruction becomes the current instruction. A rising edge on JTCLK with JTMS low, puts the controller in the Run-Test-Idle state. With JTMS high, the controller enters the Select-DR-Scan state.

13.3 JTAG Instruction Register and Instructions

The instruction register contains a shift register as well as a latched parallel output and is 3 bits in length. When the TAP controller enters the Shift-IR state, the instruction shift register is connected between JTDI and JTDO. While in the Shift-IR state, a rising edge on JTCLK with JTMS low shifts data one stage toward the serial output at JTDO. A rising edge on JTCLK in the Exit1-IR state or the Exit2-IR state with JTMS high moves the controller to the Update-IR state. The falling edge of that same JTCLK latches the data in the instruction shift register to the instruction parallel output. Instructions supported by the device and their respective operational binary codes are shown in Table 13-1.

Table 13-1. JTAG Instruction Codes

INSTRUCTIONS	SELECTED REGISTER	INSTRUCTION CODES
EXTEST	Boundary Scan	000
IDCODE	Device Identification	001
SAMPLE/PRELOAD	Boundary Scan	010
CLAMP	Bypass	011
HIGHZ	Bypass	100
----	Bypass	101
----	Bypass	110
BYPASS	Bypass	111

SAMPLE/PRELOAD. This is a mandatory instruction for the IEEE 1149.1 specification. This instruction supports two functions. The digital I/Os of the device can be sampled at the boundary scan register without interfering with the normal operation of the device and the boundary scan register can be pre-loaded for the EXTEST instruction. The positive edge of JTCLK in the Capture-DR state samples all digital input pins into the boundary scan register. The boundary scan register is connected between JTDI and JTDO. The data on JTDI pin is clocked into the boundary scan register and the data captured in the Capture-DR state is shifted out the TDO pin in the Shift-DR state.

EXTEST. This is a mandatory instruction for the IEEE 1149.1 specification. This instruction allows testing of all interconnections to the device. When the EXTEST instruction is latched in the instruction register, the following actions occur. Once enabled by the Update-IR state, the parallel outputs of all digital output pins are driven according to the values in the boundary scan registers on the positive edge of JTCLK. The boundary scan register is connected between JTDI and JTDO. The positive edge of JTCLK in the Capture-DR state samples all digital input pins into the boundary scan register. The negative edge of JTCLK in the Update-DR state causes all of the digital output pins to be driven according to the values in the boundary scan registers that have been shifted in during the Shift-DR state. The outputs are returned to their normal mode or HIZ mode at the positive edge of JTCLK during the Update-IR state when an instruction other than EXTEST or CLAMP is activated.

BYPASS. This is a mandatory instruction for the IEEE 1149.1 specification. When the BYPASS instruction is latched into the parallel instruction register, JTDI connects to JTDO through the 1-bit bypass test register. This allows data to pass from JTDI to JTDO not affecting the device's normal operation. This mode can be used to bypass one or more chips in a system with multiple chips that have their JTAG scan chain connected in series. The chips not in bypass can then be tested with the normal JTAG modes.

IDCODE. This is a mandatory instruction for the IEEE 1149.1 specification. When the IDCODE instruction is latched into the parallel instruction register, the identification test register is selected. The device identification code is loaded into the identification register on the rising edge of JTCLK following entry into the Capture-DR state. Shift-DR can be used to shift the identification code out serially through JTDO. During Test-Logic-Reset, the identification code is forced into the instruction register's parallel output.

HIGHZ. All digital outputs are placed into a high-impedance state. The bypass register is connected between JTDI and JTDO. The outputs are put into the HIZ mode when the HIZ instruction is loaded in the Update-IR state and on the positive edge of JTCLK. The outputs are returned to their normal mode or driven from the boundary scan register at the positive edge of JTCLK during the Update-IR state when an instruction other than HIZ is activated.

CLAMP. All digital output pins output data from the boundary scan parallel output while connecting the bypass register between JTDI and JTDO. The outputs do not change during the CLAMP instruction. If the previous instruction was not EXTEST, the outputs will be driven according to the values in the boundary scan register at the positive edge of JTCLK in the Update-IR state. The typical use of this instruction is in a system that has the JTAG scan chain of multiple chips connected in series, and all of the chips have their outputs initialized using the EXTEST mode. Then some of the chips are left initialized using the CLAMP mode and others have their IO controlled using the EXTEST mode. This reduces the size of the scan chain during the partial testing of the system.

13.4 JTAG ID Codes

Table 13-2. JTAG ID Codes

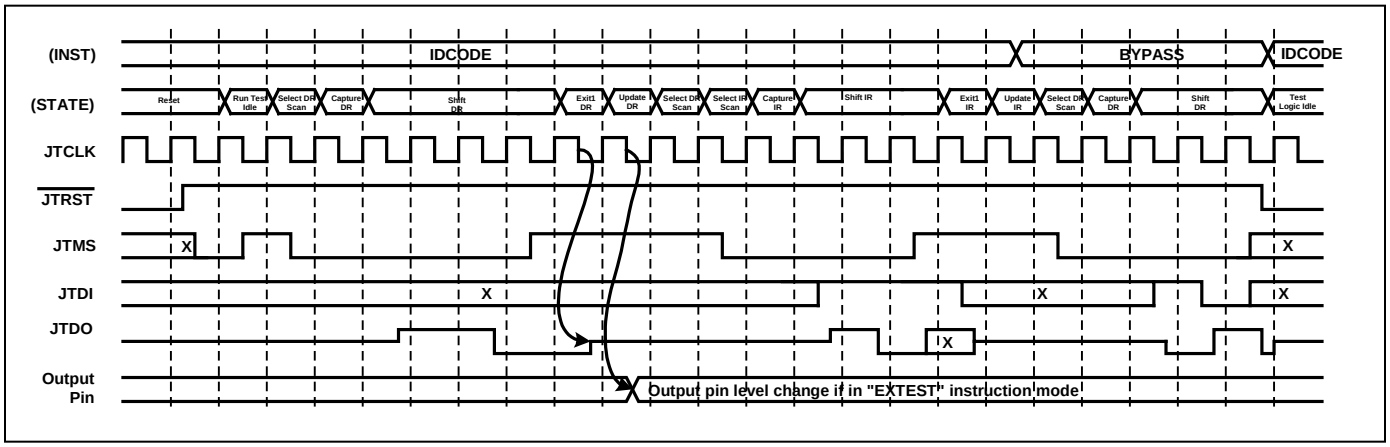
DEVICE	REVISION ID[31:28]	DEVICE CODE ID[27:12]	MANUFACTURER'S CODE ID[11:1]	REQUIRED ID[0]
DS3170	Consult factory	0000000001001111	00010100001	1

13.5 JTAG Functional Timing

This functional timing for the JTAG circuits shows:

- The JTAG controller starting from reset state
- Shifting out the first 4 LSB bits of the IDCODE
- Shifting in the BYPASS instruction (111) while shifting out the mandatory X01 pattern
- Shifting the TDI pin to the TDO pin through the bypass shift register
- An asynchronous reset occurs while shifting

Figure 13-3. JTAG Functional Timing



13.6 IO Pins

All input, output, and inout pins are inout pins in JTAG mode.

14 PIN CONFIGURATIONS

Table 14-1. DS3170 Pin Assignments for 100-Ball CSBGA (Sorted by Signal Name)

SIGNAL	BALL	SIGNAL	BALL	SIGNAL	BALL	SIGNAL	BALL
A[0]	K5	D[7]	K8	ROH	B6	TXP	E1
A[1]	J2	D[8]	J8	ROHCLK	C9	TXP	E2
A[2]	K2	D[9]	G6	ROHSOF	F8	WIDTH	H2
A[3]	H3	GPIO[1]	E8	RPOS	F10	$\overline{WR}$	C2
A[4]	J3	GPIO[2]	E7	RSER	C6	UNUSED1	D6
A[5]	K3	GPIO[3]	F7	RSOFO	B8	VDD	B1
A[6]	H4	GPIO[4]	G7	$\overline{RST}$	E6	VDD	D1
A[7]	J4	GPIO[5]	F6	RXN	A3	VDD	K4
A[8]	H5	GPIO[6]	G5	RXP	A4	VDD	K10
ALE	G4	GPIO[7]	D3	SPI	C3	VDD	D10
UNUSED2	G2	GPIO[8]	D4	TCLKI	C10	VDD	A7
$\overline{CS}$	A1	$\overline{HIZ}$	B4	TCLKO	B9	VDD_CLAD	G3
D[0]	J5	$\overline{INT}$	D8	$\overline{TEST}$	F5	VDD_JA	E3
D[1]	K9	JTCLK	A5	TLCLK	B7	VDD_RX	C5
D[10]	J9	JTDI	C4	TNEG	D9	VDD_TX	F4
D[11]	J10	JTDO	D5	TOH	C7	VSS	C1
D[12]	H8	JTMS	B3	TOHCLK	D7	VSS	K1
D[13]	H9	$\overline{JTRST}$	E5	TOHEN	E10	VSS	K6
D[14]	H10	MODE	F3	TOHSOF	G9	VSS	G10
D[15]	G8	RCLKO	A6	TPOS	E9	VSS	A10
D[2]	J6	$\overline{RD}$	B2	TSER	B10	VSS	A2
D[3]	H6	$\overline{RDY}$	J1	TSOFI	A9	VSS_CLAD	G1
D[4]	K7	REFCLK	H1	TSOFO	C8	VSS_JA	D2
D[5]	J7	RLCLK	A8	TXN	F1	VSS_RX	B5
D[6]	H7	RNEG	F9	TXN	F2	VSS_TX	E4

Table 14-2. DS3170 Pin Assignments for 100-Ball CSBGA (Sorted by Ball #)

BALL	SIGNAL	BALL	SIGNAL	BALL	SIGNAL	BALL	SIGNAL
A1	$\overline{CS}$	C6	RSER	F1	TXN	H6	D[3]
A2	VSS	C7	TOH	F2	TXN	H7	D[6]
A3	RXN	C8	TSOFO	F3	MODE	H8	D[12]
A4	RXP	C9	ROHCLK	F4	VDD_TX	H9	D[13]
A5	JTCLK	C10	TCLKI	F5	$\overline{TEST}$	H10	D[14]
A6	RCLKO	D1	VDD	F6	GPIO[5]	J1	$\overline{RDY}$
A7	VDD	D2	VSS_JA	F7	GPIO[3]	J2	A[1]
A8	RLCLK	D3	GPIO[7]	F8	ROHSOF	J3	A[4]
A9	TSOFI	D4	GPIO[8]	F9	RNEG	J4	A[7]
A10	VSS	D5	JTDO	F10	RPOS	J5	D[0]
B1	VDD	D6	UNUSED1	G1	VSS_CLAD	J6	D[2]
B2	$\overline{RD}$	D7	TOHCLK	G2	UNUSED2	J7	D[5]
B3	JTMS	D8	$\overline{INT}$	G3	VDD_CLAD	J8	D[8]
B4	$\overline{HIZ}$	D9	TNEG	G4	ALE	J9	D[10]
B5	VSS_RX	D10	VDD	G5	GPIO[6]	J10	D[11]
B6	ROH	E1	TXP	G6	D[9]	K1	VSS
B7	TLCLK	E2	TXP	G7	GPIO[4]	K2	A[2]
B8	RSOFO	E3	VDD_JA	G8	D[15]	K3	A[5]
B9	TCLKO	E4	VSS_TX	G9	TOHSOF	K4	VDD
B10	TSER	E5	$\overline{JTRST}$	G10	VSS	K5	A[0]
C1	VSS	E6	$\overline{RST}$	H1	REFCLK	K6	VSS
C2	$\overline{WR}$	E7	GPIO[2]	H2	WIDTH	K7	D[4]
C3	SPI	E8	GPIO[1]	H3	A[3]	K8	D[7]
C4	JTDI	E9	TPOS	H4	A[6]	K9	D[1]
C5	VDD_RX	E10	TOHEN	H5	A[8]	K10	VDD

Figure 14-1. DS3170 Pin Assignments—100-Ball CSBGA (Top View)

	1	2	3	4	5	6	7	8	9	10
A	CS_N	VSS	RXN	RXP	JTCLK	RCLKO	VDD	RLCLK	TSOFI	VSS
B	VDD	RD_N	JTMS	HIZ_N	VSS_RX	ROH	TLCLK	RSOFO	TCLKO	TSER
C	VSS	WR_N	SPI	JTDI	VDD_RX	RSER	TOH	TSOFO	ROHCLK	TCLKI
D	VDD	VSS_JA	GPIO[7]	GPIO[8]	JTDO	UNUSED1	TOHCLK	INT_N	TNEG	VDD
E	TXP	TXP	VDD_JA	VSS_TX	JTRST_N	RST_N	GPIO[2]	GPIO[1]	TPOS	TOHEN
F	TXN	TXN	MODE	VDD_TX	TEST_N	GPIO[5]	GPIO[3]	ROHSOF	RNEG	RPOS
G	VSS_CLAD	UNUSED2	VDD_CLAD	ALE	GPIO[6]	D[9]	GPIO[4]	D[15]	TOHSOF	VSS
H	REFCLK	WIDTH	A[3]	A[6]	A[8]	D[3]	D[6]	D[12]	D[13]	D[14]
J	RDY_N	A[1]	A[4]	A[7]	D[0]	D[2]	D[5]	D[8]	D[10]	D[11]
K	VSS	A[2]	A[5]	VDD	A[0]	VSS	D[4]	D[7]	D[1]	VDD

15 DC ELECTRICAL CHARACTERISTICS

ABSOLUTE MAXIMUM RATINGS

Voltage Range on Any Input, Bidirectional or Open Drain
Output Lead with Respect to V_{SS} ..... -0.3V to +5.5V
Supply Voltage Range (V_{DD}) with Respect to V_{SS} ..... -0.3V to +3.63V
Ambient Operating Temperature Range ..... -40°C to +85°C
Junction Operating Temperature Range ..... -40°C to +125°C
Storage Temperature Range ..... -55°C to +125°C
Soldering Temperature (reflow)
Lead(Pb)-free ..... +260°C
Containing lead(Pb) ..... +240°C

These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time can affect reliability. Ambient Operating Temperature Range is assuming the device is mounted on a JEDEC standard test board in a convection cooled JEDEC test enclosure.

Note: *The typical values listed below are not production tested.*

Table 15-1. Recommended DC Operating Conditions

(V_{DD} = 3.3V ±5%, T_j = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logic 1	V_{IH}		2.4		5.5	V
Logic 0	V_{IL}		-0.3		+0.8	V
Supply (V_{DD}) ±5%	V_{DD}		3.135	3.300	3.465	V

Table 15-2. DC Electrical Characteristics

(T_j = -40°C to +85°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current (V_{DD} = 3.465V)	I_{DD}	(Notes 1, 2)		120	145	mA
Power-Down Current (All DISABLE Bits Set)	I_{DDD}	(Note 2)		18	25	mA
Lead Capacitance	C_{IO}			7		pF
Input Leakage	I_{IL}		-10		+10	µA
Input Leakage (Input Pins with Internal Pullup Resistors)	I_{ILP}		-350		+10	µA
Output Leakage (when High Impedance)	I_{LO}		-10		+10	µA
Output Voltage (I_{OH} = -4.0mA)	V_{OH}	4mA outputs, V_{DD} = 3.135	2.4			V
Output Voltage (I_{OL} = 4.0mA)	V_{OL}	4mA outputs, V_{DD} = 3.135			0.4	V
Output Voltage (I_{OH} = -6.0mA)	V_{OH}	6mA outputs, V_{DD} = 3.135	2.4			V
Output Voltage (I_{OL} = 6.0mA)	V_{OL}	6mA outputs, V_{DD} = 3.135			0.4	V

Note 1: Mode DS3 line rate, all outputs enabled.

Note 2: All outputs loaded with rated capacitance; all inputs between V_{DD} and V_{SS}; inputs with pullups connected to V_{DD}.

Table 15-3. Output Pin Drive

PIN NAME	TYPE	DRIVE STRENGTH (mA)
TLCLK	O	6
TPOS /TDAT	O	6
TNEG	O	6
TXP	O	N/A (analog)
TXN	O	N/A (analog)
TOHCLK	O	4
TOHSOF	O	4
ROH	O	4
ROHCLK	O	4
ROHSOF	O	4
TCLKO/TGCLK	O	6
TSOFO/TDEN	O	6
RSER	O	6
RCLKOn/RGCLK	O	6
RSOFO/RDEN	O	6
D[15:0]	IO	4
$\overline{RDY}$	Oz	6
$\overline{INT}$	Oz	4
GPIO[7:0]	IO	4
JTDO	Oz	4

16 AC TIMING CHARACTERISTICS

There are several common AC characteristic definitions. These generic definitions are shown in Figure 16-1, Figure 16-2, Figure 16-3, and Figure 16-4. Definitions that are specific to a given interface are shown in that interface's subsection.

Figure 16-1. Clock Period and Duty Cycle Definitions

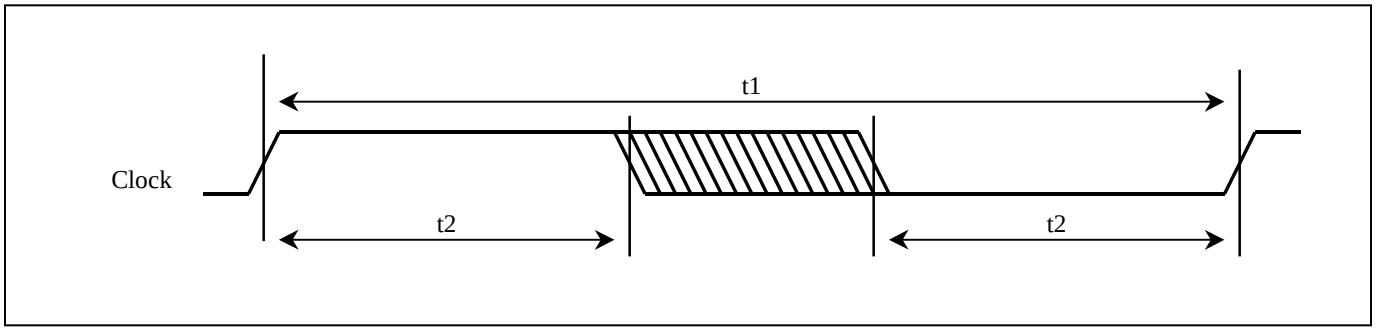


Figure 16-2. Rise Time, Fall Time, and Jitter Definitions

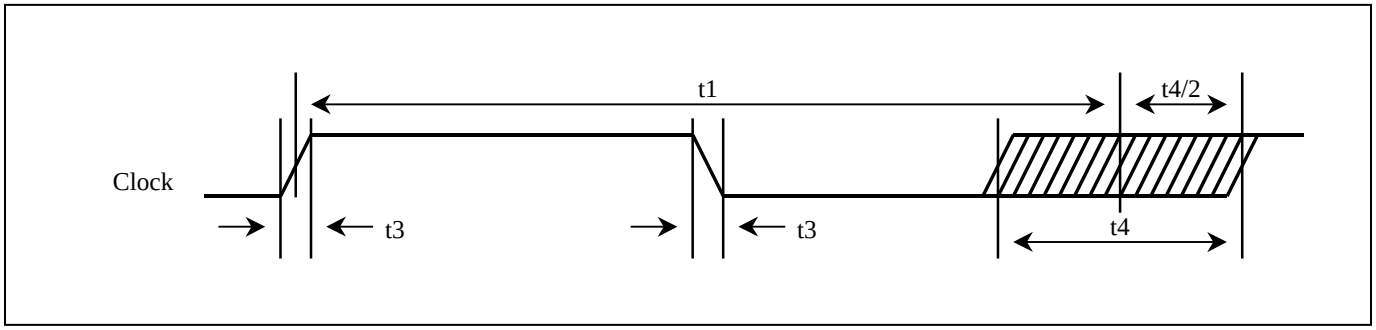


Figure 16-3. Hold, Setup, and Delay Definitions (Rising Clock Edge)

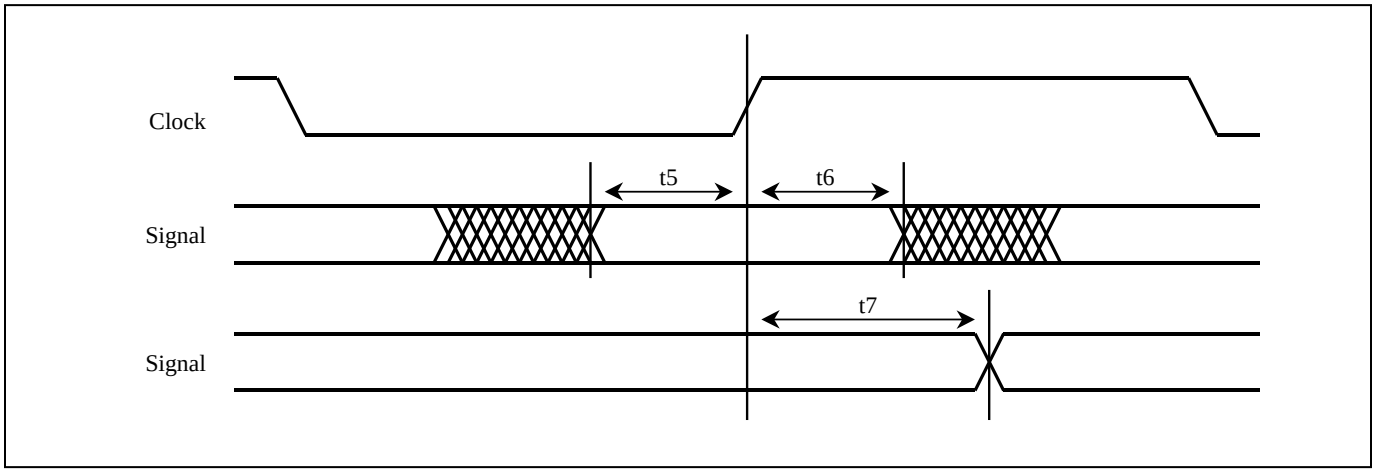


Figure 16-4. Hold, Setup, and Delay Definitions (Falling Clock Edge)

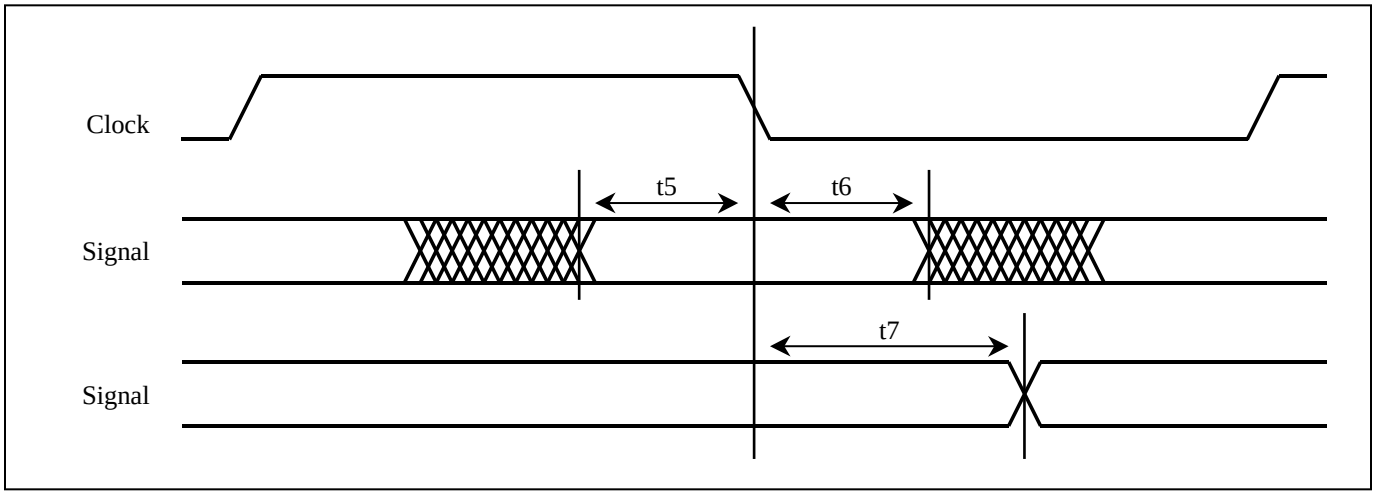


Figure 16-5. To/From Hi Z Delay Definitions (Rising Clock Edge)

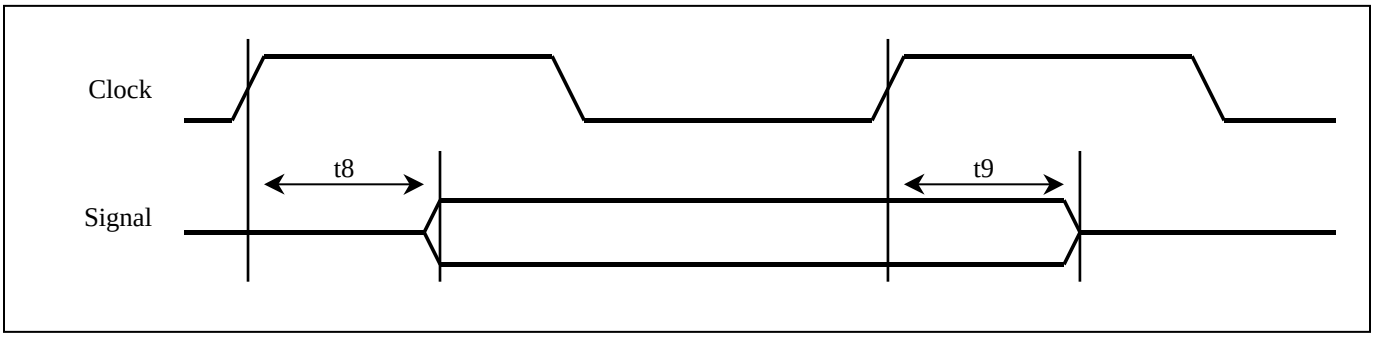
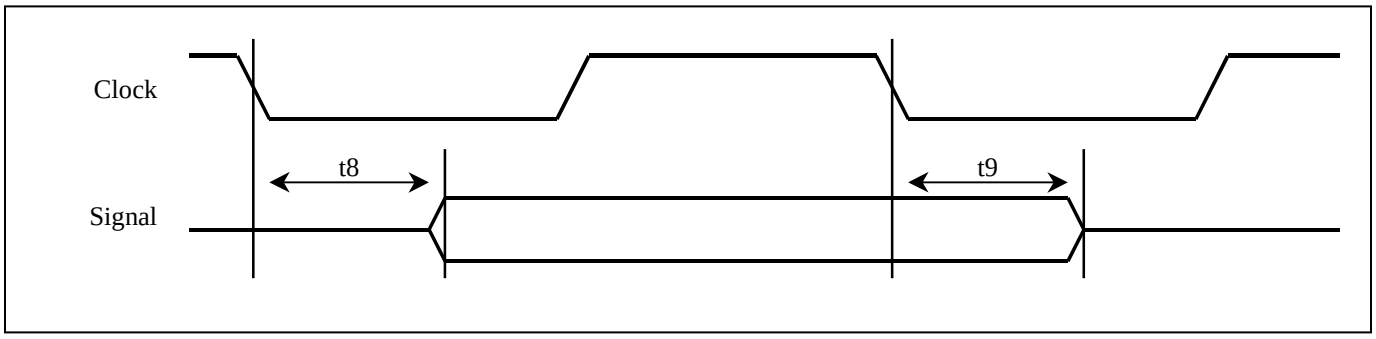


Figure 16-6. To/From Hi Z Delay Definitions (Falling Clock Edge)



16.1 Framer Data Path AC Characteristics

All AC timing characteristics are specified with a 25 pF capacitive load on all output pins, V_{IH} = 2.4V and V_{IL} = 0.8V. The voltage threshold for all timing measurements is VDD/2. The generic timing definitions shown in in Figure 16-1, Figure 16-2, Figure 16-3, and Figure 16-4 apply to this interface.

Table 16-1. Framer Interface Timing

(V_{DD} = 3.3V ±5%, T_j = -40°C to +125°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Frequency	f1(1/t1)	(Note 1)			52	MHz
CLK Clock Duty Cycle (t2/t1)	t2/t1	(Note 2)	40	50	60	%
CLK Rise or Fall Times (20% to 80%)	t3	(Note 2)			4	ns
DIN to CLK Setup Time	t5	(Note 3)	4			ns
CLK to DIN Hold Time	t6	(Note 3)	0			ns
CLK to DOUT Delay	t7	(Note 4)	2		10	ns
		(Note 5)	2		8	ns

Note 1: Any mode, TCLKI, RLCLK input clocks.
Note 2: Any mode, TCLKI, RLCLK input clocks.
Note 3: RLCLK clock input to RPOS/RDAT, RNEG/RLCV inputs.
Note 4: TCLKI, RLCLK clock inputs to TPOS/TDAT, TNEG outputs.
Note 5: TLCLKn, TCLKO, RCLKO clock outputs to TPOS/TDAT, TNEG outputs.

Table 16-2. System Port Interface Timing

(V_{DD} = 3.3V ±5%, T_j = -40°C to +125°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Frequency	f1(1/t1)	(Note 1)			52	MHz
CLK Clock Duty Cycle (t2/t1)	t2/t1	(Note 2)	40	50	60	%
CLK Rise or Fall times (20% to 80%)	t3	(Note 2)			4	ns
DIN to CLK Setup Time	t5	(Note 3)	3			ns
		(Note 4)	7			ns
CLK to DIN Hold Time	t6	(Note 3)	1			ns
		(Note 4)	1			ns
CLK to DOUT Delay	t7	(Note 5)	2		10	ns
		(Note 6)	2		8	ns

Note 1: Any mode, TCLKI, RLCLK input clocks.
Note 2: Any mode, TCLKI, RLCLK input clocks.
Note 3: TCLKI, RLCLK clock inputs to TSOFI, TSER inputs.
Note 4: TCLKO, RCLKO clock outputs to TSOFI, TSER inputs.
Note 5: TCLKI, RLCLK clock input to TSOFO/TDEN, RSER, RSOFO/RDEN outputs.
Note 6: TCLKO, RCLKO clock output to TSOFO/TDEN, RSER, RSOFO/RDEN outputs.

Table 16-3. Misc Timing

(V_{DD} = 3.3V ±5%, T_j = -40°C to +125°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Asynchronous Input High, Low Time	t1-t2, t2	(Note 1)	500			ns
Asynchronous Input Rise, Fall Time	t3	(Note 1)			10	ns

Note 1: TMEI (GPIO), PMU (GPIO), 8KREFI (GPIO) and $\overline{RST}$ inputs.

16.2 Overhead Port AC Characteristics

All AC timing characteristics are specified with a 25 pF capacitive load on all output pins, V_{IH} = 2.4V and V_{IL} = 0.8. The voltage threshold for all timing measurements is VDD/2. The generic timing definitions shown in Figure 16-1, Figure 16-2, Figure 16-3, and Figure 16-4 apply to this interface.

Table 16-4. Overhead Port Timing

(V_{DD} = 3.3V ±5%, T_j = -40°C to +125°C.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CLK Period	t1	(Note 1)	500			ns
CLK Clock High and Low Time	t1-t2, t2	(Note 1)	200			ns
DIN to CLK Setup Time	t5	(Note 2)	20			ns
CLK to DIN Hold Time	t6	(Note 2)	20			ns
CLK to DOUT Delay	t7	(Note 3)	-20		20	ns

Note 1: TOHCLK, ROHCLK output clocks.

Note 2: TOHCLK clock falling edge outputs to TOH, TOHEN inputs.

Note 3: TOHCLK, ROHCLK clock falling edge outputs to TOHSOF, ROH, ROHSOF outputs.

16.3 Micro Interface AC Characteristics

16.3.1 SPI Bus Mode

Table 16-5. SPI Bus Mode Timing

SYMBOL (1)	CHARACTERISTIC (2)	SYMBOL	MIN	MAX	UNITS
	Operating Frequency Slave	$f_{BUS(S)}$		10	MHz
t1	Cycle Time: Slave	$t_{cyc(s)}$	100	—	ns
t2	Enable Lead Time	$t_{LEAD(S)}$	15	—	ns
t3	Enable Lag Time	$t_{LAG(S)}$	15	—	ns
t4	Clock (CLK) High Time Slave	$t_{CLKH(S)}$	50	—	ns
t5	Clock (CLK) Low Time Slave	$t_{CLKL(S)}$	50	—	ns
t6	Data Setup Time (Inputs) Slave	$t_{SU(S)}$	5	—	ns
t7	Data Hold Time (Inputs) Slave	$t_{H(S)}$	15	—	ns
t8	Disable Time, Slave (3)	$t_{DIS(S)}$	—	25	ns
t9	Data Valid Time, After Enable Edge Slave (4)	$t_{V(S)}$	—	40	ns
t10	Data Hold Time, Outputs, After Enable Edge Slave	$t_{HD(S)}$	5	—	ns

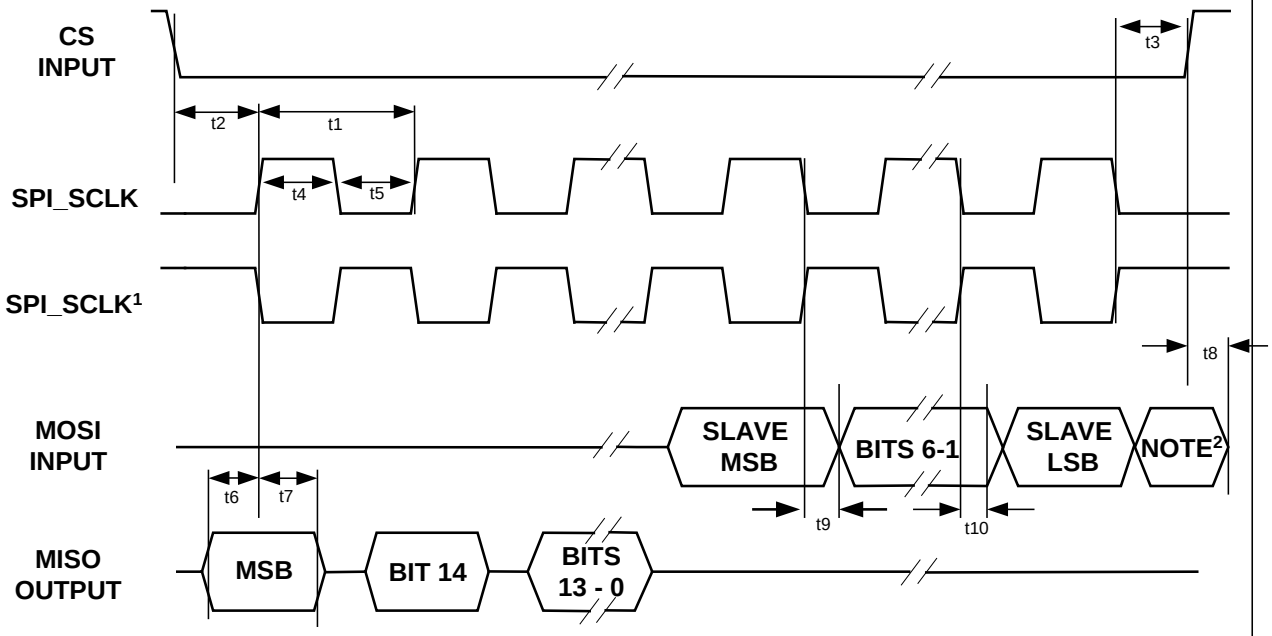
Note 1: Symbols refer to dimensions in the following figure.

Note 2: 100 pF load on all SPI pins.

Note 3: Hold time to high-impedance state.

Note 4: With 100 pF on all SPI pins.

Figure 16-7. SPI Interface Timing Diagram



NOTE:
1. Clock edge reference to data controlled by CPHA and CPOL settings. Refer to functional timing diagrams.
2. Not defined, but usually MSB of character just received.

16.3.2 Parallel Bus Mode

The AC characteristics for the external bus interface in parallel mode. This table references Figure 16-8 and Figure 16-9.

Table 16-6. Micro Interface Timing

(V_{DD} = 3.3V ±5%, Tj = -40°C to 125°C.)

SIGNAL NAME(S)	SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	NOTES
A[N:0]	t1a	Setup Time to $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active	10			ns	1
ALE	t1b	Setup Time to $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active	10			ns	1, 2
A[N:0]	t2	Setup Time to ALE Inactive	2			ns	1, 2
A[N:0]	t3	Hold Time from ALE Inactive	2			ns	1, 2
ALE	t4	Pulse Width	5			ns	1, 2
A[N:0], ALE	t5	Hold Time from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Inactive	0			ns	1
$\overline{CS}$, R/$\overline{W}$	t6	Setup Time to $\overline{RD}$, $\overline{WR}$ Active	0			ns	1
D[15:0]	t8	Output Delay Time from $\overline{RD}$, $\overline{DS}$ Active			30	ns	1
$\overline{RD}$, $\overline{WR}$, $\overline{DS}$	t9a	Pulse Width if Not Using RDY Handshake	35			ns	1, 4
$\overline{RD}$, $\overline{WR}$, $\overline{DS}$	t9b	Delay from RDY	15			ns	1
D[15:0]	t10	Output Deassert Delay Time from $\overline{RD}$, $\overline{DS}$ Inactive	2		10	ns	1, 3
$\overline{CS}$, R/$\overline{W}$	t12	Hold Time from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Inactive	0			ns	1
D[15:0]	t13	Input Setup Time to $\overline{WR}$, $\overline{DS}$ Inactive	10			ns	1
D[15:0]	t14	Input Hold Time from $\overline{WR}$, $\overline{DS}$ Inactive	5			ns	1
RDY	t15	Delay Time from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Active	5			ns	1
RDY	t16	Delay Time from $\overline{RD}$, $\overline{WR}$, $\overline{DS}$ Inactive	0			ns	1
RDY	t17	Enable Delay Time from $\overline{CS}$ Active			18	ns	1
RDY	t18	Disable Delay Time from $\overline{CS}$ Inactive			12	ns	1
RDY	t19	Ending High Pulse Width	1			ns	1
R/$\overline{W}$	t20	Setup Time to $\overline{DS}$ Active	2			ns	1
R/$\overline{W}$	t21	Hold Time to $\overline{DS}$ Inactive	2			ns	1

Note 1: The input/output timing reference level for all signals is VDD/2. Transition time (80%/20%) on $\overline{RD}$, $\overline{WR}$, and $\overline{CS}$ inputs is 5ns (max).

Note 2: Multiplexed mode timing only.

Note 3: D[15:0] output valid until not driven.

Note 4: Timing required if not using RDY handshake.

Figure 16-8. Micro Interface Nonmultiplexed Read/Write Cycle

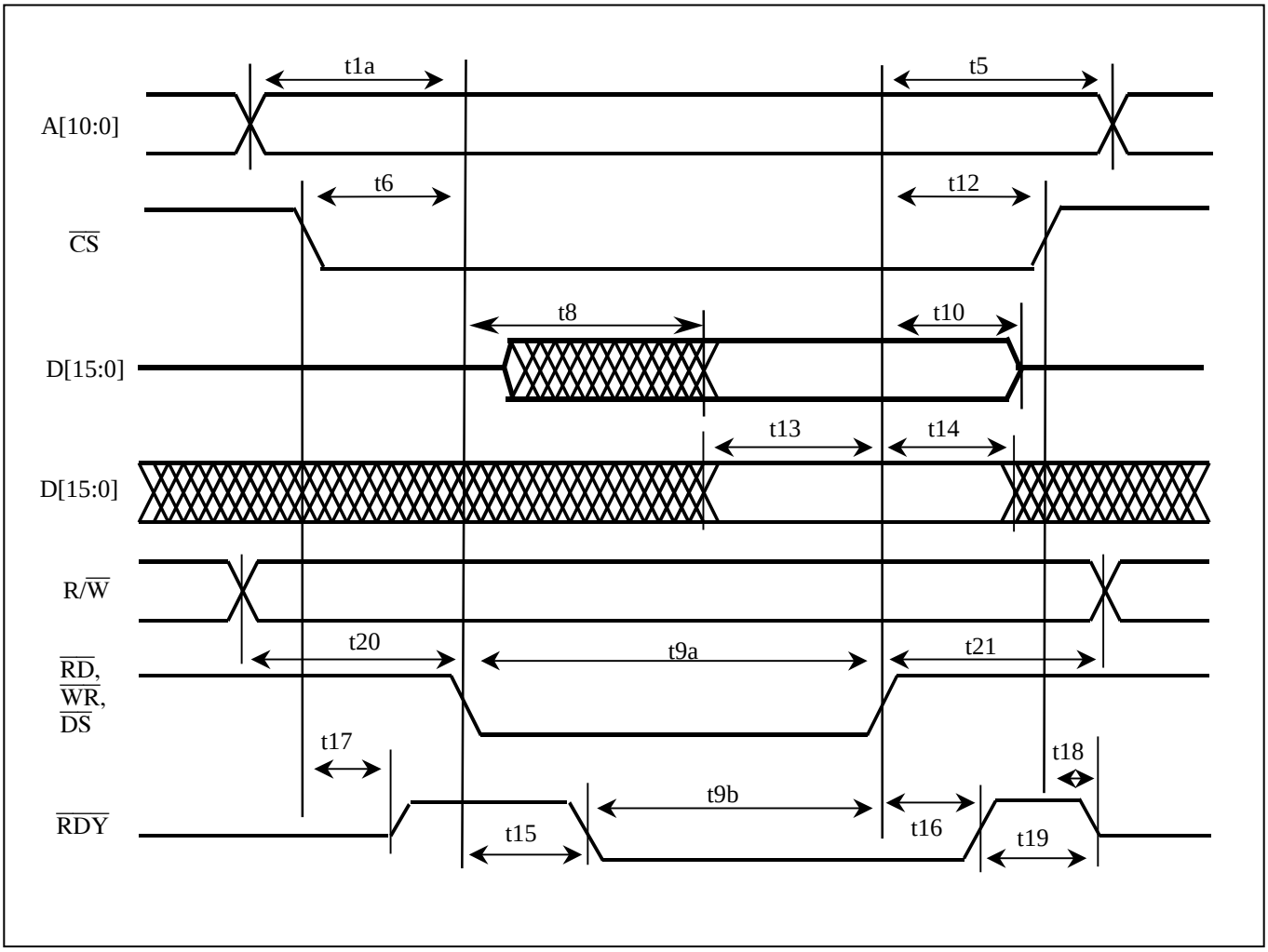
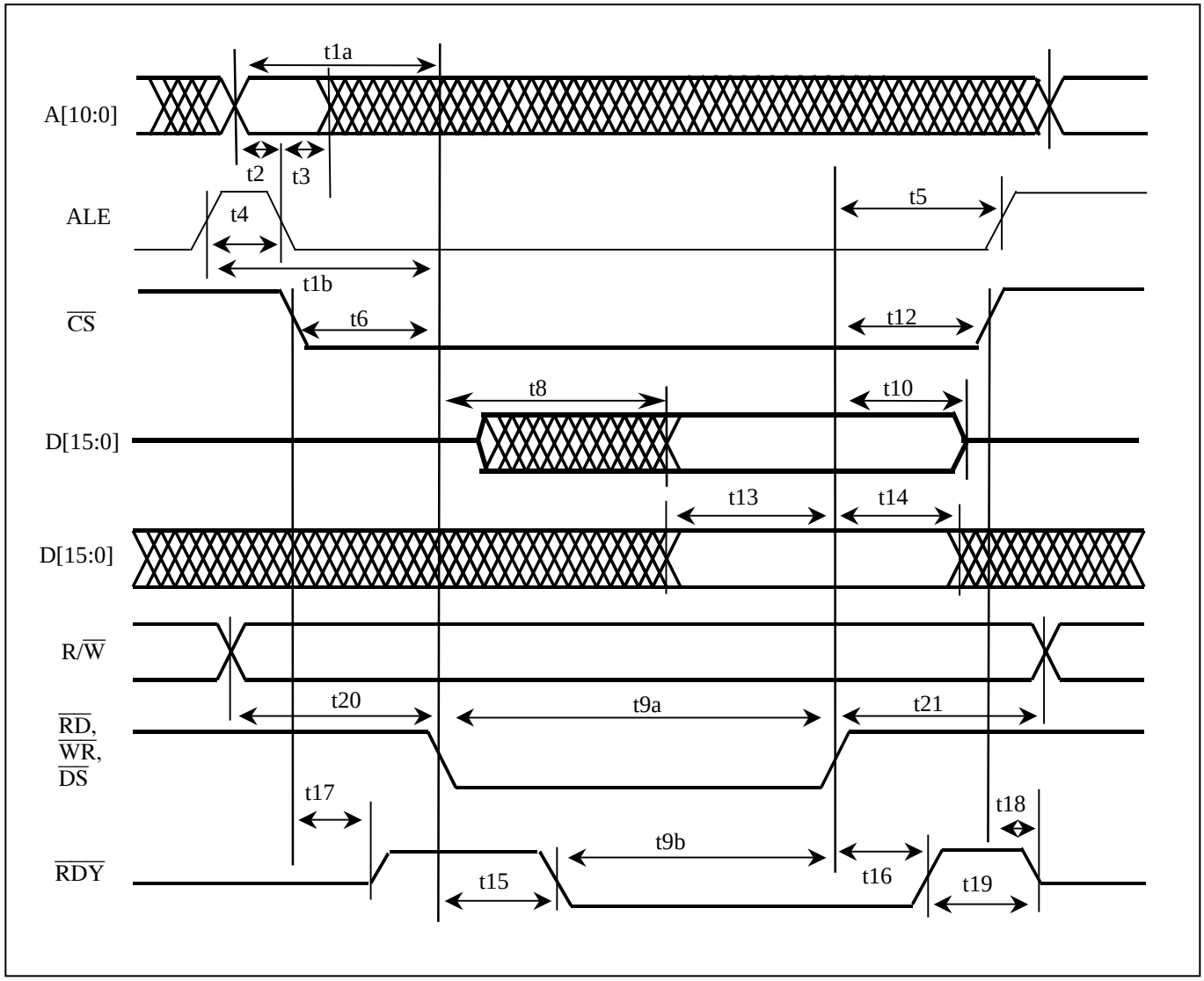


Figure 16-9. Micro Interface Multiplexed Read Cycle



16.4 CLAD Jitter Characteristics

PARAMETER	MIN	TYP	MAX	UNITS
Intrinsic Jitter (UI_{P-P})			0.04	UI_{P-P}
Intrinsic Jitter (UI_{RMS})			0.01	UI_{RMS}
Peak Jitter Transfer			1.75	dB

16.5 LIU Interface AC Characteristics

16.5.1 Waveform Templates

Table 16-7. DS3 Waveform Template

TIME (IN UNIT INTERVALS)	NORMALIZED AMPLITUDE EQUATION
UPPER CURVE	
$-0.85 \le T \le -0.68$	0.03
$-0.68 \le T \le +0.36$	$0.5 \{1 + \sin[(\pi / 2)(1 + T / 0.34)]\} + 0.03$
$0.36 \le T \le 1.4$	$0.08 + 0.407e^{-1.84(T - 0.36)}$
LOWER CURVE	
$-0.85 \le T \le -0.36$	-0.03
$-0.36 \le T \le +0.36$	$0.5 \{1 + \sin[(\pi / 2)(1 + T / 0.18)]\} - 0.03$
$0.36 \le T \le 1.4$	-0.03

Governing Specifications: ANSI T1.102 and Bellcore GR-499.

Table 16-8. DS3 Waveform Test Parameters and Limits

PARAMETER	SPECIFICATION
Rate	44.736Mbps (±20ppm)
Line Code	B3ZS
Transmission Medium	Coaxial cable (AT&T 734A or equivalent)
Test Measurement Point	At the end of 0 to 450ft of coaxial cable
Test Termination	75Ω (±1%) resistive
Pulse Amplitude	Between 0.36V and 0.85V
Pulse Shape	An isolated pulse (preceded by two zeros and followed by one or more zeros) falls within the curves listed in Figure 16-11.
Unframed All-Ones Power Level at 22.368MHz	Between -1.8dBm and +5.7dBm
Unframed All-Ones Power Level at 44.736MHz	At least 20dB less than the power measured at 22.368MHz
Pulse Imbalance of Isolated Pulses	Ratio of positive and negative pulses must be between 0.90 and 1.10.

Figure 16-10. DS3 Pulse Mask Template

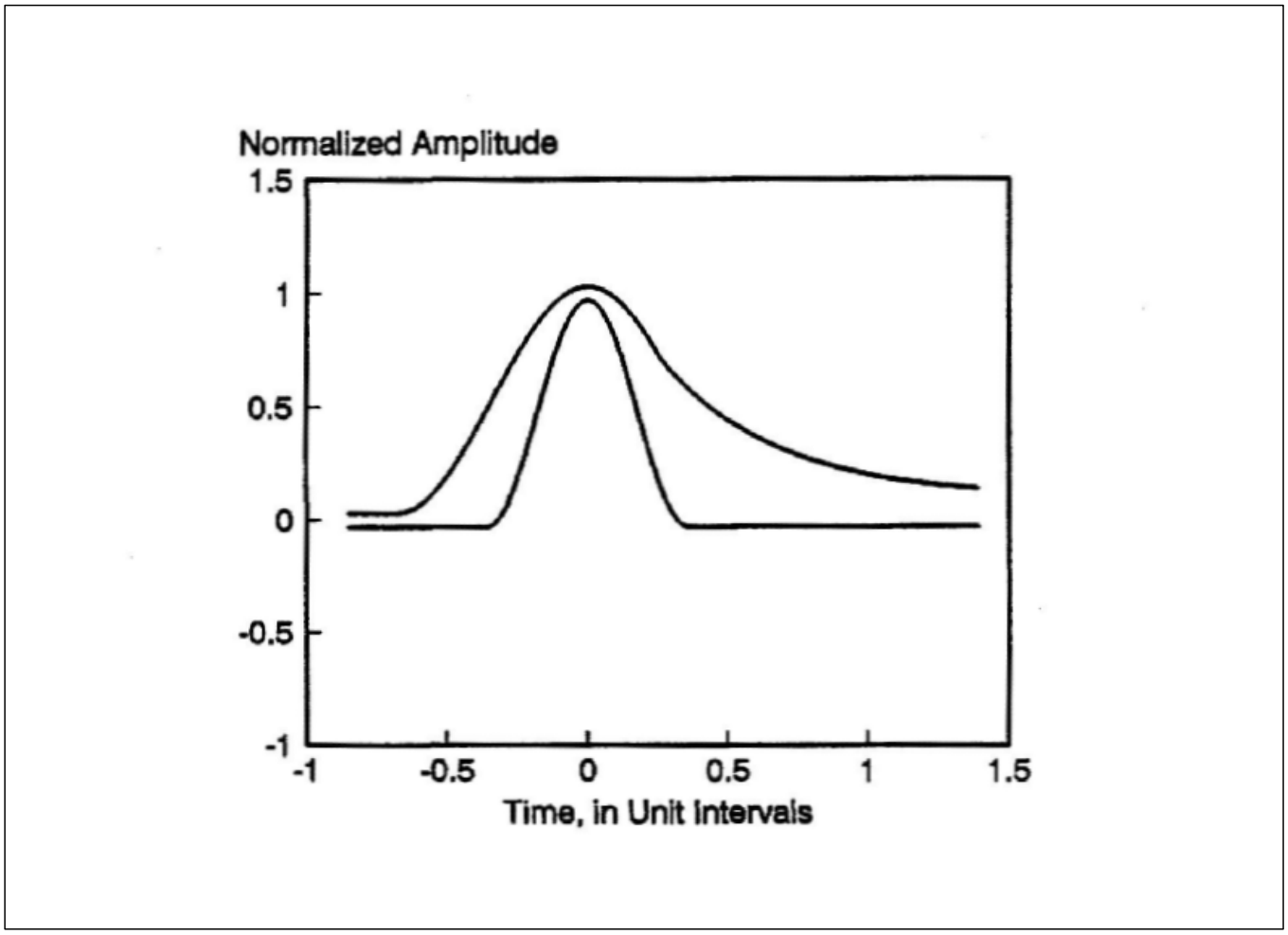
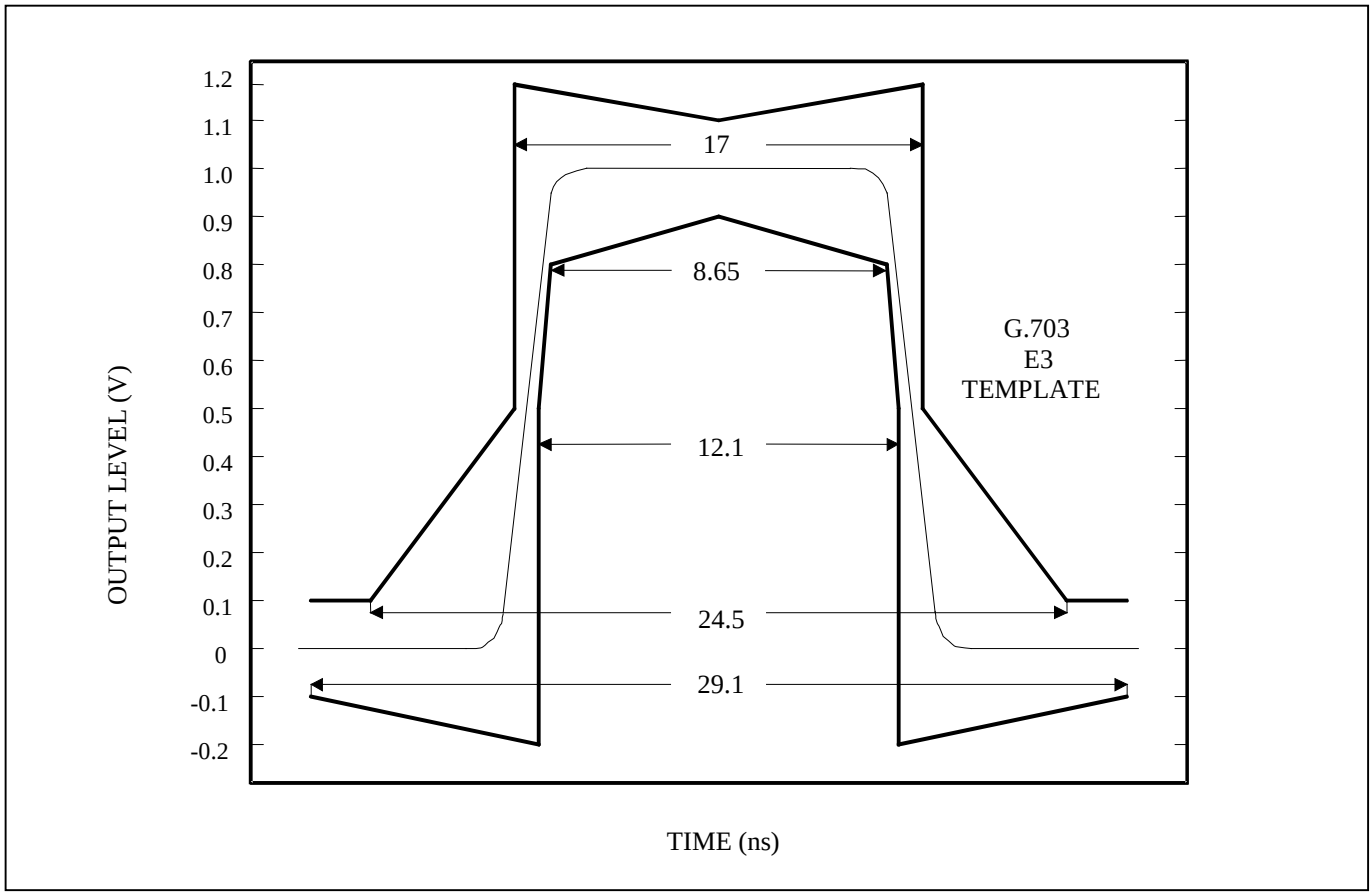


Table 16-9. E3 Waveform Test Parameters and Limits

PARAMETER	SPECIFICATION
Rate	34.368Mbps (±20ppm)
Line Code	HDB3
Transmission Medium	Coaxial cable (AT&T 734A or equivalent)
Test Measurement Point	At the transmitter
Test Termination	75Ω (±1%) resistive
Pulse Amplitude	1.0V (nominal)
Pulse Shape	An isolated pulse (preceded by two zeros and followed by one or more zeros) falls within the template shown in Figure 16-11.
Ratio of the Amplitudes of Positive and Negative Pulses at the Center of the Pulse Interval	0.95 to 1.05
Ratio of the Widths of Positive and Negative Pulses at the Nominal Half Amplitude	0.95 to 1.05

Figure 16-11. E3 Waveform Template



16.5.2 LIU Input/Output Characteristics

Table 16-10. Receiver Input Characteristics—DS3 Mode

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.)

PARAMETER	MIN	TYP	MAX	UNITS
Receive Sensitivity (Length of Cable)	900	1200		ft
Signal-to-Noise Ratio, Interfering Signal Test (Notes 1, 2)		10		
Input Pulse Amplitude, RMON = 0 (Notes 2, 3)			1000	mVpk
Input Pulse Amplitude, RMON = 1 (Note 2, 3)			200	mVpk
Analog LOS Declare, RMON = 0 (Note 4)			-24	dB
Analog LOS Clear, RMON = 0 (Note 4)	-17			dB
Analog LOS Declare, RMON = 1 (Note 4)			-38	dB
Analog LOS Clear, RMON = 1 (Note 4)	-29			dB
Intrinsic Jitter Generation (Note 4)		0.03		UI_{P-P}

Table 16-11. Receiver Input Characteristics—E3 Mode

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.)

PARAMETER	MIN	TYP	MAX	UNITS
Receive Sensitivity (Length of Cable)	900	1200		ft
Signal-to-Noise Ratio, Interfering Signal Test (Notes 1, 2)		12		
Input Pulse Amplitude, RMON = 0 (Notes 2, 3)			1300	mVpk
Input Pulse Amplitude, RMON = 1 (Notes 2, 3)			260	mVpk
Analog LOS Declare, RMON = 0 (Note 4)			-24	dB
Analog LOS Clear, RMON = 0 (Note 4)	-17			dB
Analog LOS Declare, RMON = 1 (Note 4)			-38	dB
Analog LOS Clear, RMON = 1 (Note 4)	-29			dB
Intrinsic Jitter Generation (Note 4)		0.03		UI_{P-P}

Note 1: An interfering signal (2^{15} – 1 PRBS for DS3, 2^{23} – 1 PRBS for E3, B3ZS/HDB3 encoded, compliant waveshape, nominal bit rate) is added to the wanted signal. The combined signal is passed through 0 to 900ft of coaxial cable and presented to the DS3154 receiver. This spec indicates the lowest signal-to-noise ratio that results in a bit error ratio $\leq 10^{-9}$.

Note 2: Not tested during production test.

Note 3: Measured on the line side (i.e., the BNC connector side) of the 1:2 receive transformer (Figure 2-1). During measurement, incoming data traffic is unframed 2^{15} – 1 PRBS for DS3 and unframed 2^{23} – 1 PRBS for E3.

Note 4: With respect to nominal 800mVpk signal for DS3 and nominal 1000mVpk signal for E3.

Table 16-12. Transmitter Output Characteristics—DS3 Modes

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.)

PARAMETER	MIN	TYP	MAX	UNITS
DS3 Output Pulse Amplitude, TLBO = 0 (Note 1)	700	800	900	mVpk
DS3 Output Pulse Amplitude, TLBO = 1 (Note 1)	520	700	800	mVpk
Ratio of Positive and Negative Pulse-Peak Amplitudes	0.9		1.1	
DS3 Unframed All-Ones Power Level at 22.368MHz, 3kHz Bandwidth	-1.8		+5.7	dBm
DS3 Unframed All-Ones Power Level at 44.736MHz vs. Power Level at 22.368MHz, 3kHz Bandwidth			-20	dB
Intrinsic Jitter Generation (Note 2)		0.02	0.05	UI_{P-P}

Table 16-13. Transmitter Output Characteristics—E3 Mode

(V_{DD} = 3.3V ±5%, T_A = -40°C to +85°C.)

PARAMETER	MIN	TYP	MAX	UNITS
Output Pulse Amplitude (Note 1)	900	1000	1100	mVpk
Pulse Width		14.55		ns
Ratio of Positive and Negative Pulse Amplitudes (at Centers of Pulses)	0.95		1.05	
Ratio of Positive and Negative Pulse Widths (at Nominal Half Amplitude)	0.95		1.05	
Intrinsic Jitter Generation (Note 2)		0.02	0.05	UI_{P-P}

Note 1: Measured on the line side (i.e., the BNC connector side) of the 2:1 transmit transformer (Figure 2-1).

Note 2: Measured with jitter-free clock applied to TCLK and a bandpass jitter filter with 10Hz and 800kHz cutoff frequencies. Not tested during production test.

16.6 JTAG Interface AC Characteristics

All AC timing characteristics are specified with a 50 pF capacitive load on JTDO pin and 25 pF capacitive load on all other digital output pins, V_{IH} = 2.4V and V_{IL} = 0.8. The voltage threshold for all timing measurements is VDD/2. The voltage threshold for all timing measurements is VDD/2. The generic timing definitions shown in Figure 16-1, Figure 16-2, Figure 16-3, and Figure 16-4 apply to this interface.

Table 16-14. JTAG Interface Timing

(V_{DD} = 3.3V ±5%, T_j = -40°C to +125°C.)

SIGNAL NAME(S)	SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	NOTES
JTCLK	f1	Clock Frequency (1/t1)	0		10	MHz	
JTCLK	t2	Clock High or Low Period	20			ns	
JTCLK	t3	Rise/Fall Times			5	ns	
JTMS and JTDI	t5	Hold Time from JTCLK Rising Edge	10			ns	
JTMS and JTDI	t6	Setup Time to JTCLK Rising Edge	10			ns	
JTDO	t7	Delay from JTCLK Falling Edge	0		20	ns	
JTDO	t8	Delay out of Hi Z from JTCLK Falling Edge	0		20	ns	
JTDO	t9	Delay to Hi Z from JTCLK Falling Edge	0		20	ns	
Any digital output	t7	Delay from JTCLK Falling Edge	0		20	ns	1
Any digital output	t7	Delay from JTCLK Rising Edge	0		20	ns	2
Any digital output	t8	Delay out of Hi Z from JTCLK Falling Edge	0		20	ns	1
Any digital output	t9	Delay into Hi Z from JTCLK Falling Edge	0		20	ns	1
Any digital output	t8	Delay out of Hi Z from JTCLK Rising Edge	0		20	ns	2, 3
Any digital output	t9	Delay into Hi Z from JTCLK Rising Edge	0		20	ns	2, 3

Note 1: Change during Update-DR state.

Note 2: Change during Update-IR state to or from EXTEST mode.

Note 3: Change during Update-IR state to or from HIZ mode.

17 PACKAGE INFORMATION

For the latest package outline information and land patterns (footprints), go to **www.maxim-ic.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
100 CSBGA	X100+4	**21-0352**	**90-0292**

18 THERMAL INFORMATION

Table 18-1. Thermal Information

PARAMETER	VALUE
Target Ambient Temperature Range	-40°C to +85°C
Die Junction Temperature Range	-40°C to +125°C
Theta-JA, Still Air (Note 1)	38.5°C/W

Note 1: Theta-JA is based on the package mounted on a four-layer JEDEC board and measured in a JEDEC test chamber.

19 REVISION HISTORY

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	101404	New product release.	—
1	050506	Removed LQFP package from data sheet.	1, 25, 26, 27, 208, 209, 212, 214, 215
2	3/11	Added lead(Pb)-free devices to the Ordering Information	1
		Section 4.1 Global Features corrected. From: On-chip clock rate adapter incorporates two separate internal PLLs to generate the necessary DS3 or E3 clock used internally from an input clock reference (DS3, E3, 51.84 MHz, 77.76 MHz, or 19.44 MHz) and to provide an output reference clock for external usage To: On-chip clock rate adapter incorporates two separate internal PLLs to generate the necessary DS3 or E3 clock used internally from an input clock reference (DS3, E3, 51.84 MHz, 77.76 MHz, or 19.44 MHz)	13
		Section 10.1.7 Interrupt and Pin Modes. Replaced “float” with “high impedance”	54
		Section 15 DC electrical characteristics, ABSOLUTE MAXIMUM RATINGS. Updated Soldering Temperature to include Pb and Pb free	211
		Table 15-2. DC Electrical Characteristics. Replaced “Hi-Z” with “High Impedance”	211

Note: *To obtain a revision history for the preliminary releases of this document, contact the factory at* ***www.maxim-ic.com/support****.*

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