

24-Bit, 192-kHz Sampling, Advanced Segment, Audio-Stereo Digital-to-Analog Converter

FEATURES

- **24-Bit Resolution**
- **Analog Performance (V_{CC} = 5 V):**
  - **Dynamic Range: 117 dB (typical)**
  - **SNR: 117 dB (typical)**
  - **THD+N: 0.0004% (typical)**
  - **Full-Scale Output: 2.2 Vrms (at Postamplifier)**
- **Differential Current Output: ±2.48 mA**
- **Sampling Frequency: 10 kHz to 200 kHz**
- **System Clock: 128, 192, 256, 384, 512, or 768 f_S With Autodetect**
- **Accepts 16-, 20-, and 24-Bit Audio Data**
- **Data Formats: Standard, I^2S, and Left-Justified**
- **8× Oversampling Digital Filter:**
  - **Stop-Band Attenuation: –82 dB**
  - **Pass-Band Ripple: ±0.002 dB**
- **Optional Interface to External Digital Filter Available**
- **Optional Interface to DSD Decoder for SACD Playback**
- **User-Programmable Mode Controls:**
  - **Digital Attenuation: 0 dB to –120 dB, 0.5 dB/Step**
  - **Digital De-Emphasis**
  - **Digital Filter Rolloff: Sharp or Slow**
  - **Soft Mute**
  - **Zero-Detect Mute**
  - **Zero Flags for Each Output**
- **Dual-Supply Operation:**
  - **5-V Analog, 3.3-V Digital**
- **5-V Tolerant Digital Inputs**
- **Small SSOP-28 Package**

APPLICATIONS

- **AV Receivers**
- **DVD Movie Players**
- **SACD Players**
- **HDTV Receivers**
- **Car Audio Systems**
- **Digital Multitrack Recorders**
- **Other Multichannel Audio Systems**

DESCRIPTION

The PCM1738 is a CMOS, monolithic, integrated circuit (IC) that includes stereo digital-to-analog converters (DACs) and support circuitry in a small SSOP-28 package. The data converters use a newly developed advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1738 provides balanced current outputs, allowing the user to optimize analog performance externally, and accepts industry-standard audio data formats with 16- to 24-bit data, providing easy interfacing to audio DSP and decoder chips. Sampling rates up to 200 kHz are supported. The PCM1738 also has two optional modes of operation: an external digital filter mode (for use with the DF1704, DF1706, and PMD200), and a DSD decoder interface for SACD playback applications. A full set of user-programmable functions is accessible through a 4-wire serial control port that supports register write and read functions.

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This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted)(1)

		VALUE	UNIT
Power supply voltage	$V_{CC}1$, $V_{CC}2$, and $V_{CC}3$	6.5	V
	V_{DD}	4	V
Supply voltage differences among $V_{CC}1$, $V_{CC}2$, and $V_{CC}3$		±0.1	V
Supply voltage differences, V_{CCX}, V_{DD}		$V_{CCX} – V_{DD} < 3$	V
Ground voltage differences among AGND1, AGND2, and DGND		±0.1	V
Digital input voltage, LRCK, DATA, BCK, SCKI, MDI, MC, $\overline{CS}$, MUTE, and $\overline{RST}$		–0.3 to 6.5	V
Digital input voltage, ZEROL, ZEROR, SCKO, and MDO		–0.3 to (V_{DD} + 0.3) < 4	V
Analog input voltage, $I_{OUT}R–$, $I_{OUT}R+$, $V_{COM}1$, $V_{COM}2$, $V_{COM}3$, I_{REF}, $I_{OUT}L+$, and $I_{OUT}L–$		–0.3 to (V_{CC} + 0.3) < 6.5	V
Input current (except power supply)		±10	mA
Ambient temperature under bias		–40 to 125	°C
Storage temperature		–55 to 150	°C
Junction temperature		150	°C
Lead temperature (soldering)		260	°C, 5 s
Package temperature (reflow, peak)		235	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted)

PARAMETER	TEST CONDITIONS	PCM1738E			UNIT
		MIN	TYP	MAX	
RESOLUTION			24		Bits
DATA FORMAT					
Audio data interface formats			Standard, I^2S, left-justified		
Audio data bit length			16-, 20-, 24-bit, selectable		
Audio data format			MSB-first, 2s-complement		
Sampling frequency (f_S)		10		200	kHz
System clock frequency			128, 192, 256, 384, 512, 768 f_S		

ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PCM1738E			UNIT
			MIN	TYP	MAX	
DIGITAL INPUT/OUTPUT						
Logic family				TTL compatible		
V_{IH}	Input logic level		2			VDC
V_{IL}					0.8	
I_{IH}	Input logic current	$V_{IN} = V_{DD}$			10	µA
I_{IL}		V_{IN} = 0 V			–10	
V_{OH}	Output logic level	I_{OH} = –2 mA	2.4			VDC
V_{OL}		I_{OL} = 2 mA			1	
I_{OHZ}	High-impedance output logic current(1)	$V_{OUT} = V_{DD}$			5	µA
I_{OLZ}					5	
DYNAMIC PERFORMANCE(2)						
THD+N	Total harmonic distortion + noise	f_S = 44.1 kHz, V_{OUT} = 0 dB		0.0004%	0.0008%	
		f_S = 96 kHz, V_{OUT} = 0 dB		0.0006%		
		f_S = 192 kHz, V_{OUT} = 0 dB		0.0012%		
	Dynamic range	EIAJ, A-weighted, f_S = 44.1 kHz	114	117		dB
		A-weighted, f_S = 96 kHz		117		
		A-weighted, f_S = 192 kHz		117		
SNR	Signal-to-noise ratio	EIAJ, A-weighted, f_S = 44.1 kHz	114	117		dB
		A-weighted, f_S = 96 kHz		117		
		A-weighted, f_S = 192 kHz		117		
	Channel separation	f_S = 44.1 kHz	110	115		dB
		f_S = 96 kHz		113		
		f_S = 192 kHz		111		
	Level linearity error	V_{OUT} = –110 dB		±1		dB
DC ACCURACY						
	$V_{CCM}2$ voltage			2.45		V
	$V_{CCM}2$ output current	$\Delta V_{COM}2$ < 5%		100		µA
	Gain error			±2		% of FSR
	Gain mismatch, channel-to-channel			±0.5		% of FSR
	Bipolar zero error	At bipolar zero		±0.5		% of FSR
DSD-MODE DYNAMIC PERFORMANCE at 44.1 kHz, 64 f_S(3)						
THD+N	Total harmonic distortion + noise	±2.48 mAp-p, full scale		0.0004%		
	Dynamic range	–60 dB, EIAJ, A-weighted		117		dB
SNR	Signal-to-noise ratio	EIAJ, A-weighted		117		dB
ANALOG OUTPUT						
	Output current	Full scale (0 dB)		±2.48		mAp-p
	DSD mode output current	50% output		±1.24		mAp-p
	Center current	Bipolar zero input		0		mA

(1) Pin 11 (MDO)
(2) Analog performance specifications are measured using an Audio Precision™System Two™ audio measurement system in the averaging mode. At 44.1-kHz operation, bandwidth measurement is limited to 20 kHz. At 96 kHz and 192 kHz, bandwidth measurement is limited to 40 kHz.
(3) Theoretical performance in DSD modulation index of 100%. Performance is equivalent to the PCM mode.

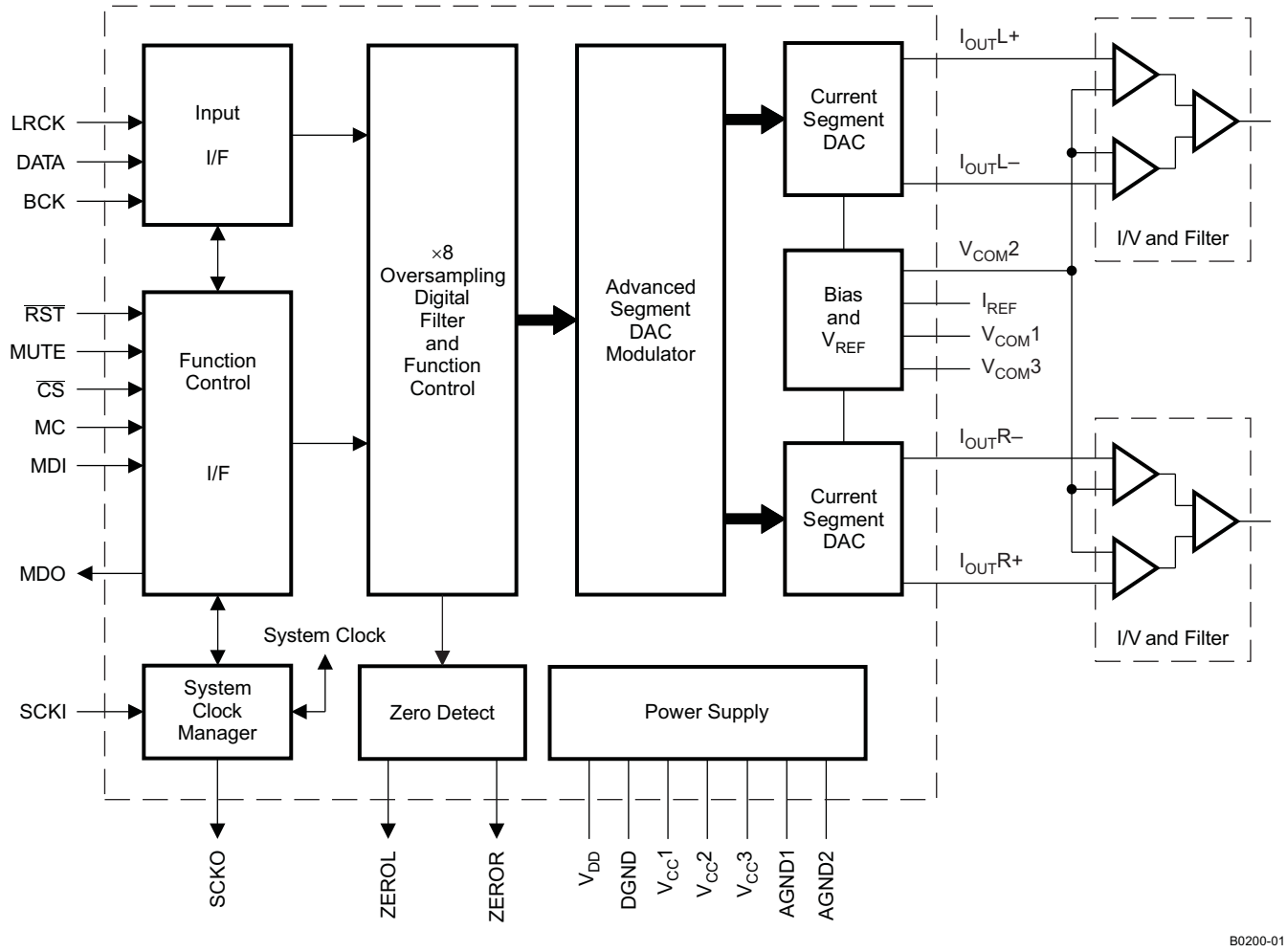
ELECTRICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted)

PARAMETER		TEST CONDITIONS	PCM1738E			UNIT
			MIN	TYP	MAX	
DIGITAL-FILTER PERFORMANCE **Filter Characteristics 1, Sharp Rolloff**						
	Pass band	±0.002 dB			0.454 f_S	Hz
	Pass band	–3 dB			0.49 f_S	Hz
	Stop band		0.546 f_S			Hz
	Pass-band ripple				±0.002	dB
	Stop-band attenuation	Stop band = 0.546 f_S	–75			dB
	Stop-band attenuation	Stop band = 0.567 f_S	–82			dB
Filter Characteristics 2, Slow Rolloff						
	Pass band	±0.04 dB			0.274 f_S	Hz
	Pass band	–3 dB			0.454 f_S	Hz
	Stop band		0.732 f_S			Hz
	Pass-band ripple				±0.002	dB
	Stop-band attenuation	Stop band = 0.732 f_S	–82			dB
	Delay time			29/f_S		sec
	De-emphasis error				±0.1	dB
POWER SUPPLY REQUIREMENTS						
V_{DD}	Voltage range		3	3.3	3.6	VDC
V_{CC}			4.75	5	5.25	
I_{DD} (4)	Supply current	V_{DD} = 3.3 V, f_S = 44.1 kHz		7	9.8	mA
		V_{DD} = 3.3 V, f_S = 96 kHz		15		
		V_{DD} = 3.3 V, f_S = 192 kHz		30		
I_{CC}		V_{CC} = 5 V, f_S = 44.1 kHz		33	46.2	mA
		V_{CC} = 5 V, f_S = 96 kHz		34.5		
		V_{CC} = 5 V, f_S = 192 kHz		36.5		
	Power dissipation	V_{DD} = 3.3 V, V_{CC} = 5 V, f_S = 44.1 kHz		188	263	mW
		V_{DD} = 3.3 V, V_{CC} = 5 V, f_S = 96 kHz		222		
		V_{DD} = 3.3 V, V_{CC} = 5 V, f_S = 192 kHz		282		
TEMPERATURE RANGE						
	Operation temperature		–25		85	°C
θ_{JA}	Thermal resistance			100		°C/W

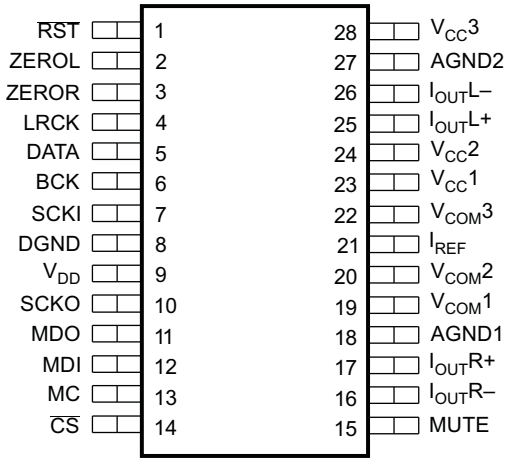
(4) SCKO is disabled. Input is bipolar zero data.

BLOCK DIAGRAM



B0200-01

PCM1738
(TOP VIEW)



P0007-04

Table 1. TERMINAL FUNCTIONS

TERMINAL		TYPE	DESCRIPTION
NAME	NO.		
AGND1	18	—	Analog ground 1
AGND2	27	—	Analog ground 2
$\overline{CS}$	14	IN	Chip select and latch for mode control (1)
BCK	6	IN	Bit-clock input. Connected to GND for DSD mode (1)
DATA	5	IN	Serial audio data input for normal operation. L-channel audio data input for external DF and DSD modes (1)
DGND	8	—	Digital ground
$I_{OUT}L+$	25	OUT	L-channel analog current output +
$I_{OUT}L-$	26	OUT	L-channel analog current output –
$I_{OUT}R+$	17	OUT	R-channel analog current output +
$I_{OUT}R-$	16	OUT	R-channel analog current output –
I_{REF}	21	—	Output current reference bias pin. Connect 16-kΩ resistor to GND.
LRCK	4	IN	Left/right clock (f_S) input for normal operation. WDCK clock input in external DF mode. Connected to GND in DSD mode (1)
MC	13	IN	Shift clock for mode control (1)
MDI	12	IN	Serial data input for mode control (1)
MDO	11	OUT	Serial data output for mode control
MUTE	15	IN	Analog output mute control for normal operation. R-channel audio data input for external DF and DSD modes (1)
$\overline{RST}$	1	IN	Reset (1)
SCKI	7	IN	System-clock input for normal operation. BCK ($64f_S$) clock input for DSD mode (1)
SCKO	10	OUT	System clock output
$V_{CC}1$	23	—	Analog power supply 1, 5-V
$V_{CC}2$	24	—	Analog power supply 2, 5-V
$V_{CC}3$	28	—	Analog power supply 3, 5-V
$V_{COM}1$	19	—	Internal bias decoupling 1
$V_{COM}2$	20	—	Internal bias decoupling 2 (common voltage for I/V)
$V_{COM}3$	22	—	Internal bias decoupling 3
V_{DD}	9	—	Digital supply, 3.3 V
ZEROL	2	OUT	Zero flag for L-channel
ZEROR	3	OUT	Zero flag for R-channel

(1) Schmitt-trigger input, 5-V tolerant.

TYPICAL PERFORMANCE CURVES

All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted).

DIGITAL FILTER

De-Emphasis Off, f_S = 44.1kHz

FREQUENCY RESPONSE (Sharp Rolloff)

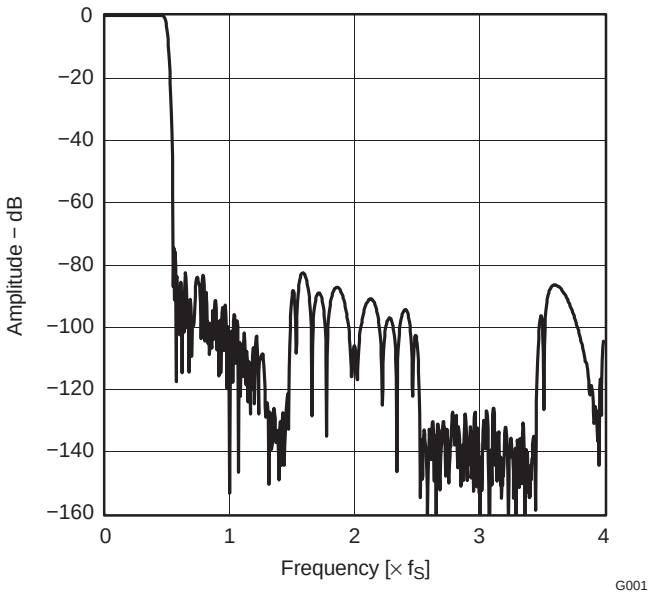


Figure 1.

PASS-BAND RIPPLE (Sharp Rolloff)

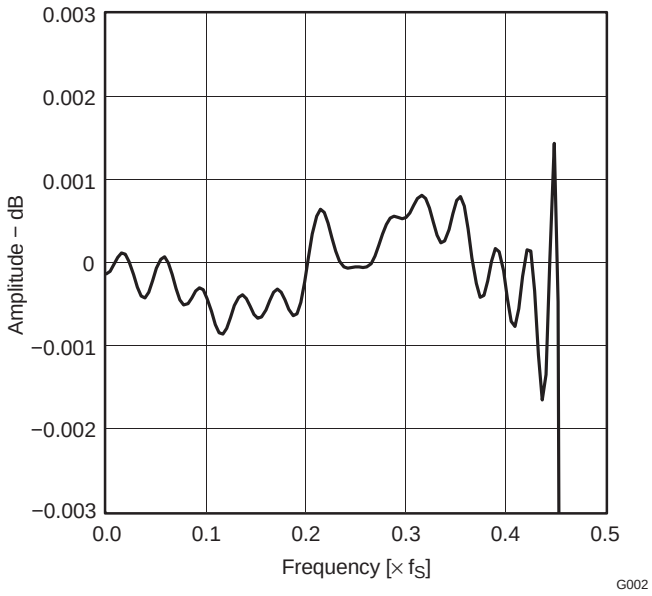


Figure 2.

FREQUENCY RESPONSE (Slow Rolloff)

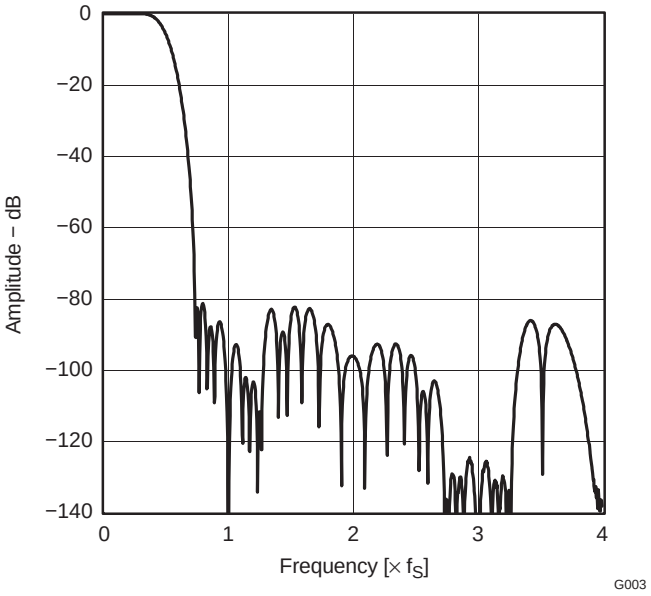


Figure 3.

TRANSITION CHARACTERISTICS (Slow Rolloff)

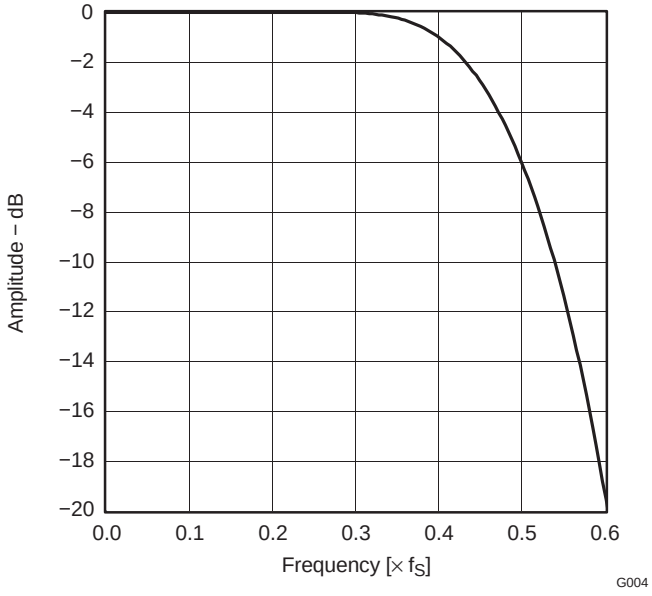


Figure 4.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted).

De-Emphasis Filter

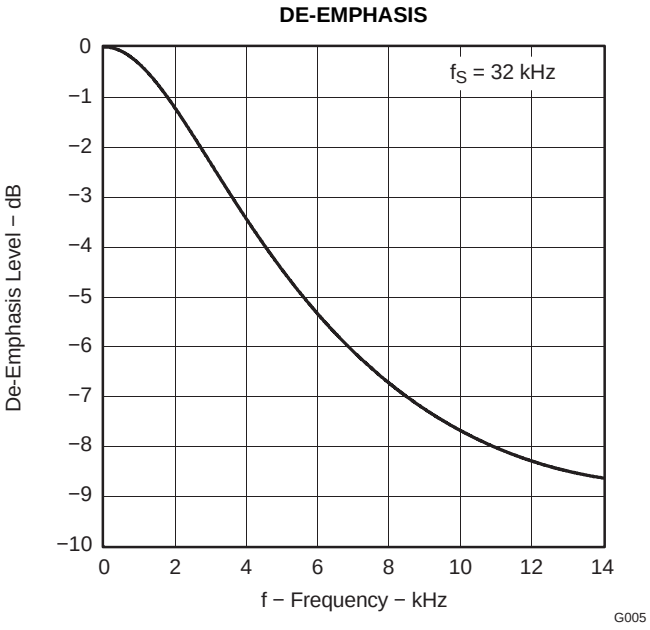


Figure 5.

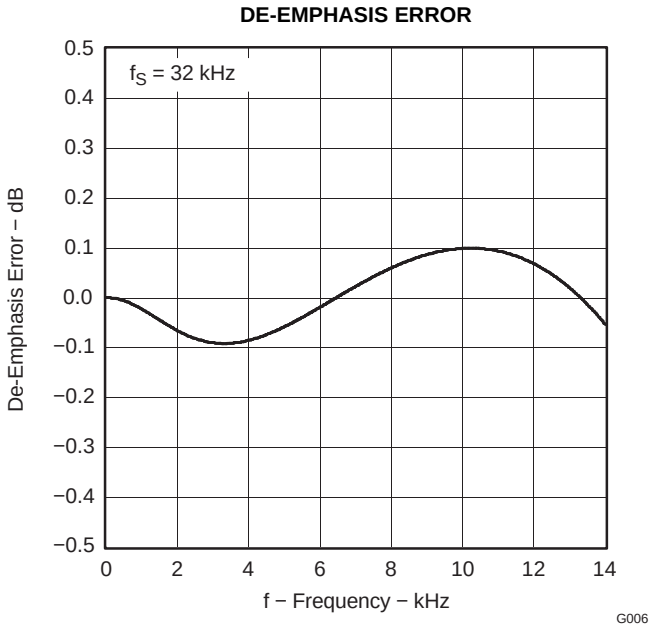


Figure 6.

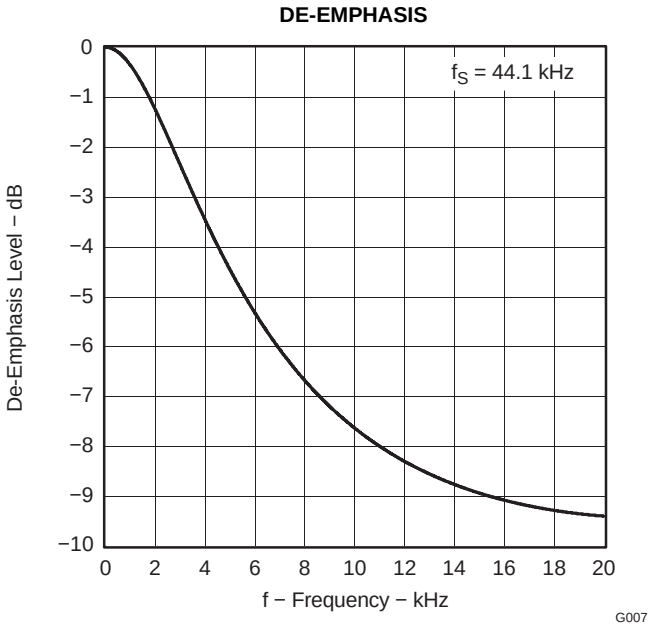


Figure 7.

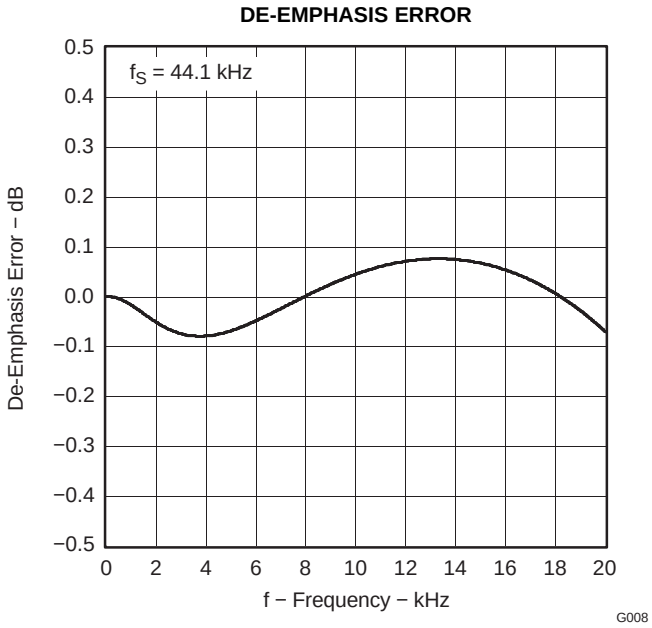


Figure 8.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted).

DE-EMPHASIS

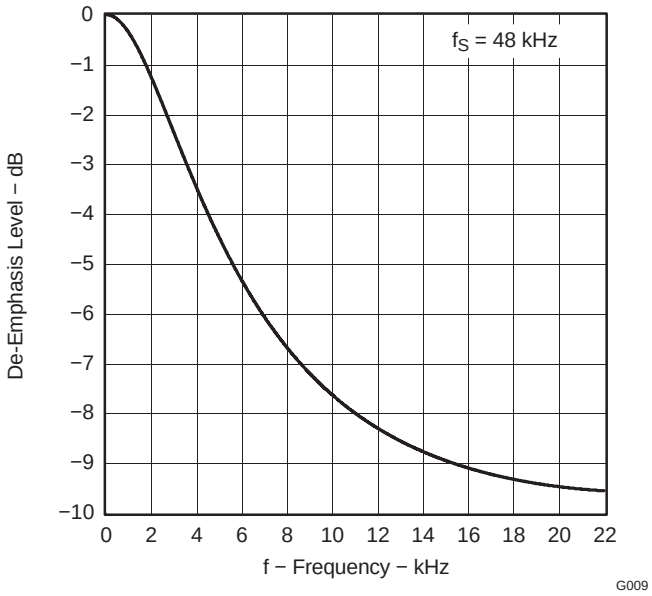


Figure 9.

DE-EMPHASIS ERROR

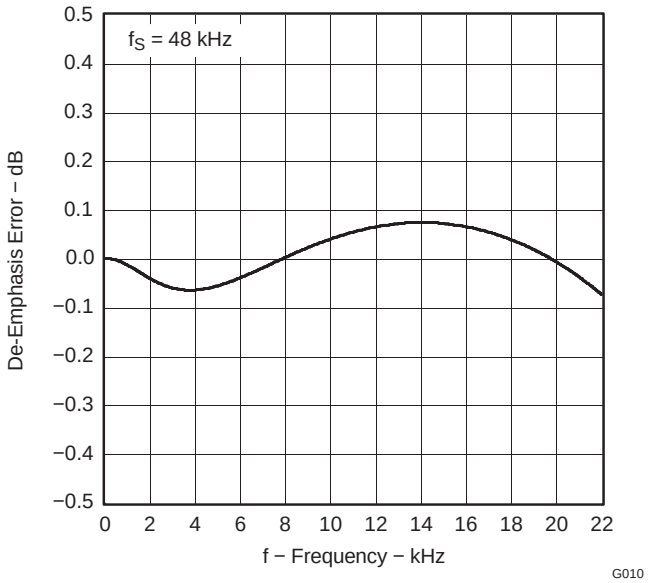


Figure 10.

ANALOG DYNAMIC PERFORMANCE

THD+N vs V_{CC}

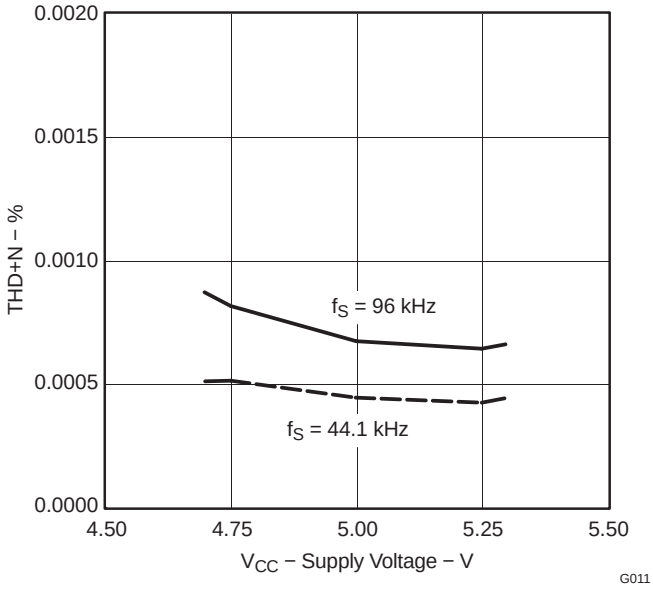


Figure 11.

THD+N vs TEMPERATURE

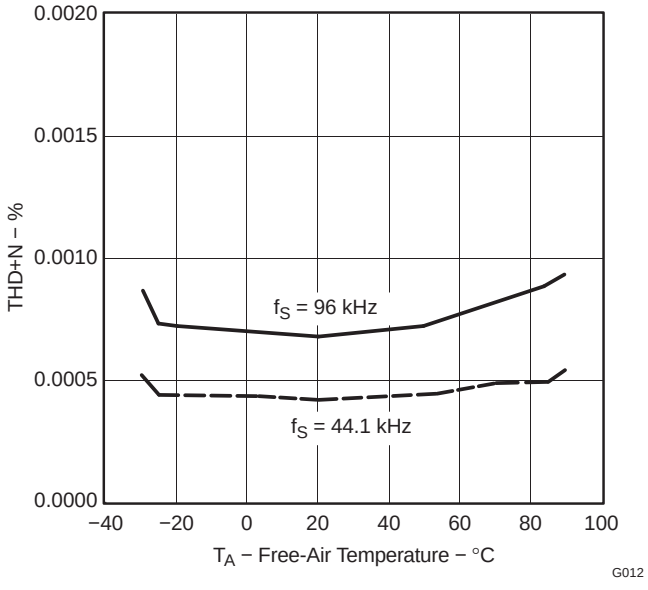


Figure 12.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted).

DYNAMIC RANGE vs V_{CC}

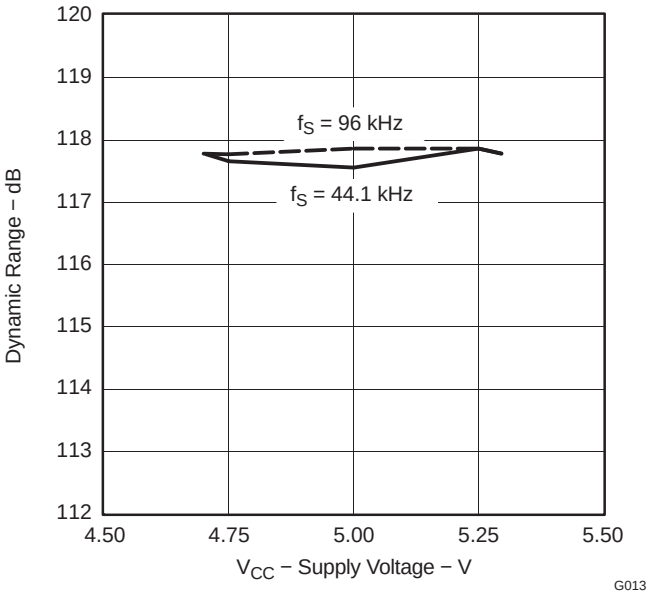


Figure 13.

DYNAMIC RANGE vs TEMPERATURE

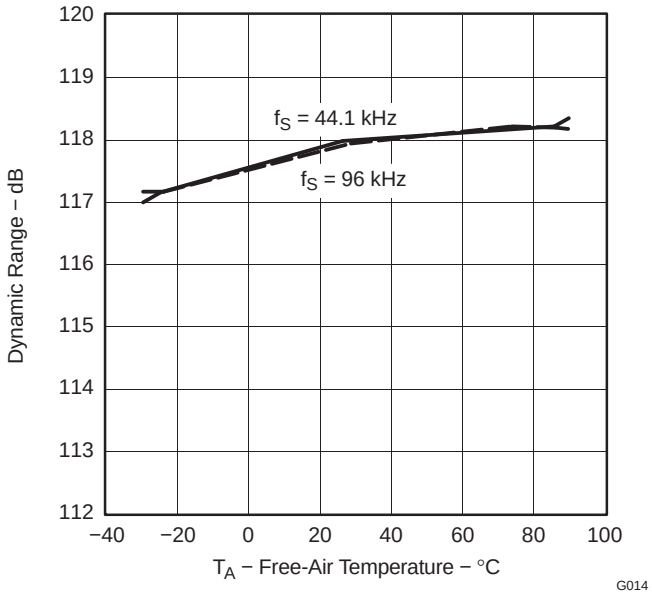


Figure 14.

SIGNAL-TO-NOISE RATIO vs V_{CC}

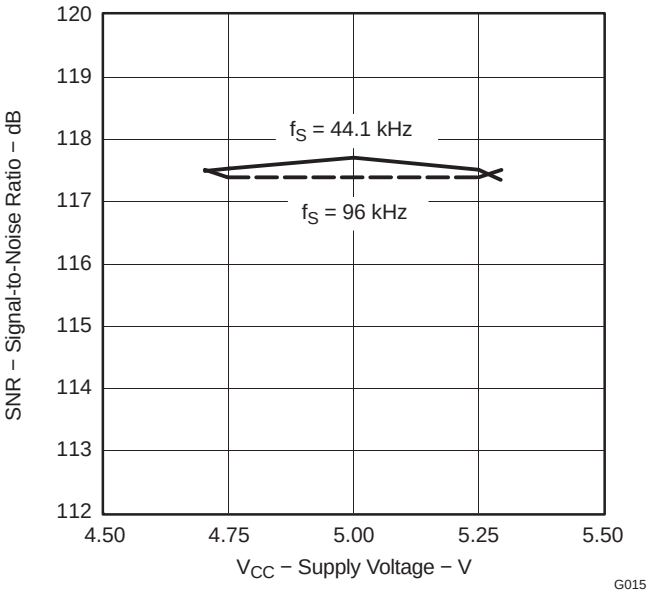


Figure 15.

SIGNAL-TO-NOISE RATIO vs TEMPERATURE

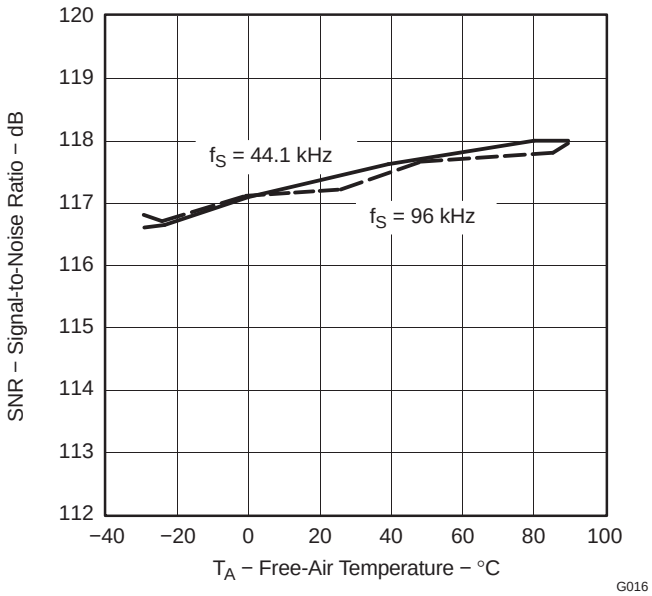


Figure 16.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted).

CHANNEL SEPARATION vs V_{CC}

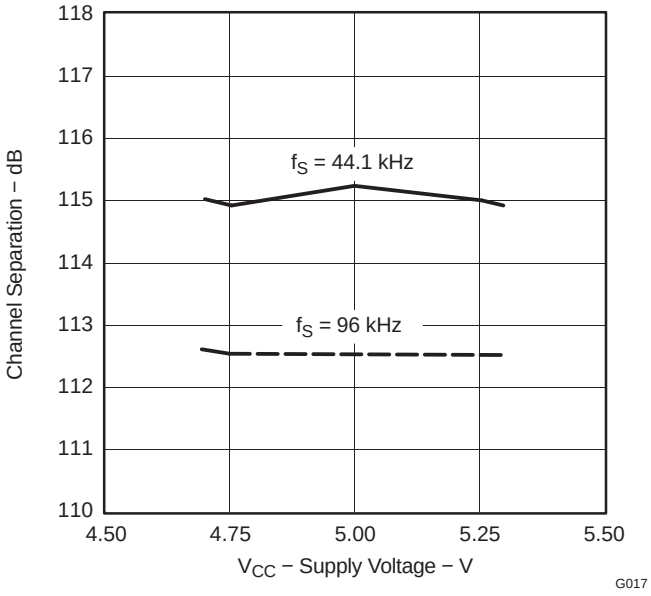


Figure 17.

CHANNEL SEPARATION vs TEMPERATURE

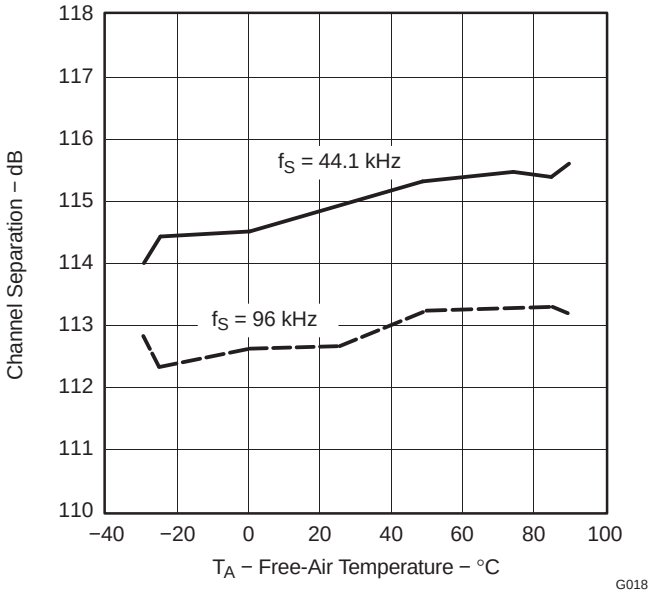


Figure 18.

–60-dB OUTPUT SPECTRUM (BW = 20 kHz)

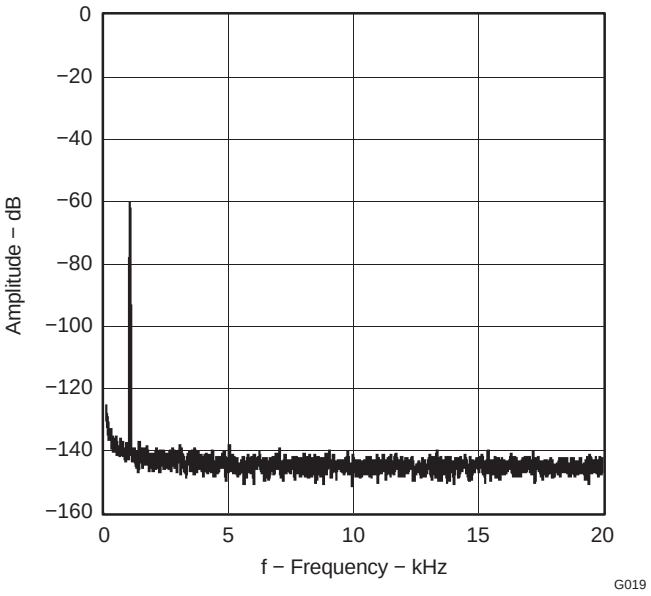


Figure 19.

–60-dB OUTPUT SPECTRUM (BW = 100 kHz)

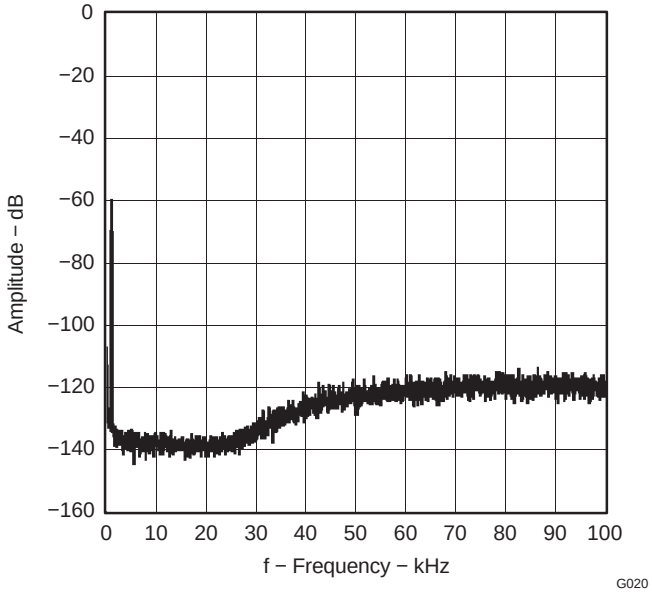


Figure 20.

TYPICAL CHARACTERISTICS (continued)

All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 256 f_S (f_S = 44.1 kHz), and 24-bit input data (unless otherwise noted).

THD+N vs LEVEL (PCM MODE)

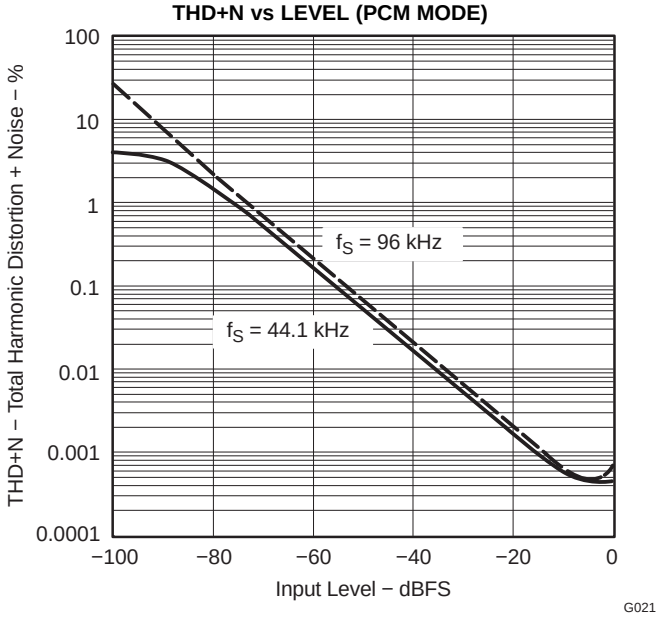


Figure 21.

All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 64 f_S (f_S = 44.1 kHz), and DSD input data (44.1 kHz, 64 f_S, DSD modulator index of 0.5) (unless otherwise noted)

–60-dB OUTPUT SPECTRUM (DSD MODE)

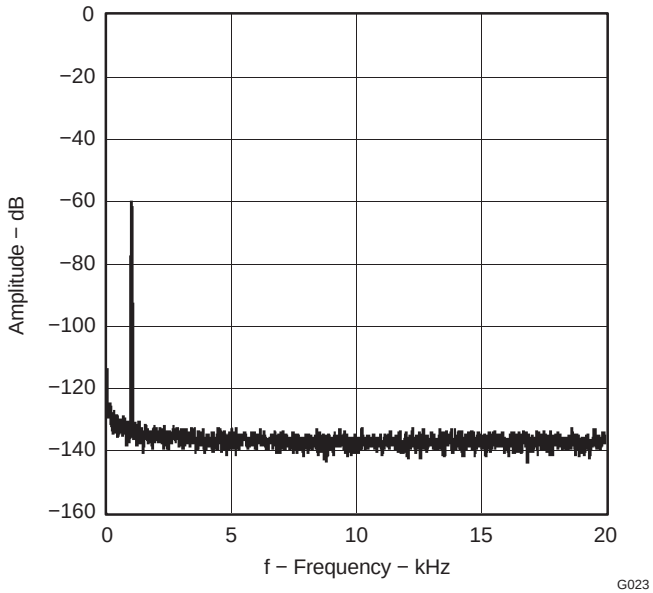


Figure 22.

THD+N vs LEVEL (DSD MODE)

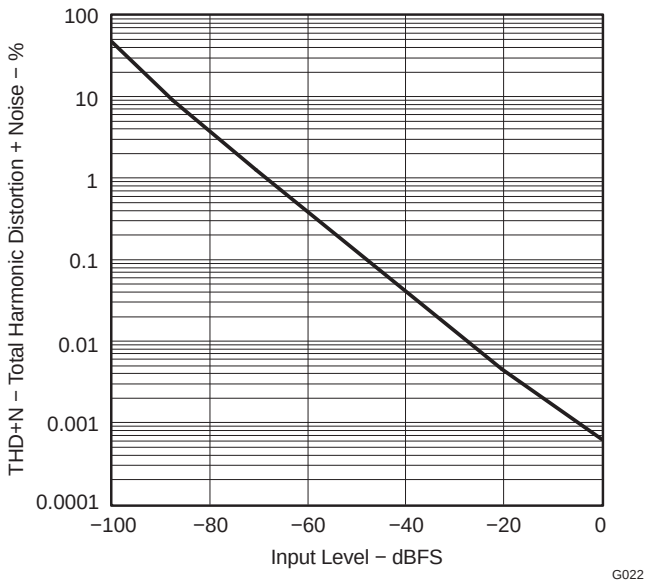


Figure 23.

ANALOG FIR FILTER PERFORMANCE FOR DSD MODE

All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 11.2896 MHz (44.1 kHz × 256 f_S), and 50% modulation DSD data input (unless otherwise noted)

DSD FILTER 1

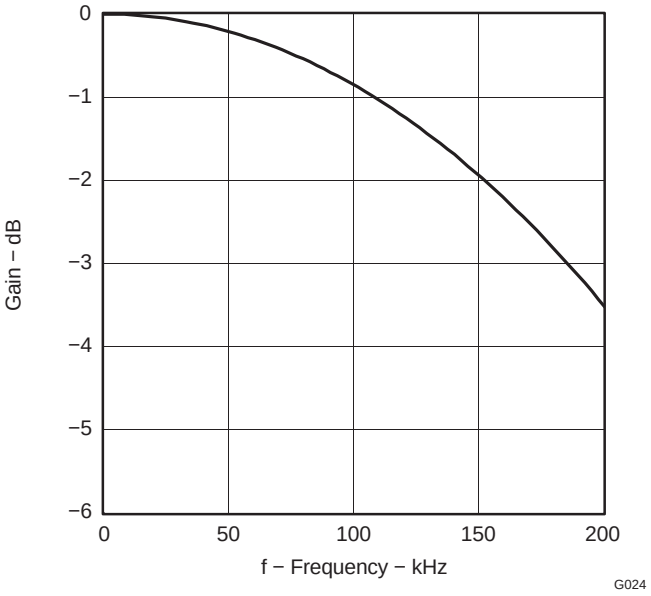


Figure 24.

DSD FILTER 1

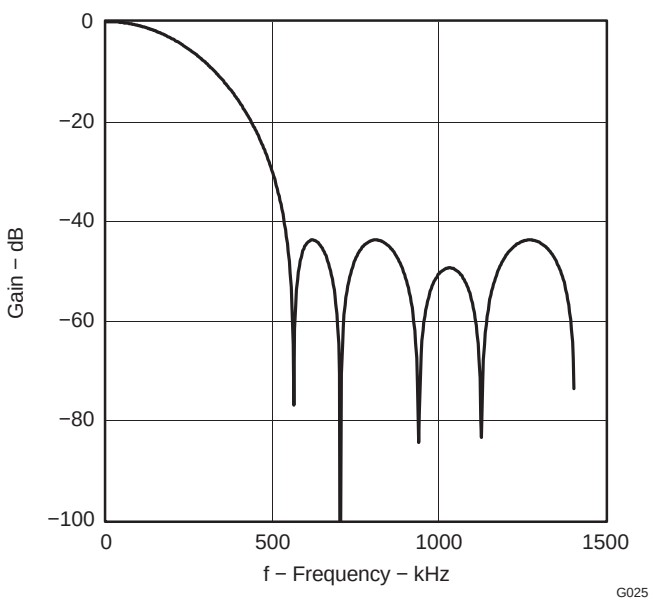


Figure 25.

DSD FITLER 2

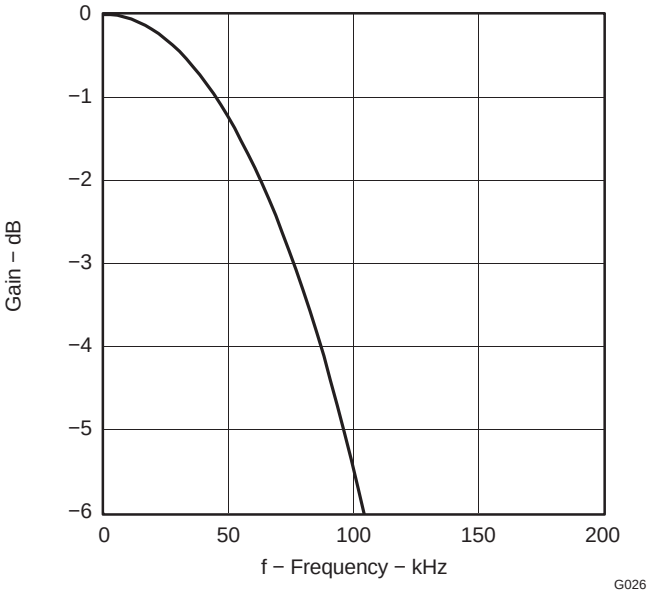


Figure 26.

DSD FITLER 2

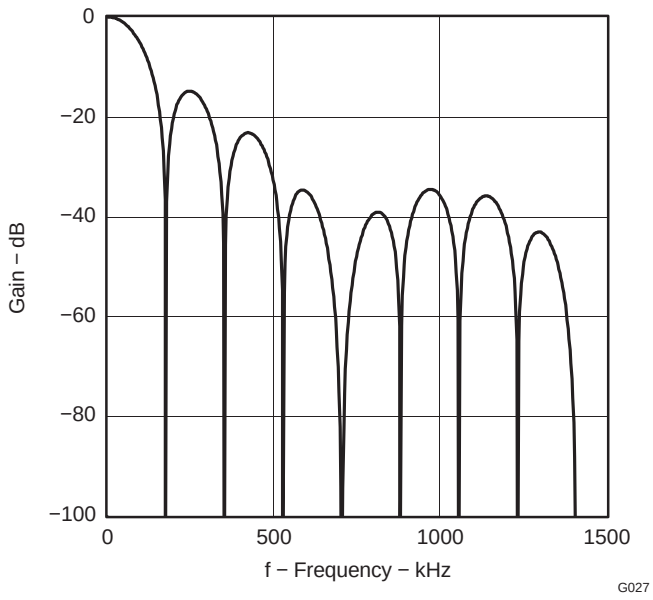


Figure 27.

ANALOG FIR FILTER PERFORMANCE FOR DSD MODE (continued)

All specifications at T_A = 25°C, V_{DD} = 3.3 V, V_{CC} = 5 V, SCKI = 11.2896 MHz (44.1 kHz × 256 f_S), and 50% modulation DSD data input (unless otherwise noted)

DSD FITLER 3

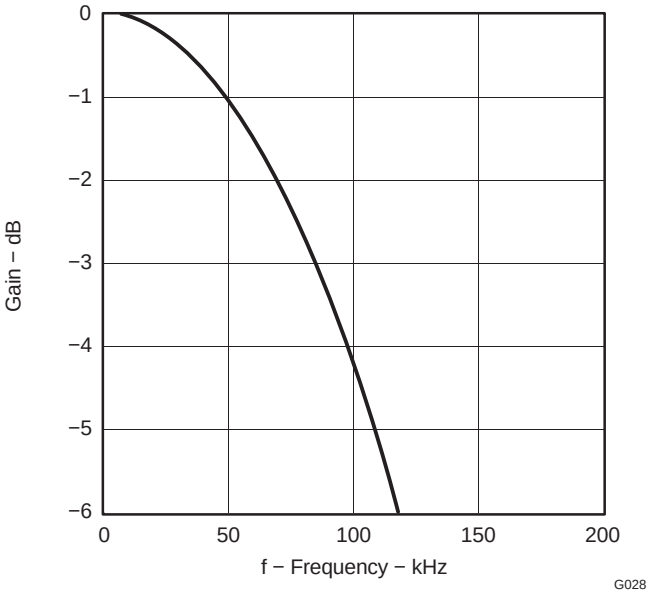


Figure 28.

DSD FITLER 3

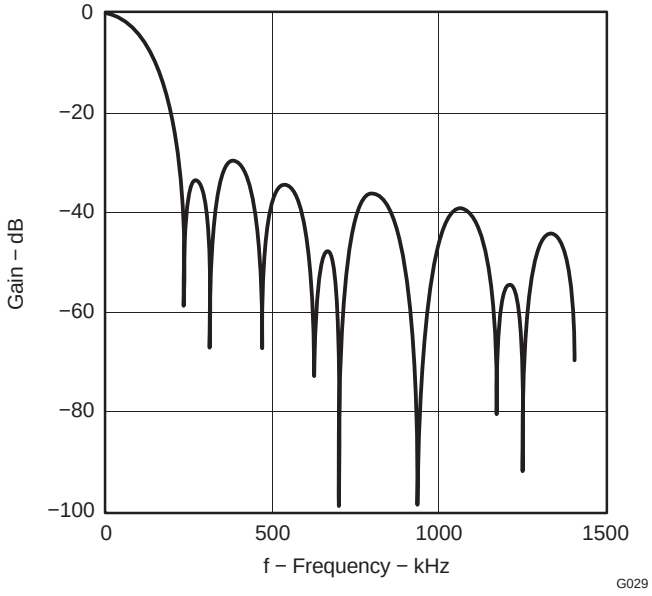


Figure 29.

DSD FITLER 4

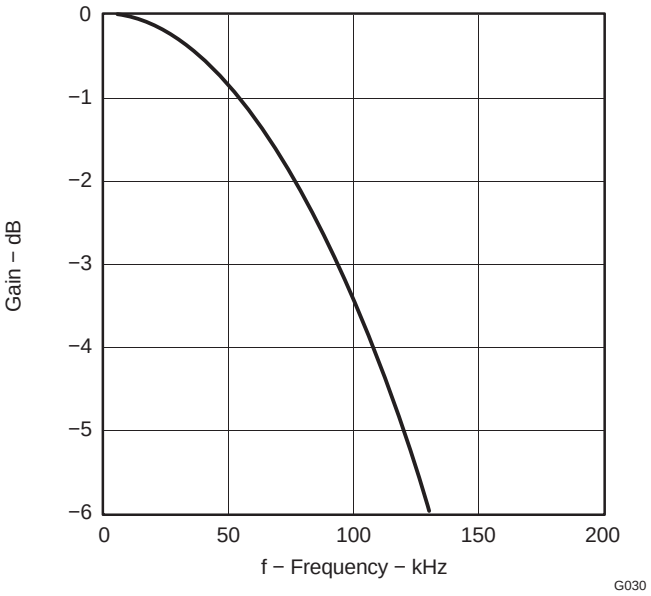


Figure 30.

DSD FITLER 4

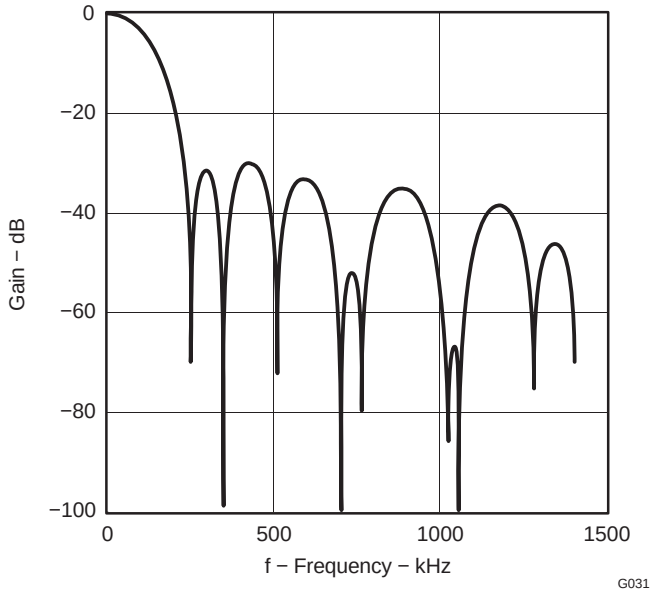


Figure 31.

SYSTEM CLOCK AND RESET FUNCTIONS

SYSTEM CLOCK INPUT

The PCM1738 requires a system clock for operating the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCKI input (pin 7). The PCM1738 has a system-clock detection circuit that automatically senses if the system clock is operating at 128 f_S to 768 f_S. Table 2 shows examples of system-clock frequencies for common audio sampling rates.

Figure 32 shows the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. The PLL1700 multiclock generator is an excellent choice for providing the PCM1738 system clock.

SYSTEM CLOCK OUTPUT

A buffered version of the system clock input is available at the SCKO output (pin 10). SCKO can operate at either full (f_{SCKI}) or half ($f_{SCKI}/2$) rate. The SCKO output frequency may be programmed using the CLKD bit of mode control register 19. The SCKO output pin can also be enabled or disabled using the CLKE bit of mode control register 19. The default is SCKO enabled.

POWER-ON AND EXTERNAL RESET FUNCTIONS

The PCM1738 includes a power-on-reset function (see Figure 33). The system clock input at SCKI should be active for at least one clock period prior to V_{DD} = 2 V. With the system clock active, and V_{DD} > 2 V, the power-on-reset function is enabled. The initialization sequence requires 1024 system clocks from the time V_{DD} > 2 V. After the initialization period, the PCM1738 is set to its reset default state, as described in the *Mode Control Registers* section of this data sheet.

The PCM1738 also includes an external reset capability using the $\overline{RST}$ input (pin 1). This allows an external controller or master reset circuit to force the PCM1738 to initialize to its reset default state.

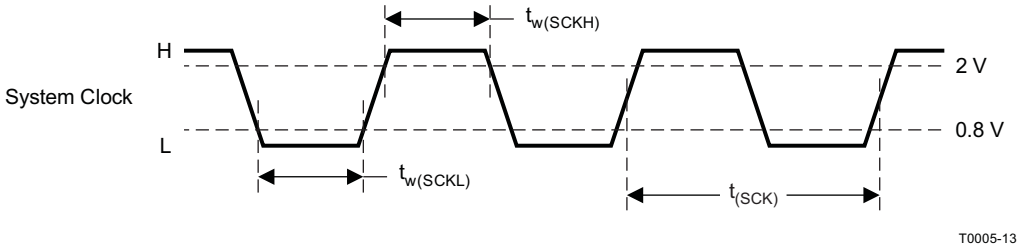
See Figure 34 for external reset operation and timing. The $\overline{RST}$ pin is set to a logic 0 for a minimum of 20 ns. The $\overline{RST}$ pin is then set to a logic-1 state that starts the initialization sequence that requires 1024 system clock periods. After the initialization sequence is complete, the PCM1738 is set to its reset default state, as described in the *Mode Control Registers* section of this data sheet.

The external reset is especially useful in applications where there is a delay between PCM1738 power up and system-clock activation. In this case, the $\overline{RST}$ pin should be held at a logic-0 level until the system clock has been activated. The $\overline{RST}$ pin may then be set to a logic-1 state to start the initialization sequence.

Table 2. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY	SYSTEM CLOCK FREQUENCY (f_{SCLK}) (MHz)					
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S
32 kHz	4.096	6.144	8.192	12.288	16.384	24.576
44.1 kHz	5.6488	8.4672	11.2896	16.9344	22.5792	33.8688
48 kHz	6.144	9.216	12.288	18.432	24.576	36.864
96 kHz	12.288	18.432	24.576	36.864	49.152	73.728
192 kHz	24.576	36.864	49.152	73.728	(1)	(1)

(1) This system clock is not supported for the given sampling frequency.



PARAMETER		MIN	MAX	UNIT
$t_{(SCK)}$	System clock cycle time	13		ns
$t_{w(SCKH)}$	System clock pulse duration, HIGH	5		ns
$t_{w(SCKL)}$	System clock pulse duration, LOW	5		ns

Figure 32. System Clock Input Timing

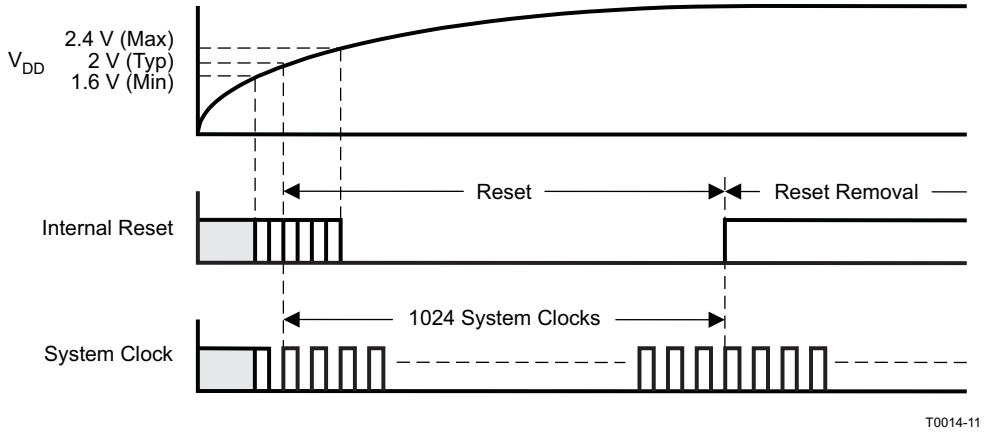
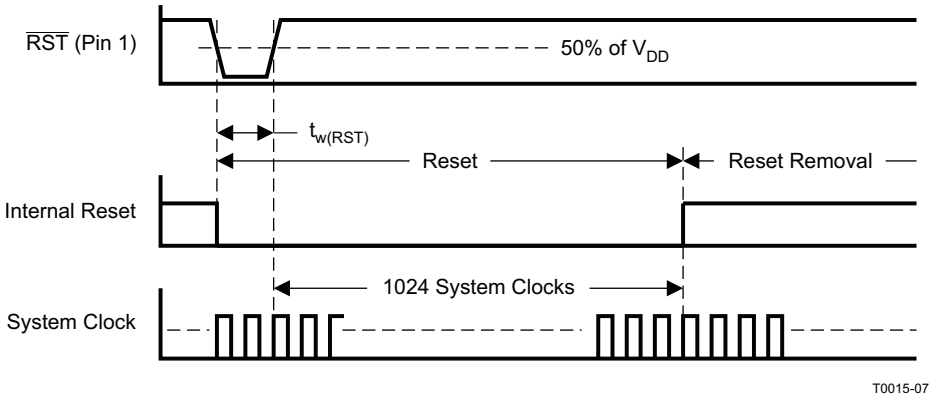


Figure 33. Power-On-Reset Timing



PARAMETER		MIN	MAX	UNIT
$t_{w(RST)}$	Reset pulse duration, LOW	20		ns

Figure 34. External Reset Timing

AUDIO DATA INTERFACE

AUDIO SERIAL INTERFACE

The audio serial interface for the PCM1738 consists of a 3-wire synchronous serial port. It includes LRCK (pin 4), BCK (pin 6), and DATA (pin 5). BCK is the serial audio bit clock, used to clock the serial data present on DATA into the audio interface serial shift register. Serial data is clocked into the PCM1738 on the rising edge of BCK. LRCK is the serial audio left/right word clock, used to latch serial data into the serial audio interface internal registers.

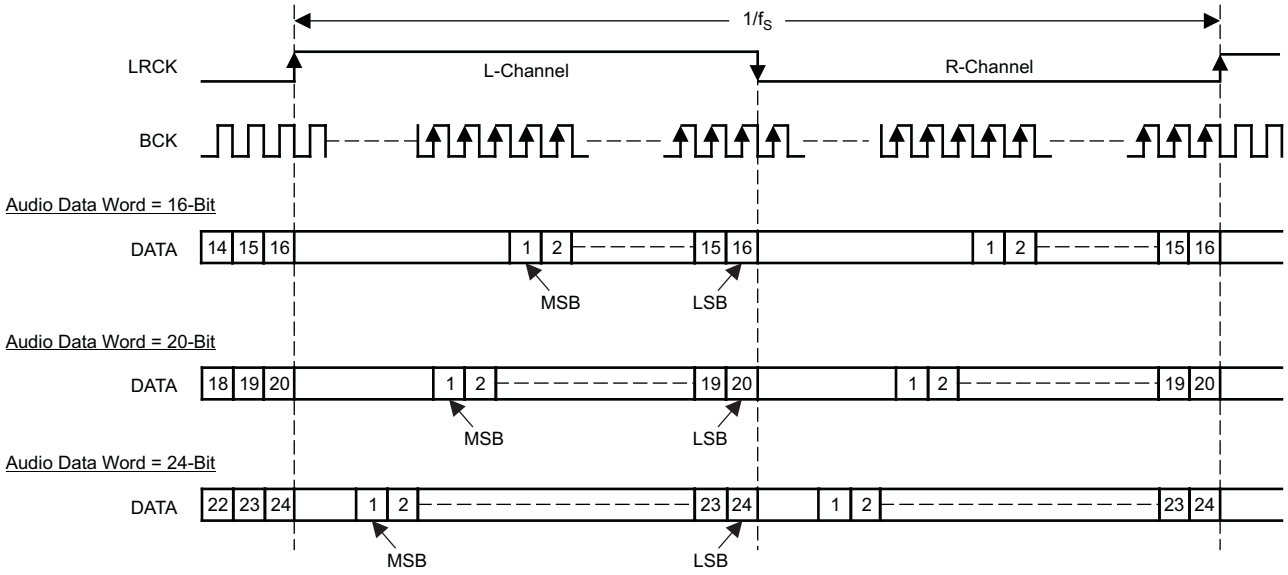
LRCK should be synchronous to the system clock. In the event these clocks are not synchronized, the PCM1738 can compensate for the phase difference internally. If the phase difference between LRCK and SCKI is greater than six bit clocks (BCK), the synchronization is performed internally. While the synchronization is processing, the analog output is forced to the bipolar zero level. The synchronization typically occurs in less than one cycle of LRCK.

Ideally, it is recommended that LRCK and BCK be derived from the system clock input or output, SCKI or SCKO. The left/right clock (LRCK) is operated at the sampling frequency, f_S.

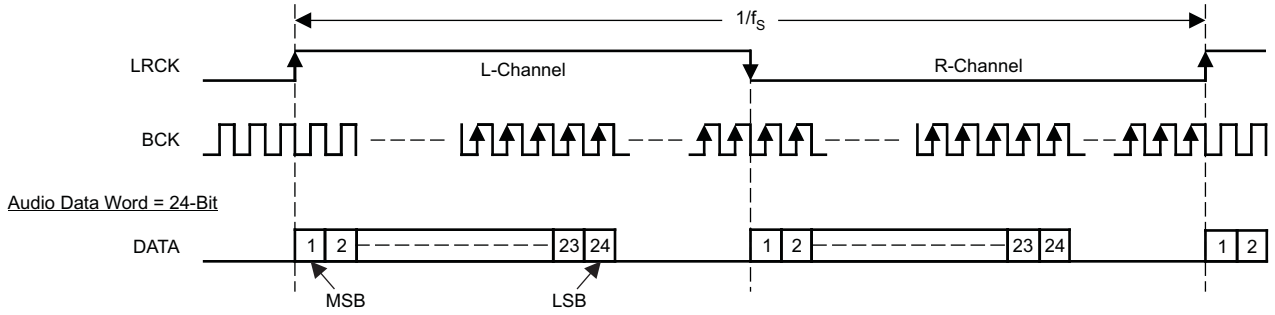
AUDIO DATA FORMATS AND TIMING

The PCM1738 supports industry-standard audio data formats, including standard right-justified, I^2S, and left-justified. The data formats are shown in Figure 35. Data formats are selected using the format bits, FMT [2:0], in mode control register 18. The default data format is 16-bit standard. All formats require binary 2s-complement, MSB-first audio data. Figure 36 shows a detailed timing diagram for the serial audio interface.

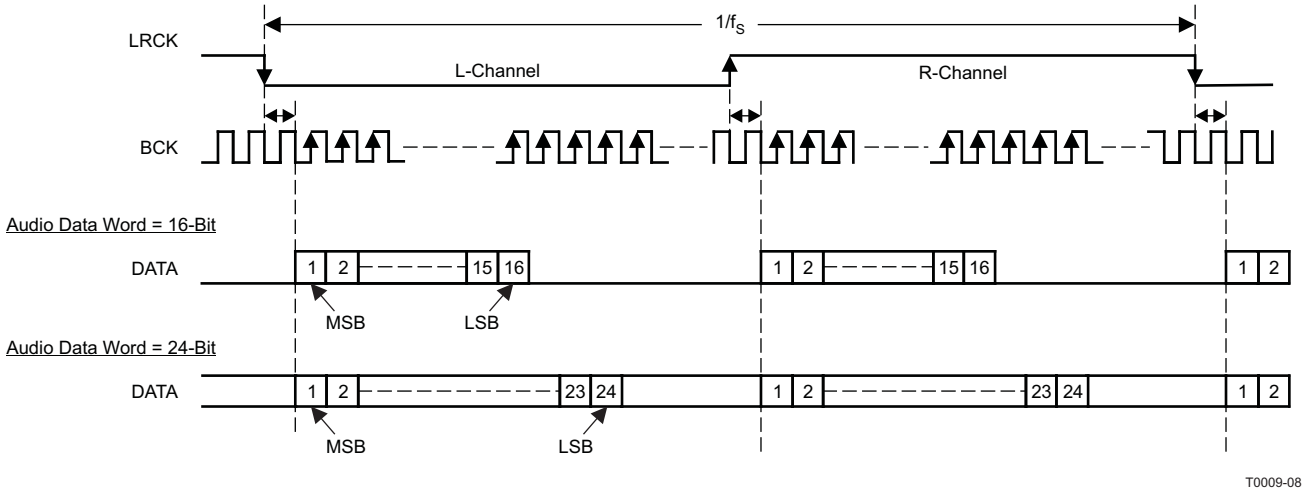
(1) Standard Data Format (Right-Justified): L-Channel = HIGH, R-Channel = LOW



(2) Left-Justified Data Format: L-Channel = HIGH, R-Channel = LOW

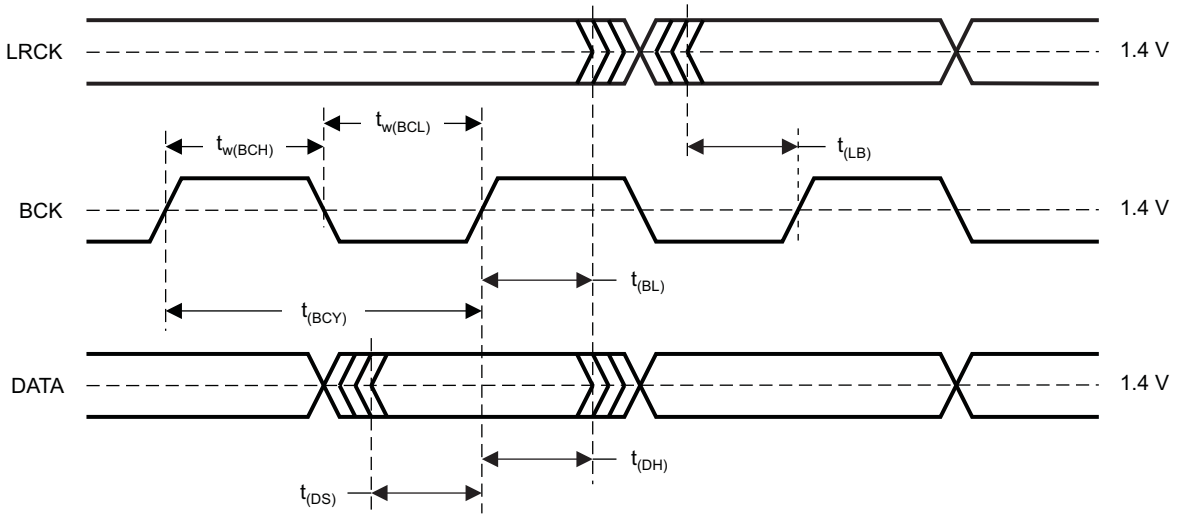


(3) I^2S Data Format: L-Channel = LOW, R-Channel = HIGH



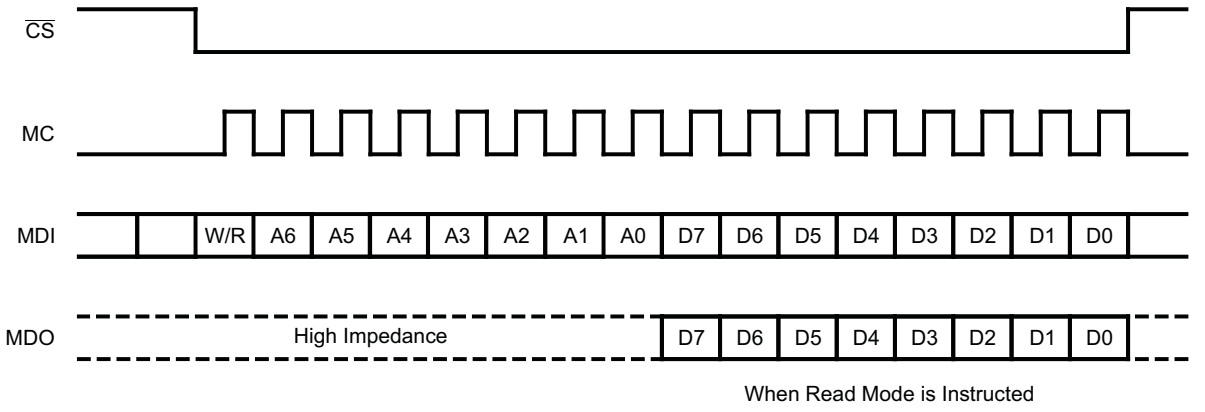
T0009-08

Figure 35. Audio Data Input Formats



PARAMETER		MIN	MAX	UNIT
$t_{(BCY)}$	BCK clock cycle time	70		ns
$t_{w(BCL)}$	BCK low-level time	30		ns
$t_{w(BCH)}$	BCK high-level time	30		ns
$t_{(BL)}$	BCK rising edge to LRCK edge	10		ns
$t_{(LB)}$	LRCK falling edge to BCK rising edge	10		ns
$t_{(DS)}$	DATA setup time	10		ns
$t_{(DH)}$	DATA hold time	10		ns
–	LRCK clock duty cycle	50% – 2 bit clocks	50% + 2 bit clocks	

Figure 36. Audio Interface Timing



NOTE: B15 is used for the selection of write or read. Setting W/R = 0 indicates a write, while W/R = 1 indicates a read.
B14–B8 are used for the register address.
B7–B0 are used for frgister data.

Figure 37. Serial Control Format

EXTERNAL DIGITAL FILTER INTERFACE AND TIMING

The PCM1738 supports an external digital-filter interface comprised of a 4-wire synchronous serial port that allows the use of an external digital filter. External filters include the DF1704 and DF1706 from Texas Instruments, the Pacific Microsonics PMD200, or a programmable digital signal processor.

The 4-wire interface includes WDCK as the word clock, BCK as the bit clock, DATAL as the L-channel data, and DATAR as the R-channel data. The external digital-filter interface is selected using the DFTH bit of mode control register 20, which functions to bypass the internal digital-filter portion of the PCM1738. The 4-wire serial port is assigned to WDCK (pin 4), BCK (pin 6), DATAL (pin 5), and DATAR (pin 15).

DSD (DIRECT STREAM DIGITAL) FORMAT INTERFACE AND TIMING

The PCM1738 supports a DSD format interface operation that includes out-of-band noise filtering using an internal analog FIR filter. For DSD operation, pin 7 is redefined as BCK, which operates at 64 $\times$ 44.1 kHz; pin 5 is redefined as DATAL (left-channel audio data), and pin 15 becomes DATAR (right-channel audio data). Pins 4 and 6 must be forced LOW in DSD mode. This configuration allows for direct interface to a DSD decoder for SACD applications. Detailed information for the DSD mode is provided in the *Application for DSD Format (DSD Mode) Interface* section of this data sheet.

FUNCTIONAL DESCRIPTIONS

ZERO DETECT

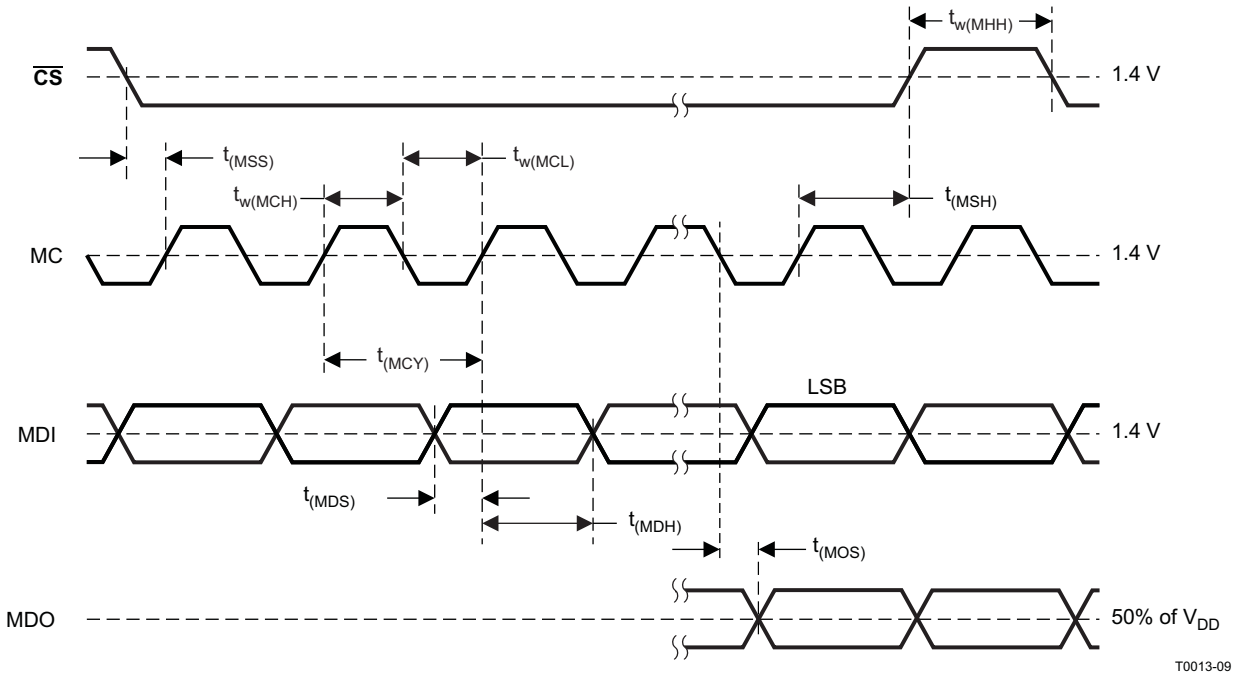
When the PCM1738 detects that the audio input data in the L-channel or R-channel is continuously zero for 1024 LRCKs, the PCM1738 sets ZEROL (pin 2) or ZEROR (pin 3) to HIGH. Setting the INZD bit of mode control register 19 can set both analog outputs to the bipolar zero level when the input data of both channels is zero.

SOFT MUTE

The PCM1738 supports mute operation by both hardware and software control. When MUTE (pin 15) is set to HIGH, both analog outputs are turned to the bipolar zero level. When the MUTE bit in mode control register 18 is set to 1, both analog outputs are also turned to the bipolar zero level. The speed to turn to the bipolar zero level is set by the ATS0 and ATS1 bits in mode congtrol register 19.

SERIAL CONTROL INTERFACE

The serial control interface is a 4-wire synchronous serial port that operates asynchronously to the serial audio interface and the system clock (SCKI). The serial control interface is used to program the on-chip mode control registers. The control interface includes MDO (pin 11), MDI (pin 12), MC (pin 13), and $\overline{CS}$ (pin 14). MDO is the serial data output, used to read back the values of the mode control registers; MDI is the serial data input, used to program the mode control registers; MC is the serial bit clock, used to shift data in and out of the control port; and $\overline{CS}$ is the mode control enable, used to enable the internal mode control register access. Figure 37 and Figure 38 show the format and timing for the serial control interface.



PARAMETER		MIN	MAX	UNIT
$t_{(MCY)}$	MC clock cycle time	100		ns
$t_{w(MCL)}$	MC low-level time	40		ns
$t_{w(MCH)}$	MC high-level time	40		ns
$t_{(MHH)}$	$\overline{CS}$ high-level time	80		ns
$t_{(MSS)}$	$\overline{CS}$ falling edge to MC rising edge	15		ns
$t_{(MSH)}$	$\overline{CS}$ hold time(1)	15		ns
$t_{(MDH)}$	MDI hold time	15		ns
$t_{(MDS)}$	MDI setup time	15		ns
$t_{(MOS)}$	MC falling edge to MDO stable		30	ns

(1) MC rising edge for LSB to $\overline{CS}$ rising edge

Figure 38. Control Interface Timing

MODE CONTROL REGISTERS

User-Programmable Mode Controls

The PCM1738 includes a number of user- programmable functions that are accessed via mode control registers. The registers are programmed using the serial control interface that was previously discussed in this data sheet. Table 3 lists the available mode control functions, along with their reset default conditions and associated register index.

Register Map

The mode control register map is shown in Table 4. Each register includes a W/R bit that indicates whether a register read (W/R = 1) or write (W/R = 0) operation is performed.

Table 3. User-Programmable Mode Controls

FUNCTION	DEFAULT	REGISTER	BIT
FUNCTIONS AVAILABLE FOR BOTH WRITE AND READ			
Digital attenuation control 0 dB to –120 dB in 0.5-dB steps	0 dB	16 for L-channel 17 for R-channel	ATL[7:0] ATR[7:0]
Attenuation load control Disabled, enabled	Attenuation disabled	18	ATLD
Attenuation speed selection ×1 f_S, ×(1/2) f_S, ×(1/4) f_S, ×(1/8) f_S	×1 f_S	19	ATS[1:0]
Soft mute control Mute disabled, enabled	Mute disabled	18	MUTE
Infinite zero mute control Disabled, enabled	Disabled	19	INZD
Input audio data format selection 16-, 20-, 24-bit standard (right-justified) format 24-bit, MSB-first, left-justified format 16-, 24-bit I^2S format	16-bit standard format	18	FMT[2:0]
De-emphasis control Disabled, enabled	De-emphasis disabled	18	DME
Sampling rate selection for de-emphasis Disabled, 44.1 kHz, 48 kHz, 32 kHz	De-emphasis disabled	18	DMF[1:0]
Digital filter rolloff selection Sharp rolloff, slow rolloff	Sharp rolloff	19	FLT
Output phase reversal Normal, reversed	Normal	19	REV
DAC operation control Enabled, disabled	DAC operation enabled	19	OPE
System clock (SCKO) output control Output Enabled, disabled	Output enabled	19	CLKE
System clock (SCKO) rate control SCKI, SCKI/2	SCKI	19	CLKD
System reset control Reset operation, normal operation	Normal operation	20	SRST
Mode control register reset control Reset operation, normal operation	Normal operation	20	MRST
Digital-filter bypass control DF enabled, DF bypassed	DF enabled	20	DFTH
Delta-sigma oversampling rate selection ×64 f_S, ×128 f_S, ×32 f_S	×64 f_S	20	OS[1:0]
Monaural mode selection Stereo, monaural	Stereo	20	MONO
Channel selection for monaural mode data L-channel, R-channel	L-channel	20	CHSL
FUNCTIONS AVAILABLE ONLY FOR READ			
Zero detection flag Not zero, zero detected	Not zero = 0 Zero detected = 1	21	ZFGL for L-channel ZFGR for R-channel

Table 4. Mode Control Register Map

REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
16	W/R	0	0	1	0	0	0	0	ATL7	ATL6	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
17	W/R	0	0	1	0	0	0	1	ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0
18	W/R	0	0	1	0	0	1	0	ATLD	FMT2	FMT1	FMT0	DMF1	DMF0	DME	MUTE
19	W/R	0	0	1	0	0	1	1	REV	ATS1	ATS0	OPE	CLKD	CLKE	FLT	INZD
20	W/R	0	0	1	0	1	0	0	RSV(1)	SRST	MRST	DFTH	MONO	CHSL	OS1	OS0
21	R	0	0	1	0	1	0	1	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	RSV(1)	ZFGR	ZFGL

(1) RSV is assigned for factory test operation.

REGISTER DEFINITIONS

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 16	W/R	0	0	1	0	0	0	0	ATL7	ATL6	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
REGISTER 17	W/R	0	0	1	0	0	0	1	ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

W/R **Read/Write Mode Select**

When W/R = 0, a write operation is performed.

When W/R = 1, a read operation is performed.

Default value: 0

ATL/R[7:0] **Digital Attenuation Level Setting**

These bits are read/write.

Default value: 1111 1111b

Each DAC output has a digital attenuator associated with it. The attenuator may be set from 0 db to –120 dB, in 0.5-dB steps. Alternatively, the attenuator may be set to infinite attenuation (or mute).

The attenuation data for each channel can be set individually. However, the data load control (ATLD bit of mode control register 18) is common to both attenuators. ATLD must be set to 1 in order to change an attenuator's setting. The attenuation level may be set using the following formula:

$$\text{Attenuation level (dB)} = 0.5\ \text{dB} \times (\text{ATL/R}[7:0]_{DEC} - 255)$$

where $\text{ATL/R}[7:0]_{DEC}$ = 0 through 255

For $\text{ATL/R}[7:0]_{DEC}$ = 0 through 14, the attenuator is set to infinite attenuation.

The following table shows attenuator levels for various settings.

ATL/R[7:0]	Decimal Value	Attenuator Level Setting
1111 1111b	255	0 dB, no attenuation (default)
1111 1110b	254	–0.5 dB
1111 1101b	253	–1 dB
•	•	•
•	•	•
0001 0000b	16	119.5 dB
0000 1111b	15	120 dB
0000 1110b	14	Mute
•	•	•
•	•	•
0000 0000b	0	Mute

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 18	W/R	0	0	1	0	0	1	0	ATLD	FMT2	FMT1	FMT0	DMF1	DMF0	DME	MUTE

W/R **Read/Write Mode Control**

When W/R = 0, a write operation is performed.

When W/R = 1, a read operation is performed.

Default value: 0

ATLD **Attenuation Load Control**

This bit is read/write.

Default value: 0

ATLD = 0	Attenuation control disabled (default)
ATLD = 1	Attenuation control enabled

The ATLD bit is used to enable loading of attenuation data set by registers 16 through 17. When ATLD = 0, the attenuation settings remain at the previously programmed level, ignoring new data loaded to registers 16 through 17. When ATLD = 1, attenuation data written to registers 16 through 17 is loaded normally.

FMT[2:0] **Audio Interface Data Format**

These bits are read/write.

Default value: 000

FMT[2:0]	Audio Data Format Selection
000	16-bit, standard-format, right-justified data (default)
001	20-bit, standard-format, right-justified data
010	24-bit, standard-format, right-justified data
011	24-bit, MSB-first, left-justified format data
100	16-bit, I^2S-format data
101	24-bit, I^2S-format data
110	Reserved
111	Reserved

The FMT[2:0] bits are used to select the data format for the serial audio interface.

For external digital-filter interface mode (DFTH mode), this register is operated as shown in the *Application for External Digital Filter Interface* section of this data sheet.

DMF[1:0] Sampling Frequency Selection for the De-Emphasis Function

These bits are read/write.

Default value: 00

DMF[1:0]	De-Emphasis Same Rate Selection
00	Disabled (default)
01	48 kHz
10	44.1 kHz
11	32 kHz

The DMF[1:0] bits are used to select the sampling frequency used for the digital de-emphasis function when it is enabled by setting the DME bit. The de-emphasis curves are shown in the *Typical Performance Curves* section of this data sheet.

For DSD mode, analog FIR filter performance may be selected using this register. Filter response plots are shown in the *Typical Performance Curves* section of this data sheet. The register map is shown in the *Application for DSD Format (DSD Mode) Interface* section of this data sheet.

DME Digital De-Emphasis Control

This bit is read/write.

Default value: 0

For DSD mode, DME must be set to 1.

DME = 0	De-emphasis disabled (default)
DME = 1	De-emphasis enabled

The DME bit is used to enable or disable the de-emphasis function for both channels.

MUTE Soft-Mute Control

This bit is read/write.

Default value: 0

MUTE = 0	MUTE disabled (default)
MUTE = 1	MUTE enabled

The MUTE bit is used to enable the soft-mute function for both channels. The mute function is also available through the MUTE control input (pin 15). Soft mute is performed by using the 256-step attenuator, cycling one step per time interval to – (mute). The time interval is set by the rate select bit (ATS), located in register 19.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 19	W/R	0	0	1	0	0	1	1	REV	ATS1	ATS0	OPE	CLKD	CLKE	FLT	INZD

W/R **Read/Write Mode Control**

When W/R = 0, a write operation is performed.

When W/R = 1, a read operation is performed.

Default value: 0

REV **Output Phase Reversal**

This bit is read/write.

Default value: 0

REV = 0	Normal output (default)
REV = 1	Inverted output

The REV bit is used to invert the output phase for both the left and right channels.

ATS[1:0] **Attenuation Rate Select**

This bit is read/write.

Default value: 00

ATS[1:0]	Attenuation Rate Selection
00	LRCK (default)
01	1/2 × LRCK
10	1/4 × LRCK
11	1/8 × LRCK

The ATS[1:0] bits are used to select the rate at which the attenuator is decremented or incremented during level transitions.

OPE **DAC Operation Control**

This bit is read/write.

Default value: 0

OPE = 0	DAC operation enabled (default)
OPE = 1	DAC operation disabled

The OPE bit is used to enable or disable the analog output for both channels. Disabling the analog outputs forces them to the bipolar zero level (BPZ), ignoring the audio data input(s).

CLKD **SCKO Frequency Selection**

This bit is read/write.

Default value: 0

CLKD = 0	Full-rate, $f_{SCKO} = f_{SCKI}$ (default)
CLKD = 1	Half-rate, $f_{SCKO} = f_{SCKI}/2$

The CLKD bit is used to determine the output frequency at the system clock output pin, SCKO.

CLKE **SCKO Output Enable**

This bit is read/write.

Default value: 0

CLKE = 0	SCKO enabled (default)
CLKE = 1	SCKO disabled

The CLKE bit is used to enable or disable the system clock output pin, SCKO.

FLT **Digital Filter Rolloff Control**

This bit is read/write.

Default value: 0

FLT = 0	Sharp rolloff (default)
FLT = 1	Slow rolloff

The FLT bit allows the user to select the digital filter rolloff characteristics. The filter responses for these selections are shown in the *Typical Performance Curves* section of this data sheet.

INZD **Infinite Zero Detect Mute Control**

This bit is read/write.

Default value: 0

INZD = 0	Infinite zero detect mute disabled (default)
INZD = 1	Infinite zero detect mute enabled

The INZD bit is used to enable or disable the zero detect mute function. Setting INZD = 1 allows the analog outputs to be set to the bipolar zero level when the PCM1738 detects zero data for both left and right channels for 1024 sampling periods (or LRCK cycles).

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 20	W/R	0	0	1	0	1	0	0	RSV	SRST	MRST	DFTH	MONO	CHSL	OS1	OS0

W/R **Read/Write Mode Control**

When W/R = 0, a write operation is performed.

When W/R = 1, a read operation is performed.

Default value: 0

SRST **System Reset Control**

This bit is read/write.

Default value: 0

SRST = 0	Normal operation (default)
SRST = 1	System reset operation

The SRST bit is used to reset the PCM1738 to the initial system condition.

MRST **Mode Control Register Reset Control**

This bit is read/write.

Default value: 0

MRST = 0	Normal operation (default)
MRST = 1	Mode control register reset operation

The MRST bit is used to set the mode control registers to their default conditions.

DFTH **Digital Filter Bypass (or Through-Mode) Control**

This bit is read/write.

Default value: 0

DFTH = 0	Digital filter enabled (default)
DFTH = 1	Digital filter bypassed for either external-digital-filter mode or DSD mode

The DFTH bit is used to enable or bypass the internal digital filter. This function is used when using the external-digital-filter interface or the DSD-mode interface.

MONO **Monaural Mode Selection**

This bit is read/write.

Default value: 0

MONO = 0	Stereo mode (default)
MONO = 1	Monaural mode

The MONO function is used to change the operation mode from normal stereo mode to monaural mode. When the monaural mode is selected, both DACs operate in balanced mode for the selected audio input data. Left- and right-channel data selection is set by the CHSL bit, described as follows.

CHSL **Channel Selection for Monaural Mode**

This bit is read/write.

Default value: 0

This bit is available when MONO = 1.

CHSL = 0	L-channel selected (default)
CHSL = 1	R-channel selected

The CHSL bit is used to set the audio data selection for the monaural mode.

OS[1:0] **Delta-Sigma Oversampling Rate Selection**

These bits are available for read/write.

Default value: 00

For DSD mode, this register is used to select the speed of BCK (pin 7) for the analog FIR filter.

OS[1:0]	Operation Speed Select
00	64× (default)
01	Reserved
10	128×
11	32×

The OS bits are used to change the oversampling ratio of the delta-sigma modulator. This function is useful when considering the output low-pass filter design that can handle a wide range of sampling rates. As an example, selecting 128× for f_S = 44.1 kHz, 64× for f_S = 96 kHz, and 32× for f_S = 192 kHz operation would require a low-pass filter with a single cutoff frequency to accommodate all three sampling rates.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
REGISTER 21	R	0	0	1	0	1	0	1	RSV	RSV	RSV	RSV	RSV	RSV	ZFGR	ZFGL

R **Read Mode Control**

Only set to 1 for read-back mode.

ZFGx **Zero Detection Flag**

When x = L or R, corresponding to the DAC output channel.

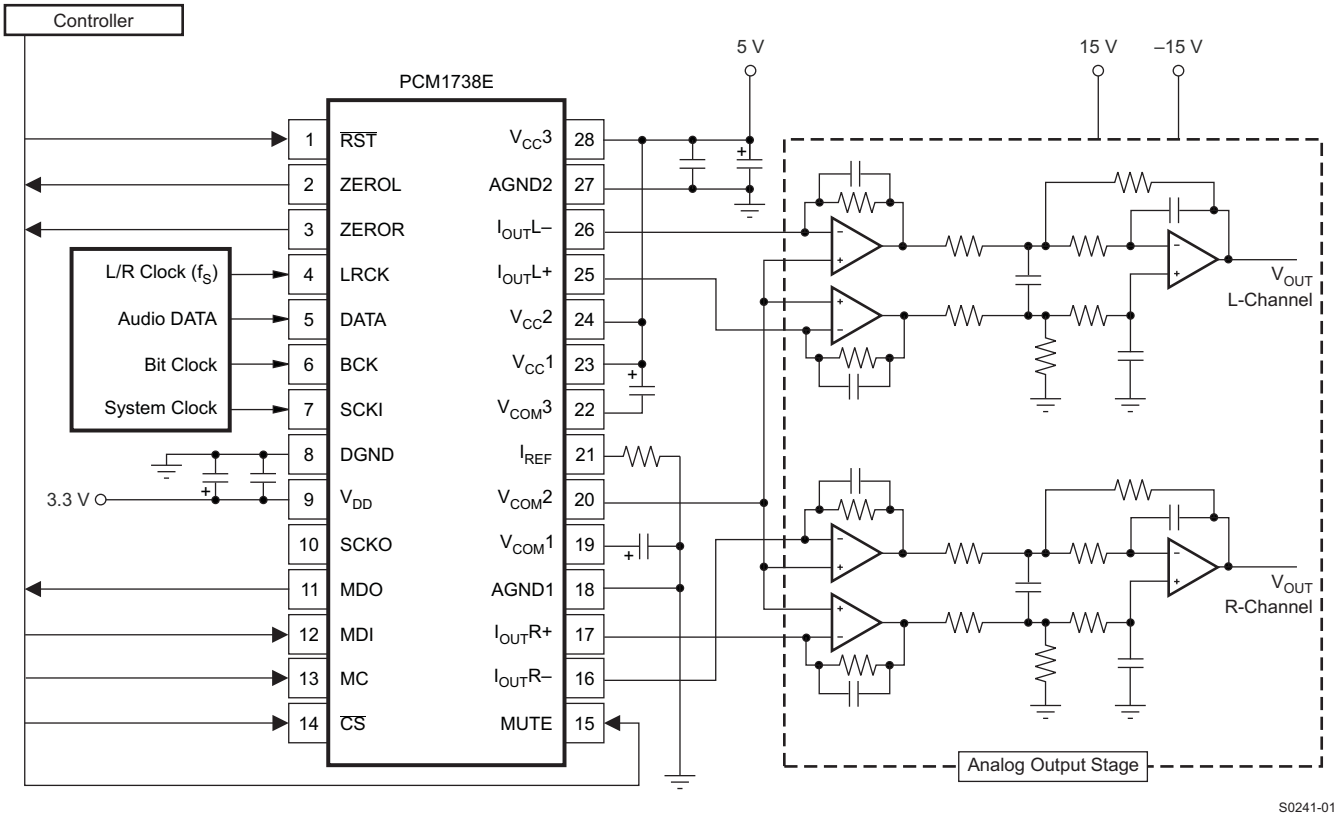
These bits are available only for readback.

Default value: 00

ZFGx = 0	Not ZERO
ZFGx = 1	ZERO detected

When the PCM1738 detects that audio input data is continuously zero for 1024 LRCKs, the ZFGx bit is set to 1 for the corresponding channel(s). Zero detect flags are also available at ZEROL (pin 2) and ZEROR (pin 3).

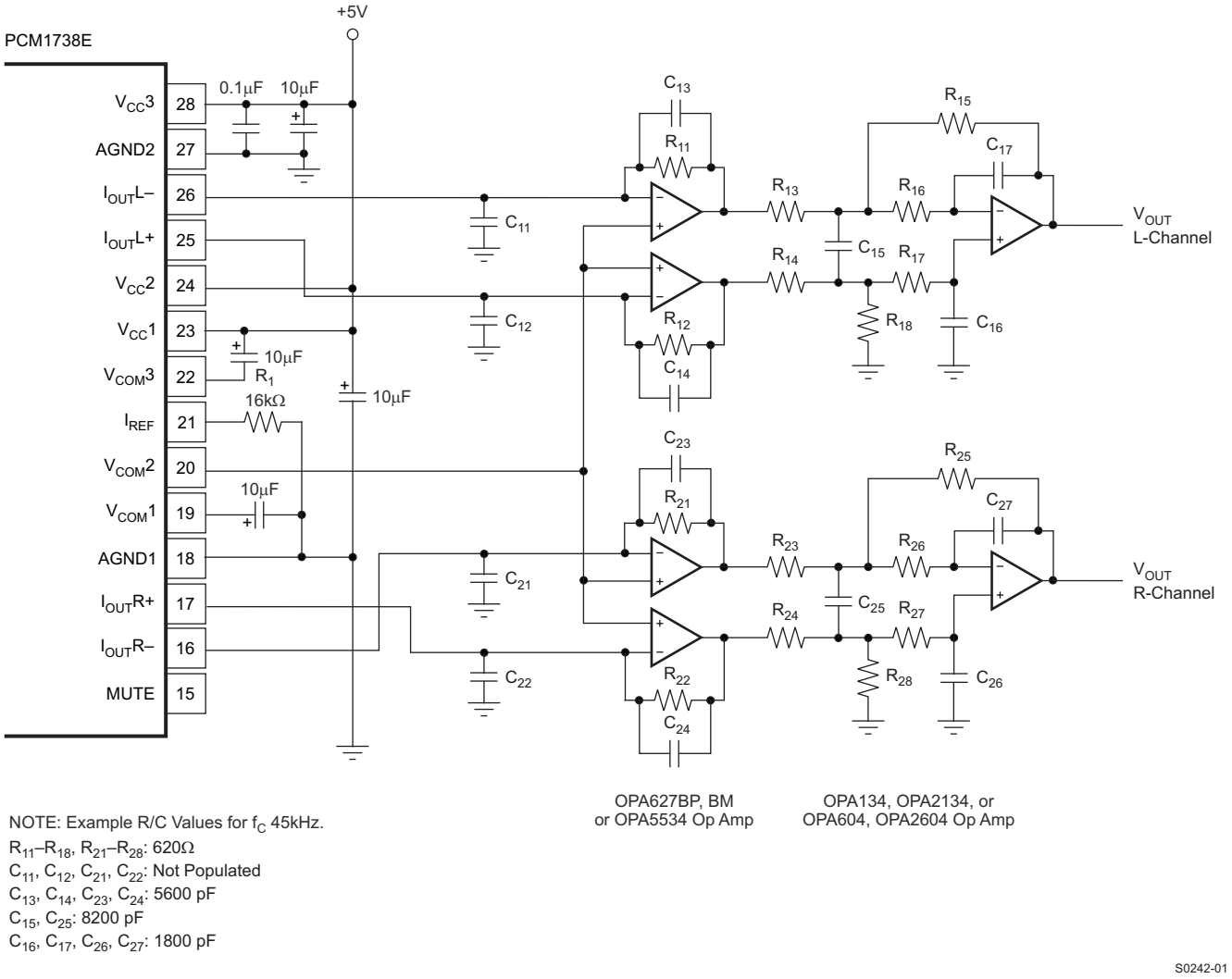
TYPICAL CONNECTION DIAGRAM IN PCM MODE



NOTE: Regarding R/C values for the analog output stage, see Figure 40.

Figure 39. Typical Application Circuit for Standard PCM Audio Operation

ANALOG OUTPUTS



NOTE: Example R/C Values for f_C 45kHz.
R_{11}–R_{18}, R_{21}–R_{28}: 620Ω
C_{11}, C_{12}, C_{21}, C_{22}: Not Populated
C_{13}, C_{14}, C_{23}, C_{24}: 5600 pF
C_{15}, C_{25}: 8200 pF
C_{16}, C_{17}, C_{26}, C_{27}: 1800 pF

S0242-01

Figure 40. Typical Application for Analog Output Stage

ANALOG OUTPUT LEVEL AND I/V CONVERTER

The signal level of the DAC current output pins ($I_{OUT}L+$, $I_{OUT}L–$, $I_{OUT}R+$, and $I_{OUT}R–$) is ±2.48 mAp-p at 0 dB (full scale). The voltage output of the I/V converter is given by the following equation:

$$V_{OUT} = \pm 2.48 \text{ mAp-p} \times R_F$$

Here, R_F is the feedback resistor in the I/V (current-to-voltage) conversion circuit, R_{11}, R_{12}, R_{21}, and R_{22} in the typical application circuit, Figure 40. The common level of the I/V conversion circuit must be the same as the common level of DAC I_{OUT} that is given by the $V_{COM}2$ reference voltage, 2.5 V dc. The non-inverting inputs of the operational amplifiers shown in the I/V circuits are connected to $V_{COM}2$ to provide the common bias voltage.

Operational Amplifiers for I/V Converter Circuit

The OPA627BP/BM, or 5534 type operational amplifier, is recommended for the I/V conversion circuit to obtain the specified audio performance. Dynamic performance, such as gain bandwidth, settling time, and slew rate of the operational amplifiers creates the audio dynamic performance of the I/V section. The input noise specification of the operational amplifiers should be considered to obtain 120-dB S/N ratio.

Analog Gain by Balanced Amplifier

The I/V converters are followed by balanced amplifier stages that sum the differential signals for each channel, creating a single-ended voltage output. In addition, the balanced amplifiers provide a second-order, low-pass filter function that band-limits the audio output signal. The cutoff frequency and gain is given by external R and C component values. In the case of Figure 40, the cutoff frequency is 45 kHz with a gain of 1. The output voltage for each channel is 6.2 Vp-p, or 2.2 Vrms.

REFERENCE CURRENT RESISTOR

As shown in the analog output application circuit, marked R_1 on Figure 40, there is a resistor connected from I_{REF} (pin 21) to the analog ground, designated as R_1. This resistor sets the current for the internal reference circuit. The value of R_1 must be 16 kΩ, ±1% in order to match the specified gain error shown in the *Electrical Characteristics* table.

APPLICATION FOR EXTERNAL DIGITAL FILTER INTERFACE

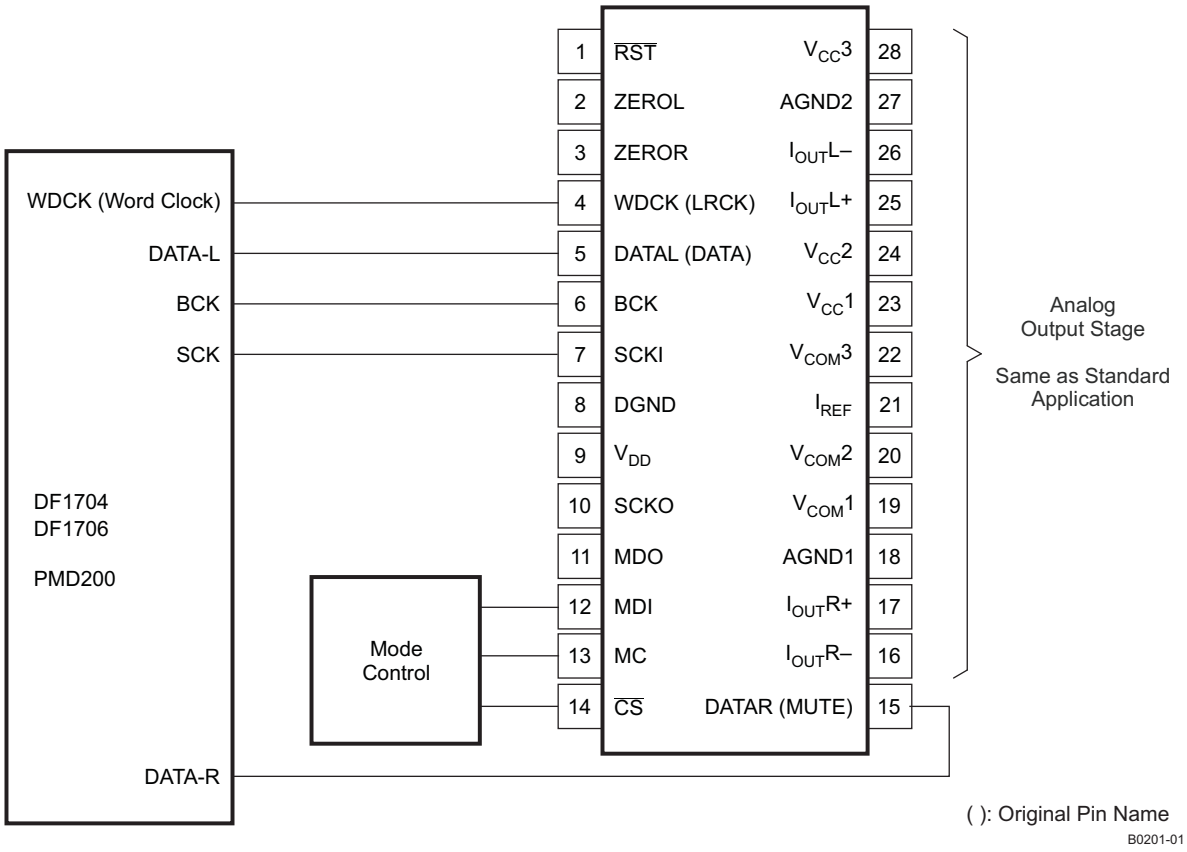


Figure 41. Connection Diagram for External Digital Filter (Internal DF Bypass Mode) Application

APPLICATIONS FOR INTERFACING WITH THE EXTERNAL DIGITAL FILTER

For some applications, it may be desirable to use an external digital filter to perform the interpolation function, as it may provide improved stop-band attenuation or other special features not available with the PCM1738's internal digital filter.

The PCM1738 supports the use of an external digital filter, including:

- The DF1704 and DF1706 from Texas Instruments
- Pacific Microsonics PMD100 HDCD filter/decoder ICs
- Programmable digital signal processors

The external digital-filter application mode is available by programming the following bits in the corresponding mode control registers:

DFTH = 1 (register 20)

DME = 0 (register 18)

The pins used to provide the serial interface for the external digital filter are shown in the application diagram of Figure 41. The word (WDCK) and bit (BCK) clock signals, as well as the audio data inputs (DATAL and DATAR) must be operated at 8× or 4× the original sampling frequency at the input of the digital filter.

SYSTEM CLOCK (SCKI) AND INTERFACE TIMING

The PCM1738, in external digital-filter mode, allows any system-clock frequency synchronized with BCK and WDCK. The system clock may be phase-free with BCK and WDCK. See Figure 43 for interface timing among WDCK, BCK, DATAL, and DATAR.

AUDIO FORMAT

In external digital-filter interface mode, the PCM1738 supports a right-justified audio format interface including 16-, 20-, and 24-bit audio data (see Figure 42) that should be selected by FMT[2:0] of mode control register 18.

FUNCTIONS AVAILABLE IN THE EXTERNAL DIGITAL-FILTER MODE

The external digital-filter mode allows access to the majority of the PCM1738's mode-control functions. Table 5 shows the register mapping available when the external digital-filter mode is selected, along with descriptions of functions that are modified for this mode selection.

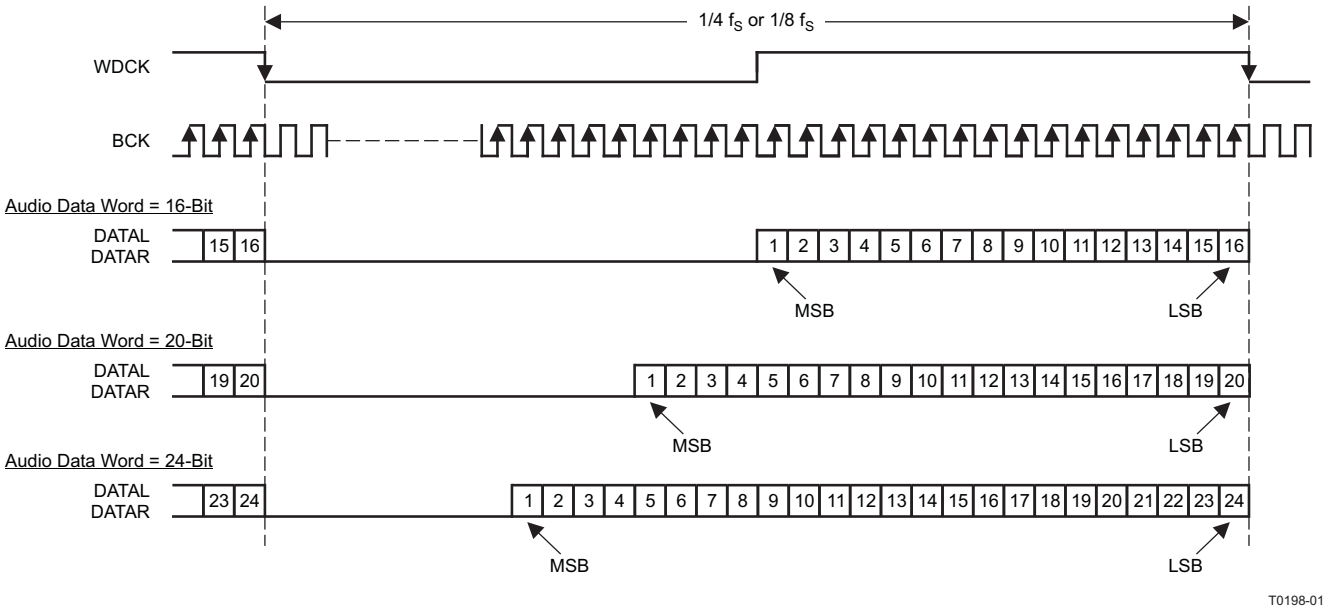
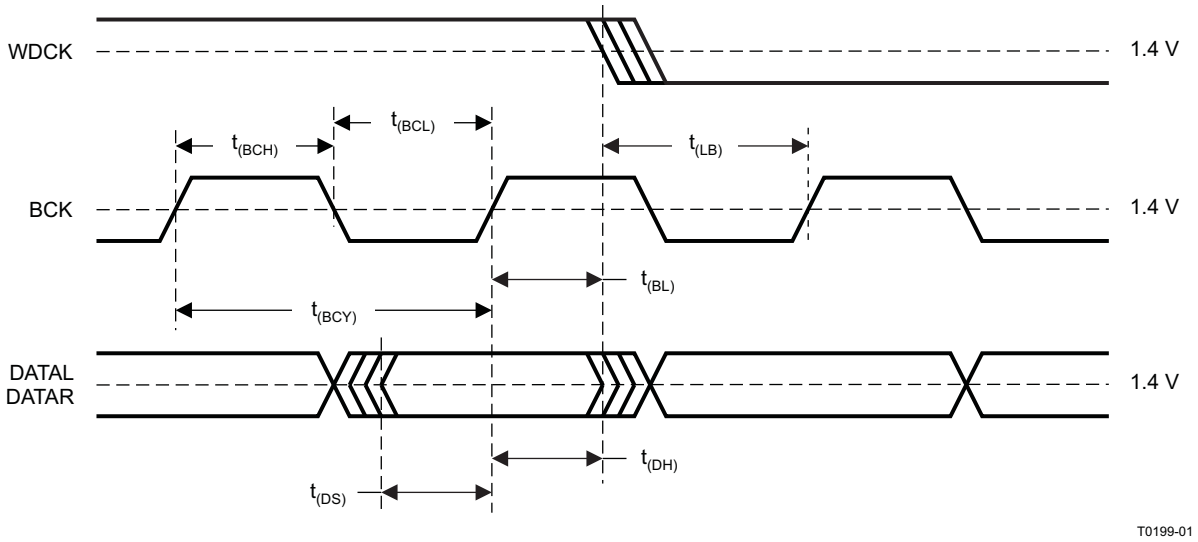


Figure 42. Audio Data Input Format for External Digital Filter (Internal DF Bypass Mode) Application



PARAMETER		MIN	MAX	UNIT
$t_{(BCY)}$	BCK clock cycle time	18		ns
$t_{w(BCL)}$	BCK pulse duration, LOW	7		ns
$t_{w(BCH)}$	BCK pulse duration, HIGH	7		ns
$t_{(BL)}$	BCK rising edge to WDCK falling edge	5		ns
$t_{(LB)}$	WDCK falling edge to BCK rising edge	5		ns
$t_{(DS)}$	DATA setup time	5		ns
$t_{(DH)}$	DATA hold time	5		ns

Figure 43. Audio Interface Timing for External Digital Filter (Internal DF Bypass Mode) Application

Table 5. Register Mapping in the External Digital-Filter Mode

REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
16	W/R	0	0	1	0	0	0	0	–(1)	–	–	–	–	–	–	–
17	W/R	0	0	1	0	0	0	1	–	–	–	–	–	–	–	–
18	W/R	0	0	1	0	0	1	0	–	FMT2	FMT1	FMT0	–	–	DME(2)	–
19	W/R	0	0	1	0	0	1	1	–	–	–	OPE	CLKD	CLKE	–	INZD
20	W/R	0	0	1	0	1	0	0	RSV	SRST	MRST	DFTH(2)	RSV	RSV	OS1	OS0
21	R	0	0	1	0	1	0	1	RSV	RSV	RSV	RSV	RSV	RSV	ZFGR	ZFGL

(1) – = function disabled. No operation regardless of data setting.
(2) These bits are required for selection of the external digital-filter mode.

FMT[2:0] Audio Data Format Selection

These bits are available for read/write.

Default Value: 000

FMT[2:0]	Audio Data Format Select
000	16-bit, right-justified format (default)
001	20-bit, right-justified format
010	24-bit, right-justified format
Other	Reserved

OS[1:0] Delta-Sigma Oversampling Rate Selection

These bits are available for read/write.

Default Value: 00

OS[1:0]	Operation Speed Select
00	$8 \times f_{WDCK}$ (default)
01	Reserved
10	$16 \times f_{WDCK}$
11	$4 \times f_{WDCK}$

The effective oversampling rate is determined by the oversampling performed by both the external digital filter and the delta-sigma modulator. For example, if the external digital filter is 8× oversampling, and the user selects OS[1:0] = 0, then the delta-sigma modulator oversamples by 8×, resulting in an effective oversampling rate of 64×.

ZFGx Zero-Detect Flag

where x = L or R, corresponding to the DAC output channel.

These bits are available only for read-back.

Default value: 00

ZFGx = 0	Not ZERO
ZFGx = 1	ZERO detected

When the PCM1738 detects that audio input data is continuously zero for 1024 WDCKs, the ZFGx bit is set to 1 for the corresponding channel(s). Zero-detect flags are also available at ZEROL (pin 2) and ZEROR (pin 3).

APPLICATION FOR DSD FORMAT (DSD MODE) INTERFACE

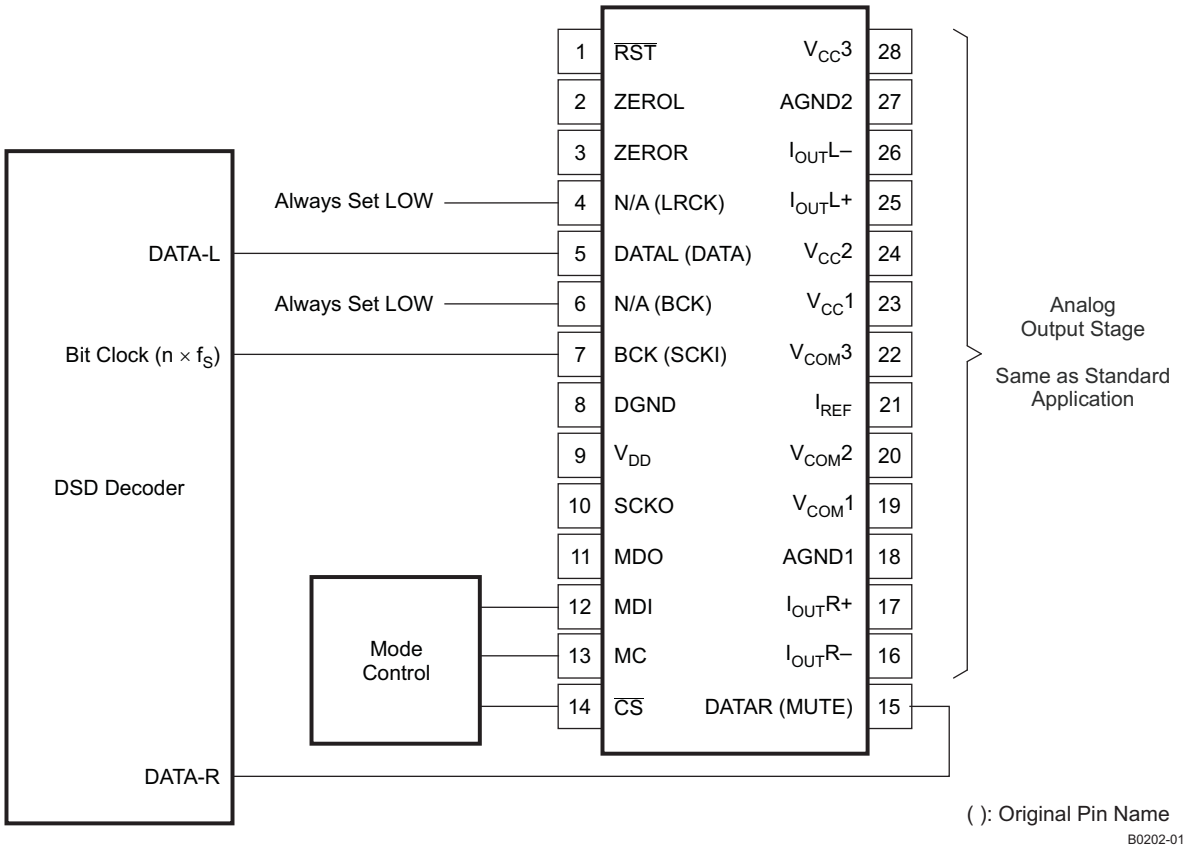


Figure 44. Connection Diagram for DSD Format Interface

FEATURES

This mode is used for interfacing directly to a DSD decoder, found in Super Audio CD (SACD) applications.

DSD mode provides a low-pass filtering function to convert the 1-bit oversampled data stream to the analog domain. The filtering is provided using an analog FIR filter structure. Four FIR responses are available and may be selected via the serial control interface. Refer to the *Typical Performance Curves* section of this data sheet for analog FIR plots. See Figure 45 and Figure 46 for timing and interface specification in DSD mode.

PIN ASSIGNMENT WHEN IN DSD-FORMAT INTERFACE

Several pins are redefined for DSD-mode operation. These include:

- DATA (pin 5)—DATAL, L-channel DSD data input
- MUTE (pin 15)—DATAR, R-channel DSD data input
- SCKI (pin 7)—bit clock (BCK) for DSD data
- LRCK (pin 4)—set LOW
- BCK (pin 6)—set LOW

Typical connection to a DSD decoder is shown in Figure 44.

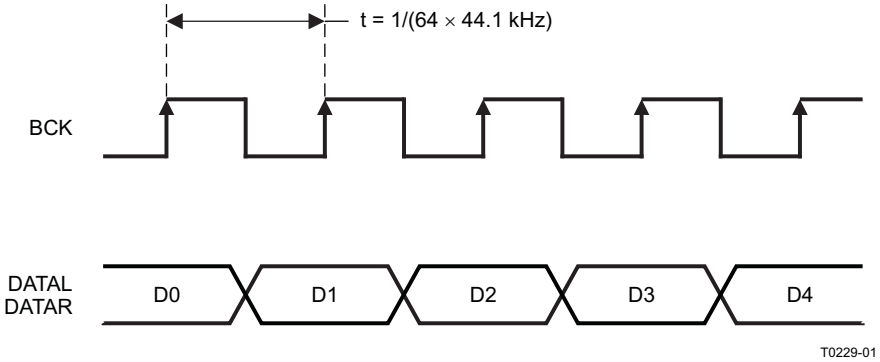
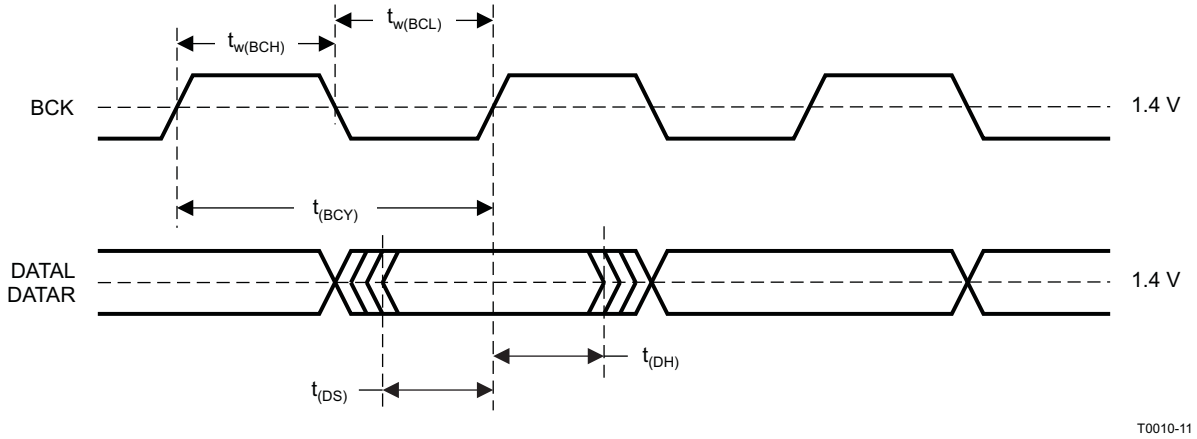


Figure 45. Normal Data Output Form From DSD Decoder



PARAMETER		MIN	MAX	UNIT
$t_{(BCY)}$	BCK clock cycle time	85[1]		ns
$t_{w(BCH)}$	BCK high-level time	30		ns
$t_{w(BCL)}$	BCK low-level time	30		ns
$t_{(DS)}$	DATAL, DATAR setup time	10		ns
$t_{(DH)}$	DATAL, DATAR hold time	10		ns

(1) 2.8224 MHz × 4. (2.8224 MHz = 64 × 44.1 kHz. This value is specified at the DSD sampling rate.)

Figure 46. Timing for DSD Audio Interface

DSD-MODE CONFIGURATION AND FUNCTION CONTROLS

Configuration for DSD interface mode:

- DFTH = 1 (register 20)
- DME = 1 (register 18)

Table 6 shows the register mapping available in DSD mode.

Table 6. Register Mapping in DSD Mode

REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
16	W/R	0	0	1	0	0	0	0	–(1)	–	–	–	–	–	–	–
17	W/R	0	0	1	0	0	0	1	–	–	–	–	–	–	–	–
18	W/R	0	0	1	0	0	1	0	–	–	–	–	DMF1	DMF0	DME(2)	–
19	W/R	0	0	1	0	0	1	1	–	–	–	OPE	CLKD	CLKE	–	–
20	W/R	0	0	1	0	1	0	0	RSV	SRST	MRST	DFTH(2)	RSV	RSV	OS1	OS0
21	R	0	0	1	0	1	0	1	RSV	RSV	RSV	RSV	RSV	RSV	–	–

(1) – = function disabled. No operation even if any data is set.
(2) These bits are required for selection of the DSD mode.

DMF[1:0] Analog FIR Performance Selection

These bits are available for read/write.

Default value: 00

DMF[1:0]	Analog FIR Performance Select
00	DSD filter 1 (default)
01	DSD filter 2
10	DSD filter 3
11	DSD filter 4

Plots for the four analog FIR filter responses are shown in the *Typical Performance Curves* of this data sheet.

OS[1:0] Analog FIR Operation Speed Selection

These bits are available for read/write.

Default value: 00

OS[1:0]	Operation Speed Select
00	f_{SCKI} (default)
01	Reserved
10	Reserved
11	$f_{SCKI}/2$

The OS bit in the DSD mode is used to select the operating rate of the analog FIR.

REQUIREMENTS FOR SYSTEM CLOCK

The bit clock (BCK) for DSD mode is required at pin 7 of the PCM1738. The frequency of the bit clock may be N times the sampling frequency. Generally, N is 64 in DSD applications.

The interface timing among the bit clock, DATAL, and DATAR is required to meet the same setup and hold-time specifications as shown for the PCM audio-format interface in Figure 36.

APPLICATION FOR MONAURAL-MODE OPERATION

Single-channel signals within stereo-audio data input are output to both $I_{OUT}L$ and $I_{OUT}R$ as differential outputs. Selection of channels to output is available with the CHSL bit in register 20. Applications, such as monaural operation,are useful for high-end audio applications to provide over 120 dB for dynamic range. A typical MONO mode application is shown in Figure 47.

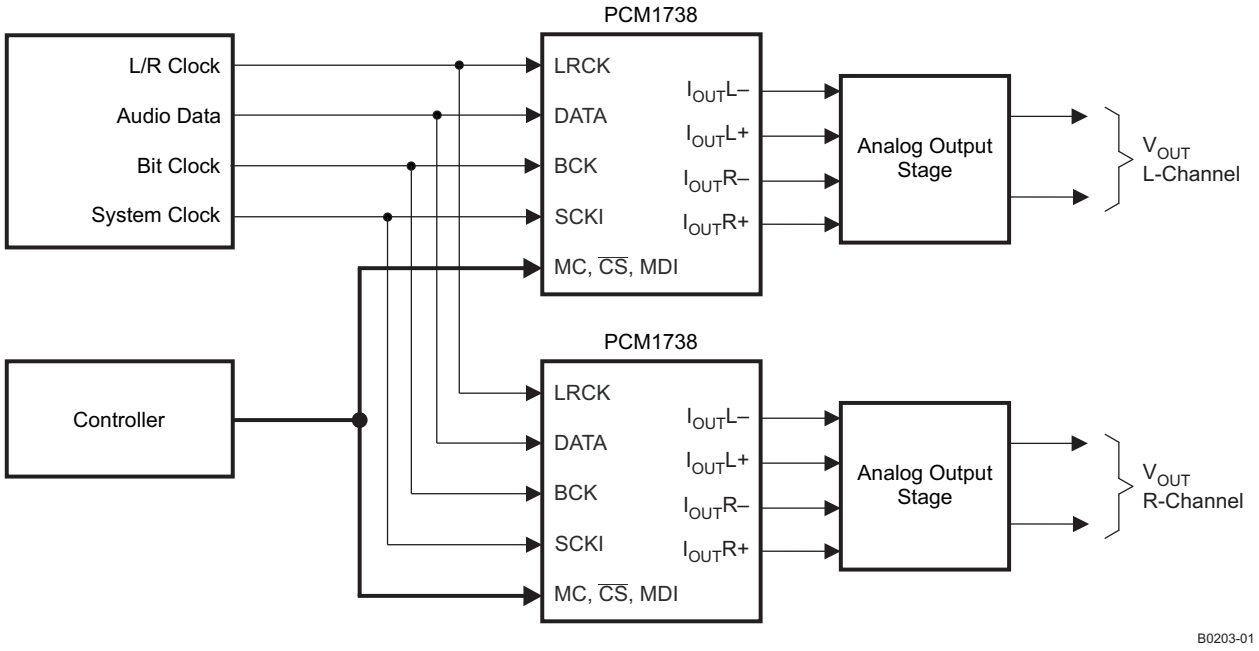


Figure 47. Connection Diagram for Monaural-Mode Interface

THEORY OF OPERATION

ADVANCED SEGMENT DAC

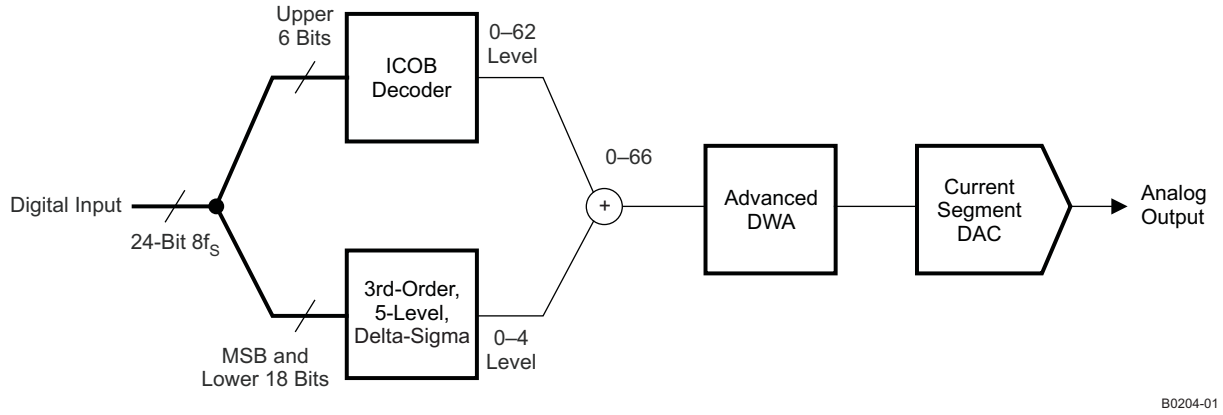


Figure 48. Architecture of Advanced Segment DAC

The PCM1738 uses the newly developed advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1738 provides balanced current outputs, allowing the user to optimize analog performance externally. The structure of the advanced segment DAC architecture is shown in Figure 48.

Digital input data from the digital interpolation filter is split into six upper bits and 18 lower bits. The upper six bits are converted to inverted complementary offset binary (ICOB) code. The lower 18 bits associated with the MSB are processed by five-level, third-order, delta-sigma modulators operated at 64 f_S by default conditions. The level of the modulator is equivalent to one LSB of the ICOB code converter (decoder). The data groups processed in the ICOB converter and the third-order delta-sigma modulator are summed together to create up to 66 levels of digital code that is then processed by data-weighted averaging (DWA) to reduce noise produced by element mismatch. The output data from the DWA block is then converted to an analog output using a differential current segment DAC.

CONSIDERATIONS FOR APPLICATIONS CIRCUITS

PCB LAYOUT GUIDELINES

A typical PCB floor plan for the PCM1738 is shown in Figure 49. A ground plane is recommended, with the analog and digital sections being isolated from one another using a split or cut in the circuit board. The PCM1738 should be oriented with the digital I/O pins facing the ground plane split/cut to allow for short, direct connections to the digital audio interface and control signals originating from the digital section of the board.

Separate power supplies are recommended for the digital and analog sections of the board. This prevents the switching noise present on the digital supply from contaminating the analog power supply and degrading the dynamic performance of the DACs. In cases where a common 5-V supply must be used for the analog and digital sections, an inductance (RF choke, ferrite bead) should be placed between the analog and digital 5-V supply connections to avoid coupling of the digital switching noise into the analog circuitry. Figure 50 shows the recommended approach for single supply applications.

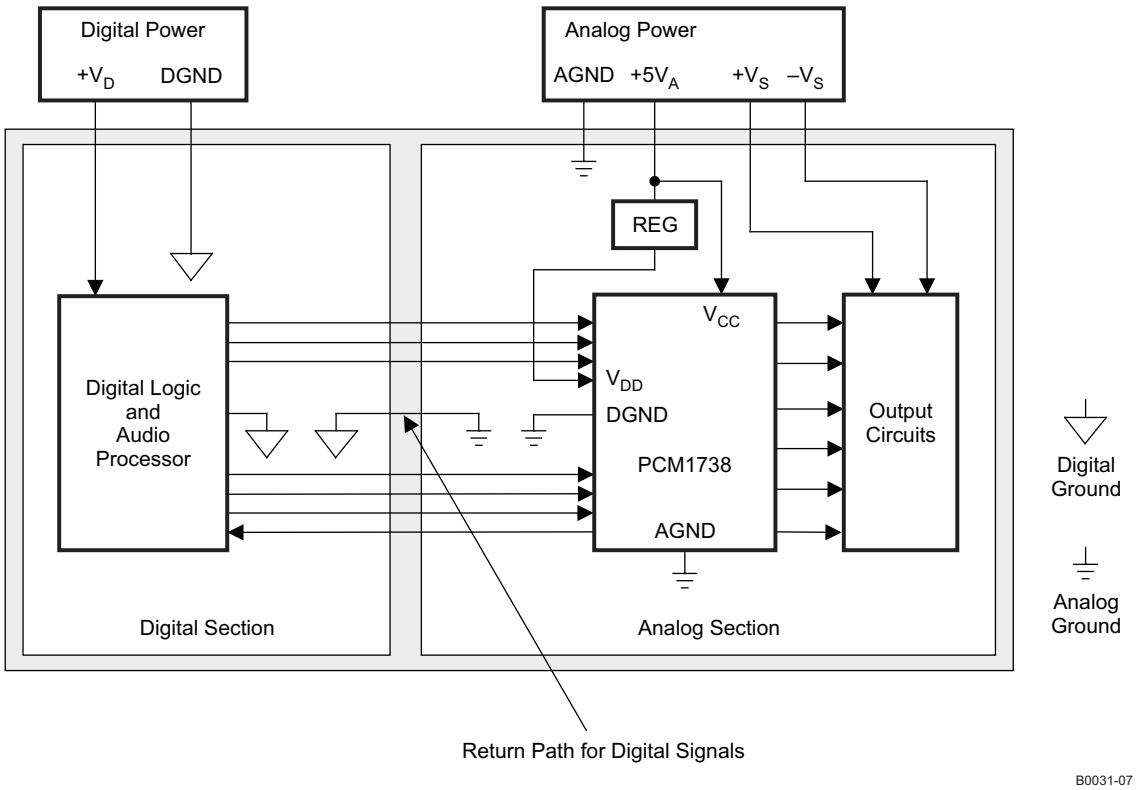


Figure 49. Recommended PCB Layout

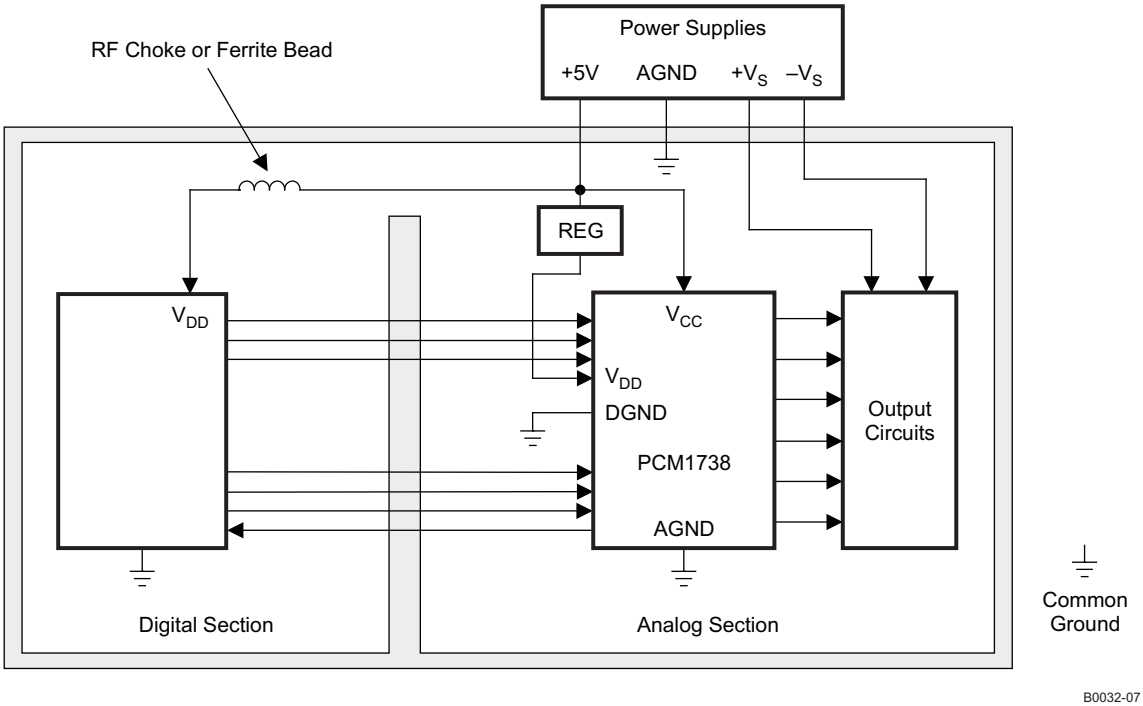


Figure 50. Single-Supply PCB Layout

BYPASS AND DECOUPLING CAPACITOR REQUIREMENTS

Various sized decoupling capacitors can be used, with no special tolerances being required. All capacitors should be located as close as physically possible to the power supply and reference pins of the PCM1738 to reduce noise pickup from surrounding circuitry. Aluminum electrolytic capacitors that are designed for hi-fi audio applications are recommended for larger values, while metal-film or monolithic ceramic capacitors are recommended for smaller values.

I/V SECTION

Using the circuit shown in Figure 40 for I/V conversion achieves data-sheet performance. To obtain 0.0005% THD+N, 117-dB signal-to-noise ratio audio performance, THD+N and input noise performance, an operational amplifier IC must be considered. Input noise of the operational amplifier directly affects the output noise level of the application.

All components of the I/V section should be located physically close to the PCM1738 current outputs. All connections should be made as short as possible to eliminate pickup of radiated noise.

POST LOW-PASS FILTER DESIGN

The out-of-band noise level and sampling spectrum level are much lower than typical delta-sigma type DACs, due to the combination of a high-performance digital filer and the advanced segment DAC architecture. The use of a second- or third-order filter is recommended for the post low-pass filter (see Figure 40 for a second-order filter) following the I/V conversion stage. The cutoff frequency of the post LPF is dependent upon the application, given the variety of sampling rates supported by the CD-DA (f_S = 44.1 kHz), DVD-M (f_S = 96 kHz), DVD-A (f_S = 192 kHz), and SACD (f_S = 44.1 kHz) systems.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1738E	NRND	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PCM1738E	
PCM1738E/2K	NRND	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PCM1738E	
PCM1738EG4	NRND	SSOP	DB	28	47	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		PCM1738E	

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

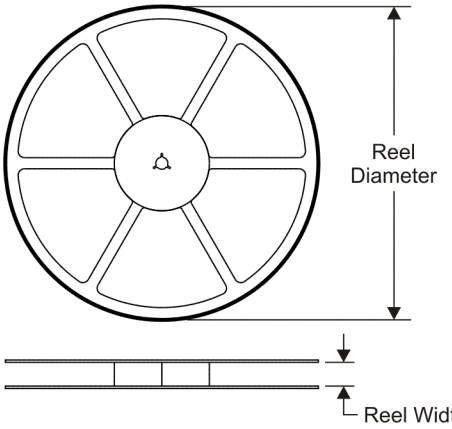
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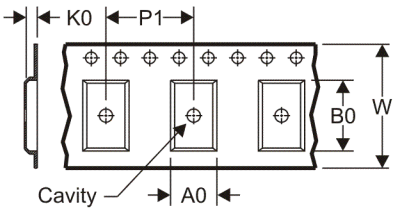
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TAPE AND REEL INFORMATION

REEL DIMENSIONS

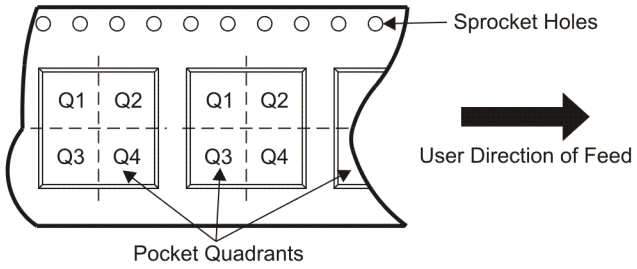


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

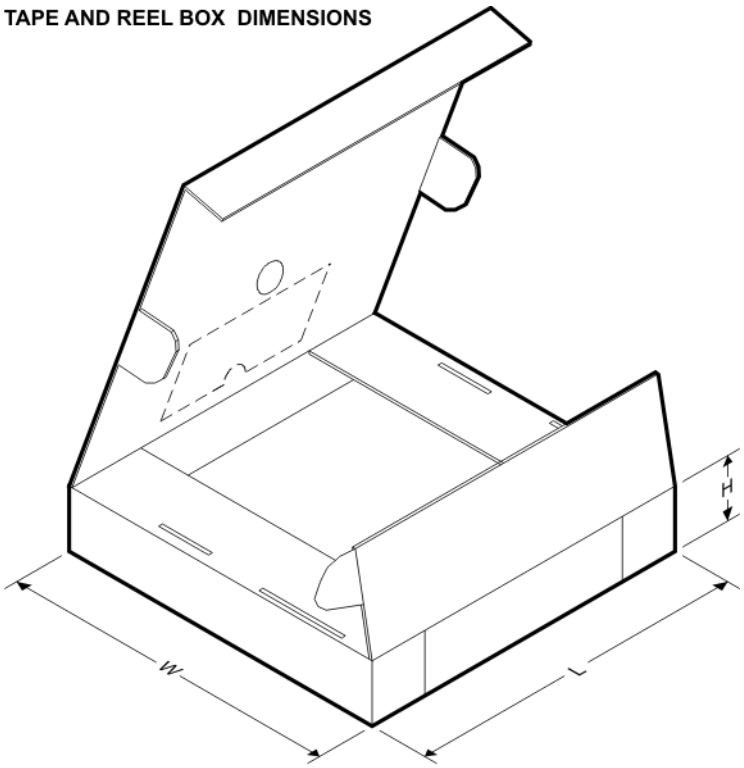
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
PCM1738E/2K	SSOP	DB	28	2000	330.0	17.4	8.5	10.8	2.4	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
PCM1738E/2K	SSOP	DB	28	2000	336.6	336.6	28.6

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