CSD18532NQ5B 60V N 沟道 NexFET™ 功率 MOSFET

1 特性

- 超低 Q_g 和 Q_{gd}
- 低热阻
- 雪崩级
- 无铅引脚镀层
- 符合 RoHS 标准
- 无卤素
- SON 5mm × 6mm 塑料封装

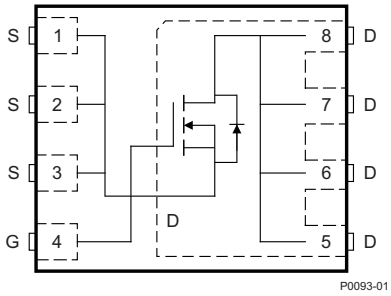
2 应用

- 直流 - 直流转换
- 次级侧同步整流器
- 隔离式转换器主级侧开关
- 电机控制

3 说明

这款采用 5mm × 6mm SON 封装的 60V、2.7mΩ NexFET™功率 MOSFET 旨在最大限度降低功率转换应用。

俯视图



P0093-01

产品概要

T_A = 25°C		典型值		单位
V_{DS}	漏源电压	60		V
Q_g	栅极电荷总量 (10V)	49		nC
Q_{gd}	栅极电荷（栅极到漏极）	7.9		nC
$R_{DS(on)}$	漏源导通电阻	V_{GS} = 6V	3.5	mΩ
		V_{GS} = 10V	2.7	
$V_{GS(th)}$	阈值电压	2.8		V

器件信息

器件	数量	包装介质	封装	发货
CSD18532NQ5B	2500	13 英寸卷带	SON 5.00mm × 6.00mm 塑料封装	卷带封装
CSD18532NQ5BT	250	7 英寸卷带		

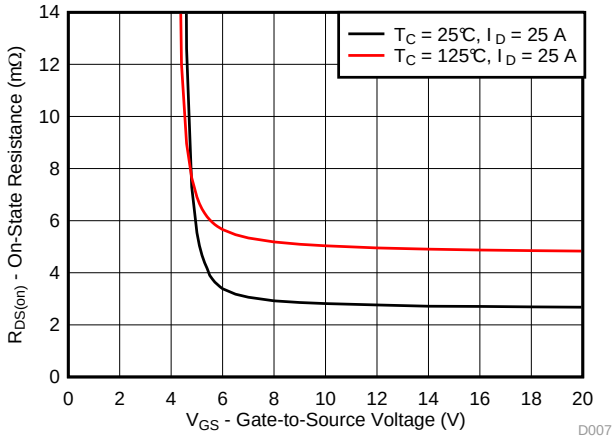
最大绝对额定值

T_A = 25°C		值	单位
V_{DS}	漏源电压	60	V
V_{GS}	栅源电压	±20	V
I_D	持续漏极电流（受封装限制）	100	A
	持续漏极电流（受芯片限制），T_C = 25°C 时测得	151	
	持续漏极电流(1)	21	
I_{DM}	脉冲漏极电流(2)	400	A
P_D	功率耗散(1)	3.1	W
	功率耗散，T_C = 25°C	156	
T_J, T_{stg}	工作结温，储存温度	–55 至 150	°C
E_{AS}	雪崩能量，单一脉冲 I_D = 85A，L = 0.1mH，R_G = 25Ω	360	mJ

(1) $R_{\theta JA}$ = 40°C/W，这是在一块厚度为 0.06 英寸环氧树脂 (FR4) 印刷电路板 (PCB) 上的 1 英寸^2，2 盎司铜焊盘上测得的典型值。

(2) 最大 $R_{\theta JC}$ = 0.8°C/W，脉冲持续时间 ≤ 100µs，占空比 ≤ 1%。

$R_{DS(on)}$ 与 V_{GS} 对比



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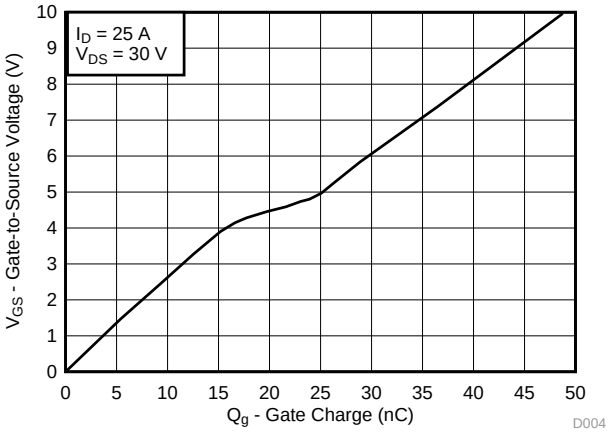
栅极电荷



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4 修订历史记录

注：之前版本的页码可能与当前版本有所不同。

Changes from Revision B (May 2017) to Revision C — **Page**

- Extended the V_{DS} on Figure 5 to 60 V ... 4

Changes from Revision A (December 2015) to Revision B — **Page**

- 已添加 *接收文档更新通知* 部分。 ... 7
- 已更改 在*建议 PCB 布局* 部分方框图中将焊盘 3 和 4 之间的尺寸从 0.028 英寸更改为了 0.050 英寸。 ... 9

Changes from Original (June 2014) to Revision A — **Page**

- 已添加 在标题中添加了部件编号。 ... 1
- 已添加 在*订购信息* 中添加了 7 英寸卷带。 ... 1
- 更新了脉冲电流条件。 ... 1
- 已添加 在*绝对最大额定值* 表格中添加了 T_C = 25°C 时的功率耗散一行。 ... 1
- Updated Figure 1 to show $R_{\theta JC}$ curves. ... 4
- Updated SOA in Figure 10 ... 6
- 已添加 *器件和文档支持* 部分。 ... 7
- 更新了*机械、封装和可订购信息* 以及机械制图。 ... 8

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5 Specifications

5.1 Electrical Characteristics

T_A = 25°C unless otherwise stated

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
STATIC CHARACTERISTICS						
BV_{DSS}	Drain-to-source voltage	V_{GS} = 0 V, I_D = 250 μA	60			V
I_{DSS}	Drain-to-source leakage current	V_{GS} = 0 V, V_{DS} = 48 V			1	μA
I_{GSS}	Gate-to-source leakage current	V_{DS} = 0 V, V_{GS} = 20 V			100	nA
$V_{GS(th)}$	Gate-to-source threshold voltage	V_{DS} = V_{GS}, I_D = 250 μA	2.4	2.8	3.4	V
$R_{DS(on)}$	Drain-to-source on-resistance	V_{GS} = 6 V, I_D = 25 A		3.5	4.4	mΩ
		V_{GS} = 10 V, I_D = 25 A		2.7	3.4	
g_{fs}	Transconductance	V_{DS} = 30 V, I_D = 25 A		140		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input capacitance	V_{GS} = 0 V, V_{DS} = 30 V, f = 1 MHz		4100	5340	pF
C_{oss}	Output capacitance			495	644	pF
C_{rss}	Reverse transfer capacitance			16	21	pF
R_G	Series gate resistance			1.2	2.4	Ω
Q_g	Gate charge total (10 V)	V_{DS} = 30 V, I_D = 25 A		49	64	nC
Q_{gd}	Gate charge gate-to-drain			7.9		nC
Q_{gs}	Gate charge gate-to-source			16		nC
$Q_{g(th)}$	Gate charge at V_{th}			11		nC
Q_{oss}	Output charge	V_{DS} = 30 V, V_{GS} = 0 V		69		nC
$t_{d(on)}$	Turnon delay time	V_{DS} = 30 V, V_{GS} = 10 V, I_{DS} = 25 A, R_G = 0 Ω		8.2		ns
t_r	Rise time			8.7		ns
$t_{d(off)}$	Turnoff delay time			20		ns
t_f	Fall time			2.7		ns
DIODE CHARACTERISTICS						
V_{SD}	Diode forward voltage	I_{SD} = 25 A, V_{GS} = 0 V		0.8	1	V
Q_{rr}	Reverse recovery charge	V_{DS} = 30 V, I_F = 25 A, di/dt = 300 A/μs		139		nC
t_{rr}	Reverse recovery time			64		ns

5.2 Thermal Information

T_A = 25°C unless otherwise stated

THERMAL METRIC		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Junction-to-case thermal resistance (1)			0.8	°C/W
$R_{\theta JA}$	Junction-to-ambient thermal resistance (1) (2)			50	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu pad on a 1.5-in × 1.5-in (3.81-cm × 3.81-cm), 0.06-in (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-in^2 (6.45-cm^2), 2-oz (0.071-mm) thick Cu.

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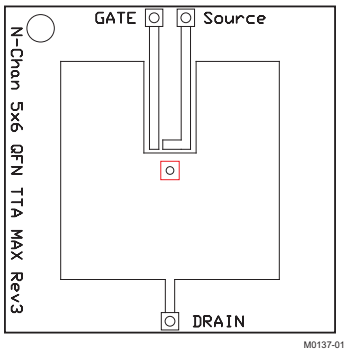
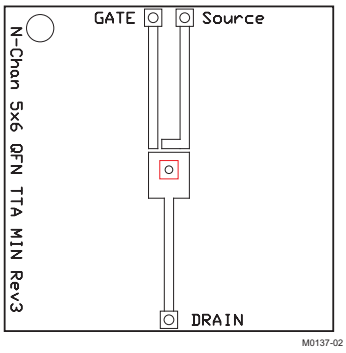


Max $R_{\theta JA}$ = 50°C/W when mounted on 1 in^2 (6.45 cm^2) of 2-oz (0.071-mm) thick Cu.



Max $R_{\theta JA}$ = 125°C/W when mounted on a minimum pad area of 2-oz. (0.071-mm) thick Cu.

5.3 Typical MOSFET Characteristics

T_A = 25°C unless otherwise stated

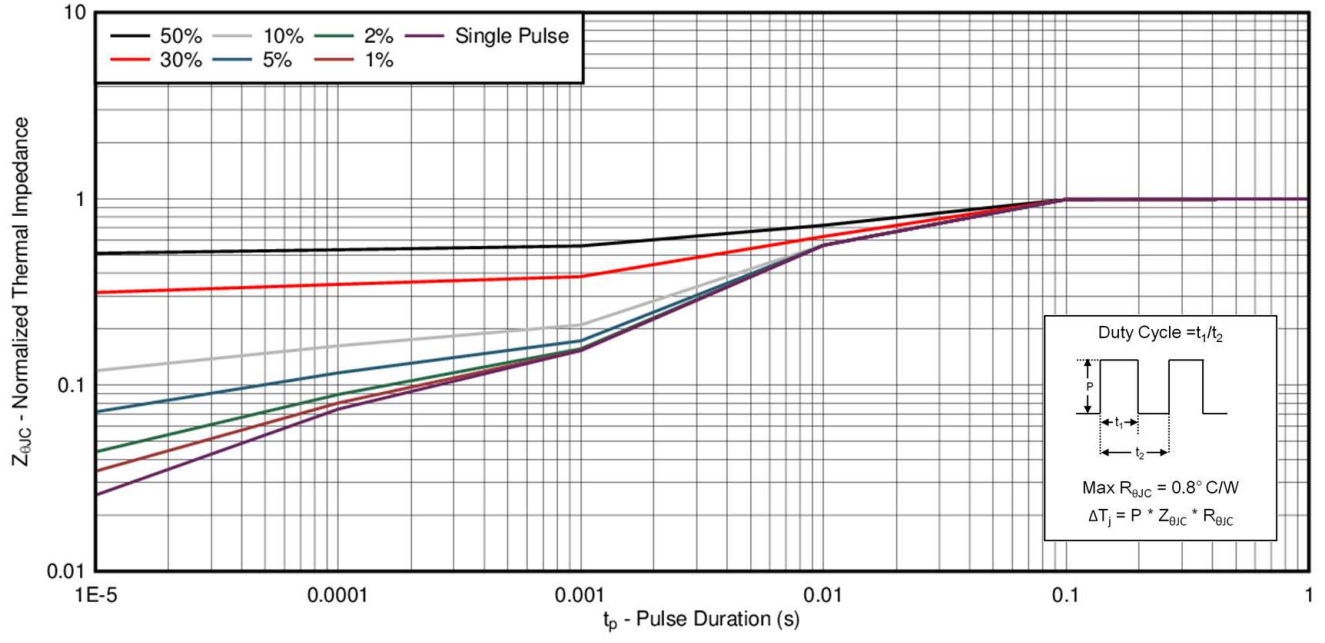


Figure 1. Transient Thermal Impedance

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Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated

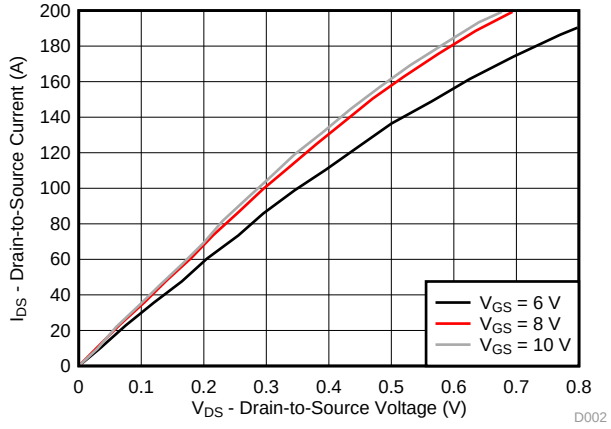

Figure 2. Saturation Characteristics

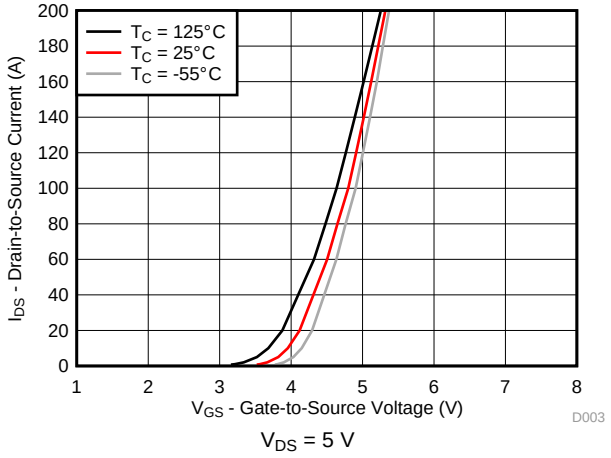

Figure 3. Transfer Characteristics

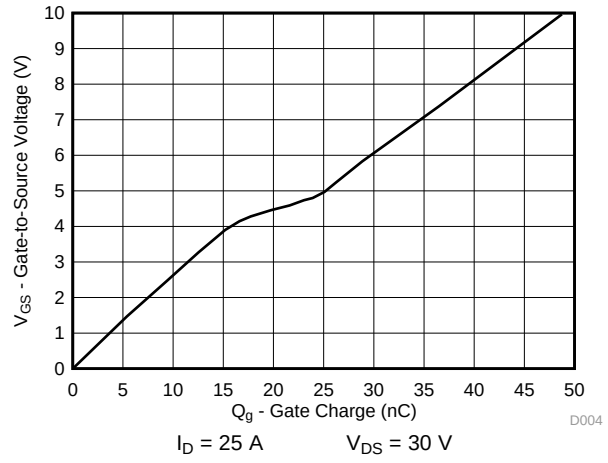

Figure 4. Gate Charge

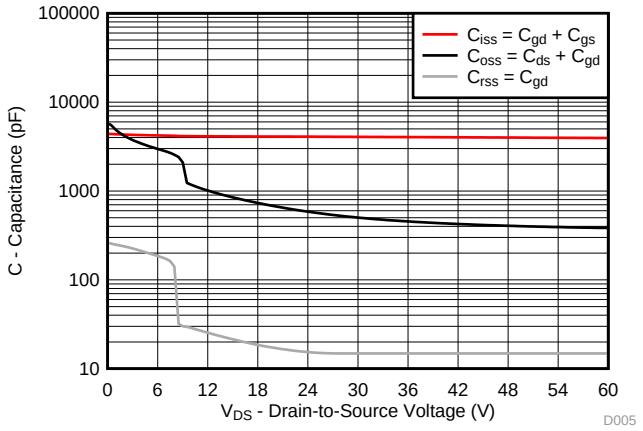

Figure 5. Capacitance

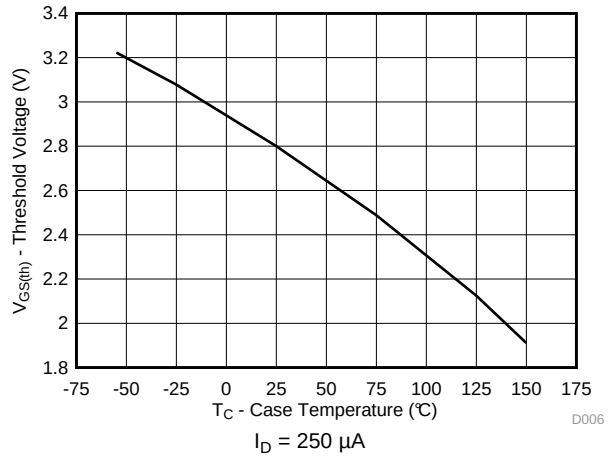

Figure 6. Threshold Voltage vs Temperature

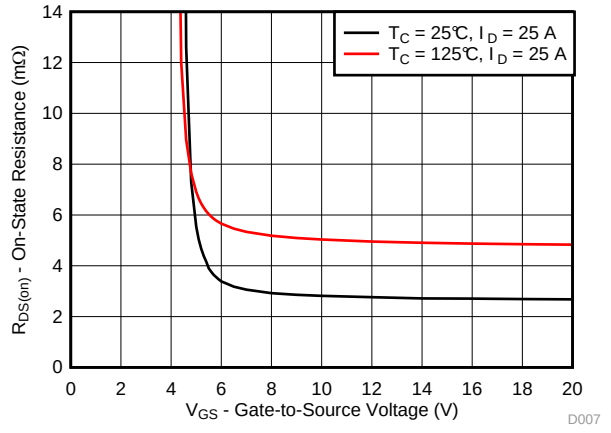

Figure 7. On-State Resistance vs Gate-to-Source Voltage

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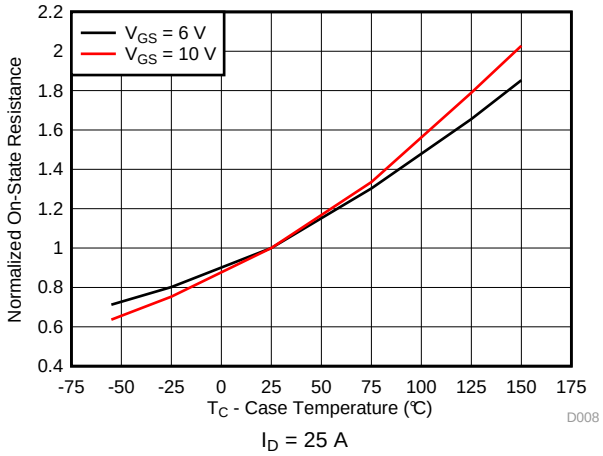
Typical MOSFET Characteristics (continued)

T_A = 25°C unless otherwise stated



ID = 25 A

Figure 8. Normalized On-State Resistance vs Temperature

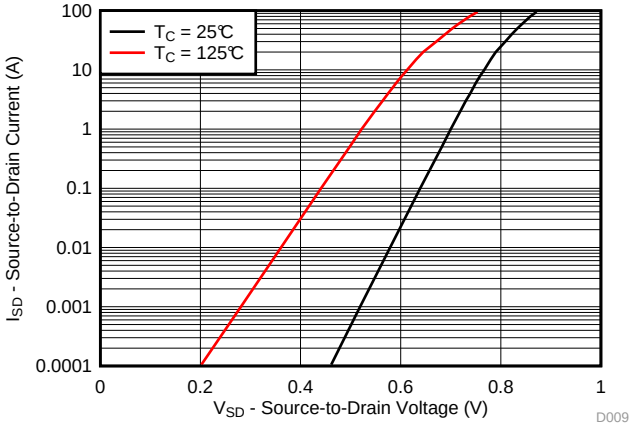
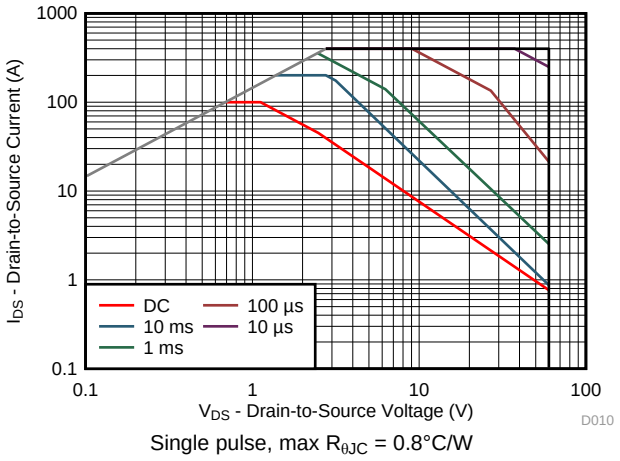


Figure 9. Typical Diode Forward Voltage



Single pulse, max $R_{\theta JC}$ = 0.8°C/W

Figure 10. Maximum Safe Operating Area

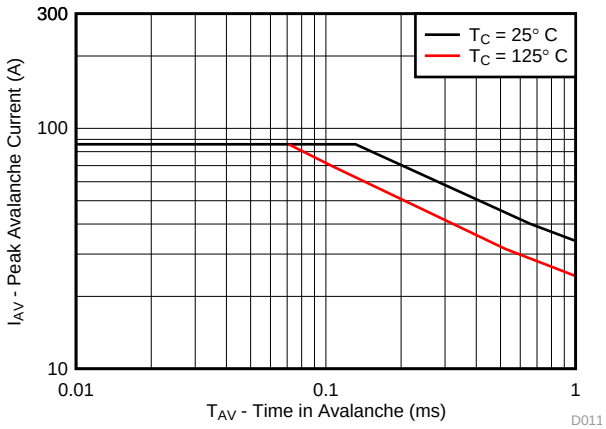


Figure 11. Single Pulse Unclamped Inductive Switching

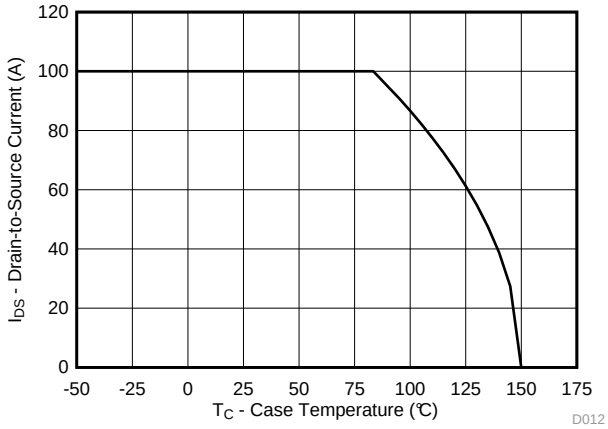


Figure 12. Maximum Drain Current vs Temperature

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6 器件和文档支持

6.1 接收文档更新通知

要接收文档更新通知，请导航至 TI.com 上的器件产品文件夹。请单击右上角的*提醒我* 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

6.2 社区资源

下列链接提供到 TI 社区资源的连接。链接的内容由各个分销商“按照原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的 《使用条款》。

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设计支持 ***TI 参考设计支持*** 可帮助您快速查找有帮助的 E2E 论坛、设计支持工具以及技术支持的联系信息。

6.3 商标

NexFET, E2E are trademarks of Texas Instruments.
All other trademarks are the property of their respective owners.

6.4 静电放电警告

这些装置包含有限的内置 ESD 保护。 存储或装卸时，应将导线一起截短或将装置放置于导电泡棉中，以防止 MOS 门极遭受静电损伤。

6.5 Glossary

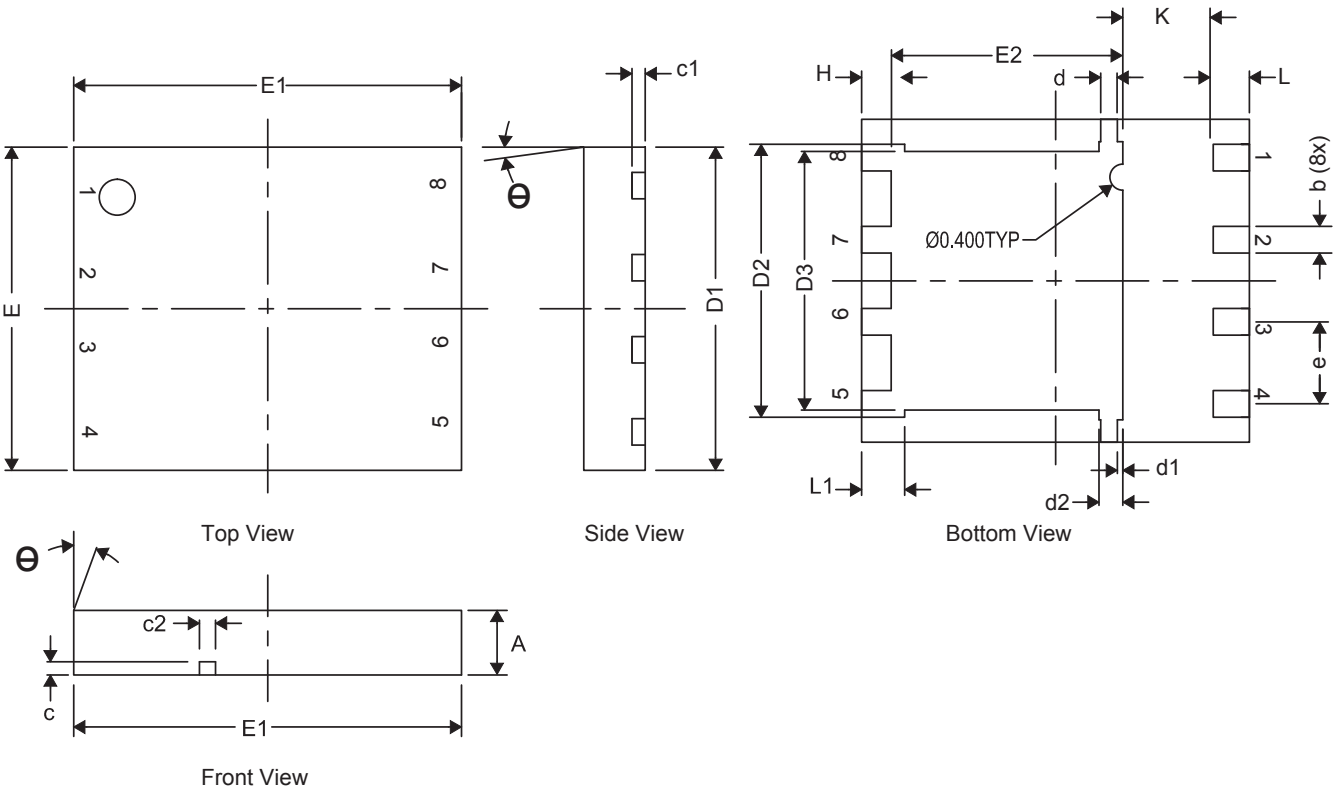
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

7 机械、封装和可订购信息

以下页面包含机械、封装和可订购信息。这些信息是指定器件的最新可用数据。数据如有变更，恕不另行通知和修订此文档。如欲获取此数据表的浏览器版本，请参阅左侧的导航。

7.1 Q5B 封装尺寸



DIM	毫米		
	最小值	标称值	最大值
A	0.80	1.00	1.05
b	0.36	0.41	0.46
c	0.15	0.20	0.25
c1	0.15	0.20	0.25
c2	0.20	0.25	0.30
D1	4.90	5.00	5.10
D2	4.12	4.22	4.32
d	0.20	0.25	0.30
E	4.90	5.00	5.10
E1	5.90	6.00	6.10
E2	3.48	3.58	3.68
e		1.27 典型值	
L	0.46	0.56	0.66
θ	0°	—	—
K		1.40 典型值	

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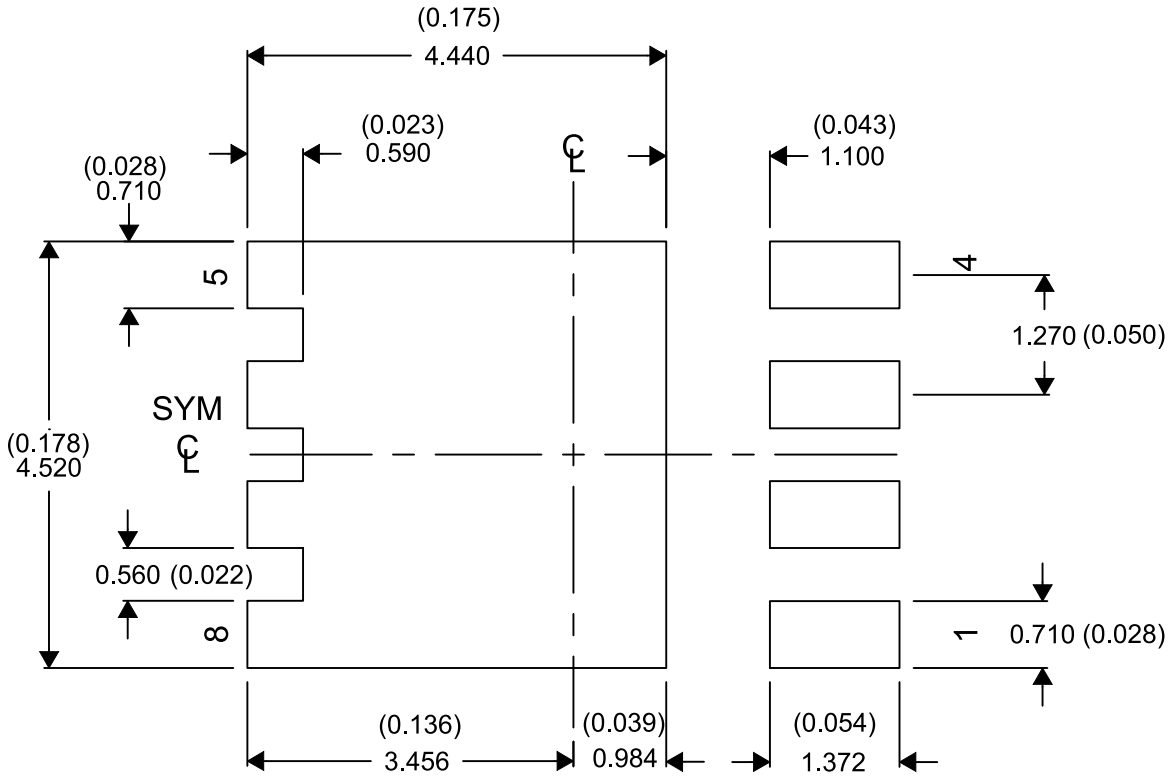
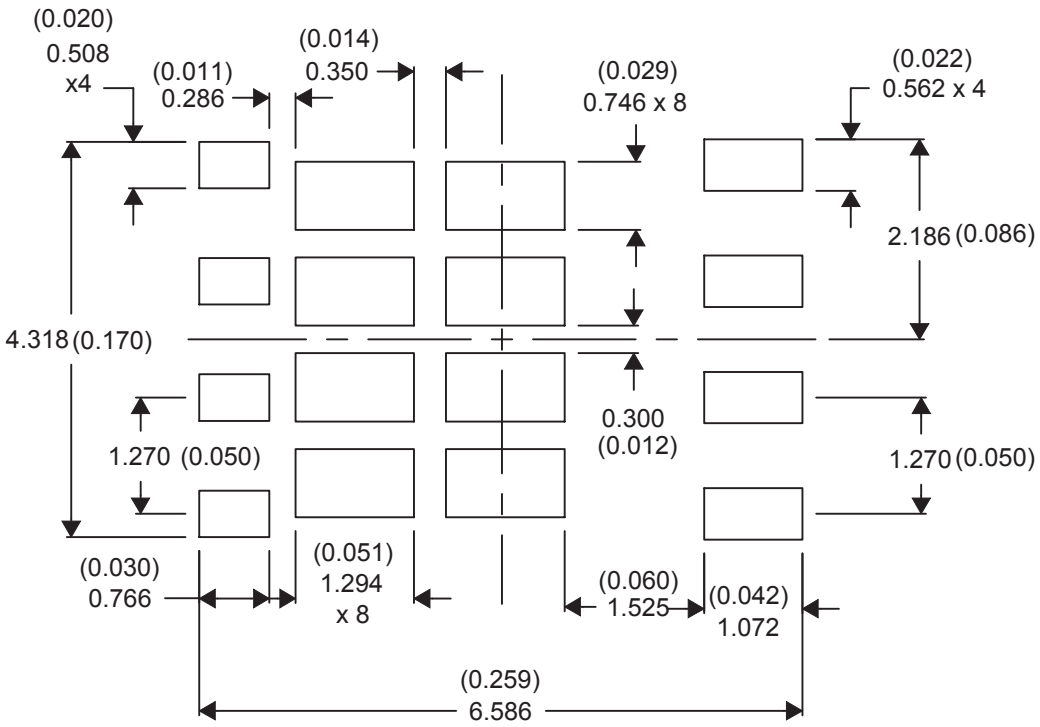
7.2 建议 PCB 布局

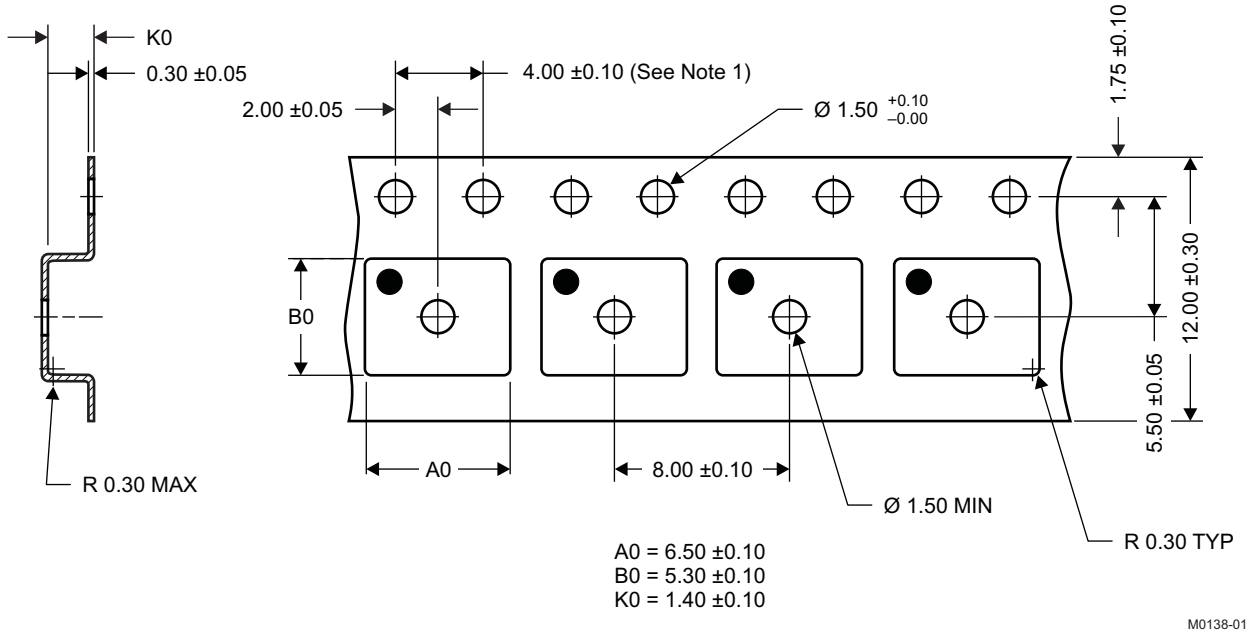


如需了解针对 PCB 设计的建议电路布局，请参阅*《通过 PCB 布局技巧来减少振铃》*(SLPA005)。

7.3 建议模板布局



7.4 Q5B 卷带信息



注释：

1. 10 个链齿孔的累积容差为 ±0.2。
2. 每 100mm 长度的翘曲不能超过 1mm，在 250mm 长度上不累积。
3. 材料：黑色抗静电聚苯乙烯。
4. 全部尺寸为 mm（除非另外注明）。
5. 高于孔眼底部 0.3mm 的平面上测量得到 A0 和 B0 值.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD18532NQ5B	ACTIVE	VSON-CLIP	DNK	8	2500	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	18532N	Samples
CSD18532NQ5BT	ACTIVE	VSON-CLIP	DNK	8	250	RoHS-Exempt & Green	SN	Level-1-260C-UNLIM	-55 to 150	18532N	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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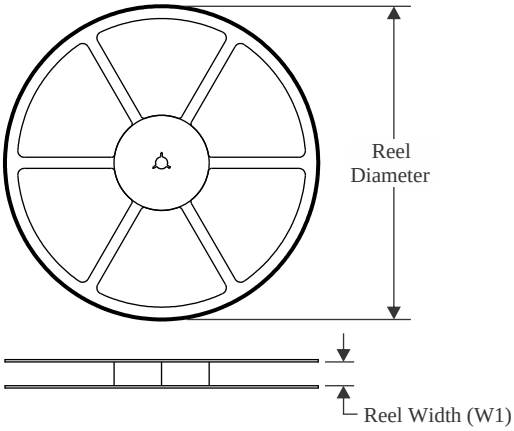
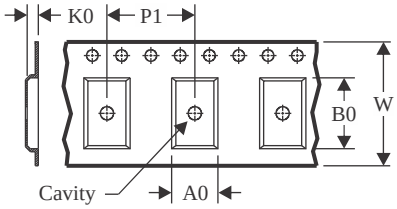
TAPE AND REEL INFORMATION

REEL DIMENSIONS

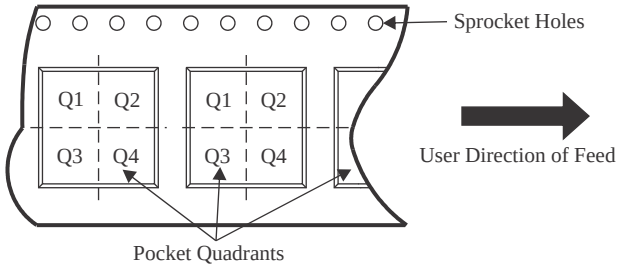


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

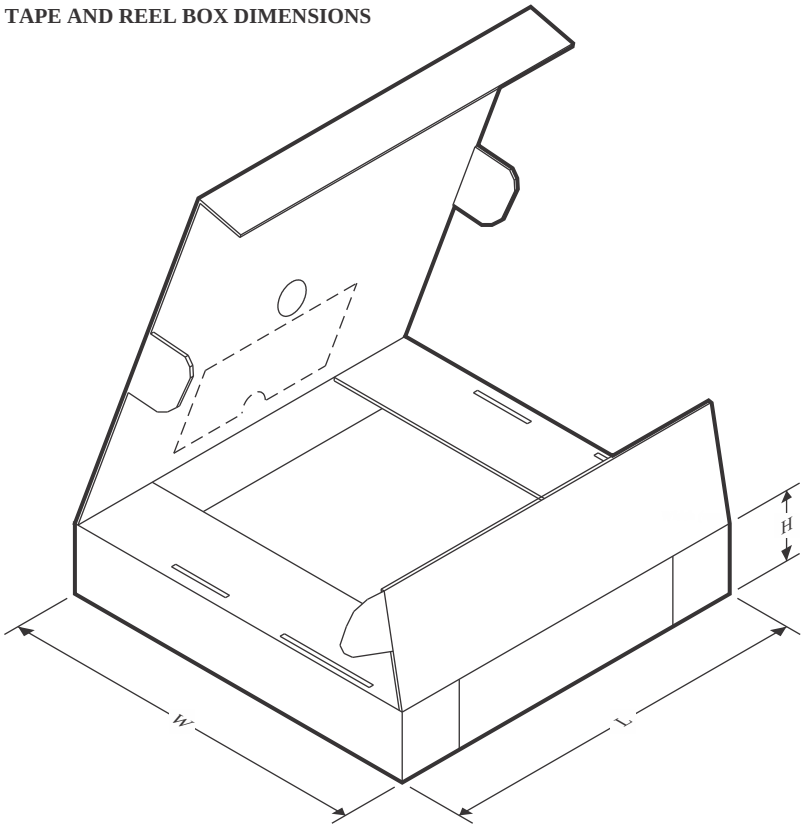
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD18532NQ5BT	VSON-CLIP	DNK	8	250	330.0	12.4	6.3	5.3	1.2	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD18532NQ5BT	VSON-CLIP	DNK	8	250	335.0	335.0	32.0

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