ELPIDA

PRELIMINARY DATA SHEET

8GB Registered DDR2 SDRAM DIMM

EBE82AF4A1RA (1024M words × 72 bits, 4 Ranks)

Specifications

- Density: 8GB
- Organization
  - 1024M words × 72 bits, 4 ranks
- Mounting 36 pieces of 2G bits DDR2 SDRAM with DDP (FBGA)
  - DDP: 2 pieces of 1Gb chips sealed in one package
- Package: 240-pin socket type dual in line memory module (DIMM)
  - PCB height: 30.0mm
  - Lead pitch: 1.0mm
  - Lead-free (RoHS compliant)
- Power supply: VDD = 1.8V ± 0.1V
- Data rate: 667Mbps/533Mbps (max.)
- Eight internal banks for concurrent operation (components)
- Interface: SSTL_18
- Burst lengths (BL): 4, 8
- /CAS Latency (CL): 3, 4, 5
- Precharge: auto precharge option for each burst access
- Refresh: auto-refresh, self-refresh
- Refresh cycles: 8192 cycles/64ms
  - Average refresh period
    7.8µs at 0°C ≤ TC ≤ +85°C
    3.9µs at +85°C < TC ≤ +95°C
- Operating case temperature range
  - TC = 0°C to +95°C

Features

- Double-data-rate architecture; two data transfers per clock cycle
- The high-speed data transfer is realized by the 4 bits prefetch pipelined architecture
- Bi-directional differential data strobe (DQS and /DQS) is transmitted/received with data for capturing data at the receiver
- DQS is edge-aligned with data for READs; center-aligned with data for WRITEs
- Differential clock inputs (CK and /CK)
- DLL aligns DQ and DQS transitions with CK transitions
- Commands entered on each positive CK edge; data referenced to both edges of DQS
- Posted /CAS by programmable additive latency for better command and data bus efficiency
- Off-Chip-Driver Impedance Adjustment and On-Die-Termination for better signal quality
- /DQS can be disabled for single-ended Data Strobe operation
- 1 piece of PLL clock driver, 2 pieces of register driver and 1 piece of serial EEPROM (2K bits EEPROM) for Presence Detect (PD)

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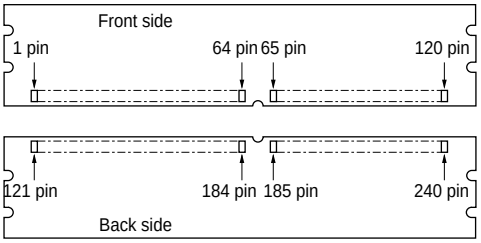
Ordering Information

Part number	Data rate Mbps (max.)	Component JEDEC speed bin*[1] (CL-tRCD-tRP)	Package	Contact pad	Mounted devices
EBE82AF4A1RA-6E-E	667	DDR2-667 (5-5-5)	240-pin DIMM (lead-free)	Gold	2G bits DDR2 SDRAM*[2]
EBE82AF4A1RA-5C-E	533	DDR2-533 (4-4-4)			

Notes: 1. Module /CAS latency = component CL + 1.

2. Please refer to 1Gb DDR2 datasheet (E0975E) for electrical characteristics.

Pin Configurations



Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
1	VREF	61	A4	121	VSS	181	VDD
2	VSS	62	VDD	122	DQ4	182	A3
3	DQ0	63	A2	123	DQ5	183	A1
4	DQ1	64	VDD	124	VSS	184	VDD
5	VSS	65	VSS	125	DQS9	185	CK0
6	/DQS0	66	VSS	126	/DQS9	186	/CK0
7	DQS0	67	VDD	127	VSS	187	VDD
8	VSS	68	Par_In	128	DQ6	188	A0
9	DQ2	69	VDD	129	DQ7	189	VDD
10	DQ3	70	A10	130	VSS	190	BA1
11	VSS	71	BA0	131	DQ12	191	VDD
12	DQ8	72	VDD	132	DQ13	192	/RAS
13	DQ9	73	/WE	133	VSS	193	/CS0
14	VSS	74	/CAS	134	DQS10	194	VDD
15	/DQS1	75	VDD	135	/DQS10	195	ODT0
16	DQS1	76	/CS1	136	VSS	196	A13
17	VSS	77	ODT1	137	NC	197	VDD
18	/RESET	78	VDD	138	NC	198	VSS
19	NC	79	VSS	139	VSS	199	DQ36
20	VSS	80	DQ32	140	DQ14	200	DQ37
21	DQ10	81	DQ33	141	DQ15	201	VSS
22	DQ11	82	VSS	142	VSS	202	DQS13
23	VSS	83	/DQS4	143	DQ20	203	/DQS13
24	DQ16	84	DQS4	144	DQ21	204	VSS
25	DQ17	85	VSS	145	VSS	205	DQ38
26	VSS	86	DQ34	146	DQS11	206	DQ39
27	/DQS2	87	DQ35	147	/DQS11	207	VSS

Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name	Pin No.	Pin name
28	DQS2	88	VSS	148	VSS	208	DQ44
29	VSS	89	DQ40	149	DQ22	209	DQ45
30	DQ18	90	DQ41	150	DQ23	210	VSS
31	DQ19	91	VSS	151	VSS	211	DQS14
32	VSS	92	/DQS5	152	DQ28	212	/DQS14
33	DQ24	93	DQS5	153	DQ29	213	VSS
34	DQ25	94	VSS	154	VSS	214	DQ46
35	VSS	95	DQ42	155	DQS12	215	DQ47
36	/DQS3	96	DQ43	156	/DQS12	216	VSS
37	DQS3	97	VSS	157	VSS	217	DQ52
38	VSS	98	DQ48	158	DQ30	218	DQ53
39	DQ26	99	DQ49	159	DQ31	219	VSS
40	DQ27	100	VSS	160	VSS	220	/CS2
41	VSS	101	SA2	161	CB4	221	/CS3
42	CB0	102	NC	162	CB5	222	VSS
43	CB1	103	VSS	163	VSS	223	DQS15
44	VSS	104	/DQS6	164	DQS17	224	/DQS15
45	/DQS8	105	DQS6	165	/DQS17	225	VSS
46	DQS8	106	VSS	166	VSS	226	DQ54
47	VSS	107	DQ50	167	CB6	227	DQ55
48	CB2	108	DQ51	168	CB7	228	VSS
49	CB3	109	VSS	169	VSS	229	DQ60
50	VSS	110	DQ56	170	VDD	230	DQ61
51	VDD	111	DQ57	171	CKE1	231	VSS
52	CKE0	112	VSS	172	VDD	232	DQS16
53	VDD	113	/DQS7	173	NC	233	/DQS16
54	BA2	114	DQS7	174	NC	234	VSS
55	/Err_Out	115	VSS	175	VDD	235	DQ62
56	VDD	116	DQ58	176	A12	236	DQ63
57	A11	117	DQ59	177	A9	237	VSS
58	A7	118	VSS	178	VDD	238	VDDSPD
59	VDD	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

Pin Description

Pin name	Function	
A0 to A13	Address input Row address Column address	 A0 to A13 A0 to A9, A11
A10 (AP)	Auto precharge	
BA0, BA1, BA2	Bank select address	
DQ0 to DQ63	Data input/output	
CB0 to CB7	Check bit (Data input/output)	
/RAS	Row address strobe command	
/CAS	Column address strobe command	
/WE	Write enable	
/CS0 to /CS3	Chip select	
CKE0, CKE1	Clock enable	
CK0	Clock input	
/CK0	Differential clock input	
DQS0 to DQS17, /DQS0 to /DQS17	Input and output data strobe	
SCL	Clock input for serial PD	
SDA	Data input/output for serial PD	
SA0 to SA2	Serial address input	
VDD	Power for internal circuit	
VDDSPD	Power for serial EEPROM	
VREF	Input reference voltage	
VSS	Ground	
ODT0, ODT1	ODT control	
/RESET	Reset pin (forces register and PLL inputs low) *1	
Par_In*2	Parity bit for the address and control bus	
/Err_Out*2	Parity error found on the address and control bus	
NC	No connection	

Notes: 1. Reset pin is connected to both OE of PLL and reset to register.

2. /Err_Out (Pin No. 55) and Par_In (Pin No. 68) are for optional function to check address and command parity.

Serial PD Matrix

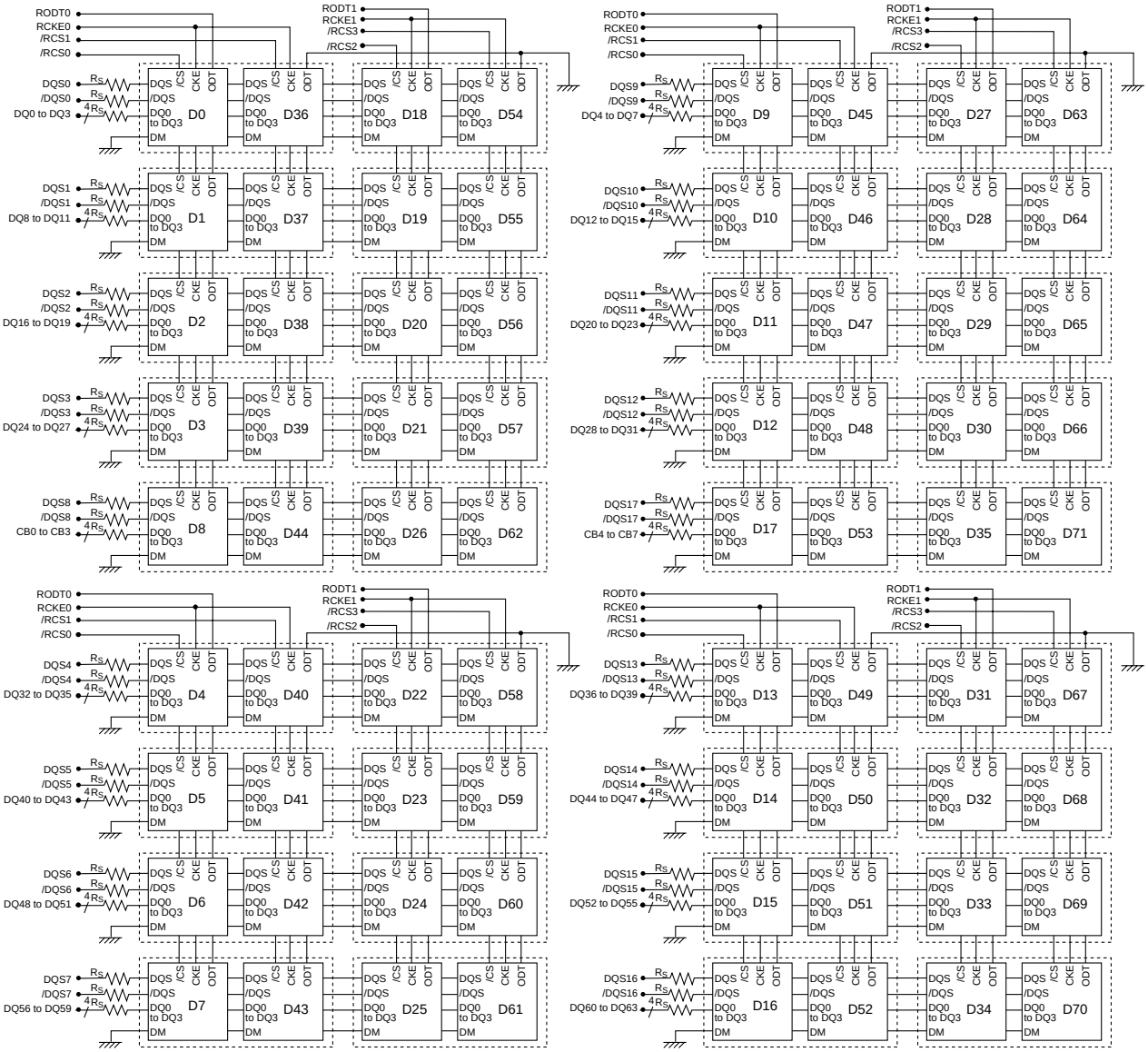
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
0	Number of bytes utilized by module manufacturer	1	0	0	0	0	0	0	0	80H	128 bytes
1	Total number of bytes in serial PD device	0	0	0	0	1	0	0	0	08H	256 bytes
2	Memory type	0	0	0	0	1	0	0	0	08H	DDR2 SDRAM
3	Number of row address	0	0	0	0	1	1	1	0	0EH	14
4	Number of column address	0	0	0	0	1	0	1	1	0BH	11
5	Number of DIMM ranks	0	1	1	1	0	0	1	1	73H	DDP/4 ranks
6	Module data width	0	1	0	0	1	0	0	0	48H	72
7	Module data width continuation	0	0	0	0	0	0	0	0	00H	0
8	Voltage interface level of this assembly	0	0	0	0	0	1	0	1	05H	SSTL 1.8V
9	DDR SDRAM cycle time, CL = 5 -6E	0	0	1	1	0	0	0	0	30H	3.0ns*[1]
	-5C	0	0	1	1	1	1	0	1	3DH	3.75ns*[1]
10	SDRAM access from clock (tAC) -6E	0	1	0	0	0	1	0	1	45H	0.45ns*[1]
	-5C	0	1	0	1	0	0	0	0	50H	0.5ns*[1]
11	DIMM configuration type	0	0	0	0	0	1	1	0	06H	ECC, Address/ command Parity
12	Refresh rate/type	1	0	0	0	0	0	1	0	82H	7.8µs
13	Primary SDRAM width	0	0	0	0	0	1	0	0	04H	× 4
14	Error checking SDRAM width	0	0	0	0	0	1	0	0	04H	× 4
15	Reserved	0	0	0	0	0	0	0	0	00H	0
16	SDRAM device attributes: Burst length supported	0	0	0	0	1	1	0	0	0CH	4,8
17	SDRAM device attributes: Number of banks on SDRAM device	0	0	0	0	1	0	0	0	08H	8
18	SDRAM device attributes: /CAS latency	0	0	1	1	1	0	0	0	38H	3, 4, 5
19	DIMM Mechanical Characteristics	0	0	0	0	0	0	1	0	02H	6.00mm max.
20	DIMM type information	0	0	0	0	0	0	0	1	01H	Registered
21	SDRAM module attributes	0	0	0	0	0	0	0	0	00H	Normal
22	SDRAM device attributes: General	0	0	0	0	0	0	1	1	03H	Weak Driver 50Ω ODT Support
23	Minimum clock cycle time at CL = 4	0	0	1	1	1	1	0	1	3DH	3.75ns*[1]
24	Maximum data access time (tAC) from clock at CL = 4	0	1	0	1	0	0	0	0	50H	0.5ns*[1]
25	Minimum clock cycle time at CL = 3	0	1	0	1	0	0	0	0	50H	5.0ns*[1]
26	Maximum data access time (tAC) from clock at CL = 3	0	1	1	0	0	0	0	0	60H	0.6ns*[1]
27	Minimum row precharge time (tRP)	0	0	1	1	1	1	0	0	3CH	15ns
28	Minimum row active to row active delay (tRRD)	0	0	0	1	1	1	1	0	1EH	7.5ns
29	Minimum /RAS to /CAS delay (tRCD)	0	0	1	1	1	1	0	0	3CH	15ns
30	Minimum active to precharge time (tRAS)	0	0	1	0	1	1	0	1	2DH	45ns
31	Module rank density	0	0	0	0	0	0	1	0	02H	2GB

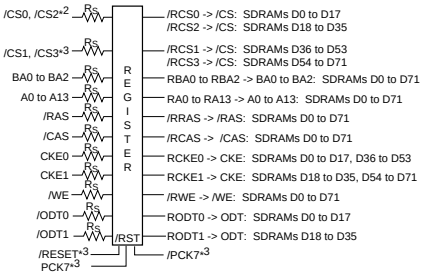
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
32	Address and command setup time before clock (tIS) -6E	0	0	1	0	0	0	0	0	20H	0.20ns*[1]
	-5C	0	0	1	0	0	1	0	1	25H	0.25ns*[1]
33	Address and command hold time after clock (tIH) -6E	0	0	1	0	0	1	1	1	27H	0.27ns*[1]
	-5C	0	0	1	1	0	1	1	1	37H	0.37ns*[1]
34	Data input setup time before clock (tDS)	0	0	0	1	0	0	0	0	10H	0.10ns*[1]
35	Data input hold time after clock (tDH) -6E	0	0	0	1	0	1	1	1	17H	0.17ns*[1]
	-5C	0	0	1	0	0	0	1	0	22H	0.22ns*[1]
36	Write recovery time (tWR)	0	0	1	1	1	1	0	0	3CH	15ns*[1]
37	Internal write to read command delay (tWTR)	0	0	0	1	1	1	1	0	1EH	7.5ns*[1]
38	Internal read to precharge command delay (tRTP)	0	0	0	1	1	1	1	0	1EH	7.5ns*[1]
39	Memory analysis probe characteristics	0	0	0	0	0	0	0	0	00H	TBD
40	Extension of Byte 41 and 42	0	0	0	0	0	1	1	0	06H	
41	Active command period (tRC)	0	0	1	1	1	1	0	0	3CH	60ns*[1]
42	Auto refresh to active/ Auto refresh command cycle (tRFC)	0	1	1	1	1	1	1	1	7FH	127.5ns*[1]
43	SDRAM tCK cycle max. (tCK max.)	1	0	0	0	0	0	0	0	80H	8ns*[1]
44	Dout to DQS skew -6E	0	0	0	1	1	0	0	0	18H	0.24ns*[1]
	-5C	0	0	0	1	1	1	1	0	1EH	0.30ns*[1]
45	Data hold skew (tQHS) -6E	0	0	1	0	0	0	1	0	22H	0.34ns*[1]
	-5C	0	0	1	0	1	0	0	0	28H	0.40ns*[1]
46	PLL relock time	0	0	0	0	1	1	1	1	0FH	15µs
47 to 61		0	0	0	0	0	0	0	0	00H	
62	SPD Revision	0	0	0	1	0	0	1	0	12H	Rev. 1.2
63	Checksum for bytes 0 to 62 -6E	0	1	0	0	0	1	0	0	44H	
	-5C	1	0	0	0	1	0	0	0	88H	
64 to 65	Manufacturer's JEDEC ID code	0	1	1	1	1	1	1	1	7FH	Continuation code
66	Manufacturer's JEDEC ID code	1	1	1	1	1	1	1	0	FEH	Elpida Memory
67 to 71	Manufacturer's JEDEC ID code	0	0	0	0	0	0	0	0	00H	
72	Manufacturing location	×	×	×	×	×	×	×	×	××	(ASCII-8bit code)
73	Module part number	0	1	0	0	0	1	0	1	45H	E
74	Module part number	0	1	0	0	0	0	1	0	42H	B
75	Module part number	0	1	0	0	0	1	0	1	45H	E
76	Module part number	0	0	1	1	1	0	0	0	38H	8
77	Module part number	0	0	1	1	0	0	1	0	32H	2
78	Module part number	0	1	0	0	0	0	0	1	41H	A
79	Module part number	0	1	0	0	0	1	1	0	46H	F
80	Module part number	0	0	1	1	0	1	0	0	34H	4

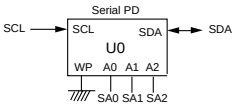
Byte No.	Function described	Bit7	Bit6	Bit5	Bit4	Bit3	Bit2	Bit1	Bit0	Hex value	Comments
81	Module part number	0	1	0	0	0	0	0	1	41H	A
82	Module part number	0	0	1	1	0	0	0	1	31H	1
83	Module part number	0	1	0	1	0	0	1	0	52H	R
84	Module part number	0	1	0	0	0	0	0	1	41H	A
85	Module part number	0	0	1	0	1	1	0	1	2DH	—
86	Module part number -6E	0	0	1	1	0	1	1	0	36H	6
	-5C	0	0	1	1	0	1	0	1	35H	5
87	Module part number -6E	0	1	0	0	0	1	0	1	45H	E
	-5C	0	1	0	0	0	0	1	1	43H	C
88	Module part number	0	0	1	0	1	1	0	1	2DH	—
89	Module part number	0	1	0	0	0	1	0	1	45H	E
90	Module part number	0	0	1	0	0	0	0	0	20H	(Space)
91	Revision code	0	0	1	1	0	0	0	0	30H	Initial
92	Revision code	0	0	1	0	0	0	0	0	20H	(Space)
93	Manufacturing date	×	×	×	×	×	×	×	×	××	Year code (BCD)
94	Manufacturing date	×	×	×	×	×	×	×	×	××	Week code (BCD)
95 to 98	Module serial number										
99 to 127	Manufacture specific data										

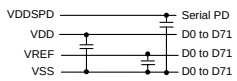
Note: 1. These specifications are defined based on component specification, not module.

Block Diagram







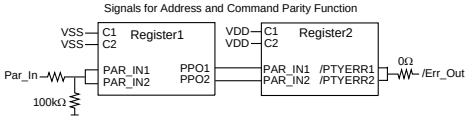


D0 to D71: 1G bits DDR2 SDRAM
U0: 2k bits EEPROM
R_S: 22Ω
PLL: CU2A877
Register: SSTUB32868H



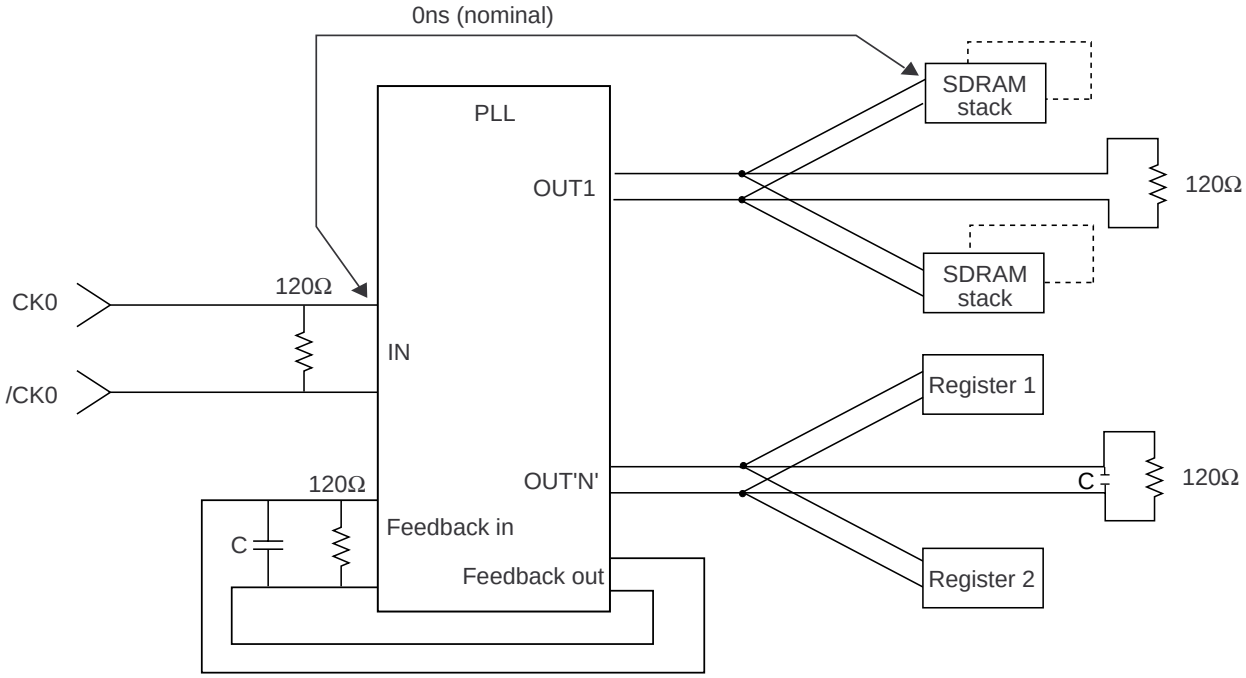
Notes:
1. DQ wiring may be changed within a nibble.
2. /CS0 connects to /DCS0, /CS1 to /DCS1 on register1, /CS2 connects to /DCS0, /CS3 to /DCS1 on register2. /CS1 connects to /CSR on register1 and /DCS on register2.
3. /RESET, PCK7 and /PCK7 connect to all registers. Other signals connect to one of two registers.

Signals for Address and Command Parity Function



Register1 share a part of address/command input signal set.
Register2 share the other part of address/command input signal set.
0Ω resistor on /Err_Out is not populated for non-parity card.

Differential Clock Net Wiring (CK0, /CK0)



Notes: 1. The clock delay from the input of the PLL clock to the input of any SDRAM or register willl be set to 0ns (nominal).

2. Input, output and feedback clock lines are terminated from line to line as shown, and not from line to ground.

3. Only one PLL output is shown per output type. Any additional PLL outputs will be wired in a similar manner.

4. Termination resistors for the PLL feedback path clocks are located as close to the input pin of the PLL as possible.

Electrical Specifications

- All voltages are referenced to VSS (GND).

Absolute Maximum Ratings

Parameter	Symbol	Value	Unit	Notes
Voltage on any pin relative to VSS	VT	–0.5 to +2.3	V	1
Supply voltage relative to VSS	VDD	–0.5 to +2.3	V	
Short circuit output current	IOS	50	mA	1
Power dissipation	PD	18	W	
Operating case temperature	TC	0 to +95	°C	1, 2
Storage temperature	Tstg	–55 to +100	°C	1

Notes: 1. DDR2 SDRAM component specification.

2. Supporting 0°C to +85°C and being able to extend to +95°C with doubling auto-refresh commands in frequency to a 32ms period (tREFI = 3.9µs) and higher temperature self-refresh entry via the control of EMRS (2) bit A7 is required.

Caution

Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

DC Operating Conditions (TC = 0°C to +85°C) (DDR2 SDRAM Component Specification)

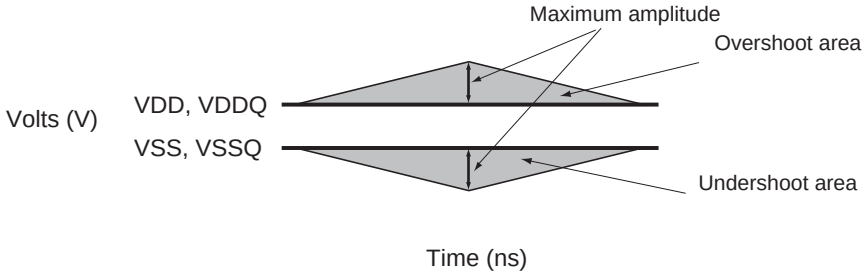
Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	VDD, VDDQ	1.7	1.8	1.9	V	4
	VSS	0	0	0	V	
	VDDSPD	1.7	—	3.6	V	
Input reference voltage	VREF	0.49 × VDDQ	0.50 × VDDQ	0.51 × VDDQ	V	1, 2
Termination voltage	VTT	VREF – 0.04	VREF	VREF + 0.04	V	3
DC input logic high	VIH (DC)	VREF + 0.125	—	VDDQ + 0.3	V	
DC input low	VIL (DC)	–0.3	—	VREF – 0.125	V	
AC input logic high -6E	VIH (AC)	VREF + 0.200	—	—	V	
-5C	VIH (AC)	VREF + 0.250	—	—	V	
AC input logic low -6E	VIL (AC)	—	—	VREF – 0.200	V	
-5C	VIL (AC)	—	—	VREF – 0.250	V	

Notes: 1. The value of VREF may be selected by the user to provide optimum noise margin in the system. Typically the value of VREF is expected to be about 0.5 × VDDQ of the transmitting device and VREF are expected to track variations in VDDQ.

2. Peak to peak AC noise on VREF may not exceed ±2% VREF (DC).
3. VTT of transmitting device must track VREF of receiving device.
4. VDDQ must be equal to VDD.

AC Overshoot/Undershoot Specification (DDR2 SDRAM Component Specification)

Parameter	Pins	Specification	Unit
Maximum peak amplitude allowed for overshoot	Command, Address, CKE, ODT	0.5	V
Maximum peak amplitude allowed for undershoot		0.5	V
Maximum overshoot area above VDD DDR2-667		0.8	V-ns
DDR2-533		1.0	V-ns
Maximum undershoot area below VSS DDR2-667		0.8	V-ns
DDR2-533		1.0	V-ns
Maximum peak amplitude allowed for overshoot	CK, /CK	0.5	V
Maximum peak amplitude allowed for undershoot		0.5	V
Maximum overshoot area above VDD DDR2-667		0.23	V-ns
DDR2-533		0.28	V-ns
Maximum undershoot area below VSS DDR2-667		0.23	V-ns
DDR2-533		0.28	V-ns
Maximum peak amplitude allowed for overshoot	DQ, DQS, /DQS, UDQS, /UDQS, LDQS, /LDQS, RDQS, /RDQS, DM, UDM, LDM	0.5	V
Maximum peak amplitude allowed for undershoot		0.5	V
Maximum overshoot area above VDDQ DDR2-667		0.23	V-ns
DDR2-533		0.28	V-ns
Maximum undershoot area below VSSQ DDR2-667		0.23	V-ns
DDR2-533		0.28	V-ns



Overshoot/Undershoot Definition

DC Characteristics 1 (TC = 0°C to +85°C, VDD = 1.8V ± 0.1V, VSS = 0V)

Parameter	Symbol	Grade	max.	Unit	Test condition	
Operating current (ACT-PRE)	IDD0		TBD	mA	one bank; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS min.(IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	
Operating current (ACT-READ-PRE)	IDD1		TBD	mA	one bank; IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRC = tRC (IDD), tRAS = tRAS min.(IDD); tRCD = tRCD (IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	
Precharge power-down standby current	IDD2P		TBD	mA	all banks idle; tCK = tCK (IDD); CKE is L; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	
Precharge quiet standby current	IDD2Q		TBD	mA	all banks idle; tCK = tCK (IDD); CKE is H, /CS is H; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	
Idle standby current	IDD2N		TBD	mA	all banks idle; tCK = tCK (IDD); CKE is H, /CS is H; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	
Active power-down standby current	IDD3P-F		TBD	mA	all banks open; tCK = tCK (IDD); CKE is L; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0
	IDD3P-S		TBD	mA		Slow PDN Exit MRS(12) = 1
Active standby current	IDD3N		TBD	mA	all banks open; tCK = tCK (IDD), tRAS = tRAS max.(IDD), tRP = tRP (IDD); CKE is H, /CS is H between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	
Operating current (Burst read operating)	IDD4R		TBD	mA	all banks open, continuous burst reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS max.(IDD), tRP = tRP (IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data pattern is same as IDD4W	
Operating current (Burst write operating)	IDD4W		TBD	mA	all banks open, continuous burst writes; BL = 4, CL = CL(IDD), AL = 0; tCK = tCK (IDD), tRAS = tRAS max.(IDD), tRP = tRP (IDD); CKE is H, /CS is H between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	

Parameter	Symbol	Grade	max	Unit	Test condition
Auto-refresh current	IDD5		TBD	mA	tCK = tCK (IDD); Refresh command at every tRFC (IDD) interval; CKE is H, /CS is H between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING
Self-refresh current	IDD6		TBD	mA	Self Refresh Mode; CK and /CK at 0V; CKE ≤ 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING
Operating current (Bank interleaving)	IDD7		TBD	mA	all bank interleaving reads, IOUT = 0mA; BL = 4, CL = CL(IDD), AL = tRCD (IDD) –1 × tCK(IDD); tCK = tCK (IDD), tRC = tRC (IDD), tRRD = tRRD (IDD), tFAW = tFAW (IDD), tRCD = 1 × tCK (IDD); CKE is H, /CS is H between valid commands; Address bus inputs are STABLE during DESELECTs; Data pattern is same as IDD4W;

Notes: 1. IDD specifications are tested after the device is properly initialized.

2. Input slew rate is specified by AC Input Test Condition.
3. IDD parameters are specified with ODT disabled.
4. Data bus consists of DQ, DM, DQS, /DQS, RDQS and /RDQS. IDD values must be met with all combinations of EMRS bits 10 and 11.
5. Definitions for IDD

   L is defined as VIN ≤ VIL (AC) (max.)

   H is defined as VIN ≥ VIH (AC) (min.)

   STABLE is defined as inputs stable at an H or L level

   FLOATING is defined as inputs at VREF = VDDQ/2

   SWITCHING is defined as:

   inputs changing between H and L every other clock cycle (once per two clocks) for address and control signals, and inputs changing between H and L every other data transfer (once per clock) for DQ signals not including masks or strobes.
6. Refer to AC Timing for IDD Test Conditions.

AC Timing for IDD Test Conditions

For purposes of IDD testing, the following parameters are to be utilized.

	DDR2-667	DDR2-533	
Parameter	5-5-5	4-4-4	Unit
CL (IDD)	5	4	tCK
tRCD (IDD)	15	15	ns
tRC (IDD)	60	60	ns
tRRD (IDD)	7.5	7.5	ns
tFAW (IDD)	37.5	37.5	ns
tCK (IDD)	3	3.75	ns
tRAS (min.)(IDD)	45	45	ns
tRAS (max.)(IDD)	70000	70000	ns
tRP (IDD)	15	15	ns
tRFC (IDD)	127.5	127.5	ns

DC Characteristics 2 (TC = 0°C to +85°C, VDD, VDDQ = 1.8V ± 0.1V)

(DDR2 SDRAM Component Specification)

Parameter	Symbol	Value	Unit	Notes
Input leakage current	|ILI|	2	µA	VDD ≥ VIN ≥ VSS
Output leakage current	|ILO|	5	µA	VDDQ ≥ VOUT ≥ VSS
Minimum required output pull-up under AC test load	VOH	VTT + 0.603	V	5
Maximum required output pull-down under AC test load	VOL	VTT – 0.603	V	5
Output timing measurement reference level	VOTR	0.5 × VDDQ	V	1
Output minimum sink DC current	IOL	+13.4	mA	3, 4, 5
Output minimum source DC current	IOH	–13.4	mA	2, 4, 5

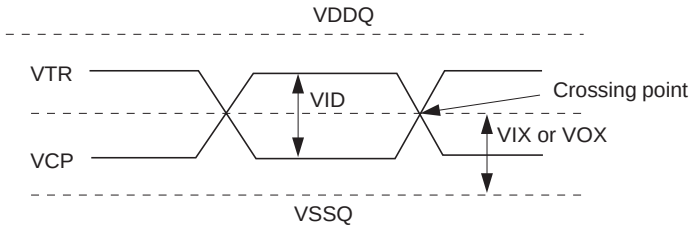
Notes: 1. The VDDQ of the device under test is referenced.
2. VDDQ = 1.7V; VOUT = 1.42V.
3. VDDQ = 1.7V; VOUT = 0.28V.
4. The DC value of VREF applied to the receiving device is expected to be set to VTT.
5. After OCD calibration to 18Ω at TC = 25°C, VDD = VDDQ = 1.8V.

DC Characteristics 3 (TC = 0°C to +85°C, VDD, VDDQ = 1.8V ± 0.1V)

(DDR2 SDRAM Component Specification)

Parameter	Symbol	min.	max.	Unit	Notes
AC differential input voltage	VID (AC)	0.5	VDDQ + 0.6	V	1, 2
AC differential cross point voltage	VIX (AC)	0.5 × VDDQ – 0.175	0.5 × VDDQ + 0.175	V	2
AC differential cross point voltage	VOX (AC)	0.5 × VDDQ – 0.125	0.5 × VDDQ + 0.125	V	3

Notes: 1. VID (AC) specifies the input differential voltage |VTR -VCP| required for switching, where VTR is the true input signal (such as CK, DQS, RDQS) and VCP is the complementary input signal (such as /CK, /DQS, /RDQS). The minimum value is equal to VIH (AC) – VIL (AC).
2. The typical value of VIX(AC) is expected to be about 0.5 × VDDQ of the transmitting device and VIX(AC) is expected to track variations in VDDQ . VIX(AC) indicates the voltage at which differential input signals must cross.
3. The typical value of VOX(AC) is expected to be about 0.5 × VDDQ of the transmitting device and VOX(AC) is expected to track variations in VDDQ . VOX(AC) indicates the voltage at which differential output signals must cross.



Differential Signal Levels*1, 2

ODT DC Electrical Characteristics (TC = 0°C to +85°C, VDD, VDDQ = 1.8V ± 0.1V)

(DDR2 SDRAM Component Specification)

Parameter	Symbol	min.	typ.	max.	Unit	Note
Rtt effective impedance value for EMRS (A6, A2) = 0, 1; 75 Ω	Rtt1(eff)	60	75	90	Ω	1
Rtt effective impedance value for EMRS (A6, A2) = 1, 0; 150 Ω	Rtt2(eff)	120	150	180	Ω	1
Rtt effective impedance value for EMRS (A6, A2) = 1, 1; 50 Ω	Rtt3(eff)	40	50	60	Ω	1
Deviation of VM with respect to VDDQ/2	ΔVM	–6	—	+6	%	1

Note: 1. Test condition for Rtt measurements.

Measurement Definition for Rtt (eff)

Apply VIH (AC) and VIL (AC) to test pin separately, then measure current I(VIH(AC)) and I(VIL(AC)) respectively. VIH(AC), and VDDQ values defined in SSTL_18.

$$Rtt(eff) = \frac{VIH(AC) - VIL(AC)}{I(VIH(AC)) - I(VIL(AC))}$$

Measurement Definition for ΔVM

Measure voltage (VM) at test pin (midpoint) with no load.

$$\Delta VM = \left(\frac{2 \times VM}{VDDQ} - 1 \right) \times 100$$

OCD Default Characteristics (TC = 0°C to +85°C, VDD, VDDQ = 1.8V ± 0.1V)

(DDR2 SDRAM Component Specification)

Parameter	min.	typ.	max.	Unit	Notes
Output impedance	12.6	18	23.4	Ω	1, 5
Pull-up and pull-down mismatch	0	—	4	Ω	1, 2
Output slew rate	1.5	—	5	V/ns	3, 4

Notes: 1. Impedance measurement condition for output source DC current: VDDQ = 1.7V; VOUT = 1420mV; (VOUT–VDDQ)/IOH must be less than 23.4Ω for values of VOUT between VDDQ and VDDQ–280mV. Impedance measurement condition for output sink DC current: VDDQ = 1.7V; VOUT = 280mV; VOUT/IOL must be less than 23.4Ω for values of VOUT between 0V and 280mV.

2. Mismatch is absolute value between pull up and pull down, both are measured at same temperature and voltage.
3. Slew rate measured from VIL(AC) to VIH(AC).
4. The absolute value of the slew rate as measured from DC to DC is equal to or greater than the slew rate as measured from AC to AC. This is guaranteed by design and characterization.
5. DRAM I/O specifications for timing, voltage, and slew rate are no longer applicable if OCD is changed from default settings.

Pin Capacitance (TA = 25°C, VDD = 1.8V ± 0.1V)

Parameter	Symbol	Pins	min.	max.	Unit	Notes
Input capacitance	CI1	Address, /RAS, /CAS, /WE, /CS, CKE, ODT	2.0	3.5	pF	1
Input capacitance	CI2	CK, /CK	2.0	3.0	pF	2
Input/output pin capacitance	CI/O	DQ, DQS, /DQS, UDQS, /UDQS, LDQS, /LDQS, RDQS, /RDQS, DM, UDM, LDM, CB				
-6E			2.5	3.5	pF	3
-5C			2.5	4.0		

Notes: 1. Register component specification.
2. PLL component specification.
3. DDR2 SDRAM component specification.

AC Characteristics (TC = 0°C to +85°C, VDD, VDDQ = 1.8V ± 0.1V, VSS, VSSQ = 0V) [DDR2-667]

(DDR2 SDRAM Component Specification)

- New units tCK(avg) and nCK, are introduced in DDR2-800 and DDR2-667
  tCK(avg): actual tCK(avg) of the input clock under operation.
  nCK: one clock cycle of the input clock, counting the actual clock edges.

		-6E			
Speed bin		DDR2-667 (5-5-5)			
Parameter	Symbol	min.	max.	Unit	Notes
Active to read or write command delay	tRCD	15	—	ns	
Precharge command period	tRP	15	—	ns	
Active to active/auto-refresh command time	tRC	60	—	ns	
DQ output access time from CK, /CK	tAC	–450	+450	ps	10
DQS output access time from CK, /CK	tDQSCK	–400	+400	ps	10
CK high-level width	tCH (avg)	0.48	0.52	tCK (avg)	13
CK low-level width	tCL(avg)	0.48	0.52	tCK (avg)	13
CK half period	tHP	Min. (tCL(abs), tCH(abs))	—	ps	6, 13
Clock cycle time (CL = 6)	tCK (avg)	3000	8000	ps	13
(CL = 5)	tCK (avg)	3000	8000	ps	13
(CL = 4)	tCK (avg)	3750	8000	ps	13
(CL = 3)	tCK (avg)	5000	8000	ps	13
DQ and DM input hold time	tDH (base)	175	—	ps	5
DQ and DM input setup time	tDS (base)	100	—	ps	4
Control and Address input pulse width for each input	tIPW	0.6	—	tCK (avg)	
DQ and DM input pulse width for each input	tDIPW	0.35	—	tCK (avg)	
Data-out high-impedance time from CK,/CK	tHZ	—	tAC max.	ps	10
DQS, /DQS low-impedance time from CK,/CK	tLZ (DQS)	tAC min.	tAC max.	ps	10
DQ low-impedance time from CK,/CK	tLZ (DQ)	2 × tAC min	tAC max.	ps	10
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	—	240	ps	
DQ hold skew factor	tQHS	—	340	ps	7
DQ/DQS output hold time from DQS	tQH	tHP – tQHS	—	ps	8
DQS latching rising transitions to associated clock edges	tDQSS	–0.25	+0.25	tCK (avg)	
DQS input high pulse width	tDQSH	0.35	—	tCK (avg)	
DQS input low pulse width	tDQSL	0.35	—	tCK (avg)	
DQS falling edge to CK setup time	tDSS	0.2	—	tCK (avg)	
DQS falling edge hold time from CK	tDSH	0.2	—	tCK (avg)	
Mode register set command cycle time	tMRD	2	—	nCK	
Write postamble	tWPST	0.4	0.6	tCK (avg)	
Write preamble	tWPRE	0.35	—	tCK (avg)	
Address and control input hold time	tIH (base)	275	—	ps	5
Address and control input setup time	tIS (base)	200	—	ps	4
Read preamble	tRPRE	0.9	1.1	tCK (avg)	11
Read postamble	tRPST	0.4	0.6	tCK (avg)	12

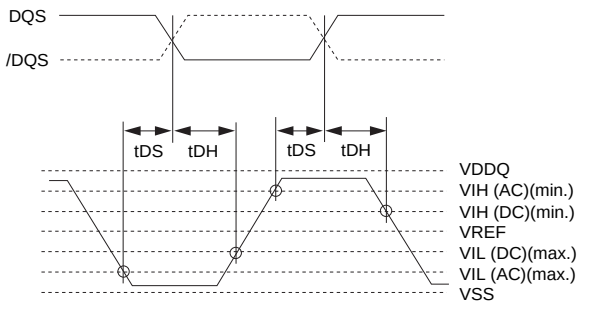
Speed bin		-6E DDR2-667 (5-5-5)			
Parameter	Symbol	min.	max.	Unit	Notes
Active to precharge command	tRAS	45	70000	ns	
Active to auto-precharge delay	tRAP	tRCD min.	—	ns	
Active bank A to active bank B command period	tRRD	7.5	—	ns	
Four active window period	tFAW	37.5	—	ns	
/CAS to /CAS command delay	tCCD	2	—	nCK	
Write recovery time	tWR	15	—	ns	
Auto precharge write recovery + precharge time	tDAL	WR + RU (tRP/ tCK (avg))	—	nCK	1, 9
Internal write to read command delay	tWTR	7.5	—	ns	14
Internal read to precharge command delay	tRTP	7.5	—	ns	
Exit self-refresh to a non-read command	tXSNR	tRFC + 10	—	ns	
Exit self-refresh to a read command	tXSRD	200	—	nCK	
Exit precharge power down to any non-read command	tXP	2	—	nCK	
Exit active power down to read command	tXARD	2	—	nCK	3
Exit active power down to read command (slow exit/low power mode)	tXARDS	7 – AL	—	nCK	2, 3
CKE minimum pulse width (high and low pulse width)	tCKE	3	—	nCK	
Output impedance test driver delay	tOIT	0	12	ns	
MRS command to ODT update delay	tMOD	0	12	ns	
Auto-refresh to active/auto-refresh command time	tRFC	127.5	—	ns	
Average periodic refresh interval (0°C ≤ TC ≤ +85°C)	tREFI	—	7.8	µs	
(+85°C < TC ≤ +95°C)	tREFI	—	3.9	µs	
Minimum time clocks remains ON after CKE asynchronously drops low	tDELAY	tIS + tCK(avg) + tIH	—	ns	

AC Characteristics [DDR2-533]

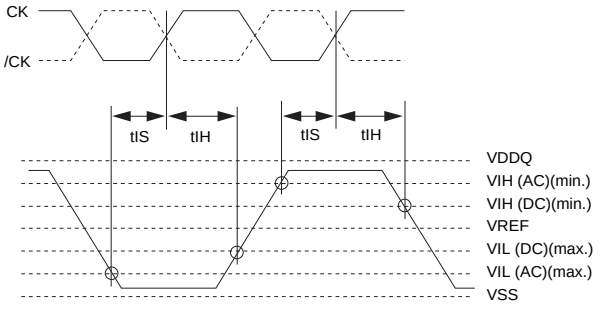
Speed bin		-5C DDR2-533 (4-4-4)			
Parameter	Symbol	min.	max.	Unit	Notes
Active to read or write command delay	tRCD	15	—	ns	
Precharge command period	tRP	15	—	ns	
Active to active/auto-refresh command time	tRC	60	—	ns	
DQ output access time from CK, /CK	tAC	–500	+500	ps	
DQS output access time from CK, /CK	tDQSCK	–450	+450	ps	
CK high-level width	tCH	0.45	0.55	tCK	
CK low-level width	tCL	0.45	0.55	tCK	
CK half period	tHP	Min. (tCL, tCH)	—	ps	
Clock cycle time (CL = 6)	tCK	3750	8000	ps	
(CL = 5)	tCK	3750	8000	ps	
(CL = 4)	tCK	3750	8000	ps	
(CL = 3)	tCK	5000	8000	ps	
DQ and DM input hold time (differential strobe)	tDH (base)	225	—	ps	5
DQ and DM input hold time (single-ended strobe)	tDH1 (base)	–25	—	ps	
DQ and DM input setup time (differential strobe)	tDS (base)	100	—	ps	4
DQ and DM input setup time (single-ended strobe)	tDS1 (base)	–25	—	ps	
Control and Address input pulse width for each input	tIPW	0.6	—	tCK	
DQ and DM input pulse width for each input	tDIPW	0.35	—	tCK	
Data-out high-impedance time from CK,/CK	tHZ	—	tAC max.	ps	
Data-out low-impedance time from CK,/CK	tLZ	tAC min.	tAC max.	ps	
DQS-DQ skew for DQS and associated DQ signals	tDQSQ	—	300	ps	
DQ hold skew factor	tQHS	—	400	ps	
DQ/DQS output hold time from DQS	tQH	tHP – tQHS	—	ps	
DQS latching rising transitions to associated clock edges	tDQSS	–0.25	+0.25	tCK	
DQS input high pulse width	tDQSH	0.35	—	tCK	
DQS input low pulse width	tDQSL	0.35	—	tCK	
DQS falling edge to CK setup time	tDSS	0.2	—	tCK	
DQS falling edge hold time from CK	tDSH	0.2	—	tCK	
Mode register set command cycle time	tMRD	2	—	tCK	
Write postamble	tWPST	0.4	0.6	tCK	
Write preamble	tWPRE	0.35	—	tCK	
Address and control input hold time	tIH (base)	375	—	ps	5
Address and control input setup time	tIS (base)	250	—	ps	4
Read preamble	tRPRE	0.9	1.1	tCK	
Read postamble	tRPST	0.4	0.6	tCK	
Active to precharge command	tRAS	45	70000	ns	

Speed bin		-5C DDR2-533 (4-4-4)			
Parameter	Symbol	min.	max.	Unit	Notes
Active to auto-precharge delay	tRAP	tRCD min.	—	ns	
Active bank A to active bank B command period	tRRD	7.5	—	ns	
Four active window period	tFAW	37.5	—	ns	
/CAS to /CAS command delay	tCCD	2	—	tCK	
Write recovery time	tWR	15	—	ns	
Auto precharge write recovery + precharge time	tDAL	WR + RU(tRP/tCK)	—	tCK	1, 9
Internal write to read command delay	tWTR	7.5	—	ns	14
Internal read to precharge command delay	tRTP	7.5	—	ns	
Exit self-refresh to a non-read command	tXSNR	tRFC + 10	—	ns	
Exit self-refresh to a read command	tXSRD	200	—	tCK	
Exit precharge power-down to any non-read command	tXP	2	—	tCK	
Exit active power-down to read command	tXARD	2	—	tCK	3
Exit active power-down to read command (slow exit/low power mode)	tXARDS	6 – AL	—	tCK	2, 3
CKE minimum pulse width (high and low pulse width)	tCKE	3	—	tCK	
Output impedance test driver delay	tOIT	0	12	ns	
MRS command to ODT update delay	tMOD	0	12	ns	
Auto-refresh to active/auto-refresh command time	tRFC	127.5	—	ns	
Average periodic refresh interval (0°C ≤ TC ≤ +85°C)	tREFI	—	7.8	µs	
(+85°C < TC ≤ +95°C)	tREFI	—	3.9	µs	
Minimum time clocks remains ON after CKE asynchronously drops low	tDELAY	tIS + tCK + tIH	—	ns	

Notes: 1. For each of the terms above, if not already an integer, round to the next higher integer.
2. AL: Additive Latency.
3. MRS A12 bit defines which active power down exit timing to be applied.
4. The figures of Input Waveform Timing 1 and 2 are referenced from the input signal crossing at the VIH(AC) level for a rising signal and VIL(AC) for a falling signal applied to the device under test.
5. The figures of Input Waveform Timing 1 and 2 are referenced from the input signal crossing at the VIL(DC) level for a rising signal and VIH(DC) for a falling signal applied to the device under test.



Input Waveform Timing 1 (tDS, tDH)



Input Waveform Timing 2 (tIS, tIH)

6. tHP is the minimum of the absolute half period of the actual input clock. tHP is an input parameter but not an input specification parameter. It is used in conjunction with tQHS to derive the DRAM output timing tQH.

   The value to be used for tQH calculation is determined by the following equation;

   tHP = min (tCH(abs), tCL(abs)),

   where,

   tCH(abs) is the minimum of the actual instantaneous clock high time;

   tCL(abs) is the minimum of the actual instantaneous clock low time;

7. tQHS accounts for:

   a. The pulse duration distortion of on-chip clock circuits, which represents how well the actual tHP at the input is transferred to the output; and

   b. The worst case push-out of DQS on one transition followed by the worst case pull-in of DQ on the next transition, both of which are independent of each other, due to data pin skew, output pattern effects, and p-channel to n-channel variation of the output drivers.

8. tQH = tHP – tQHS, where:

   tHP is the minimum of the absolute half period of the actual input clock; and tQHS is the specification value under the max column.

   {The less half-pulse width distortion present, the larger the tQH value is; and the larger the valid data eye will be.}

   Examples:

   a. If the system provides tHP of 1315ps into a DDR2-667 SDRAM, the DRAM provides tQH of 975ps (min.)

   b. If the system provides tHP of 1420ps into a DDR2-667 SDRAM, the DRAM provides tQH of 1080ps (min.)

9. RU stands for round up. WR refers to the tWR parameter stored in the MRS.

10. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.)

    For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per) min. = –272ps and tERR(6-10per) max. = +293ps, then tDQSCK min.(derated) = tDQSCK min. – tERR(6-10per) max. = –400ps – 293ps = –693ps and tDQSCK max.(derated) = tDQSCK max. – tERR(6-10per) min. = 400ps + 272ps = +672ps. Similarly, tLZ(DQ) for DDR2-667 derates to tLZ(DQ) min.(derated) = –900ps – 293ps = –1193ps and tLZ(DQ) max.(derated)= 450ps + 272ps = +722ps.

11. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(per) of the input clock. (output deratings are relative to the SDRAM input clock.)

    For example, if the measured jitter into a DDR2-667 SDRAM has tJIT(per) min. = –72ps and tJIT(per) max. = +93ps, then tRPRE min.(derated) = tRPRE min. + tJIT(per) min. = 0.9 × tCK(avg) – 72ps = +2178ps and tRPRE max.(derated) = tRPRE max. + tJIT(per) max. = 1.1 × tCK(avg) + 93ps = +2843ps.

12. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tJIT(duty) of the input clock. (output deratings are relative to the SDRAM input clock.)

    For example, if the measured jitter into a DDR2-667 SDRAM has tJIT(duty) min. = –72ps and tJIT(duty) max. = +93ps, then tRPST min.(derated) = tRPST min. + tJIT(duty) min. = 0.4 × tCK(avg) – 72ps = +928ps and tRPST max.(derated) = tRPST max. + tJIT(duty) max. = 0.6 × tCK(avg) + 93ps = +1592ps.

13. Refer to the Clock Jitter table.

14. tWTR is at least two clocks (2 × tCK or 2 × nCK) independent of operation frequency.

ODT AC Electrical Characteristics (DDR2 SDRAM Component Specification)

Parameter	Symbol	min.	max.	Unit	Notes
ODT turn-on delay	tAOND	2	2	tCK	
ODT turn-on -6E	tAON	tAC(min)	tAC(max) + 700	ps	1, 3
-5C	tAON	tAC(min)	tAC(max) + 1000	ps	1
ODT turn-on (power down mode)	tAONPD	tAC(min) + 2000	2tCK + tAC(max) + 1000	ps	
ODT turn-off delay	tAOFD	2.5	2.5	tCK	5, 6
ODT turn-off	tAOF	tAC(min)	tAC(max) + 600	ps	2, 4, 5, 6
ODT turn-off (power down mode)	tAOFPD	tAC(min) + 2000	2.5tCK + tAC(max) + 1000	ps	
ODT to power down entry latency	tANPD	3	3	tCK	
ODT power down exit latency	tAXPD	8	8	tCK	

Notes: 1. ODT turn on time min is when the device leaves high impedance and ODT resistance begins to turn on.
ODT turn on time max is when the ODT resistance is fully on. Both are measured from tAOND.

2. ODT turn off time min is when the device starts to turn off ODT resistance.
ODT turn off time max is when the bus is in high impedance. Both are measured from tAOFD.

3. When the device is operated with input clock jitter, this parameter needs to be derated by the actual tERR(6-10per) of the input clock. (output deratings are relative to the SDRAM input clock.)

4. When the device is operated with input clock jitter, this parameter needs to be derated by {–tJIT(duty) max. – tERR(6-10per) max. } and { –tJIT(duty) min. – tERR(6-10per) min. } of the actual input clock.(output deratings are relative to the SDRAM input clock.)
For example, if the measured jitter into a DDR2-667 SDRAM has tERR(6-10per) min. = –272ps, tERR(6-10per) max. = +293ps, tJIT(duty) min. = –106ps and tJIT(duty) max. = +94ps, then tAOF min.(derated) = tAOF min. + { –tJIT(duty) max. – tERR(6-10per) max. } = –450ps + { –94ps – 293ps} = –837ps and tAOF max.(derated) = tAOF max. + { –tJIT(duty) min. – tERR(6-10per) min. } = 1050ps + { 106ps + 272ps} = +1428ps.

5. For tAOFD of DDR2-533, the 1/2 clock of tCK in the 2.5 × tCK assumes a tCH, input clock high pulse width of 0.5 relative to tCK. tAOF min. and tAOF max. should each be derated by the same amount as the actual amount of tCH offset present at the DRAM input with respect to 0.5. For example, if an input clock has a worst case tCH of 0.45, the tAOF min. should be derated by subtracting 0.05 × tCK from it, whereas if an input clock has a worst case tCH of 0.55, the tAOF max. should be derated by adding 0.05 × tCK to it. Therefore, we have;

tAOF min.(derated) = tAC min. – [0.5 – Min.(0.5, tCH min.)] × tCK

tAOF max.(derated) = tAC max. + 0.6 + [Max.(0.5, tCH max.) – 0.5] × tCK

or

tAOF min.(derated) = Min.(tAC min., tAC min. – [0.5 – tCH min.] × tCK)

tAOF max.(derated) = 0.6 + Max.(tAC max., tAC max. + [tCH max. – 0.5] × tCK)

where tCH min. and tCH max. are the minimum and maximum of tCH actually measured at the DRAM input balls.

6. For tAOFD of DDR2-667, the 1/2 clock of nCK in the 2.5 × nCK assumes a tCH(avg), average input clock high pulse width of 0.5 relative to tCK(avg). tAOF min. and tAOF max. should each be derated by the same amount as the actual amount of tCH(avg) offset present at the DRAM input with respect to 0.5. For example, if an input clock has a worst case tCH(avg) of 0.48, the tAOF min. should be derated by subtracting 0.02 × tCK(avg) from it, whereas if an input clock has a worst case tCH(avg) of 0.52, the tAOF max. should be derated by adding 0.02 × tCK(avg) to it. Therefore, we have;

tAOF min.(derated) = tAC min. – [0.5 – Min.(0.5, tCH(avg) min.)] × tCK(avg)

tAOF max.(derated) = tAC max. + 0.6 + [Max.(0.5, tCH(avg) max.) – 0.5] × tCK(avg)

or

tAOF min.(derated) = Min.(tAC min., tAC min. – [0.5 – tCH(avg) min.] × tCK(avg))

tAOF max.(derated) = 0.6 + Max.(tAC max., tAC max. + [tCH(avg) max. – 0.5] × tCK(avg))

where tCH(avg) min. and tCH(avg) max. are the minimum and maximum of tCH(avg) actually measured at the DRAM input balls.

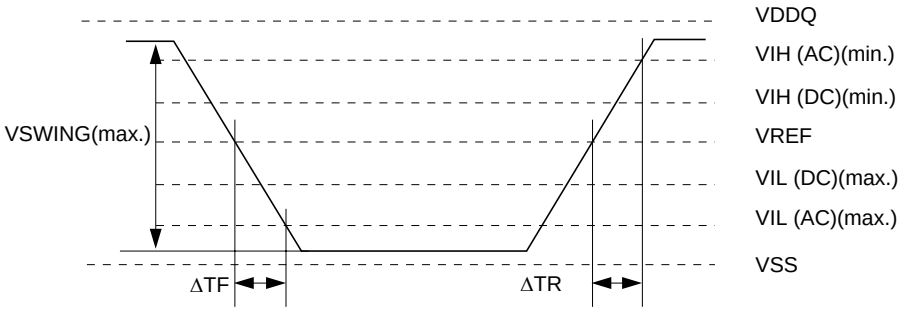
AC Input Test Conditions (DDR2 SDRAM Component Specification)

Parameter	Symbol	Value	Unit	Notes
Input reference voltage	VREF	0.5 × VDDQ	V	1
Input signal maximum peak to peak swing	VSWING(max.)	1.0	V	1
Input signal minimum slew rate	SLEW	1.0	V/ns	2, 3

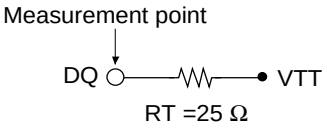
Notes: 1. Input waveform timing is referenced to the input signal crossing through the VIH/IL (AC) level applied to the device under test.

2. The input signal minimum slew rate is to be maintained over the range from VREF to VIH(AC) (min.) for rising edges and the range from VREF to VIL(AC) (max.) for falling edges as shown in the below figure.

3. AC timings are referenced with input waveforms switching from VIL(AC) to VIH(AC) on the positive transitions and VIH(AC) to VIL(AC) on the negative transitions.



AC Input Test Signal Wave forms



Output Load

Clock Jitter [DDR2-667]

		-6E			
Frequency (Mbps)		667			
Parameter	Symbol	min.	max.	Unit	Notes
Average clock period	tCK (avg)	3000	8000	ps	1
Clock period jitter	tJIT (per)	–125	125	ps	5
Clock period jitter during DLL locking period	tJIT (per, lck)	–100	100	ps	5
Cycle to cycle period jitter	tJIT (cc)	—	250	ps	6
Cycle to cycle clock period jitter during DLL locking period	tJIT (cc, lck)	—	200	ps	6
Cumulative error across 2 cycles	tERR (2per)	–175	175	ps	7
Cumulative error across 3 cycles	tERR (3per)	–225	225	ps	7
Cumulative error across 4 cycles	tERR (4per)	–250	250	ps	7
Cumulative error across 5 cycles	tERR (5per)	–250	250	ps	7
Cumulative error across n=6,7,8,9,10 cycles	tERR (6-10per)	–350	350	ps	7
Cumulative error across n=11, 12,…49,50 cycles	tERR (11-50per)	–450	450	ps	7
Average high pulse width	tCH (avg)	0.48	0.52	tCK (avg)	2
Average low pulse width	tCL (avg)	0.48	0.52	tCK (avg)	3
Duty cycle jitter	tJIT (duty)	–125	125	ps	4

Notes: 1. tCK (avg) is calculated as the average clock period across any consecutive 200cycle window.

$$tCK(avg) = \left\{\sum_{j=1}^{N} tCKj\right\} \Big/ N$$

N = 200

2. tCH (avg) is defined as the average high pulse width, as calculated across any consecutive 200 high pulses.

$$tCH(avg) = \left\{\sum_{j=1}^{N} tCHj\right\} \Big/ (N \times tCK(avg))$$

N = 200

3. tCL (avg) is defined as the average low pulse width, as calculated across any consecutive 200 low pulses.

$$tCL(avg) = \left\{\sum_{j=1}^{N} tCLj\right\} \Big/ (N \times tCK(avg))$$

N = 200

4. tJIT (duty) is defined as the cumulative set of tCH jitter and tCL jitter. tCH jitter is the largest deviation of any single tCH from tCH (avg). tCL jitter is the largest deviation of any single tCL from tCL (avg). tJIT (duty) is not subject to production test.

   tJIT (duty) = Min./Max. of {tJIT (CH), tJIT (CL)}, where:

   tJIT (CH) = {tCH_j- tCH (avg) where j = 1 to 200}

   tJIT (CL) = {tCL_j – tCL (avg) where j = 1 to 200}

5. tJIT (per) is defined as the largest deviation of any single tCK from tCK (avg).

   tJIT (per) = Min./Max. of { tCK_j – tCK (avg) where j = 1 to 200}

   tJIT (per) defines the single period jitter when the DLL is already locked. tJIT (per, lck) uses the same definition for single period jitter, during the DLL locking period only. tJIT (per) and tJIT (per, lck) are not subject to production test.

6. tJIT (cc) is defined as the absolute difference in clock period between two consecutive clock cycles:
   tJIT (cc) = Max. of $|tCK_{j+1} - tCK_j|$
   tJIT (cc) is defines the cycle to cycle jitter when the DLL is already locked. tJIT (cc, lck) uses the same definition for cycle to cycle jitter, during the DLL locking period only. tJIT (cc) and tJIT (cc, lck) are not subject to production test.
7. tERR (nper) is defined as the cumulative error across multiple consecutive cycles from tCK (avg).
   tERR (nper) is not subject to production test.

$$tERR(nper) = \left\{ \sum_{j=1}^{n} tCKj \right\} - n \times tCK(avg))$$

$2 \leq n \leq 50$ for tERR (nper)

8. These parameters are specified per their average values, however it is understood that the following relationship between the average timing and the absolute instantaneous timing hold at all times.
   (minimum and maximum of spec values are to be used for calculations in the table below.)

Parameter	Symbol	min.	max.	Unit
Absolute clock period	tCK (abs)	tCK (avg) min. + tJIT (per) min.	tCK (avg) max. + tJIT (per) max.	ps
Absolute clock high pulse width	tCH (abs)	tCH (avg) min. × tCK (avg) min. + tJIT (duty) min.	tCH (avg) max. × tCK (avg) max. + tJIT (duty) max.	ps
Absolute clock low pulse width	tCL (abs)	tCL (avg) min. × tCK (avg) min. + tJIT (duty) min.	tCL (avg) max. × tCK (avg) max. + tJIT (duty) max.	ps

Example: For DDR2-667, tCH(abs) min. = (0.48 × 3000 ps) - 125ps = 1315ps

Pin Functions

CK, /CK (input pin)

The CK and the /CK are the master clock inputs. All inputs except DMs, DQSs and DQs are referred to the cross point of the CK rising edge and the VREF level. When a read operation, DQSs and DQs are referred to the cross point of the CK and the /CK. When a write operation, DQs are referred to the cross point of the DQS and the VREF level. DQSs for write operation are referred to the cross point of the CK and the /CK.

/CS (input pin)

When /CS is low, commands and data can be input. When /CS is high, all inputs are ignored. However, internal operations (bank active, burst operations, etc.) are held.

/RAS, /CAS, and /WE (input pins)

These pins define operating commands (read, write, etc.) depending on the combinations of their voltage levels. See “Command operation”.

A0 to A13 (input pins)

Row address (AX0 to AX13) is determined by the A0 to the A13 level at the cross point of the CK rising edge and the VREF level in a bank active command cycle. Column address (AY0 to AY9, AY11) is loaded via the A0 to the A9 and A11 at the cross point of the CK rising edge and the VREF level in a read or a write command cycle. This column address becomes the starting address of a burst operation.

A10 (AP) (input pin)

A10 defines the precharge mode when a precharge command, a read command or a write command is issued. If A10 = high when a precharge command is issued, all banks are precharged. If A10 = low when a precharge command is issued, only the bank that is selected by BA1, BA0 is precharged. If A10 = high when read or write command, auto-precharge function is enabled. While A10 = low, auto-precharge function is disabled.

BA0, BA1, BA2 (input pin)

BA0, BA1 and BA2 are bank select signals (BA). The memory array is divided into 8 banks: bank 0 to bank 7. (See Bank Select Signal Table)

[Bank Select Signal Table]

	BA0	BA1	BA2
Bank 0	L	L	L
Bank 1	H	L	L
Bank 2	L	H	L
Bank 3	H	H	L
Bank 4	L	L	H
Bank 5	H	L	H
Bank 6	L	H	H
Bank 7	H	H	H

Remark: H: VIH. L: VIL.

CKE (input pin)

CKE controls power down and self-refresh. The power down and the self-refresh commands are entered when the CKE is driven low and exited when it resumes to high.

The CKE level must be kept for 1 CK cycle at least, that is, if CKE changes at the cross point of the CK rising edge and the VREF level with proper setup time tIS, at the next CK rising edge CKE level must be kept with proper hold time tIH.

DQ, CB (input and output pins)

Data are input to and output from these pins.

DQS (input and output pin)

DQS and /DQS provide the read data strobes (as output) and the write data strobes (as input).

VDD (power supply pins)

1.8V is applied. (VDD is for the internal circuit.)

VDDSPD (power supply pin)

1.8V is applied (For serial EEPROM).

VSS (power supply pin)

Ground is connected.

/RESET(input pin)

LVCMOS reset input. When /RESET is Low, all registers are reset.

Par_IN (Parity input pin)

Parity bit for the address and control bus.

/Err_Out (Error output pin)

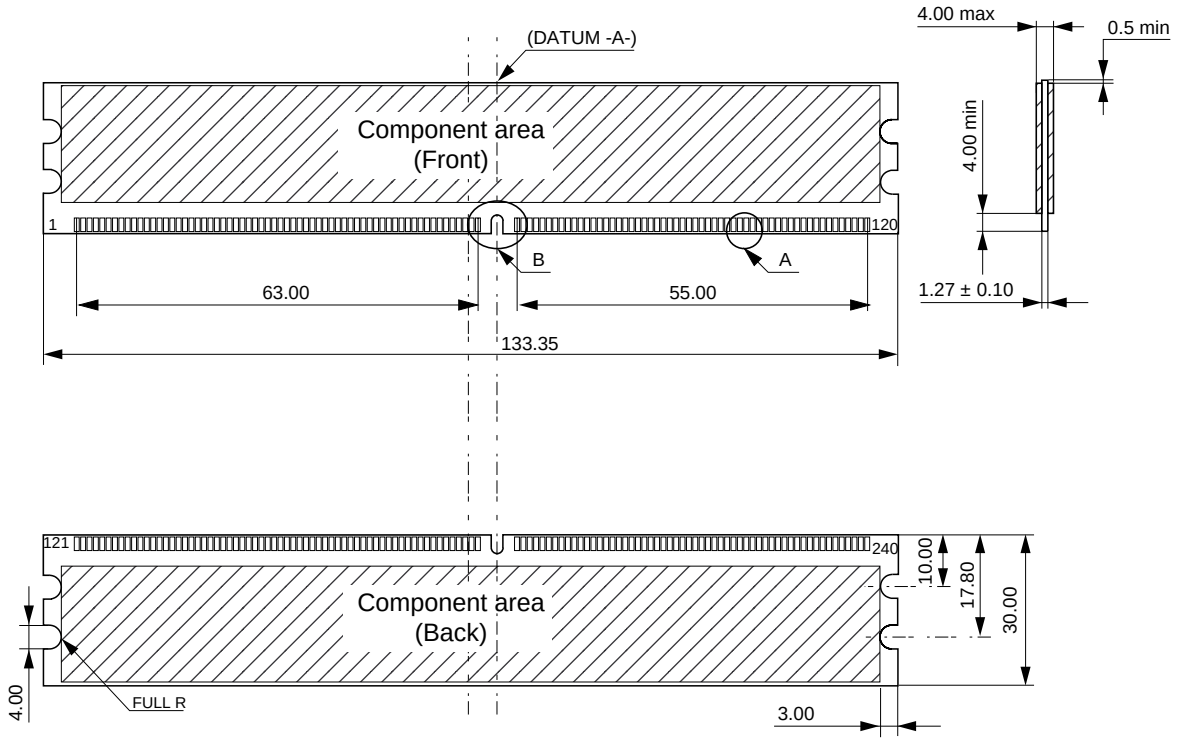
Parity error found on the address and control bus.

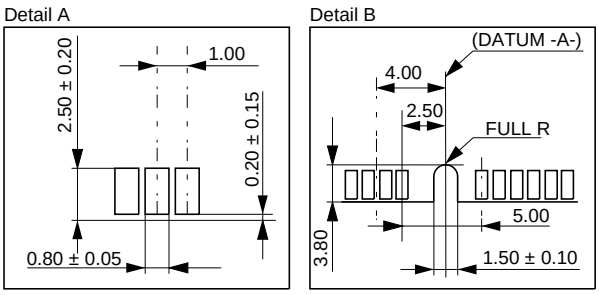
Detailed Operation Part and Timing Waveforms

Refer to the EDE1104ACSE, EDE1108ACSE, EDE1116ACSE datasheet (E0975E). DM pins of component device fixed to VSS level on the module board. DIMM /CAS latency = component CL + 1 for registered type.

Physical Outline

Unit: mm





ECA-TS2-0093-01

CAUTION FOR HANDLING MEMORY MODULES

When handling or inserting memory modules, be sure not to touch any components on the modules, such as the memory ICs, chip capacitors and chip resistors. It is necessary to avoid undue mechanical stress on these components to prevent damaging them.
In particular, do not push module cover or drop the modules in order to protect from mechanical defects, which would be electrical defects.

When re-packing memory modules, be sure the modules are not touching each other.
Modules in contact with other modules may cause excessive mechanical stress, which may damage the modules.

MDE0202

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR MOS DEVICES

Exposing the MOS devices to a strong electric field can cause destruction of the gate oxide and ultimately degrade the MOS devices operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it, when once it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. MOS devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. MOS devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor MOS devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS DEVICES

No connection for CMOS devices input pins can be a cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. The unused pins must be handled in accordance with the related specifications.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Power-on does not necessarily define initial status of MOS devices. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the MOS devices with reset function have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. MOS devices are not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for MOS devices having reset function.

CME0107

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2) Usage in exposure to direct sunlight or the outdoors, or in dusty places.
3) Usage involving exposure to significant amounts of corrosive gas, including sea air, CL_2, H_2S, NH_3, SO_2, and NO_X.
4) Usage in environments with static electricity, or strong electromagnetic waves or radiation.
5) Usage in places where dew forms.
6) Usage in environments with mechanical vibration, impact, or stress.
7) Usage near heating elements, igniters, or flammable items.

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