wavefront SEMICONDUCTOR

AL1101
24-Bit Analog-to-Digital Converter

ClockEZ™ ADC Converter AL1101

General Description

The AL1101 is a 24-bit sigma-delta stereo analog-to-digital audio converter using Wavefront's ClockEZ™ technology. With dynamic range of 107dB, simplified interface, and low power consumption, the AL1101 (and its companion AL1201 DAC) is a best-in-class solution for 44.1kHz and 48kHz operation.

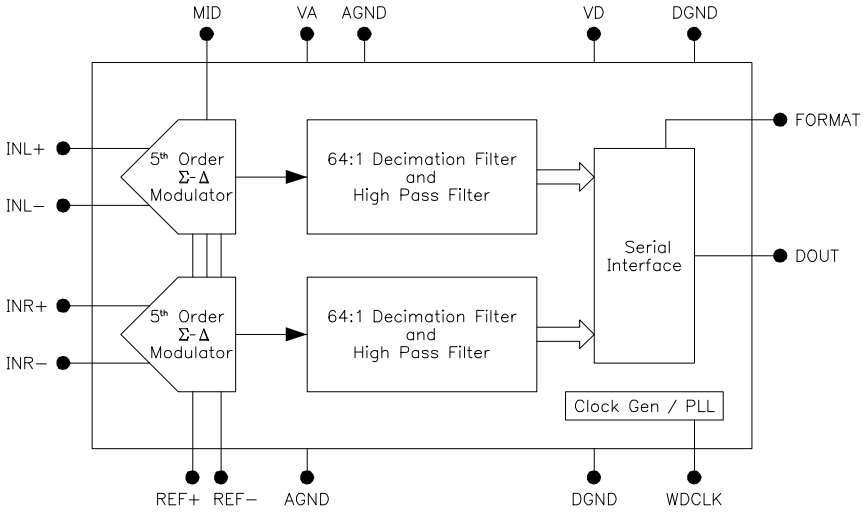
Applications

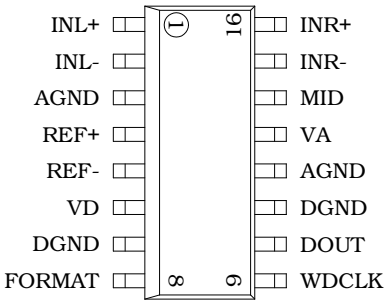
- Digital Mixing Boards
- Signal Processors
- Digital Effects Boxes
- Digital Recorders
- Computer Sound Boards
- Karaoke Systems
- Car Audio Systems

Features

- 24-bit conversion
- 107dB dynamic range (A-wt)
- 0.002% THD (input = -1dBFS)
- ClockEZ™ circuitry: internal PLL derives all necessary timing signals from one external Fs clock
- 64X oversampling, 5th order 1-bit Σ-Δ modulator
- 64:1 linear-phase digital decimation filter
- Sample rate: 24kHz to 55kHz
- Digital high-pass filter
- Low power: 110mW (Fs = 48kHz)
- Serial output selectable: 32/24 bits/frame
- Full scale differential input = ±4V
- 5V operation

Architecture Block diagram and Package





16 pin SOIC
150 mils wide

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Pin Descriptions

Pin#	Name	Pin Type	Description
1	INL+	In	Positive analog input, left channel.
2	INL-	In	Negative analog input, left channel.
3	AGND	Ground	Analog ground.
4	REF+	Power	Positive reference, connect to V_{DD} thru 1kΩ resistor, connect 0.1µF bypass capacitor to REF-.
5	REF-	Ground	Negative reference, connect to GND
6	VD	Power	Digital supply, connect 0.1µF bypass capacitor to GND.
7	DGND	Ground	Digital ground
8	FORMAT	In	Format select: 0=32 bits/frame, 1=24bits/frame.
9	WDCLK	In	Sample frequency wordclock, 24kHz<Fs<55kHz.
10	DOUT	Out	Serial data output.
11	DGND	Ground	Digital ground.
12	AGND	Ground	Analog ground.
13	VA	Power	Analog supply, connect 0.1µF bypass capacitor to GND.
14	MID	I/O	Mid reference, connect 0.1µF bypass capacitor to GND.
15	INR-	In	Negative analog input, right channel.
16	INR+	In	Positive analog input, right channel.

Electrical Characteristics

Parameter	Description/Condition	Min	Typ	Max	Units
Recommended Operating Conditions					
VA	Analog supply voltage	4.5	5.0	5.5	V
VD	Digital supply voltage	4.5	5.0	5.5	V
IA	Analog supply current		16		mA
ID	Digital supply current		6		mA
AGND	Analog ground	-	0.0	-	V
DGND	Digital ground	-	0.0	-	V
Fs	Sample rate	24	48	50	kHz
Temp	Temperature	0	25	70	°C
C_{LOAD}	DOUT load capacitance			30	pF
Analog Characteristics [1]					
Dynamic Range	Input = -60dBFS (A-weighted)		107		dB
THD+N	Input = -1dBFS -20dBFS -60dBFS		-95 -84 -44		dB
Crosstalk	Input = -1dBFS		-130		dB
Input Voltage	[IN+]-[IN-] fullscale [2] Interchannel match Common mode DC bias	±4.0	 0.01 2.5	±4.2	V dB V
Input Impedance	Differential		160k		Ω
REF Current	I_{REF} [3]		130		µA
Power Consumption			110		mW
Gain Error				±0.34	%
CMRR	Common mode rejection ratio		75		dB
PSRR	Power supply rejection ratio		70		dB
Digital Filter Characteristics [4]					
Passband	-3dB bandwidth [5,6] Ripple (20Hz – 21.77kHz)	2.5		21.77k ±0.025	Hz dB
Stopband	Frequency [5] Attenuation	26.23k -76			Hz dB
Group Delay			37.9		1/Fs
Group Delay Distortion			0		µs
Highpass Filter	Fc [5] -0.1dB frequency		2.5 16.4		Hz Hz
Digital Inputs (WDCLK, FORMAT)					
V_{IH}	Logical "1" input voltage	0.55VD			V
V_{IL}	Logical "0" input voltage			0.1VD	V
I_{IN}	Input leakage current			1	µA
C_{IN}	Input capacitance		5		pF
Output (DOUT)					
V_{OH}	Logical "1" output voltage	0.9VD			V
V_{OL}	Logical "0" output voltage			0.1VD	V
I_{OH}	Logical "1" output current		-0.5		mA
I_{OL}	Logical "0" output current		0.5		mA

Note 1: Temp = 25°C, VA = VD = REF+ = 5V, Fs = 48kHz, F_{INPUT} = 1kHz, Bandwidth = 20Hz-20kHz.

Note 2: Full scale input scales linearly with REF potential ([REF+]-[REF-]).

Note 3: REF current scales linearly with Fs.

Note 4: Temp = 25°C, VA = VD = REF+ = 5V, Fs = 48kHz, F_{INPUT} = 1kHz.

Note 5: Passband, stopband, and highpass frequencies scale with Fs.

Note 6: Passband is compensated for an external single-pole 80kHz lowpass filter at analog inputs (0.26dB at 20kHz). Compensation scales with Fs.

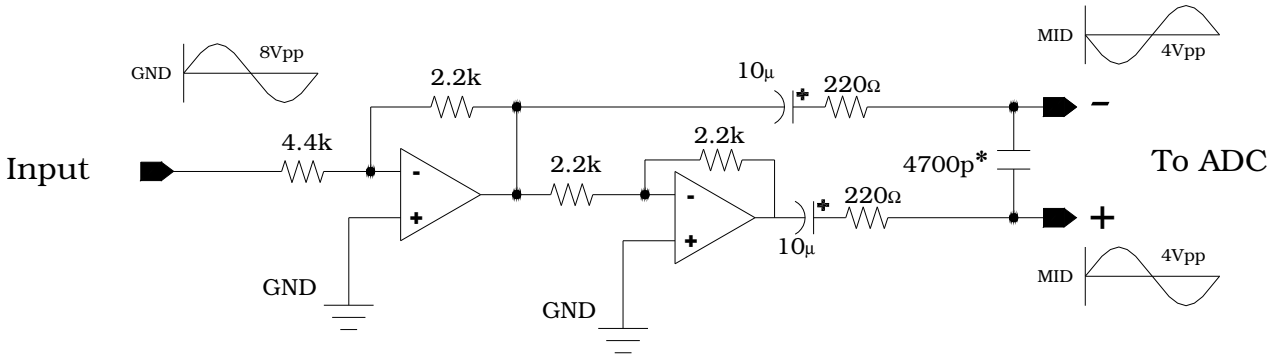
Architecture Details

Differential Analog Inputs

The AL1101 inputs are self-biased to MID potential. Input signals larger than maximum levels (±4V differential, or +0.5V to +4.5V at the pin) and smaller than supply voltages are output-limited to maximum positive and negative levels in the digital section (7FFFFFH and 800000H respectively).

The digital section of the AL1101 compensates for the passband amplitude deviation of an external single-pole 80kHz anti-alias filter (@ Fs=48k, scaling with Fs). To remove high-frequency noise at the differential inputs, the capacitor between the differential inputs should be located as close as possible to the input pins.

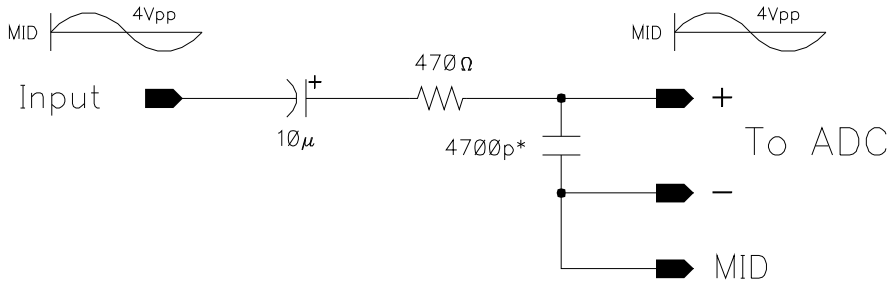
Single-Ended Input Conditioning Circuit



*Note: Position capacitor as close to pins as possible.
Film or high quality ceramic capacitor suggested.

If decreasing component count is an important factor, and a decrease in performance specifications is acceptable, the AL1101 inputs may be driven unbalanced with a simple passive component conditioning circuit. The lowpass filter has fc = 72kHz.

Unbalanced Input Conditioning Circuit



*Note: Position capacitor as close to pins as possible.
Film or high quality ceramic capacitor suggested.

The AL1101 can properly receive input logical "1" voltages of 0.55VD. This means the AL1101 can interface directly with logic signals supplied from 3.3V systems. No special interface circuitry is required.

Serial Output Interface

The AL1101 presents its two's complement serial output data in a standard MSB-first format. Two bitrates are provided: The 32-bits-per-frame rate (FORMAT low) is suitable for use in systems where 256*Fs master clocks are present. The 24-bits-per-frame rate (FORMAT high) is convenient when interfacing with circuits where 384*Fs master clocks are present.

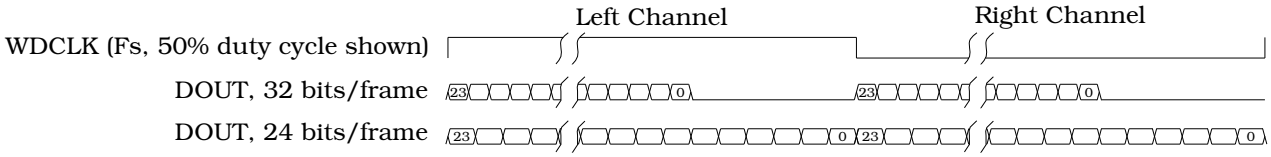
The output sample period is defined between rising edges of wordclock (WDCLK) input. Nominally, this is a 50% duty-cycle clock at frequency Fs, but it can be a pulse with

$$Ts/256 < \text{Pulse Width} < (255/256)*Ts; \quad Ts=1/Fs.$$

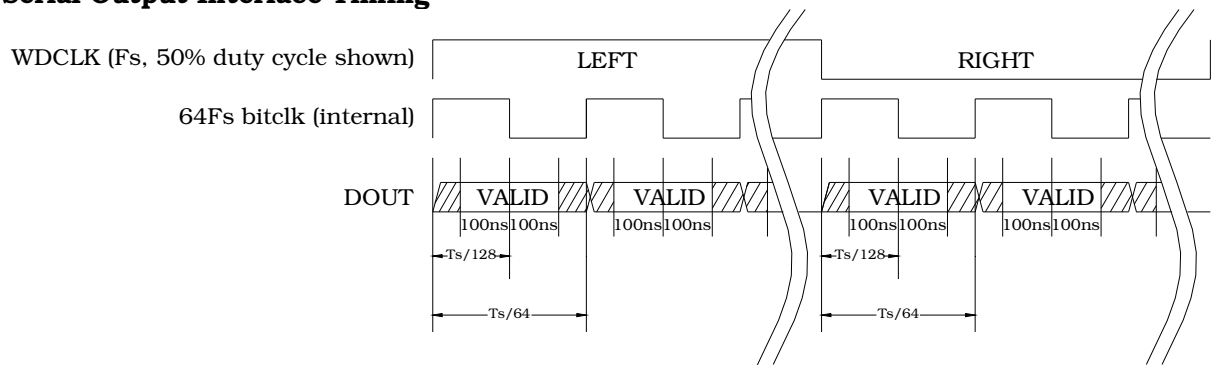
Left channel data output starts when WDCLK rises, and right channel data output starts Ts/2 seconds later (on falling edge of WDCLK if WDCLK has a 50% duty cycle).

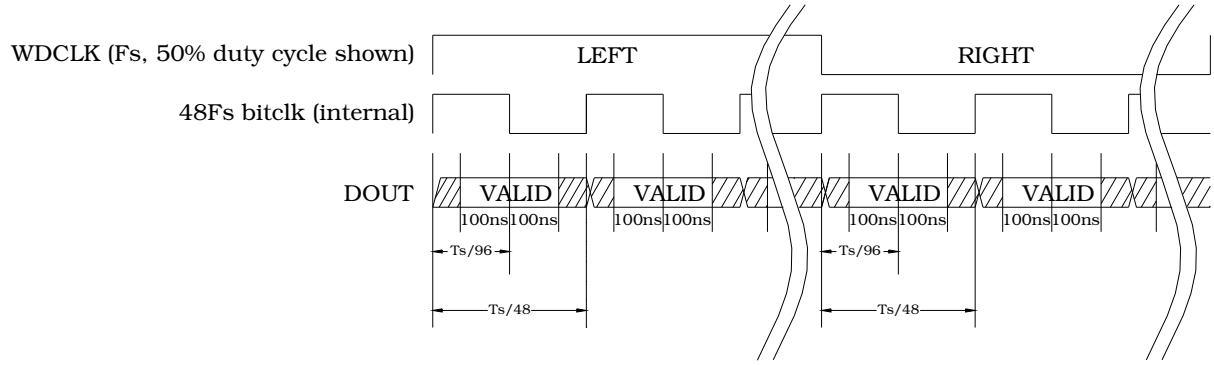
The serial bits are output on the rising edge of an internally generated bitclock (whose rising edge is aligned with rising edge of WDCLK) that runs at 64*Fs when FORMAT is low (32-bits-per-frame), or 48*Fs when FORMAT is high (24-bits-per-frame). The data is valid ±100ns from the center of these bit-frames.

Serial Output Interface Formats



Serial Output Interface Timing





Digital High Pass Output Filter

The AL1101 has an internal 2.5Hz single pole digital filter, which removes any offset present in the internal amplifiers and prevents DC codes from appearing at the data outputs. The response of the filter is -0.067dB at 20Hz.

Clock Generator and PLL

The AL1101 contains an internal PLL that locks to the rising edge of WDCLK and produces all necessary high frequency clocks and timing signals to operate the device. This high quality PLL will reject any high-frequency jitter on the incoming wordclock (jitter rejection corner at approximately 4kHz).

The PLL allows a simplified user interface and eliminates the need of running high frequency clocks to the part on PCB traces. This reduces unwanted RF noise and coupling problems that can occur when such clock signals are required on input pins for a device.

Reference and MID

The differential potential between the REF+ and REF- pins (connected to +5V and GND respectively) determines the amount of charge that is added to or removed from the modulator's first stage during each input sample period (64*Fs). It is very important that REF+ is well bypassed to REF- (0.1µF ceramic capacitor as close as possible to the pins) to remove the unwanted effects of high frequency noise.

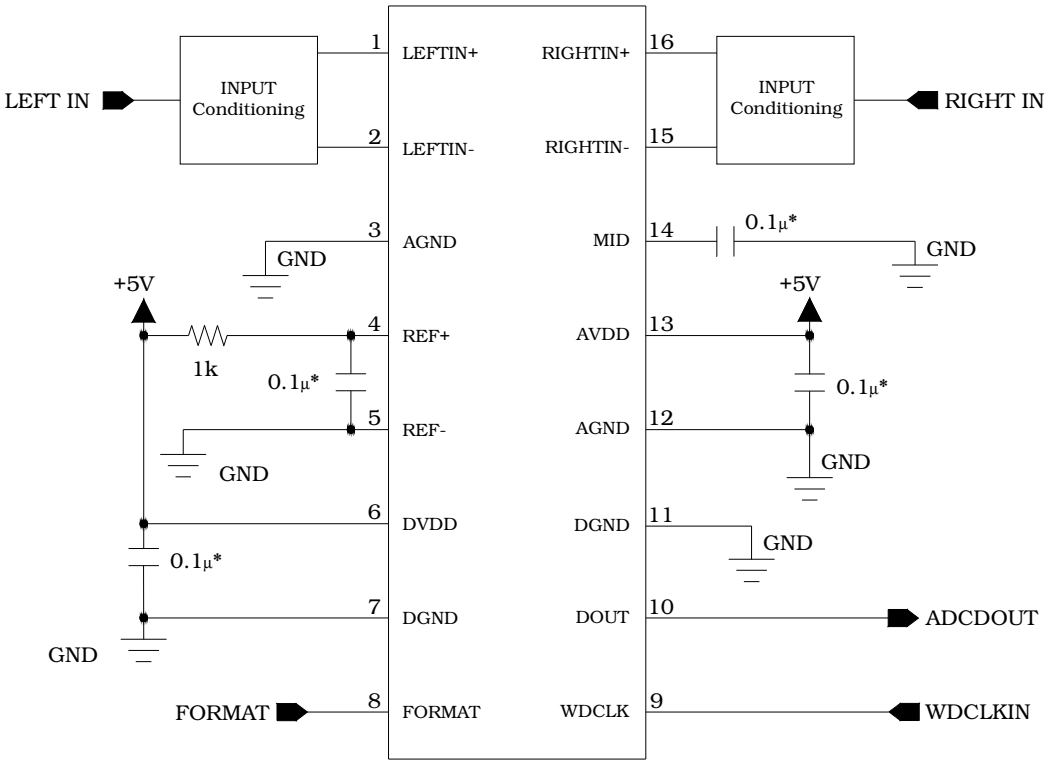
The MID potential is developed on-chip (VA/2 Volts) and is used to bias the internal amplifiers in the modulator, and to provide the reference point which determines the polarity of the modulator output. It requires a 0.1µF bypass capacitor to GND at the pin. No load current should be taken from the MID pin.

Power Supplies and Ground

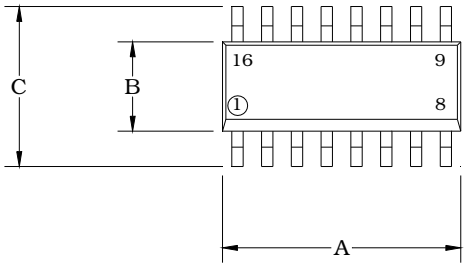
A single low-impedance +5V supply is all that is required to achieve the specified performance. A +5V supply plane on the PCB is recommended if possible. VA and VD may be directly connected to +5V, and REF+ should be isolated with a 1kΩ resistor to +5V.

A single low impedance ground plane can be used for all GND connections, simplifying PCB layout. Each supply pin should be bypassed to GND with a 0.1µF ceramic capacitor positioned as close to the pins as possible.

Suggested Connections

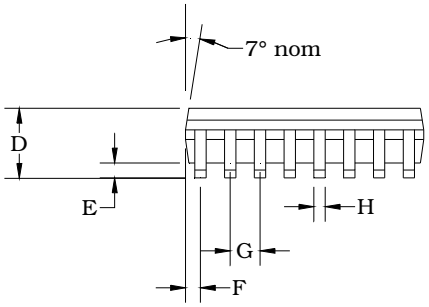


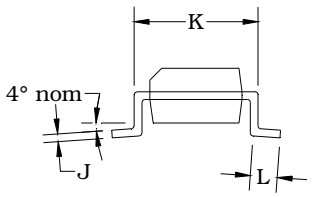
Package Dimensions



Dimensions (Typical)		
	Inches	Millimeters
A	0.389”	9.88
B	0.154”	3.91
C	0.236”	5.99
D	0.100”	2.50
E	0.008”	0.20
F	0.025”	0.64
G	0.050”	1.27
H	0.017”	0.42
J	0.011”	0.27
K	0.170”	4.32
L	0.033”	0.83

Note: Dimension “A” does not include mold flash, protrusions, or gate burrs.





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