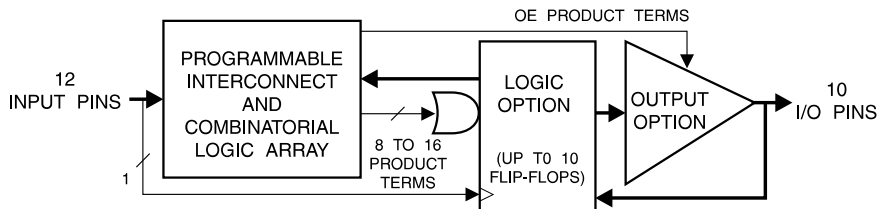


## Features

- Industry-standard Architecture
- 12 ns Maximum Pin-to-pin Delay
- Zero Power – 25  $\mu$ A Maximum Standby Power (Input Transition Detection)
- CMOS and TTL Compatible Inputs and Outputs
- Advanced Electrically-erasable Technology
  - Reprogrammable
  - 100% Tested
- Latch Feature Holds Inputs to Previous Logic State
- High-reliability CMOS Process
  - 20 Year Data Retention
  - 100 Erase/Write Cycles
  - 2,000V ESD Protection
  - 200 mA Latchup Immunity
- Commercial and Industrial Temperature Ranges
- Dual-in-line and Surface Mount Standard Pinouts
- PCI Compliant

## Block Diagram



## Description

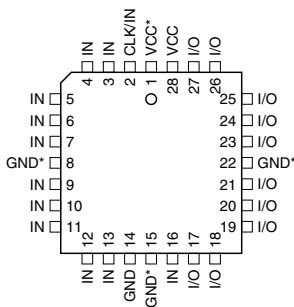
The ATF22V10CZ/CQZ is a high-performance CMOS (electrically-erasable) programmable logic device (PLD) which utilizes Atmel's proven electrically-erasable *(continued)*

## Pin Configurations

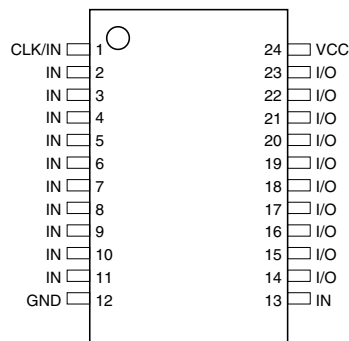
All Pinouts Top View

Pin Name	Function
CLK	Clock
IN	Logic Inputs
I/O	Bi-directional Buffers
VCC	+5V Supply

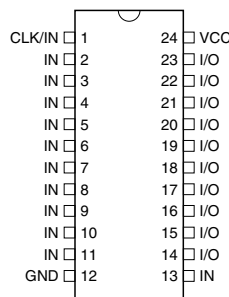
PLCC



TSSOP



DIP/SOIC



Note: For PLCC, P1, P8, P15 and P22 can be left unconnected. For superior performance, connect VCC to pin 1 and GND to 8, 15, and 22.



High-  
performance  
EE PLD

ATF22V10CZ  
ATF22V10CQZ





Flash memory technology. Speeds down to 12 ns with zero standby power dissipation are offered. All speed ranges are specified over the full 5V  $\pm$ 10% range for industrial temperature ranges; 5V  $\pm$ 5% for commercial range 5-volt devices. The ATF22V10CZ/CQZ provides a low voltage and edge-sensing “zero” power CMOS PLD solution with “zero” standby power (5  $\mu$ A typical). The ATF22V10CZ/CQZ provides a “zero” power CMOS PLD solution with 5V operating voltages, powering down automatically to the zero power-mode through Atmel’s patented Input Transition Detection (ITD) circuitry when the device is idle, offering “zero” (25  $\mu$ A worst case) standby power. This feature allows the user to manage total system power to

meet specific application requirements and enhance reliability. Pin “keeper” circuits on input and output pins eliminate static power consumed by pull-up resistors. The “CQZ” combines the low high-frequency  $I_{CC}$  of the “Q” design with the “Z” feature.

The ATF22V10CZ/CQZ incorporates a superset of the generic architectures, which allows direct replacement of the 22V10 family and most 24-pin combinatorial PLDs. Ten outputs are each allocated 8 to 16 product terms. Three different modes of operation, configured automatically with software, allow highly complex logic functions to be realized.

### Absolute Maximum Ratings\*

Temperature Under Bias.....	-40°C to +85°C
Storage Temperature.....	-65°C to +150°C
Voltage on Any Pin with Respect to Ground.....	-2.0V to +7.0V <sup>(1)</sup>
Voltage on Input Pins with Respect to Ground During Programming.....	-2.0V to +14.0V <sup>(1)</sup>
Programming Voltage with Respect to Ground.....	-2.0V to +14.0V <sup>(1)</sup>

\*NOTICE: Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note: 1. Minimum voltage is -0.6V DC, which may undershoot to -2.0V for pulses of less than 20 ns. Maximum output pin voltage is  $V_{CC} + 0.75V$  DC, which may overshoot to 7.0V for pulses of less than 20 ns.

### DC and AC Operating Conditions

	Commercial	Industrial
Operating Temperature (Ambient)	0°C - 70°C	-40°C - 85°C
$V_{CC}$ Power Supply	5V $\pm$ 5%	5V $\pm$ 10%

### Compiler Mode Selection

	PAL Mode (5828 Fuses)	GAL Mode (5892 Fuses)
Synario	ATF22V10C (DIP) ATF22V10C (PLCC)	ATF22V10C DIP (UES) ATF22V10C PLCC (UES)
WINCUPPL	P22V10 P22V10LCC	G22V10 G22V10LCC

## Functional Logic Diagram Description

The Functional Logic Diagram describes the ATF22V10CZ/CQZ architecture.

The ATF22V10CZ/CQZ has 12 inputs and 10 I/O macrocells. Each macrocell can be configured into one of four output configurations: active high/low, registered/combinatorial output. The universal architecture of the ATF22V10CZ/CQZ can be programmed to emulate most 24-pin PAL devices.

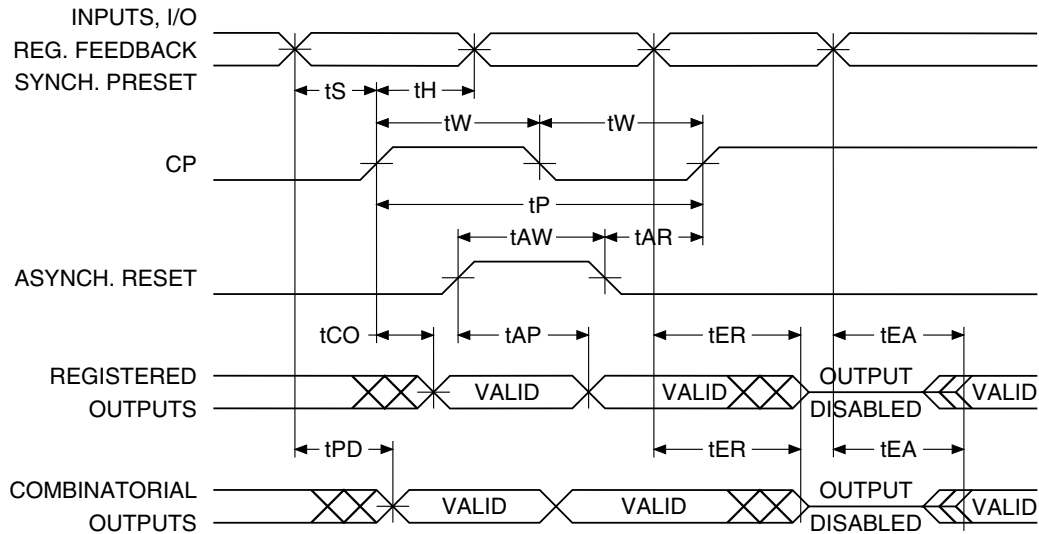
Unused product terms are automatically disabled by the compiler to decrease power consumption. A security fuse, when programmed, protects the contents of the ATF22V10CZ/CQZ. Eight bytes (64 fuses) of User Signature are accessible to the user for purposes such as storing project name, part number, revision or date. The User Signature is accessible regardless of the state of the security fuse.

## DC Characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units	
$I_{IL}$	Input or I/O Low Leakage Current	$0 \leq V_{IN} \leq V_{IL} (\text{Max})$ $3.5 \leq V_{IN} \leq V_{CC}$			-10	$\mu\text{A}$	
$I_{IH}$	Input or I/O High Leakage Current				10	$\mu\text{A}$	
$I_{CC}$	Clocked Power Supply Current	$V_{CC} = \text{Max}$ Outputs Open, $f = 15 \text{ MHz}$	CZ-12, 15	Com	90	150	mA
			CZ-15	Ind	90	180	mA
			CQZ-20	Com	40	60	mA
			CQZ-20	Ind	40	80	mA
$I_{SB}$	Power Supply Current, Standby	$V_{CC} = \text{Max}$ $V_{IN} = \text{MAX}$ Outputs Open	CZ-12, 15	Com	5	25	$\mu\text{A}$
			CZ-15	Ind	5	50	$\mu\text{A}$
			CQZ-20	Com	5	25	$\mu\text{A}$
			CQZ-20	Ind	5	50	$\mu\text{A}$
$I_{OS}^{(1)}$	Output Short Circuit Current	$V_{OUT} = 0.5\text{V}$			-130	mA	
$V_{IL}$	Input Low Voltage		-0.5		0.8	V	
$V_{IH}$	Input High Voltage		2.0		$V_{CC} + 0.75$	V	
$V_{OL}$	Output Low Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = \text{Min},$ $I_{OL} = 16 \text{ mA}$			0.5	V	
$V_{OH}$	Output High Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CCIO} = \text{Min},$ $I_{OH} = -4.0 \text{ mA}$		2.4		V	

Notes: 1. Not more than one output at a time should be shorted. Duration of short circuit test should not exceed 30 sec.

## AC Waveforms

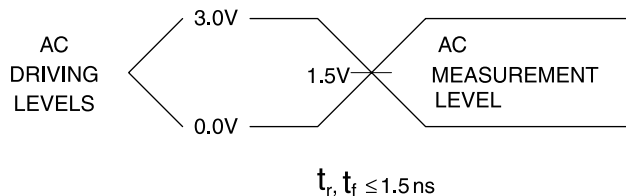


## AC Characteristics<sup>(1)</sup>

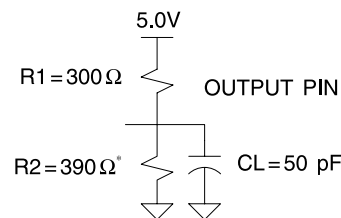
Symbol	Parameter	-12		-15		-20		Units
		Min	Max	Min	Max	Min	Max	
$t_{PD}$	Input or Feedback to Non-registered Output	3	12	3	15	3	20	ns
$t_{CF}$	Clock to Feedback		6		4.5		8	ns
$t_{CO}$	Clock to Output	2	8	2	8	2	12	ns
$t_S$	Input or Feedback Setup Time	10		10		14		ns
$t_H$	Input Hold Time	0		0		0		ns
$t_W$	Clock Width	6		6		10		ns
$f_{MAX}$	External Feedback $1/(t_S + t_{CO})$ Internal Feedback $1/(t_S + t_{CF})$ No Feedback $1/(t_P)$		55.5 62 83.3		55.5 69 83.3		38.5 45.5 50.0	MHz MHz MHz
$t_{EA}$	Input to Output Enable - Product Term	3	12	3	15	3	20	ns
$t_{ER}$	Input to Output Disable - Product Term	2	15	3	15	3	20	ns
$t_{PZX}$	OE Pin to Output Enable	2	12	2	15	2	20	ns
$t_{PXZ}$	OE Pin to Output Disable	2	15	2	15	2	20	ns
$t_{AP}$	Input or I/O to Asynchronous Reset of Register	3	10	3	15	3	22	ns
$t_{SP}$	Setup Time, Synchronous Preset	10		10		14		ns
$t_{AW}$	Asynchronous Reset Width	7		8		20		ns
$t_{AR}$	Asynchronous Reset Recovery Time	5		6		20		ns
$t_{SPR}$	Synchronous Preset to Clock Recovery Time	10		10		14		ns

Note: 1. See ordering information for valid part numbers.

## Input Test Waveforms and Measurement Levels



## Output Test Loads



Note: Similar competitor devices are specified with slightly different loads. These load differences may affect output signals' delay and slew rate. Atmel devices are tested with sufficient margins to meet compatible device specification conditions.

## Pin Capacitance

f = 1 MHz, T = 25°C<sup>(1)</sup>

	Typ	Max	Units	Conditions
C <sub>IN</sub>	8	10	pF	V <sub>IN</sub> = 0V; f = 1.0 MHz
C <sub>I/O</sub>	8	10	pF	V <sub>OUT</sub> = 0V; f = 1.0 MHz

Note: 1. Typical values for nominal supply voltage. This parameter is only sampled and is not 100% tested.

## Power-up Reset

The registers in the ATF22V10CZ/CQZ are designed to reset during power-up. At a point delayed slightly from V<sub>CC</sub> crossing V<sub>RST</sub>, all registers will be reset to the low state. The output state will depend on the polarity of the buffer.

This feature is critical for state machine initialization. However, due to the asynchronous nature of reset and the uncertainty of how V<sub>CC</sub> actually rises in the system, the following conditions are required:

1. The V<sub>CC</sub> rise must be monotonic and start below 0.7V.
2. The clock must remain stable during T<sub>PR</sub>.
3. After T<sub>PR</sub> occurs, all input and feedback setup times must be met before driving the clock pin high.

## Preload of Register Outputs

The ATF22V10CZ/CQZ's registers are provided with circuitry to allow loading of each register with either a high or a low. This feature will simplify testing since any state can be forced into the registers to control test sequencing. A JEDEC file with preload is generated when a source file with vectors is compiled. Once downloaded, the JEDEC file preload sequence will be done automatically by most of the approved programmers after the programming.

## Electronic Signature Word

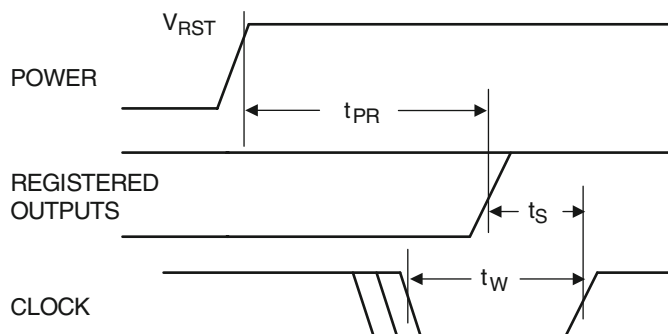
There are 64 bits of programmable memory that are always available to the user, even if the device is secured. These bits can be used for user-specific data.

## Security Fuse Usage

A single fuse is provided to prevent unauthorized copying of the ATF22V10CZ/CQZ fuse patterns. Once programmed, fuse verify and preload are inhibited. However, the 64-bit User Signature remains accessible. The security fuse should be programmed last, as its effect is immediate.

## Programming/Erasing

Programming/erasing is performed using standard PLD programmers. See CMOS PLD Programming Hardware & Software Support for information on software/programming.



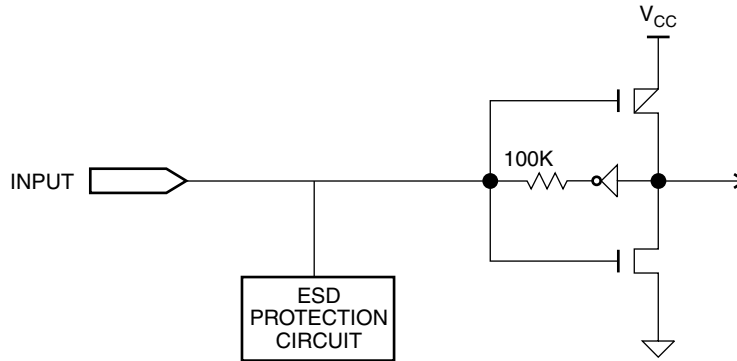
Parameter	Description	Typ	Max	Units
T <sub>PR</sub>	Power-up Reset Time	600	1000	ns
V <sub>RST</sub>	Power-up Reset Voltage	3.8	4.5	V

## Input and I/O Pull-ups

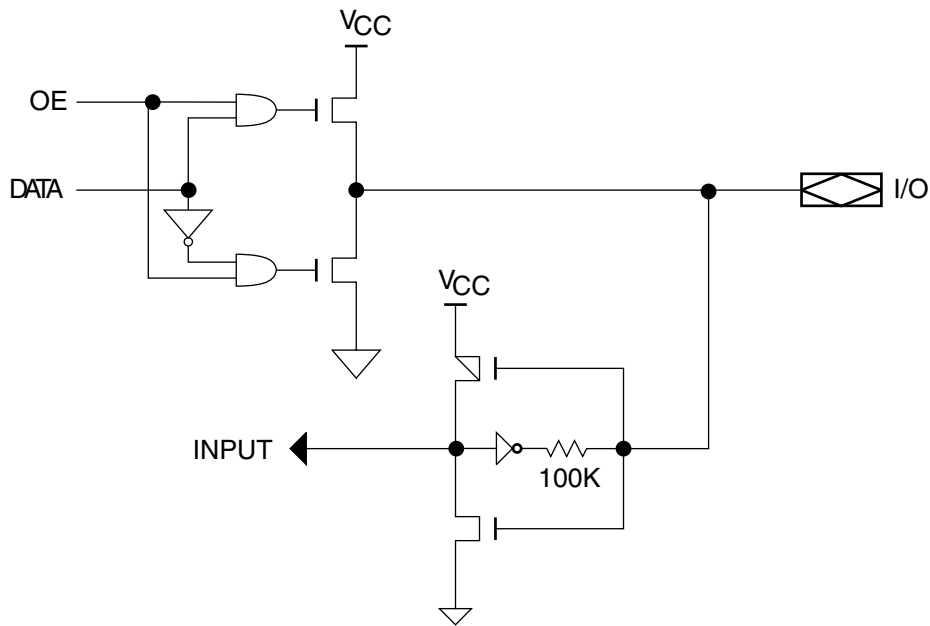
All ATF22V10CZ/CQZ family members have internal input and I/O pin-keeper circuits. Therefore, whenever inputs or I/Os are not being driven externally, they will maintain their last driven state. This ensures that all logic array inputs and

device outputs are at known states. These are relatively weak active circuits that can be easily overridden by TTL-compatible drivers (see input and I/O diagrams below).

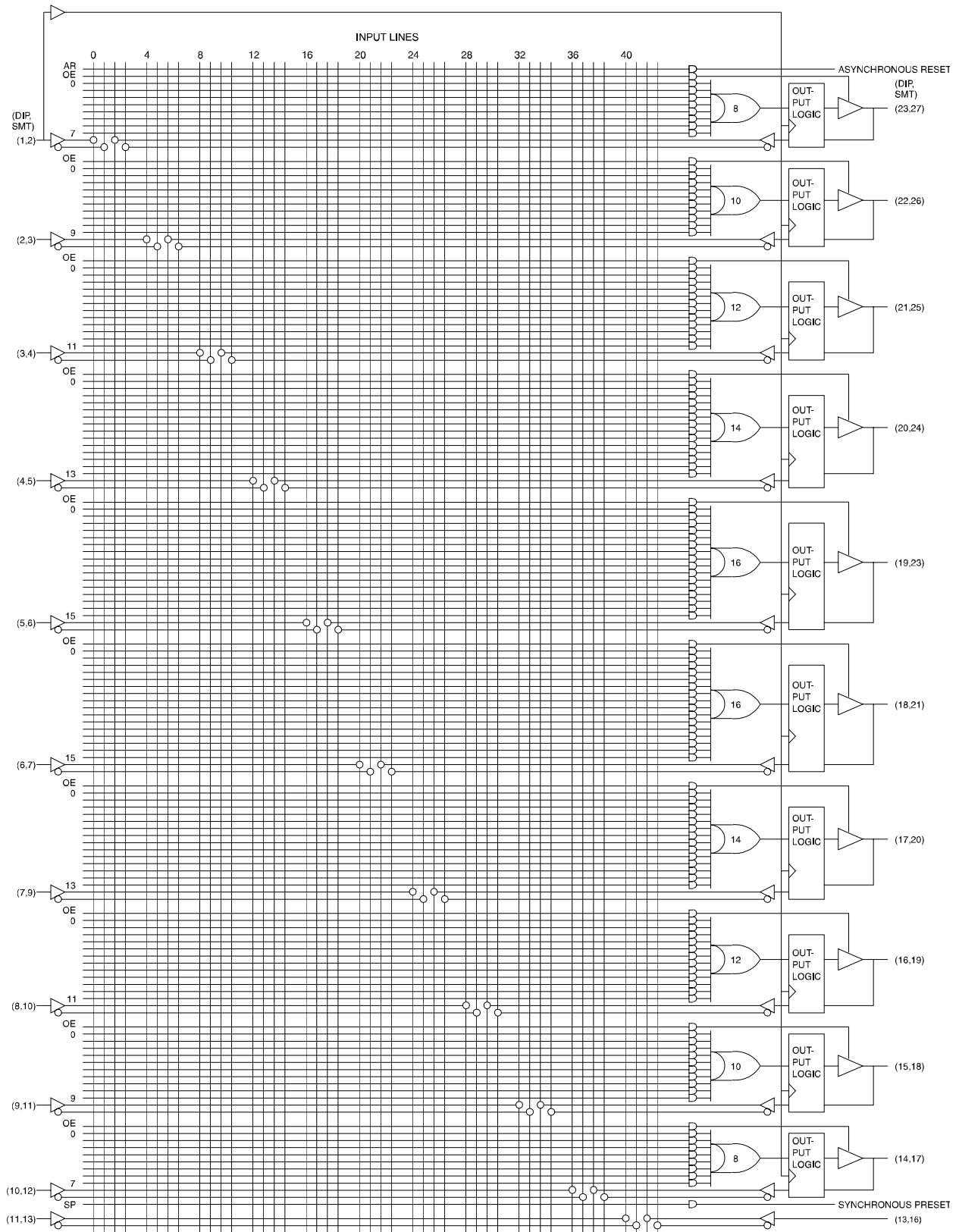
### Input Diagram



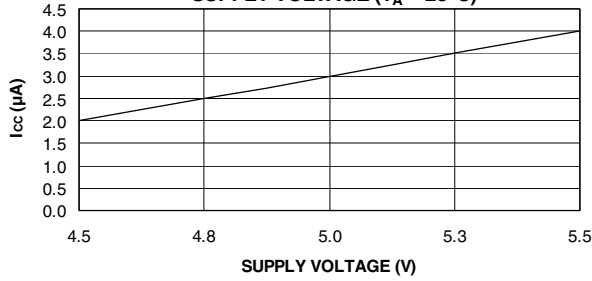
### I/O Diagram



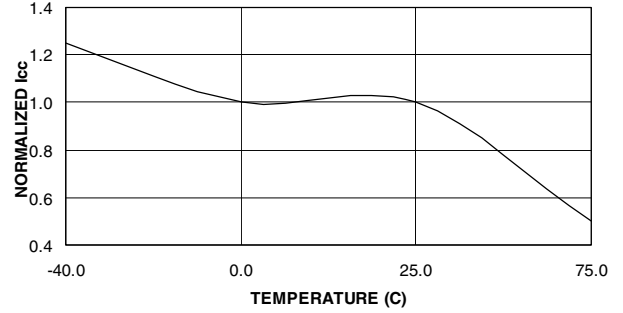
## Functional Logic Diagram ATF22V10CZ/CQZ



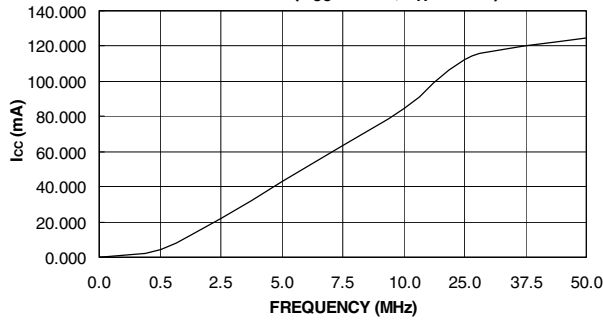
**ATF22V10CZ/CQZ STAND-BY  $I_{CC}$  vs. SUPPLY VOLTAGE ( $T_A = 25^\circ\text{C}$ )**



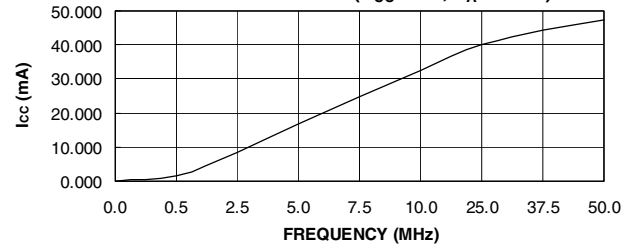
**NORMALIZED  $I_{CC}$  vs. TEMP**



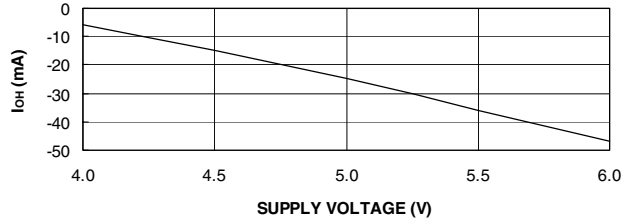
**ATF22V10CZ SUPPLY CURRENT vs. INPUT FREQUENCY ( $V_{CC} = 5.0\text{V}$ ,  $T_A = 25^\circ\text{C}$ )**



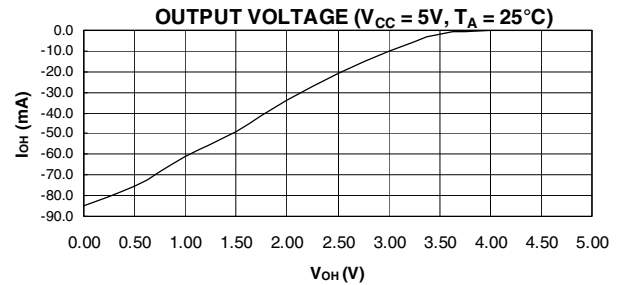
**ATF22V10CQZ SUPPLY CURRENT vs. INPUT FREQUENCY ( $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ )**



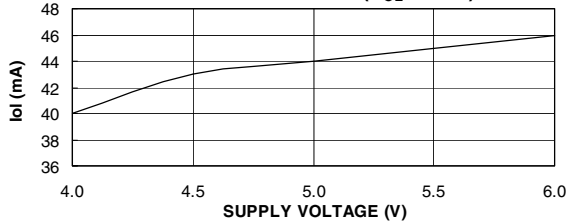
**ATF22V10CZ/CQZ OUTPUT SOURCE CURRENT vs. SUPPLY VOLTAGE ( $V_{OH} = 2.4\text{V}$ )**



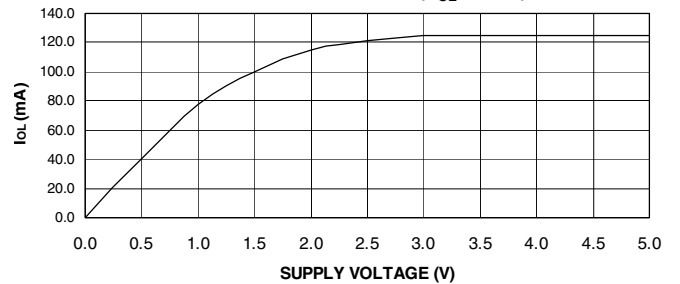
**ATF22V10CZ/CQZ OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE ( $V_{CC} = 5\text{V}$ ,  $T_A = 25^\circ\text{C}$ )**



**ATF22V10CZ/CQZ OUTPUT SINK CURRENT vs. SUPPLY VOLTAGE ( $V_{OL} = 0.5\text{V}$ )**

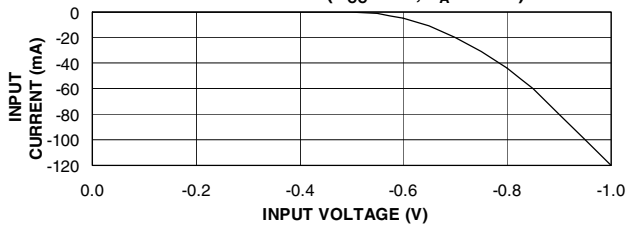


**ATF22V10CZ/CQZ OUTPUT SINK CURRENT vs. SUPPLY VOLTAGE ( $V_{OL} = 0.5\text{V}$ )**

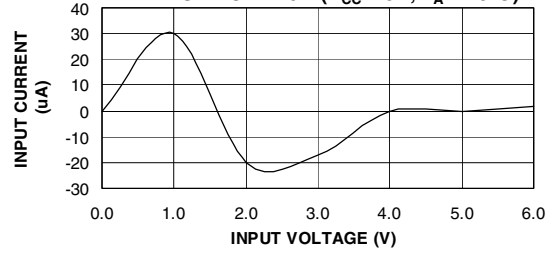




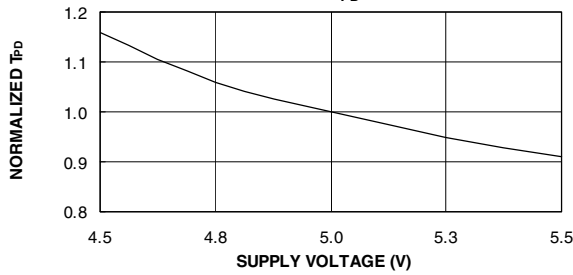
**ATF22V10CZ/CQZ INPUT CLAMP CURRENT VS INPUT VOLTAGE ( $V_{CC} = 5V$ ,  $T_A = 35^\circ C$ )**



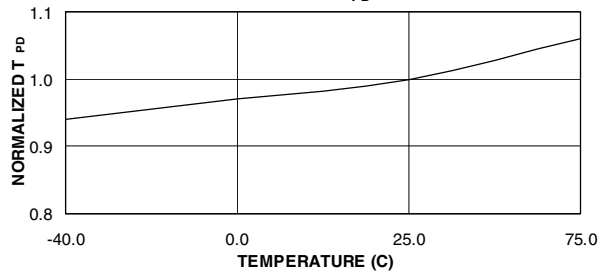
**ATF22V10CZ/CQZ INPUT CURRENT VS INPUT VOLTAGE ( $V_{CC} = 5V$ ,  $T_A = 25^\circ C$ )**



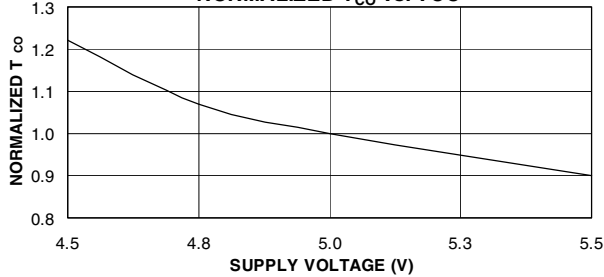
**NORMALIZED  $T_{PD}$  vs. VCC**



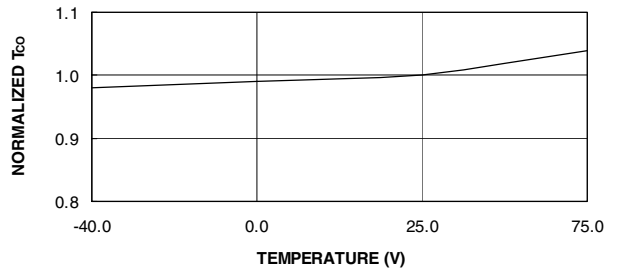
**NORMALIZED  $T_{PD}$  vs. TEMP**



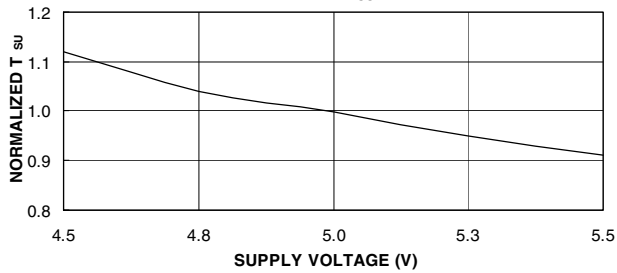
**NORMALIZED  $T_{CO}$  vs. VCC**



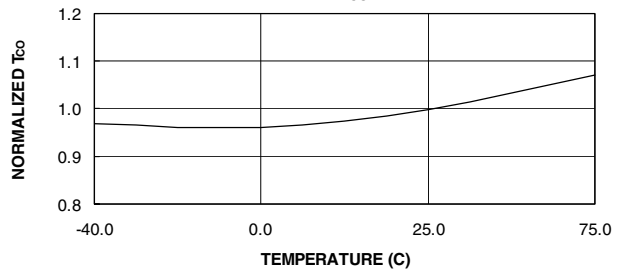
**NORMALIZED  $T_{CO}$  vs. TEMP**



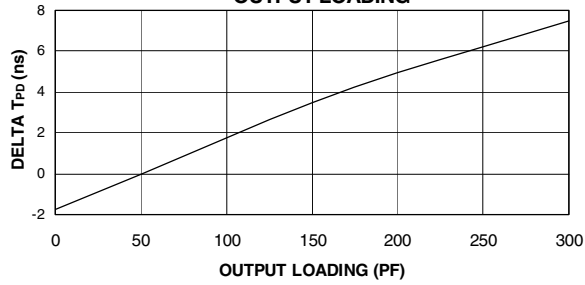
**NORMALIZED  $T_{SU}$  vs VCC**



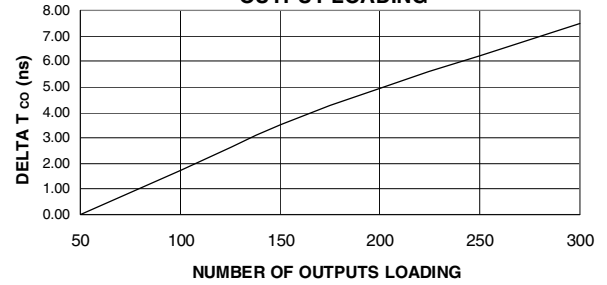
**NORMALIZED  $T_{SU}$  vs. TEMP**



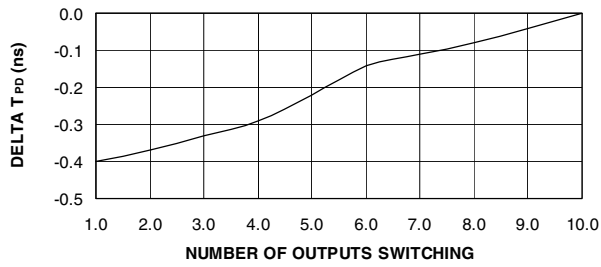
**ATF22V10C DELTA  $T_{PD}$  vs. OUTPUT LOADING**



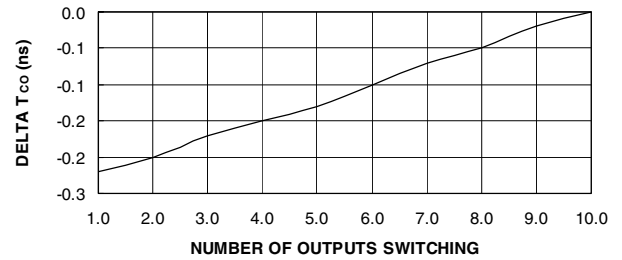
**ATF22V10C DELTA  $T_{CO}$  vs. OUTPUT LOADING**



**DELTA  $T_{PD}$  vs. # OF OUTPUT SWITCHING**



**DELTA  $T_{CO}$  vs. # OF OUTPUT SWITCHING**



## ATF22V10CZ/CQZ Ordering Information

$t_{PD}$ (ns)	$t_S$ (ns)	$t_{CO}$ (ns)	Ordering Code	Package	Operation Range		
12	10	8	ATF22V10CZ-12JC	28J 24P3 24S 24X	Commercial (0°C to 70°C)		
			ATF22V10CZ-12PC				
			ATF22V10CZ-12SC				
			ATF22V10CZ-12XC				
15	4.5	8	ATF22V10CZ-15JC	28J 24P3 24S 24X	Commercial (0°C to 70°C)		
			ATF22V10CZ-15PC				
			ATF22V10CZ-15SC				
			ATF22V10CZ-15XC	28J 24P3 24S 24X	Industrial (-40°C to +85°C)		
			ATF22V10CZ-15JI				
			ATF22V10CZ-15PI				
20	14	12	ATF22V10CZ-15SI	28J 24P3 24S 24X	Industrial (-40°C to +85°C)		
			ATF22V10CZ-15XI				
			ATF22V10CQZ-20JC			28J 24P3 24S 24X	Commercial (0°C to 70°C)
			ATF22V10CQZ-20PC				
			ATF22V10CQZ-20SC				
			ATF22V10CQZ-20XC				
			ATF22V10CQZ-20JI	28J 24P3 24S 24X	Industrial (-40°C to +85°C)		
			ATF22V10CQZ-20PI				
ATF22V10CQZ-20SI							
ATF22V10CQZ-20XI							

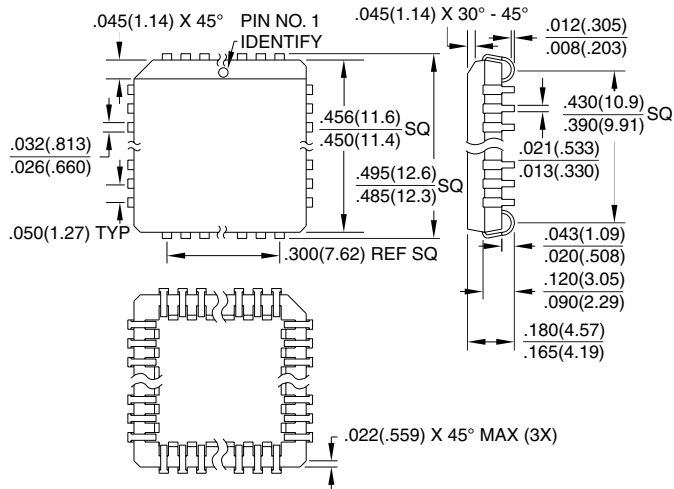
### Using “C” Product for Industrial

To use commercial product for Industrial temperature ranges, down-grade one speed grade from the “I” to the “C” device (7 ns “C” = 10 ns “I”) and de-rate power by 30%.

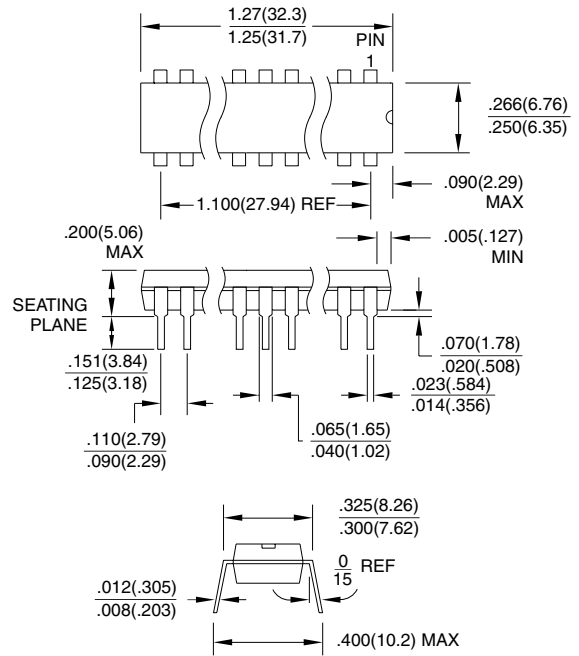
Package Type	
<b>28J</b>	28-lead, Plastic J-leaded Chip Carrier (PLCC)
<b>24P3</b>	24-pin, 0.300", Plastic Dual Inline Package (PDIP)
<b>24S</b>	24-lead, 0.300" Wide, Plastic Gull-Wing Small Outline (SOIC)
<b>24X</b>	24-lead, 4.4 mm Wide, Plastic Thin Shrink Small Outline (TSSOP)

## Packaging Information

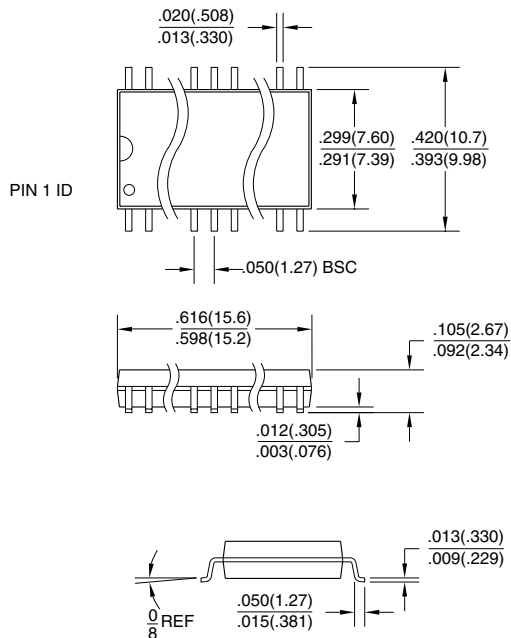
**28J**, 28-lead, Plastic J-leaded Chip Carrier (PLCC)  
 Dimensions in Inches and (Millimeters)  
 JEDEC STANDARD MS-018 AB



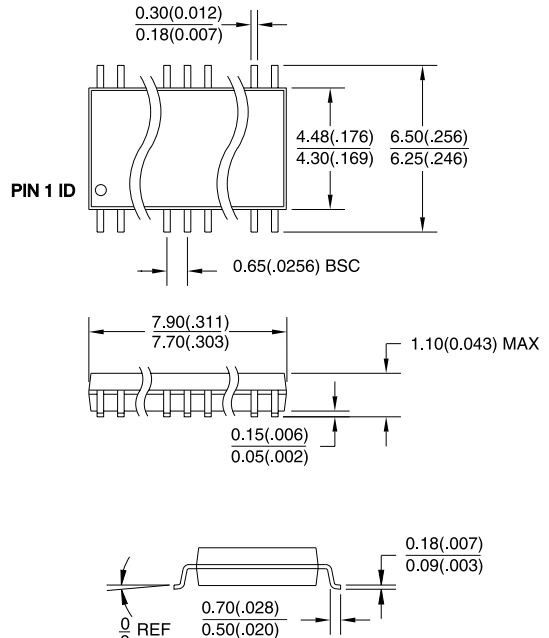
**24P3**, 24-pin, 0.300" Wide,  
 Plastic Dual Inline Package (PDIP)  
 Dimensions in Inches and (Millimeters)  
 JEDEC STANDARD MS-001 AF



**24S**, 24-lead, 0.300" Wide,  
 Plastic Gull-Wing Small Outline (SOIC)  
 Dimensions in Inches and (Millimeters)



**24X**, 24-lead, 4.4 mm Wide, Plastic Thin Shrink  
 Small Outline (TSSOP)  
 Dimensions in Inches and (Millimeters)





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