AN937
Application Note

Designing with L4971, 1.5 A high efficiency DC-DC converter

Introduction

The L4971 is a 1.5 A monolithic dc-dc converter, step- down, operating at fix frequency continuous mode. It is designed in BCD60 II technology, and it is available in two plastic packages, DIP8 and SO16L.

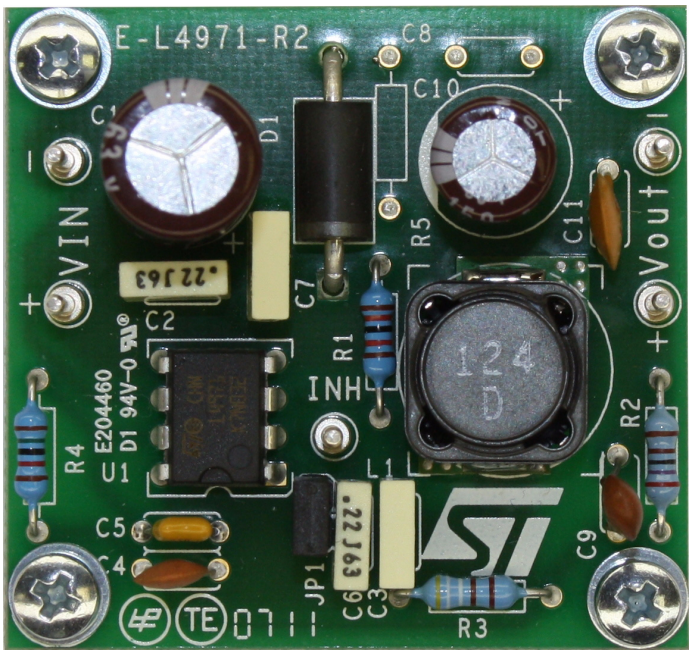
One direct fixed output voltage at 3.3 V ±1% is available, adjustable for higher output voltage values, till 40 V, by an external voltage divider.

The operating input supply voltage ranges from 8 V to 55 V, while the absolute value, with no load, is 60V. New internal design solutions and superior technology performance allow to generate a device with improved efficiency in all the operating conditions and with reduced EMI due to an innovative internal driving circuit, and reduced external component counts.

While internal limiting current and thermal shutdown are today considered standard protection functions, mandatory for a safe load supply, oscillator with voltage feed forward improves line regulation and overall control loop.

Soft-start avoids output over voltage at turn-on, while, shorting this pin to ground, the device is completely disabled, going into zero consumption state.

Figure 1. Demonstration board



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1 Device description

For a better understanding of the device and it's working principle, a short description of the main building blocks is given here below, with packaging options and complete block diagram.

Figure 2 show s the two packaging options, with the pin function assignments.

Figure 2. Pin Connections

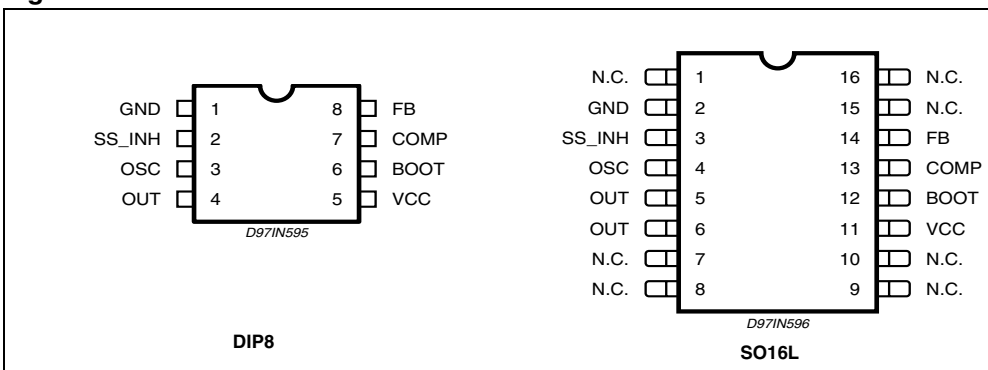
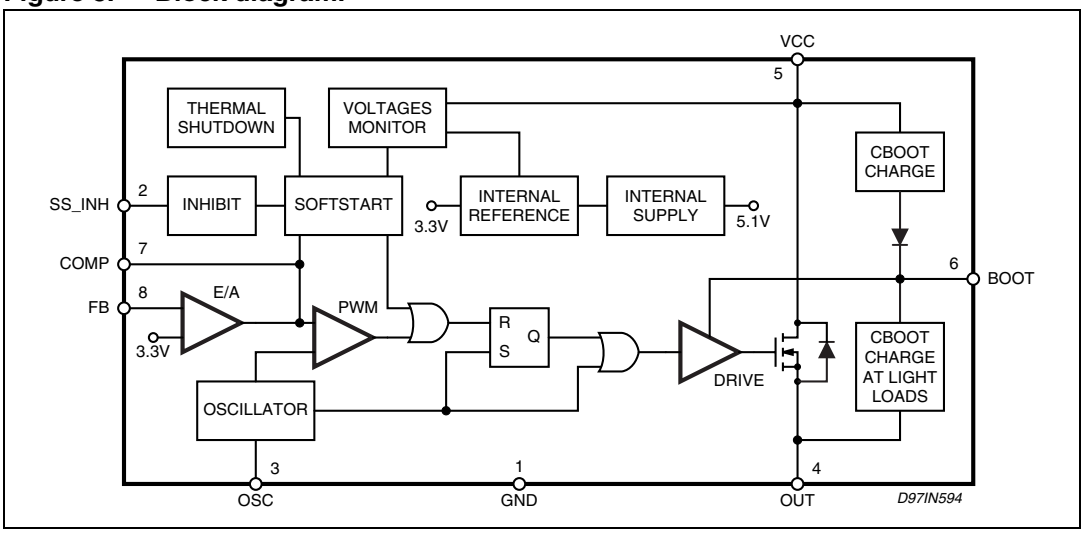


Figure 3. Block diagram.



2 Power supply, UVLO and voltage reference

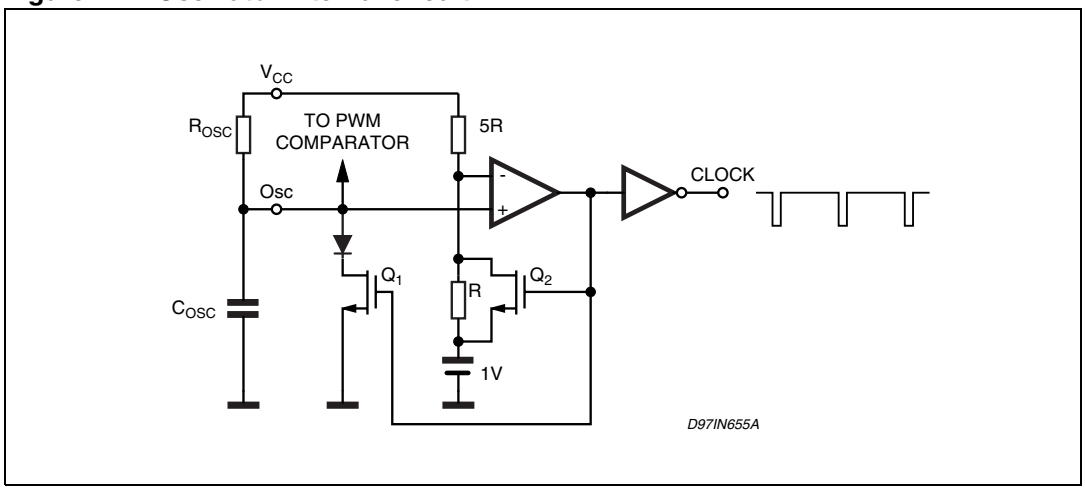
The device is provided with an internal stabilized power supply (of about 12 V typ.) that powers the analog and digital control blocks and the bootstrap section.

From this pre regulator, a 3.3V reference voltage ±2%, is internally available.

2.1 Oscillator and voltage feed forward

Just one pin is necessary to implement the oscillator function, with inherent voltage feedforward.

Figure 4. Oscillator internal circuit



A resistor Rosc and a capacitor Cosc connected as shown in *Figure 4*, allow the setting of the desired switching frequency in agreement with the below formula:

$$F_{SW} = \frac{1}{(R_{oasc} \cdot C_{osc}) \ln\left(\frac{6}{5}\right) + 100 \cdot C_{osc}}$$

Where F_{sw} is in kHz, R_{osc} in kΩ and C_{osc} in nF.

The oscillator capacitor, C_{osc}, is discharged by an internal MOS transistor of 100 Ω of R_{dson} (Q1) and during this period the internal threshold is set at 1 V by a second MOS, Q2. When the oscillator voltage capacitor reaches the 1V threshold the output comparator turn-off the MOS Q1 and turn-on the MOS Q2, restarting the C_{osc} charging.

The oscillator block, shown in *Figure 4*, generates a sawtooth wave signal that sets the switching frequency of the system.

This signal, compared with the output of the error amplifier, generates the PWM signal that will modulate the conduction time of the power output stage.

The way the oscillator has been integrated, does not require additional external components to benefit of the voltage feed forward function.

The oscillator peak-to-valley voltage is proportional to the supply voltage, and the voltage feed forward is operative from 8 V to 55 V of input supply.

$$\Delta V_{osc} = \frac{V_{CC} - 1}{6}$$

Also the $\Delta V/\Delta t$ of the sawtooth is directly proportional to the supply voltage. As Vcc increases, the Ton time of the power transistor decreases in such a way to provide to the choke, and finally also the load, the product Volt. sec constant.

Figure 6 show how the duty cycle varies as a result of the change on the $\Delta V/\Delta t$ of the sawtooth with the Vcc. The output of the error amplifier doesn't change to maintain the output voltage constant and in regulation. With this function on board, the output response time is greatly reduced in presence of an abrupt change on the supply voltage, and the output ripple voltage at the mains frequency is greatly reduced too.

Figure 5. Device switching frequency vs Rosc and Cosc

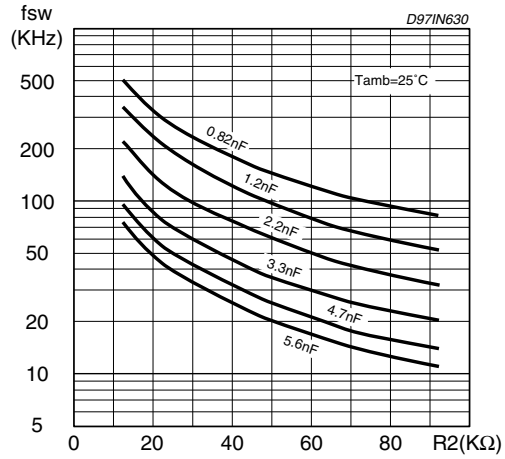


Figure 6. Voltage feed forward function

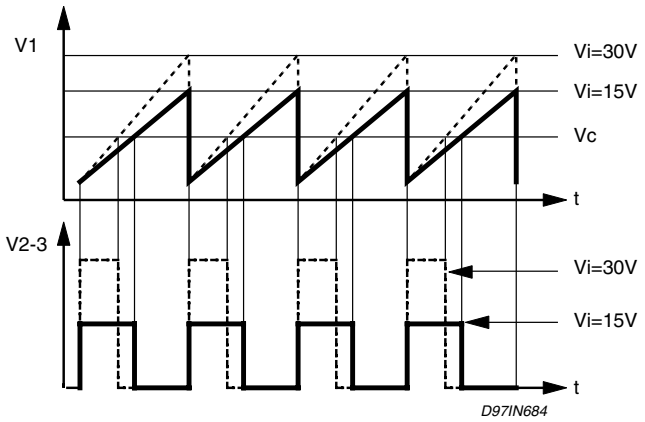
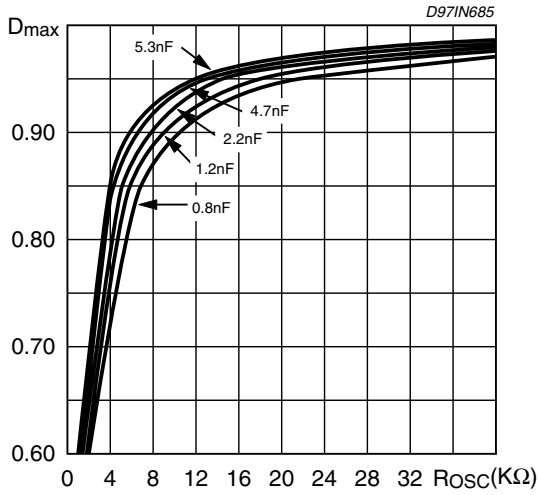


Figure 7. Maximum duty cycle vs. Rosc and Cosc as parameter



In fact, the slope of the ramp is modulated by the input ripple voltage, generally present in the order of some tents of Volt, for both off-line and dc-dc converters using mains transformers.

The charge and discharge time is approximately to:

$$Tch = R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right)$$

$$Tdis = 100 \cdot C_{osc}$$

The maximum duty cycle is a function of Tch, Tdis and an internal delay and is represented by the equation:

$$Dmax = \frac{R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right) - 80 \cdot 10^{-9}}{R_{osc} \cdot C_{osc} \cdot \ln\left(\frac{6}{5}\right) + 100 \cdot C_{osc}}$$

and is represented in *Figure 7*:

2.2 Current protection

The L4971 has two current limit levels, pulse by pulse and hiccup modes.

Increasing the output current till the pulse by pulse limiting current threshold (Ith1 typ. value of 2.5 A) the controller reduces the on-time till the value of T_B = 300 ns that is a blanking time in which the current limit protection does not trigger. This minimum time is necessary to avoid undesirable intervention of the protection due to the spike current generated during the recovery time of the freewheeling diode.

In this condition, because of this fixed blanking time, the output current is given by:

$$I_{max} = \frac{[V_{CC} \cdot T_B \cdot F_{SW} - V_f \cdot (1 - T_B \cdot F_{SW})]}{[R_O + (R_D + R_L)(1 - T_B \cdot F_{SW}) + (R_{dson} + R_L)T_B \cdot F_{SW}]}$$

In *Figure 8*, the pulse by pulse protection is sufficient to limit the current.

In *Figure 9* the pulse by pulse protection is no more effective to limit the current due to the minimum Ton fixed by the blanking time TB, and the hiccup protection intervenes because the output peak current reaches the relative threshold. At the pulse by pulse intervention (point A) the output voltage drops because of the Ton reduction, and the current is almost constant. Going versus the short circuit condition, the current is only limited by the series resistances RD and RL (see relation above) and could reach the hiccup threshold (point B), set 20% higher than the pulse by pulse. Once the hiccup limiting current is operating, in output short circuit condition, the delivered average output current decreases dramatically at very low values (point C).

Figure 8. Output characteristics

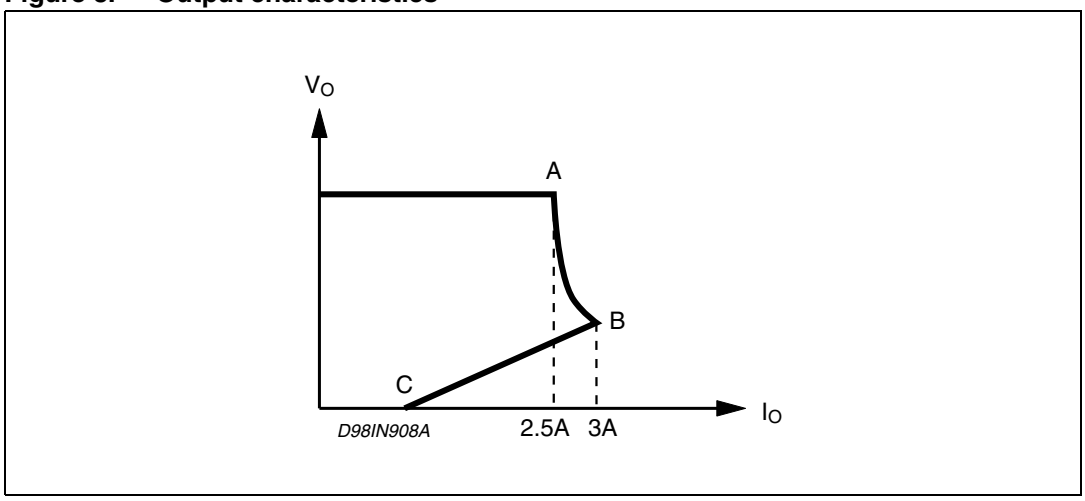


Figure 9. Output characteristics

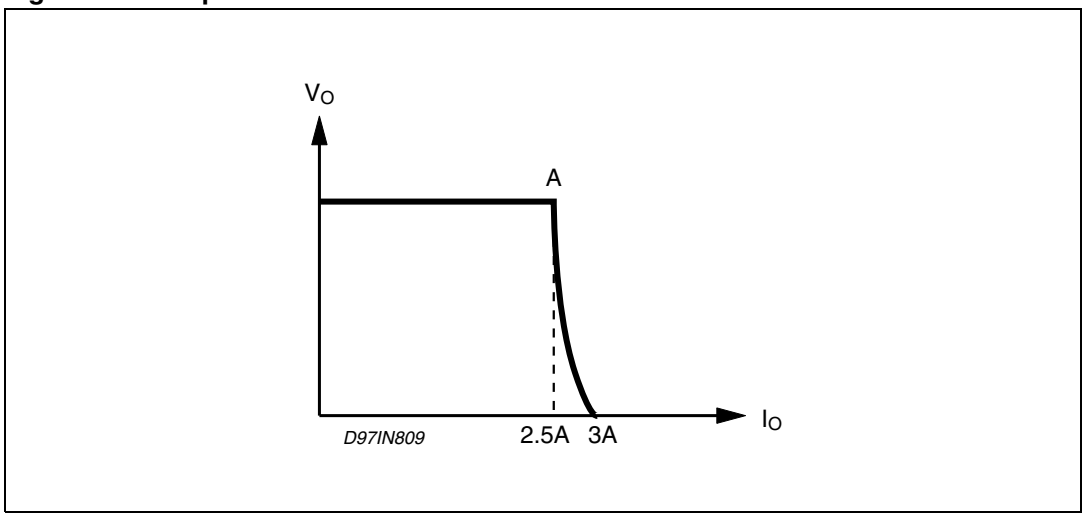


Figure 10. Current limiting internal schematic circuit

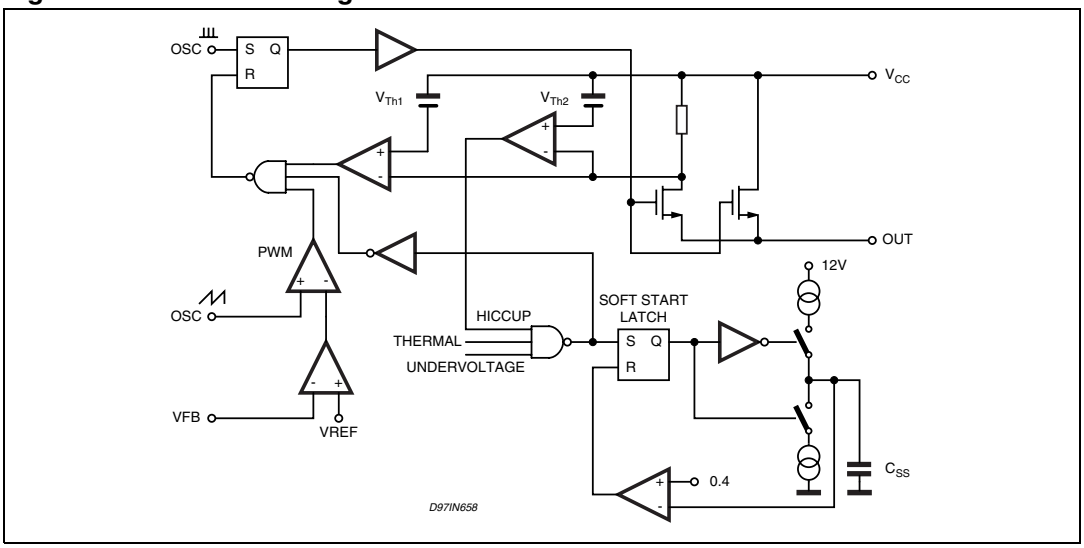


Figure 11. Output current and soft start voltage

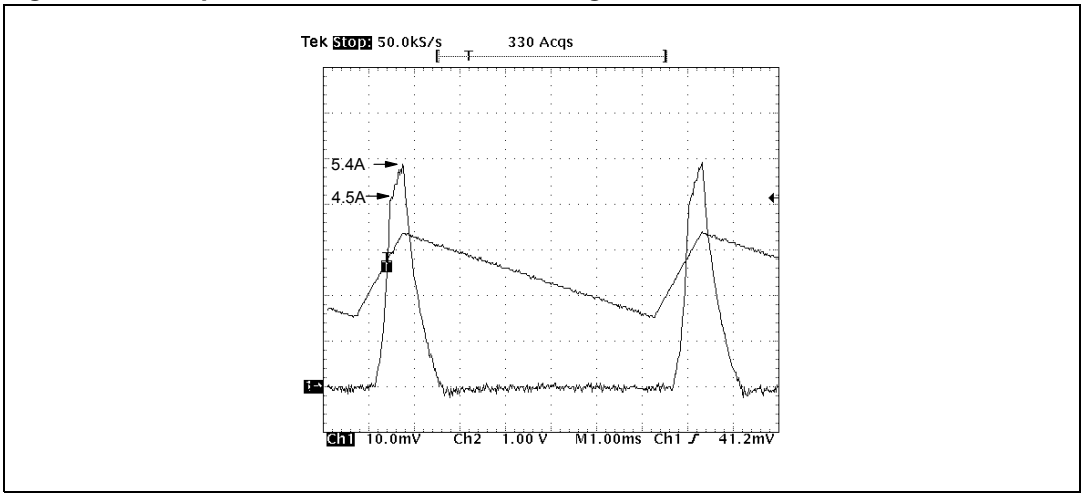


Figure 10 shows the internal current limiting circuitry. Vth1 is the pulse by pulse while Vth2 is the hiccup threshold.

The sense resistor is in series with a small MOS realized as a partition of the main DMOS.

The Vth2 comparator (20% higher than Vth1) sets the soft start latch, initializing the discharge of the soft start capacitor with a constant current (about 22 mA). Reaching about 0.4 V, the valley comparator resets the soft start latch, restarting a new recharge cycle.

Figure 11 shows the typical waveforms of the current in the output inductor and the soft start voltage (pin 2).

During the recharging of the soft start capacitor, the Ton increases gradually and, if the short circuit is still present, when Ton>TB and the output peak current reaches the threshold, the hiccup protection intervenes again. So, the value of the soft start capacitor must not be too high (in this case the Ton increases slowly thus taking much time to reach the TB value) to avoid that during the soft start slope, the current exceeds the limit before the protection activation.

The following diagrams of *Figure 13* and *Figure 14* show the maximum allowed soft-start capacitor as a function of the input voltage, inductor value and switching frequency. A minimum value of the soft start capacitance is necessary to guarantee, in short circuit condition, the functionality of the limiting current circuitry.

In fact, with a capacitor too small, the frequency of the current peaks (see *Figure 11*) is high and the mean current value in short circuit increases.

Example: for a maximum input voltage of 55 V at 100 kHz, with an inductor of 260 mH, it is possible to use a soft start capacitor lower than 470 µF. With such a value, the soft start time (see *Figure 19*) of about 10 ms for an output voltage of 5 V.

Figure 12. Maximum soft start capacitance with f_{SW} = 100 kHz

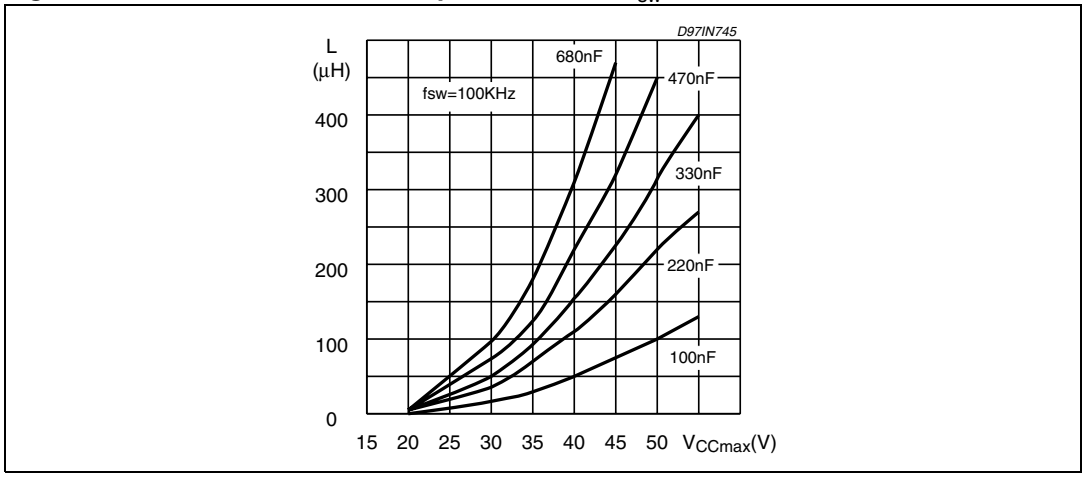
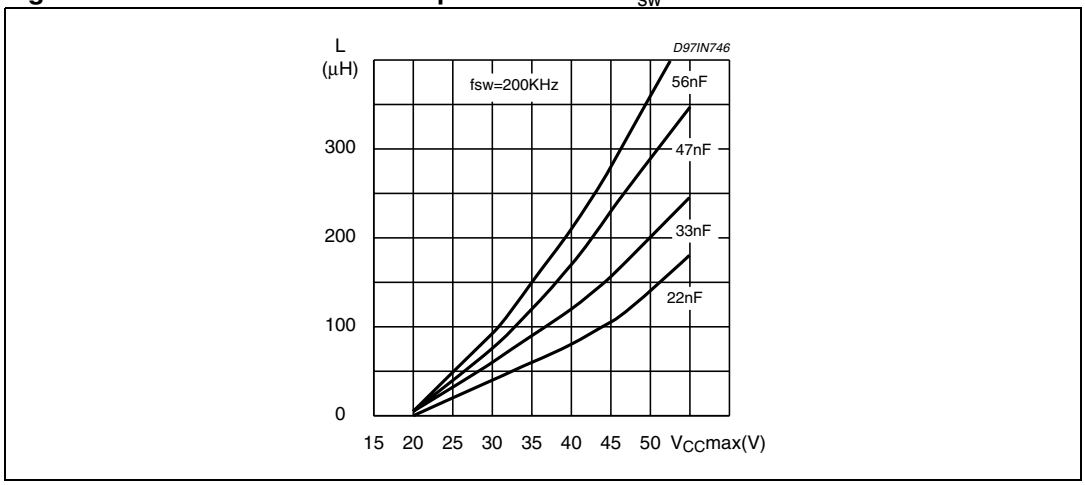


Figure 13. Maximum soft start capacitance with f_{SW} = 200 kHz

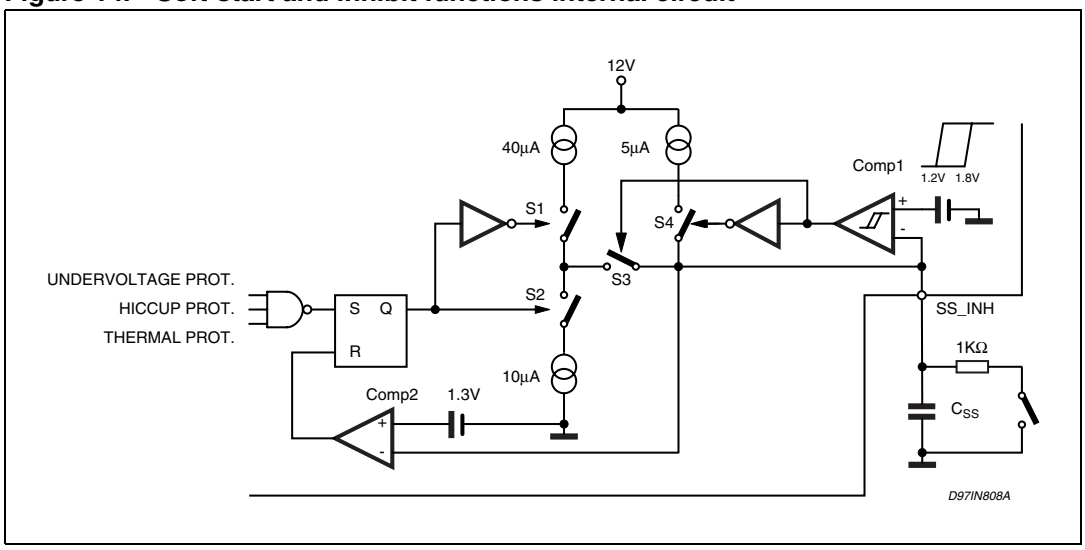


2.3 Soft-start and inhibit functions

The soft start and the inhibit functions are designed using one pin only, pin2. Soft-start is requested to initialize all internal functions with a correct start-up of the system without overstressing the power stage, avoiding the intervention of the current protection, and having an output voltage rising smoothly without output overshoots.

At Vcc Turn-on or having had an intervention of inhibit function, an initial 5 µA internal current generator starts to charge the soft-start capacitor, from 0 V to about 1.8 V. From this hysteretic threshold, a 40 µA current generator is activated, putting in off state the previous generator.

Figure 14. Soft-start and inhibit functions internal circuit



At this point, the output PWM starts, initiating the rising phase of the output voltage.

The soft-start capacitor is quickly discharged in case of:

- Thermal protection intervention
- Hiccup limiting current condition
- Supply voltage lower than UVLO off threshold.

The soft-start and inhibit schematic diagram is shown in *Figure 14*.

At device turn-on, the soft-start capacitor has no charge, with 0 V at its terminals.

From 0 V to 1.8 V, switch S3 is opened and S4 is closed.

Soft-start capacitor is charged with 5 µA.

At 1.8 V, comp1 change the output status, opening S4 and closing S3, and the device starts to generate the PWM signal, rising smoothly the output voltage.

Till this moment, S2 is opened, S1 closed.

By closing S3, the soft-start capacitor is charged with 40µA reaching its saturation voltage.

This procedure is repeated at each Vcc turn-on.

Figure 15. Timing diagram in inhibit, overcurrent and turn off condition

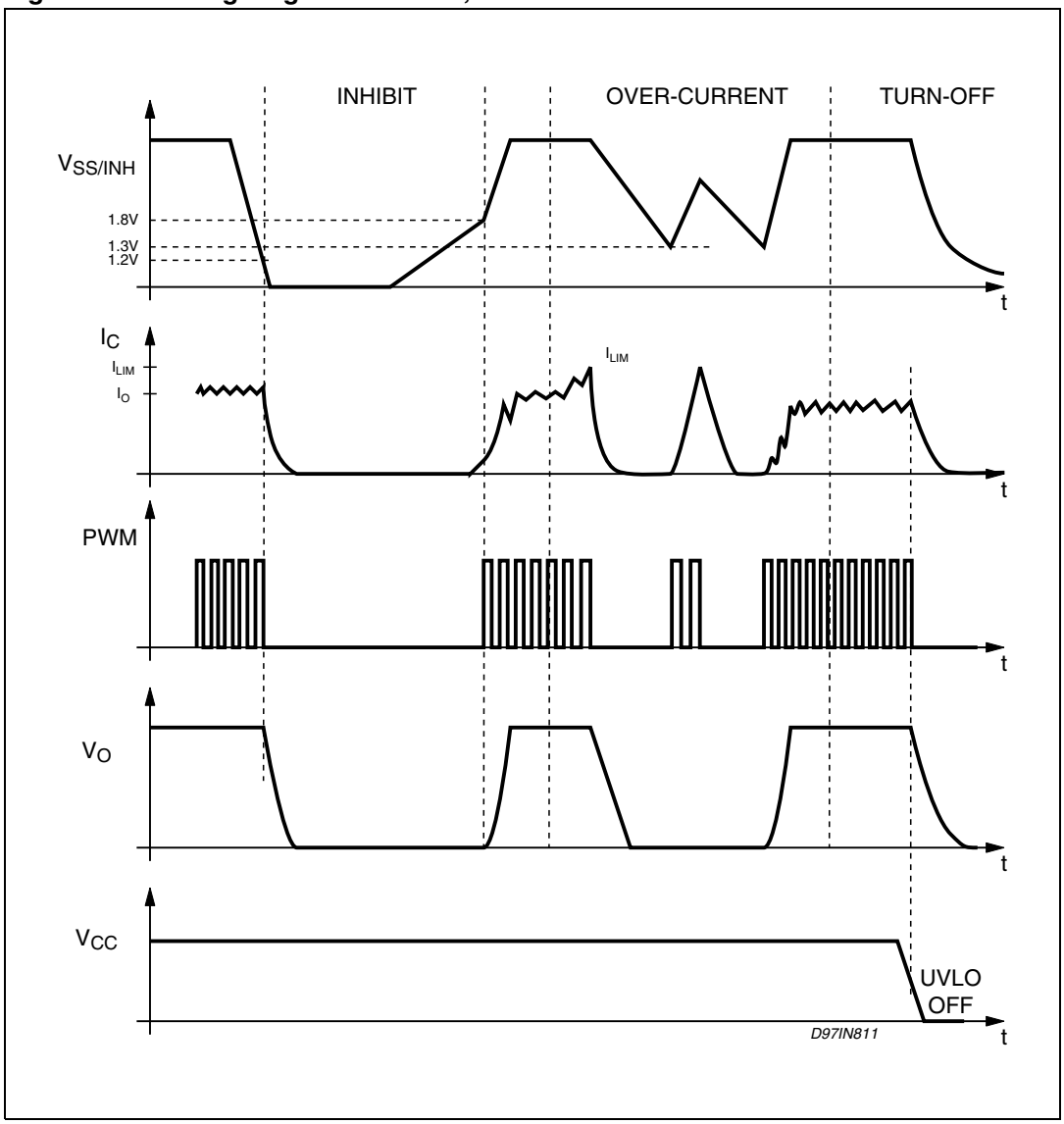
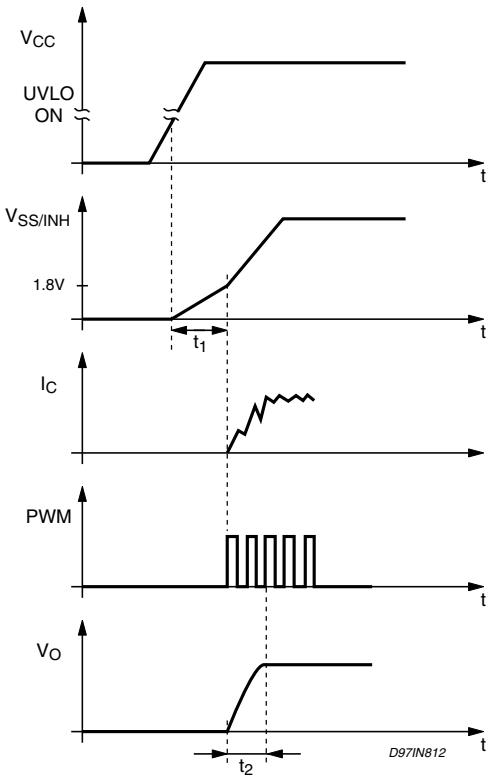


Figure 16. Start up sequence



Turning Vcc off, the soft-start capacitor is discharged with a constant 10 µA (S2 closed, S3 closed, S1 and S4 open), from the moment when Vcc is crossing the UVLO off threshold.

The final discharge value is 1.2 V. In case of the Css is discharged using an external grounded element when the voltage at Css reaches the threshold of 1.3 V Comp2 resets the flip flop, S1 is closed, S2 is opened and the 40 mA current generator is activated.

The external switch, sinking some mA, discharges the soft-start under the 1.2 V Comp1 threshold, opening S3 and closing S4. At this point the device is in disable, sourcing only 5 µA through pin 2. When the external grounding element is removed, the device restarts charging the soft start capacitance, initially, with 5 µA till the voltage reaches the 1.8 V threshold and Comp1 connects the 40 µA charging current generator. In case of thermal shutdown or overcurrent protection intervention the power is turned off and the flip flop turns off S2 and turns on S1. The soft-start is discharged till the voltage reaches the 1.3 V threshold, and Comp2 resets the flip flop. S1 is closed, S2 is opened and the soft-start capacitance is charged again.

Figure 15 shows the systems signals during Inhibit, overcurrent and Vcc turn off.

t1 and t2 can be calculated by the following equations:

$$t1 = 0.36 \cdot Css; \qquad t2 = \frac{V_O}{Ich \cdot 6 \cdot D_{max}} \cdot C_{ss}$$

where Dmax is 0.95, Css is in µF and Ich is in µA. Soft-start time (t2) versus output voltage and Css is shown in *Figure 17*.

Thanks to the voltage feed forward, the start-up time (t2) is not affected by the input voltage.

Figure 18 shows the output voltage start-up using different soft-start capacitance values:

It is mandatory a minimum capacitor value of 22 nF. The pin 2 cannot be left open.

Figure 17. Soft-start time (t2) vs Vo and Css

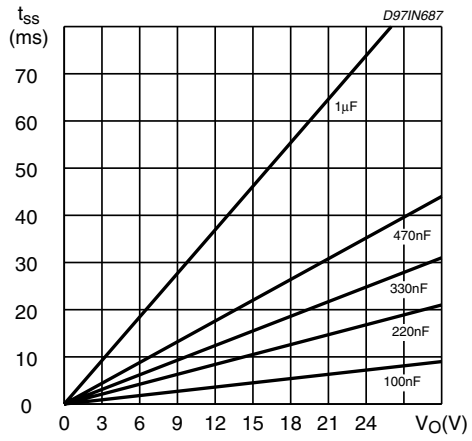
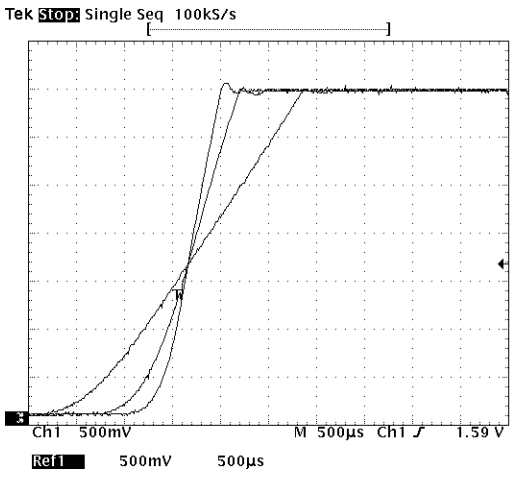


Figure 18. Output rising voltage with Css 56 nF, 100 nF, 22 0nF



2.4 Feedback disconnection

In case of feedback disconnection, the duty cycle increases versus the max allowed value bringing the output voltage close to the input supply. This condition could destroy the load.

To avoid this dangerous condition, the device is forcing a little current (1.4 μA typical) out of the pin 8 (E/A Feedback).

If the feedback is disconnected, open loop, and the impedance at pin 8 is higher than 3.5 MΩ, the voltage at this pin goes higher than the internal reference voltage located on the non-inverting error amplifier input, and turns-off the power device.

2.5 Zero load

In normal operation, the output regulation is also guaranteed because the bootstrap capacitor is recharged, cycle by cycle, by means of the energy flowing into the choke.

Under light load conditions, this topology tends to operate in burst mode, with random repetition rate of the bursts. An internal new function makes this device capable of keeping the output voltage in full regulation with 1mA of load current only.

Between 1 mA and 500 μA, the output is kept in regulation up to 8% above the nominal value.

Here the circuitry providing the control:

1. A comparator located on the bootstrap section is sensing the bootstrap voltage; when this is lower than 5 V, the internal power VDMOS is forced ON for one cycle and OFF for the next.
2. During this operation mode, i.e. 500 μA of load current, the E/A control is lost. To avoid output over voltage, a comparator with one input connected to pin 8, and the second input connected to a threshold 8% higher that nominal output, turns OFF the internal power device the output is reaching that threshold.
   When the output current, or rather, the current flowing into the choke, is lower than 500 μA, that is also the consumption of the bootstrap section, the output voltage starts to increase, approaching the supply voltage.

2.6 Output overvoltage protection (OVP)

The output overvoltage protection, OVP, is realized by using an internal comparator, which input is connected to pin 8, the feedback, that turns-off the power stage when the OVP threshold is reached. This threshold is typically 8% higher than the feedback voltage.

When a voltage divider is requested for adjusting the output voltage, the OVP intervention will be set at:

$$V_{OVP} = 1.08 \cdot V_{fB} \cdot \frac{(Ra + Rb)}{Rb}$$

where Ra is the resistor connected to the output.

2.7 Power stage

The power stage is realized by a N-channel D-MOS transistor with a Vdss in excess of 60 V and typ R_{dson} of 290 mΩ (measured at the device pins).

Minimizing the R_{dson}, means also minimize the conduction losses.

But also the switching losses have to be taken into consideration. mainly for the two following reasons:

a) They are affecting the system efficiency and the device power dissipation

b) Because they generate EMI.

2.8 Turn - on

At turn-on of the power element, or better, the rise time of the current (di/dt) at turn-on is the most critical parameter to compromise.

At a first approach, it looks that faster is the rise time and lower are the turn-on losses.

It's not completely true.

There is a limit, and it's introduce by the recovery time of the recirculation diode.

Above this limit, about 100 A/usec, only disadvantages are obtained:

1. Turn-on overcurrent is decreasing efficiency and system reliability
2. Big EMI increase.

The L4971 has been developed with a special focus on this dynamic area.

An innovative and proprietary gate driver, with two different timings, has been introduced.

When the diode reverse voltage is reaching about 3 V, the gate is sourced with low current (see *Figure 20*) to assure the complete recovery of the diode without generating unwanted extra peak currents and noise. After this threshold, the gate drive current is quickly increased, producing a fast rise time till the peak current, so maintaining the efficiency very high.

Figure 19. Turn on and Turn off (pin 2, 3)

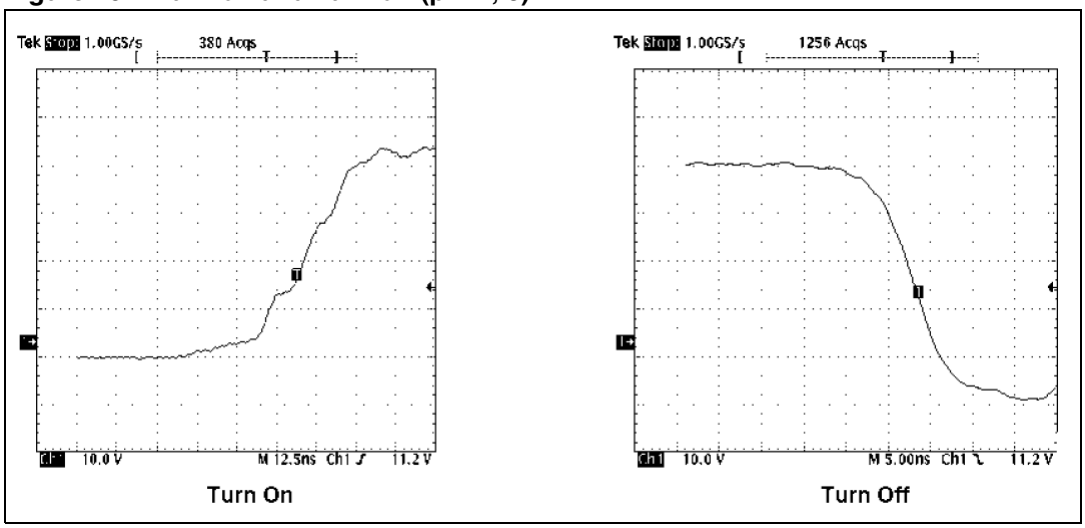
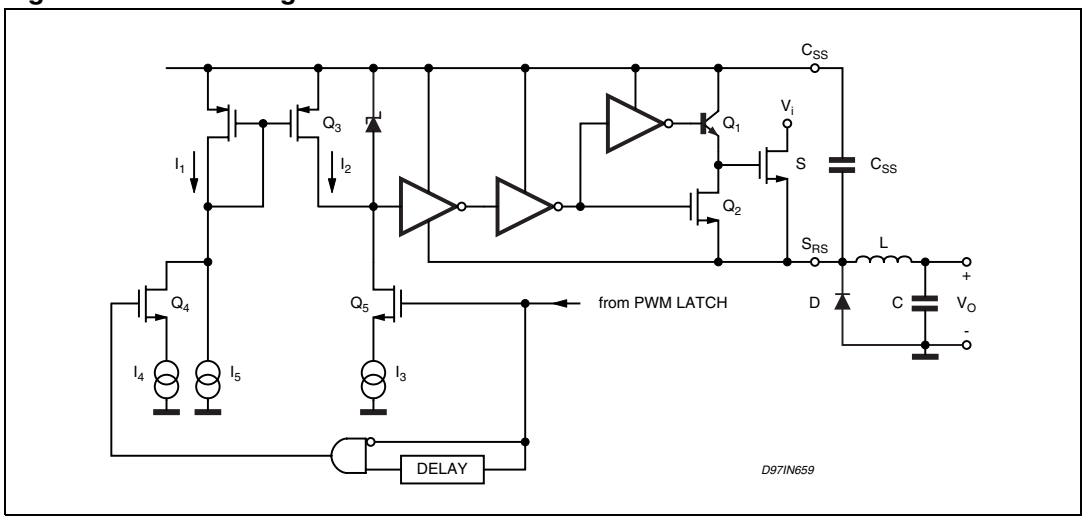


Figure 20. Power stage internal circuit



2.9 Turn - off

The turn-off behavior, is shown at *Figure 19*.

Figure 20 shows the details of the internal power stage and driver, where at Q2 is demanded the turn-off of the power switch, S.

3 Typical application

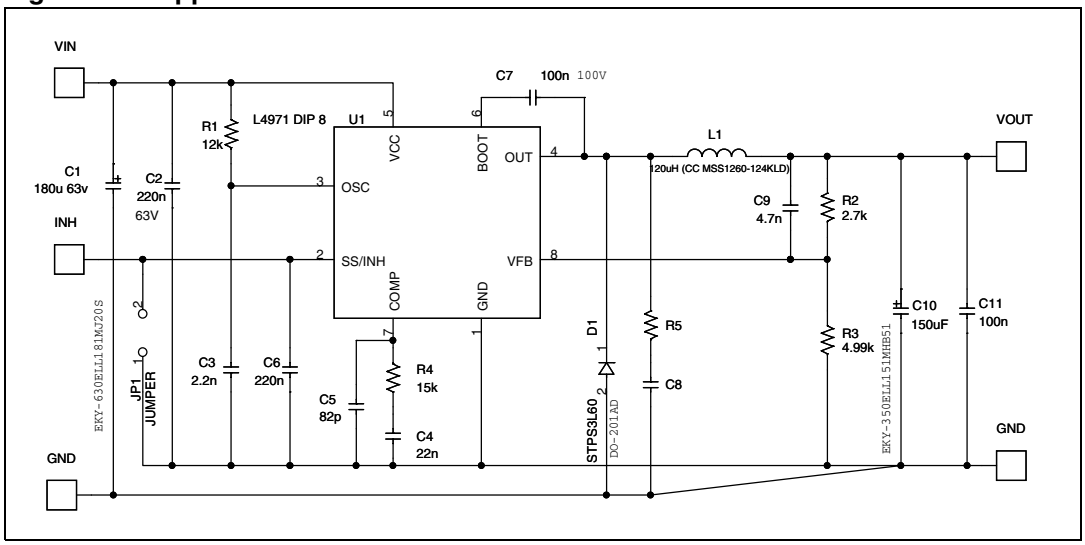
Figure 22 shows the typical application circuit, where the input supply voltage, Vcc, can range from 8 to 55 V operating, and the output voltage adjustable from 3.3 V to 40 V.

The selected components, and in particular input and output capacitors, are able to sustain the device voltage ratings, and the corresponding RMS currents.

3.1 Electrical specification

- Input voltage range: 8 V - 55 V
- Output voltage: 5.1 V ±3% (Line, load and thermal)
- Output ripple: 51 mV
- Output current range: 1 mA - 1.5 A
- Max output ripple current: 30% Iomax
- Max output current: 1.5 A
- Switching frequency: 200 kHz

Figure 21. Application circuit



3.2 Input capacitor

The input capacitor has to be able to support the max input operating voltage of the device and the max rms input current. The input current is squared and the quality of these capacitors has to be very high to minimize its power dissipation generated by the internal ESR, improving the system reliability. Moreover, input capacitors are also affecting the system efficiency.

The max Irms current flowing through the input capacitors is:

$$I_{rms} = I_O \cdot \sqrt{D - \frac{2 \cdot D^2}{\eta} + \frac{D^2}{\eta^2}}$$

where η is the expected system efficiency, D is the duty cycle and Io the output dc current.

This function reaches the maximum value at D = 0.5 and the equivalent rms current is equal to Io/2. The following diagram *Figure 23* is the graphical representation of the above equation, with an estimated efficiency of 85%, at different output currents.

The maximum and minimum duty cycles are:

$$D_{max} = \frac{V_O + V_f}{V_{ccmin} + V_f} = 0.66 \qquad D_{max} = \frac{V_O + V_f}{V_{ccmax} + V_f} = 0.1$$

where Vf is the freewheeling diode forward voltage. This formula is not taking into account the power MOS Rdson, considering negligible the inherent voltage drop, respect input and output voltages. At full load, 1.5 A, and D=0.5, the rms capacitor current to be sustained is of 0.75 A.

The selected 180 µF/63 V KY, guarantying a life time of 10000 hours at an ambient temperature of 105°C and switching frequency of 100 kHz, can support 1.15 A RMS current.

Figure 22. Efficiency vs. output current

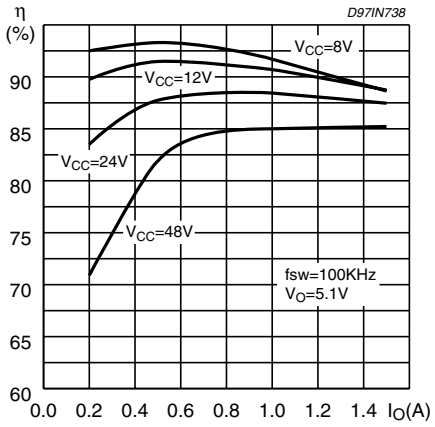
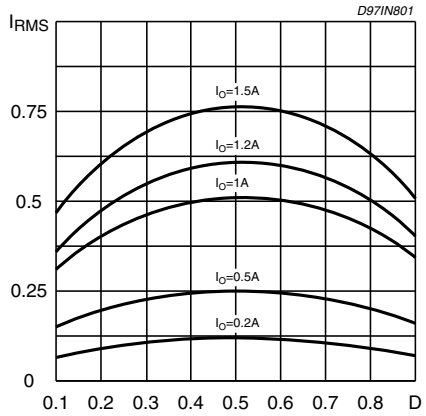


Figure 23. Input capacitance rms current vs. duty cycle



3.3 Output voltage selection

An external voltage divider is required to set the regulated output voltage: I

$$V_o = V_{REF} \cdot \left(1 + \frac{R2}{R3}\right)$$

where V_{REF} is 3.3 V

3.4 Inductor selection

The criteria used in fixing the inductor value has been dictated by the wanted output ripple voltage, 51mV max., performance obtained of course in combination with output capacitors too.

The inductor ripple current, fixed at 30% of Iomax, i.e., 0.45 A, requires an inductor value of:

Equation 1

$$L_O = V_O \cdot \frac{(1 - D_{min})}{\Delta I_L \cdot f_{sw}}$$

It is possible to plot as a function of Vo and Vccmax at 150 kHz and 200 kHz (see *Figure 24* and *Figure 25*)

Figure 24. Ideal inductor value requested for 30% ripple current, as a function of max. input voltage and output (f_{SW}=150 kHz)

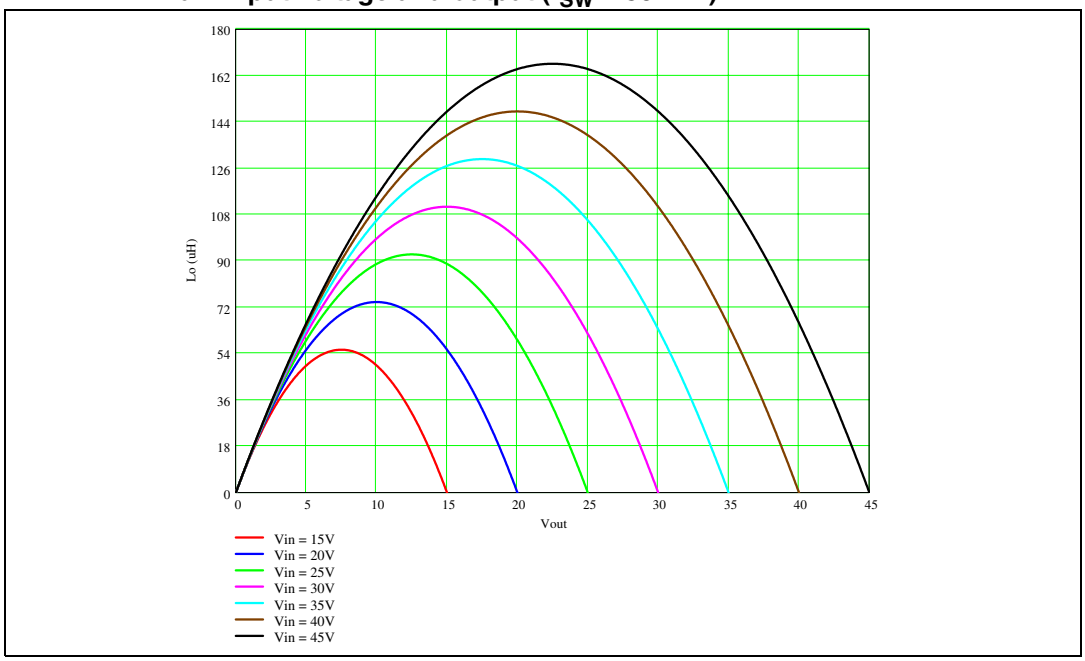
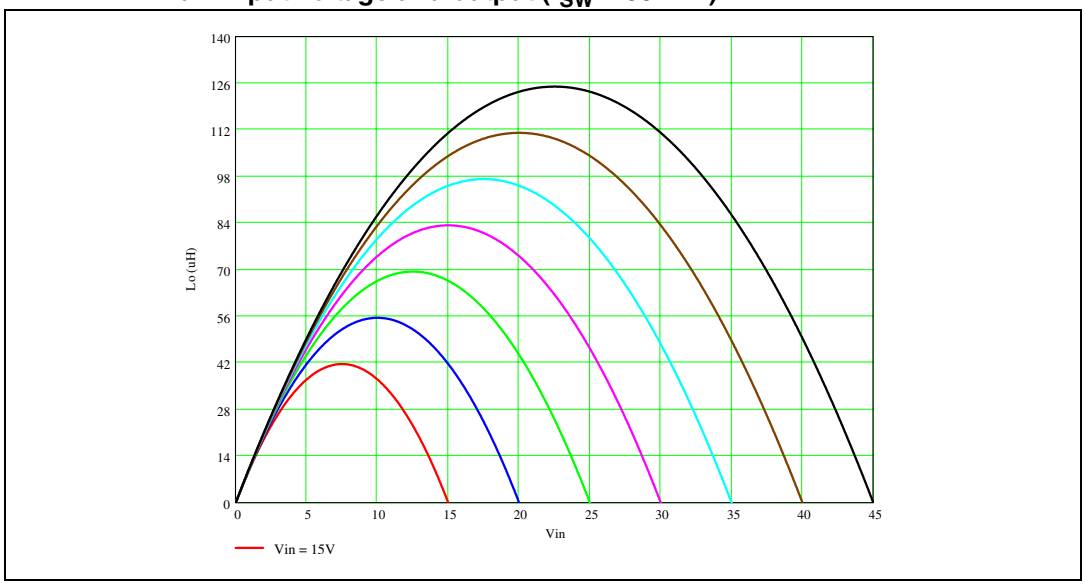


Figure 25. Ideal inductor value requested for 30% ripple current, as a function of max. input voltage and output (f_{SW}=200 kHz)



The 120 µH value of the selected inductor is useful to keep the current ripple below 0.3*I_{LOAD} over the input / output voltage range operating at 200 kHz.

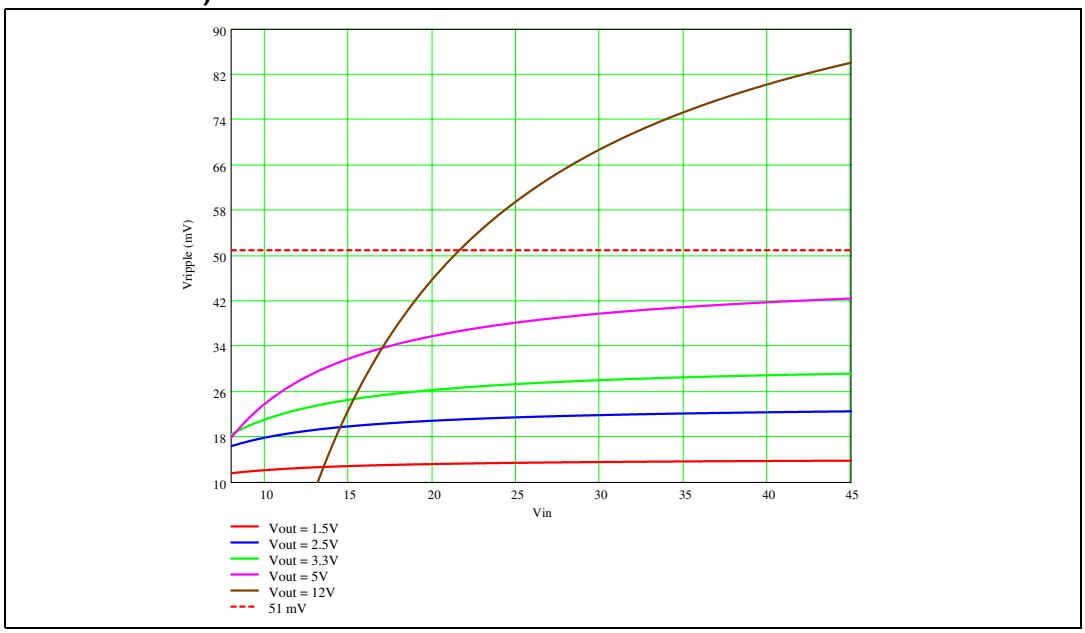
3.5 Output capacitors

The output capacitors selection, Co, is mainly driven by the output ripple voltage that has to be guaranteed, in this case 1% max. of Vo.

The output ripple is defined by the ESR of Co and by the ripple current flowing through it.

The output capacitance is of 150 µF/35 V KY (Nippon Chemi-con), having an ESR of 150 mΩ at 20 °C. The ideal ripple voltage over the input voltage range is shown in *Figure 26*.

Figure 26. Ideal ripple voltage as a function of input and output voltage (f_{SW}=200 kHz)



Co has also to support load transients. An idea of the magnitude of the output voltage drop during load transients is given below:

Equation 2

$$\Delta V_O = \frac{(\Delta I_O)^2 \cdot L_O}{2 \cdot C_O \cdot (V_{inmin} \cdot D_{max} - V_O)}$$

where ΔI_o is the load current change, from 0.5 A to 1.5 A, Dmax is the max. duty cycle, 95%, Vo nominal is 5.1 V, and finally L is 68 µH.

Equation 2, normalized at Vo, is represented in the following diagram, Fig. 27, as a function of the minimum input voltage.

These curves are represented for different output capacitor 2x150 µF, 2x220 µF, 2x330 µF all KY, 35 V.

3.6 Compensation network

The complete control loop block diagram is shown in *Figure 29*. The error amplifier basic characteristics are:

gm = 2.5mS

Ro = 1.2MΩ

Avo = 60dB

Isource/sink = 300 µA

Figure 27. Output drop (%) vs minimum input voltage

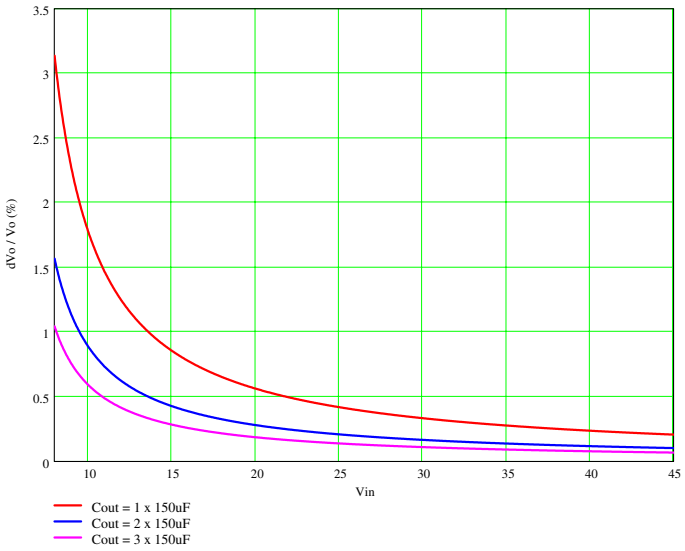
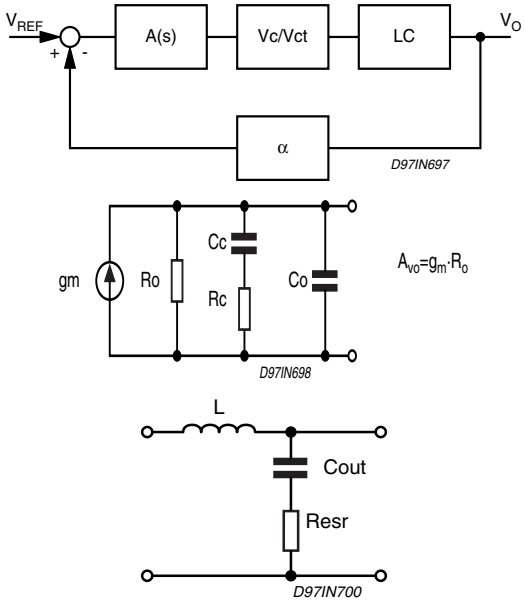


Figure 28. Block diagram compensation loop



3.7 Error amplifier and compensation blocks

The open loop gain is:

$$A(s) = gm \cdot \frac{R_O \cdot (1 + s \cdot R_c \cdot C_c)}{s^2 \cdot R_o \cdot C_o \cdot R_c \cdot C_c + s \cdot (R_o \cdot C_c + R_o \cdot C_o + R_c \cdot C_c) + 1}$$

where Cout is the parallel between the output and the external capacitance of the Error Amplifier and Ro the E/A output impedance. Rc and Cc are the compensation values.

3.8 LC filter

$$A_{o(s)} = \frac{1 + R_{esr} \cdot C_{out} \cdot s}{L \cdot C_{out} \cdot s^2 + R_{esr} \cdot s + 1}$$

3.9 PWM gain

$$\frac{V_{CC}}{V_{ct}} = \frac{V_{CC} \cdot 6}{V_{CC} - 1} \approx 6$$

where Vct is the peak to peak sawtooth oscillator.

3.10 Voltage divider and leading network

$$A_{o(s)} = \frac{R_3}{R_2 + R_3} \cdot \frac{1 + R_2 \cdot C_9}{1 + s \cdot \frac{R_2 \cdot R_3}{R_2 + R_3} \cdot C_9}$$

Poles and zeros value are:

$$F_o = \frac{1}{2 \cdot \pi R_{esr} \cdot C_{out}} = \frac{1}{2 \cdot \pi \cdot 0.130 \cdot 150 \cdot 10^{-6}} = 8.2KHz$$

$$F_p = \frac{1}{2 \cdot \pi \cdot \sqrt{L \cdot C_{out}}} = \frac{1}{2 \cdot \pi \cdot \sqrt{120 \cdot 10^{-6} \cdot 150 \cdot 10^{-6}}} = 1.2kHz$$

$$F_{ocomp} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_c} = \frac{1}{2 \cdot \pi \cdot 15 \cdot 10^3 \cdot 22 \cdot 10^{-9}} = 492Hz$$

$$F_{p1} = \frac{1}{2 \cdot \pi \cdot R_o \cdot C_c} = \frac{1}{2 \cdot \pi \cdot 1.2 \cdot 10^{6} \cdot 22 \cdot 10^{-9}} = 6.029Hz$$

$$F_{p2} = \frac{1}{2 \cdot \pi \cdot R_c \cdot C_o} = \frac{1}{2 \cdot \pi \cdot 15 \cdot 10^{3} \cdot 82 \cdot 10^{-12}} = 125KHz$$

$$F_{oLN} = \frac{1}{2 \cdot \pi \cdot R_2 \cdot C_9} = \frac{1}{2 \cdot \pi \cdot 2.7 \cdot 10^{3} \cdot 4.7 \cdot 10^{-9}} = 12KHz$$

$$F_{pLN} = \frac{1}{2 \cdot \pi \cdot \frac{R_2 \cdot R_3}{R_2 + R_3} \cdot C_9} = \frac{1}{2 \cdot \pi \cdot 1.75 \cdot 10^{3} \cdot 4.7 \cdot 10^{-9}} = 19KHz$$

Using a compensation network with R4= 15 kΩ, C4 = 22 nF and C5 = 82 pF, the gain and Phase Bode plots are shown in Fig. 31-32. The cut-off frequency and the phase margin are:

V_{OUT} = 3.3V	Fc = 36KHz	Phase margin = 62°
V_{OUT} = 5V	Fc = 34KHz	Phase margin = 70°
V_{OUT} = 12V	Fc = 18KHz	Phase margin = 92°
V_{OUT} = 15V	Fc = 14KHz	Phase margin = 88°
V_{OUT} = 18V	Fc = 11KHz	Phase margin = 83°
V_{OUT} = 24V	Fc = 8.6KHz	Phase margin = 74°

Figure 29. Gain Bode plot open loop

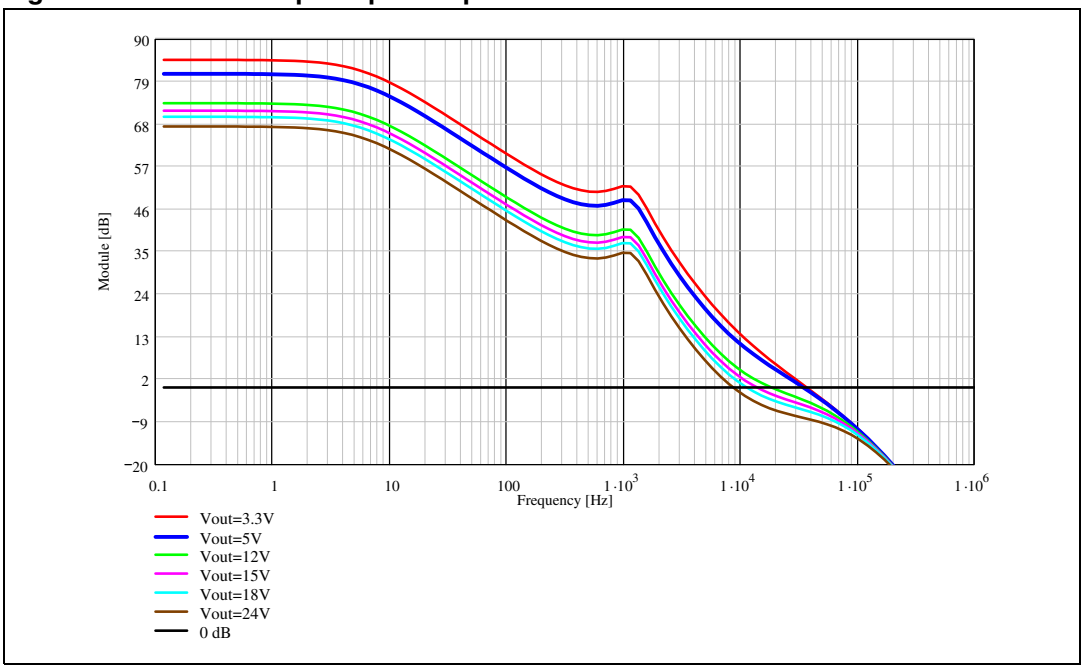


Figure 30. Phase Bode plot open loop

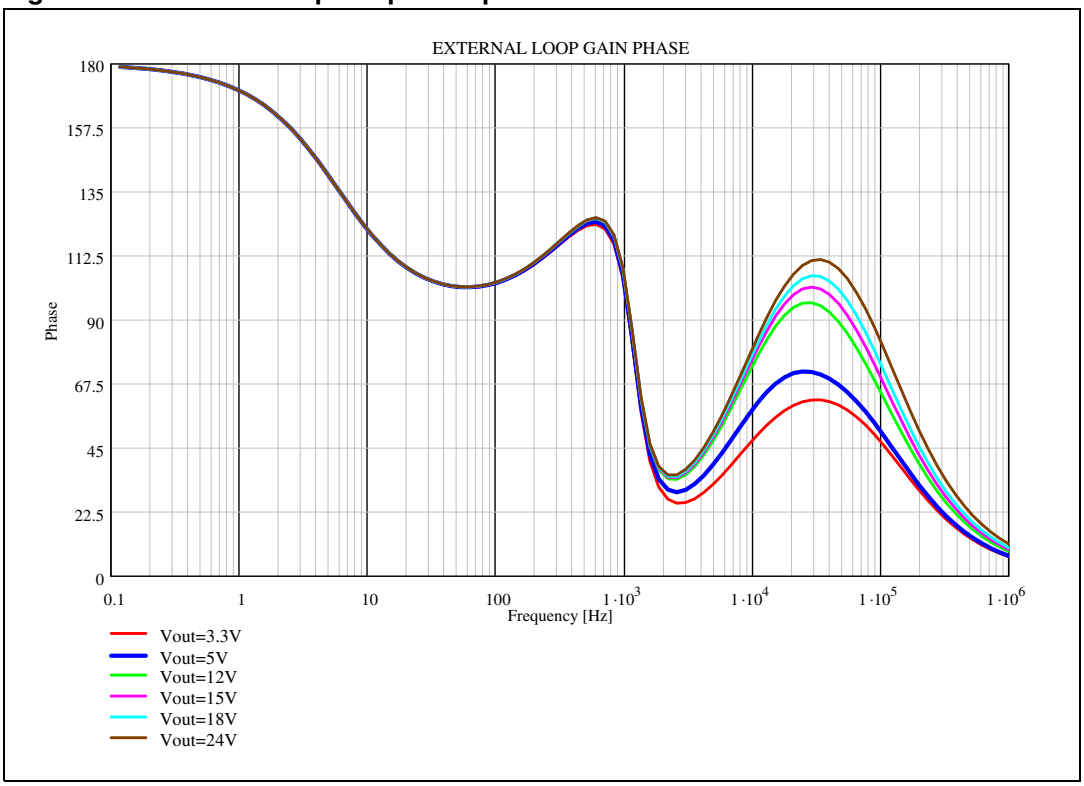


Table 1. Component list (fsw = 200 kHz, V_{OUT}= 5 V)

Reference	Description	Part number	Manufacturer
R1	Resistor 12 KΩ 1% 1/4W		
R2	Resistor 2.7 KΩ 1% 1/4W		
R3	Resistor 4.99 KΩ 1% 1/4W		
R4	Resistor 15 KΩ 1% 1/4W		
R5	Not mounted		
C1	Capacitor 180 µF 63V	EKY-630ELL181MJ20S	Nippon Chemi-con
C2 - C6	Capacitor 220 nF 63V		
C3	Capacitor 2.2 nF 100V		
C4	Capacitor 22 nF 50V		
C5	Capacitor 82 pF 50V		
C7 - C11	Capacitor 100 nF 100V		
C8	Not mounted		
C9	Capacitor 4.7 nF 50V		
C10	Capacitor 150 µF 35V	EKY-350ELL151MHB5D	Nippon Chemi-con
L1	120 µH I_{RMS} = 1.85A I_{SAT} = 1.92A	MSS1260-124KLD	Coilcraft
U1		L4971	STMicroelectronics

Table 2. Resistor divider for V_{OUT} =12 V

Reference	Description	Part number	Manufacturer
R2	Resistor 2.7 kΩ 1%		
R3	Resistor 1 kΩ 1%		

Table 3. Resistor divider for V_{OUT} =3.3 V

Reference	Description	Part number	Manufacturer
R2	RESISTOR 2.7 KΩ 1%		
R3	NOT MOUNTED		

Figure 31. Evaluation board (components side)

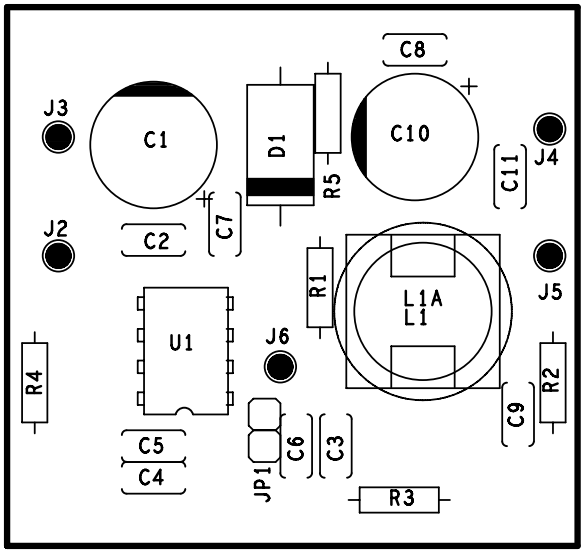


Figure 32. Evaluation board (bottom side)

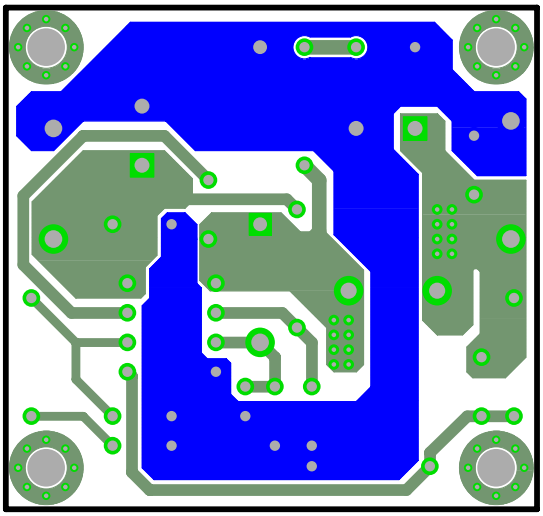
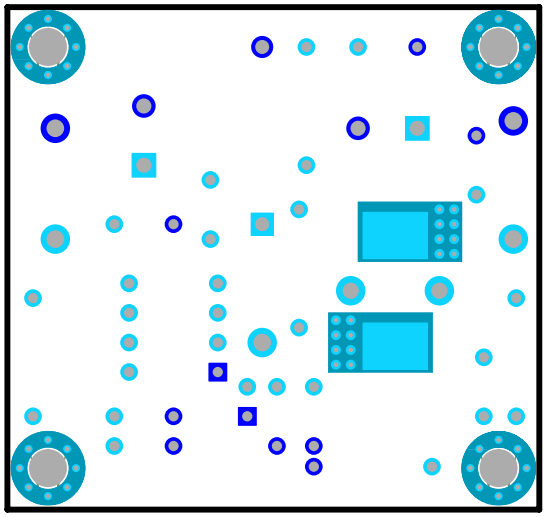


Figure 33. Evaluation board (top side)



4 Revision history

Table 4. Document revision history

Date	Revision	Changes
October 2004	13	First Issue in EDOCS
May 2005	14	Updated the Layout look & feel. Changed name of the D1 on the fig. 21
03-May-2011	15	Updated the evaluation board description

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