128Mbit DDR SDRAM

1M x 32Bit x 4 Banks
Double Data Rate Synchronous RAM
with Bi-directional Data Strobe and DLL

Revision 1.3

August 2001

Samsung Electronics reserves the right to change products or specification without notice.

Revision History

Revision 1.3 (August 2, 2001)

- Removed K4D263238M-QC40 with VDD&VDDQ=2.8V
- Changed VDD&VDDQ of K4D263238M-QC45 from 2.8V to 2.5V.
- Changed tCK(max) from 7ns to 10ns.

Revision 1.2 (July 12, 2001)

- Corrected CAS latency of K4D263238M-QC45 from CL3 to CL4
- The specification for the 222MHz/250MHz is preliminary one.

Revision 1.1 (March 5, 2000)

- Added K4D263238M-QC40 with VDD&VDDQ=2.8V
- Changed VDD/VDDQ of K4D263238M-QC45 from 2.5V to 2.8V. Accordingly, DC current characteristics values have been changed.
  - Changed CAS latency of K4D263238M-QC45 from CL4 to CL3.
- Changed tWPREH of K4D263238M-QC50 from 0.3tCK to 0.25tCK

Revision 1.0 (December 13, 2000)

• Defined capacitance values
• Chagned tRCDWR of K4D263238M-QC60 from 1tCK to 2tCK

Revision 0.5 (December 8, 2000)

• Changed AC input level from Vref ± 0.31V to Vref ± 0.35V
• Changed tRC/tRFC/tRAS/tRP/tRCDRD/tRCDWR from ns unit based from clock unit based.
• Changed V_{IN} /V_{OUT}/V_{DDQ} in absolute maximum ratings from -1.0V ~3.6V to -0.5V ~ 3.6V.

Revision 0.4 (November 29, 2000) - *Preliminary*

• Removed K4D263238M-QC40
• Several AC parameters of K4D263238M-QC45 have been changed
  - Changed tDQSQ from 0.4ns to 0.45ns. Changed tQH from tHP-0.6ns to tHP-0.45ns.
  - Changed tDQSCK & tAC from 0.6ns to 0.7ns
  - Changed tDQSS from 0.75tCK/1.25tCK to 0.8tCK/1.2tCK. Accordingly, changed tWPREH from 0.25tCK to 0.3tCK.
  - Changed tDS/tDH from 0.4ns to 0.45ns. Changed tIS/tIH from 0.9ns to 1.0ns
  - Corrected tDAL from 5tCK to 6tCK
• Several AC parameters of K4D263238M-QC50 have been changed
  - Changed tQH from tHP-0.6ns to tHP-0.45ns.
  - Changed tDQSCK & tAC from 0.6ns to 0.7ns
  - Changed tDQSS from 0.75tCK/1.25tCK to 0.8tCK/1.2tCK. Accordingly, changed tWPREH from 0.25tCK to 0.3tCK.
  - Corrected tDAL from 5tCK to 6tCK
• Several AC parameters of K4D263238M-QC55 have been changed
  - Changed tDQSQ from 0.45ns to 0.5ns. Changed tOH from tHP-0.6ns to tHP-0.5ns.
  - Changed tDQSCK & tAC from 0.6ns to 0.75ns
  - Changed tDS/tDH from 0.45ns to 0.5ns. Changed tIS/tIH from 1.0ns to 1.1ns
  - Changed tRC/tRFC from 60.5ns/71.5ns to 66ns/77ns. Changed tRP from 16.5ns to 22ns.
  - Corrected tRCDWR from 5.5ns to 11ns. Corrected tDAL from 5tCK to 6tCK
• Changed tQH of K4D263238M-QC60 from tHP-0.75ns to tHP-0.5ns
• Add DC Characteristics value
• Define V_{IH}(max) / V_{IL}(min) as a note in Power & DC operating Condition table
• Changed refresh cycle time from 16ms to 32ms.Accordingly, tREF has been changed from 3.9us to 7.8us.
• Changed I_{IL},I_{OL} test condition from 0V≤ V_{IN} ≤V_{DD}+0.3V to 0V≤ V_{IN} ≤V_{DD}.

Revision 0.3 (June 8, 2000)

• Removed Block Write function

Revision 0.2 (April 10, 2000)

• Separated tRCD into tRCDRD and tRCDWR
  - tRCDRD: Row to Column delay for READ
  - tRCDWR: Row to Column delay at WRITE

Revision 0.1 (March 16, 2000)

• Define the spec based on Vdd&Vddq=2.5V
• Maximum target frequency upto 250MHz@CL4
• Removed Write Interrupt by Read function

Revision 0.0 (December 27, 1999) - *Target Spec*

• Defined Target Specification

1M x 32Bit x 4 Banks Double Data Rate Synchronous RAM with Bi-directional Data Strobe and DLL

FEATURES

- 2.5V ± 5% power supply
- SSTL_2 compatible inputs/outputs
- 4 banks operation
- MRS cycle with address key programs
  - -. Read latency 3,4 (clock)
  - -. Burst length (2, 4, 8 and Full page)
  - -. Burst type (sequential & interleave)
- Full page burst length for sequential burst type only
- Start address of the full page burst should be even
- All inputs except data & DM are sampled at the positive going edge of the system clock
- Differential clock input
- No Write Interrupted by Read function
- Data I/O transactions on both edges of Data strobe
- DLL aligns DQ and DQS transitions with Clock transition
- Edge aligned data & data strobe output
- Center aligned data & data strobe input
- DM for write masking only
- Auto & Self refresh
- 32ms refresh period (4K cycle)
- 100pin TQFP package
- Maximum clock frequency up to 222MHz
- Maximum data rate up to 444Mbps/pin

ORDERING INFORMATION

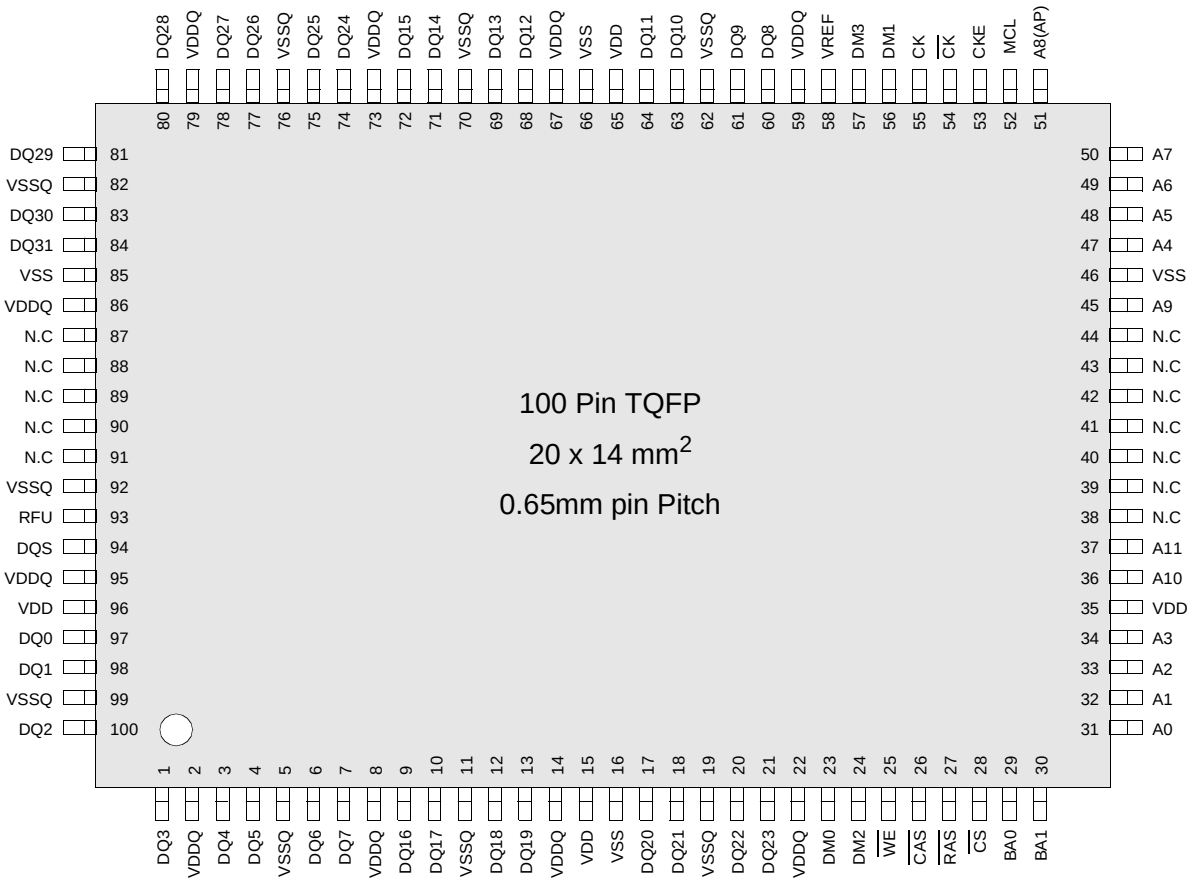
Part NO.	Max Freq.	Max Data Rate	Interface	Package
K4D263238M-QC45	222MHz	444Mbps/pin	SSTL_2	100 TQFP
K4D263238M-QC50	200MHz	400Mbps/pin		
K4D263238M-QC55	183MHz	366Mbps/pin		
K4D263238M-QC60	166MHz	333Mbps/pin		

GENERAL DESCRIPTION

FOR 1M x 32Bit x 4 Bank DDR SDRAM

The K4D263238 is 134,217,728 bits of hyper synchronous data rate Dynamic RAM organized as 4 x 1,048,576 words by 32 bits, fabricated with SAMSUNG′s high performance CMOS technology. Synchronous features with Data Strobe allow extremely high performance up to 1.8GB/s/chip. I/O transactions are possible on both edges of the clock cycle. Range of operating frequencies, programmable burst length and programmable latencies allow the device to be useful for a variety of high performance memory system applications.

PIN CONFIGURATION (Top View)



PIN DESCRIPTION

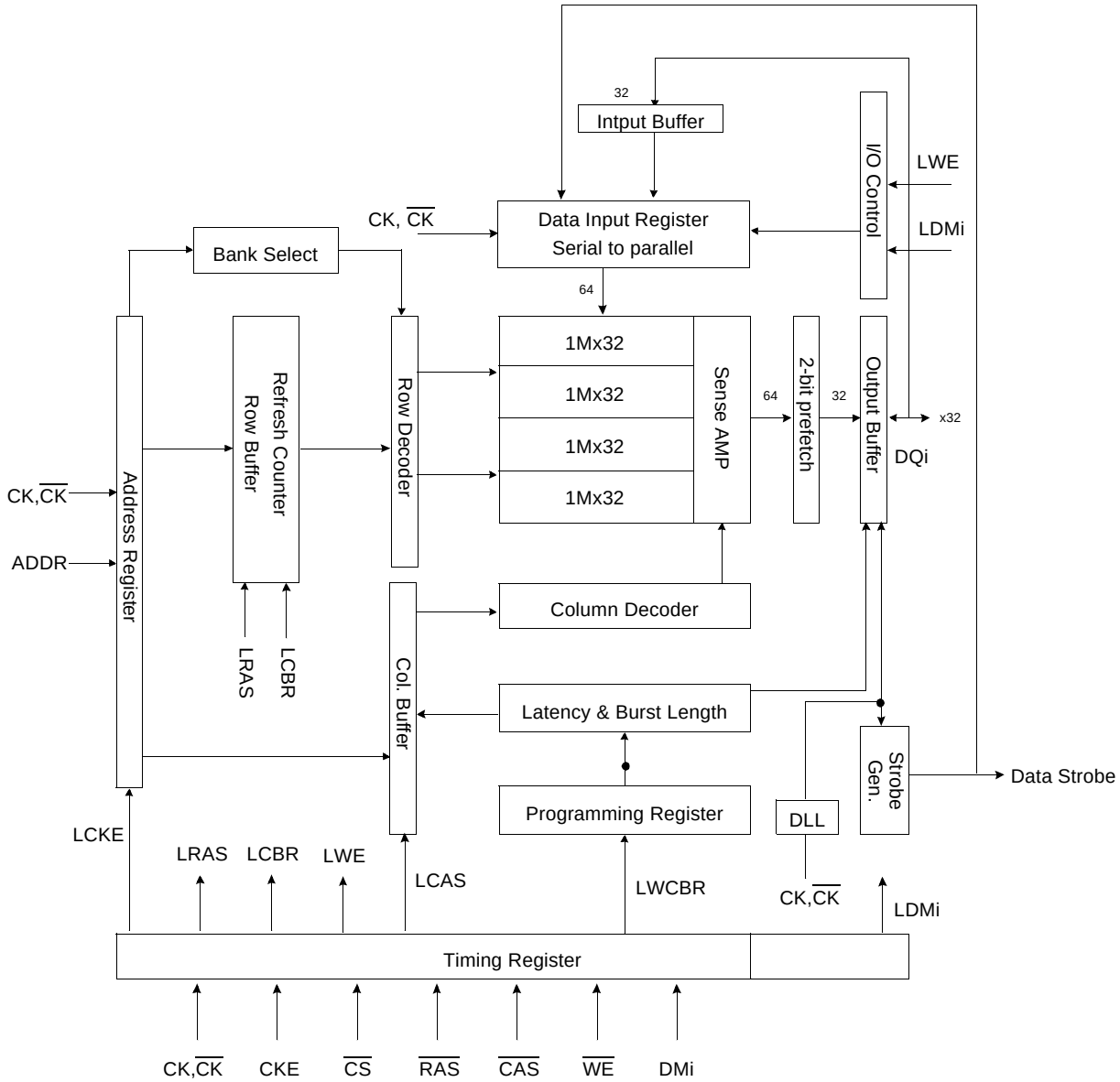
CK,$\overline{CK}$	Differential Clock Input	BA_0, BA_1	Bank Select Address
CKE	Clock Enable	A_0 ~A_{11}	Address Input
$\overline{CS}$	Chip Select	DQ_0 ~ DQ_{31}	Data Input/Output
$\overline{RAS}$	Row Address Strobe	V_{DD}	Power
$\overline{CAS}$	Column Address Strobe	V_{SS}	Ground
$\overline{WE}$	Write Enable	V_{DDQ}	Power for DQ′s
DQS	Data Strobe	V_{SSQ}	Ground for DQ′s
DMi	Data Mask	MCL	Must Connect Low
RFU	Reserved for Future Use		

INPUT/OUTPUT FUNCTIONAL DESCRIPTION

Symbol	Type	Function
CK, $\overline{CK}$*1	Input	The differential system clock Input. All of the inputs are sampled on the rising edge of the clock except DQ′s and DM′s that are sampled on both edges of the DQS.
CKE	Input	Activates the CK signal when high and deactivates the CK signal when low. By deactivating the clock, CKE low indicates the Power down mode or Self refresh mode.
$\overline{CS}$	Input	$\overline{CS}$ enables the command decoder when low and disabled the command decoder when high. When the command decoder is disabled, new commands are ignored but previous operations continue.
$\overline{RAS}$	Input	Latches row addresses on the positive going edge of the CK with $\overline{RAS}$ low. Enables row access & precharge.
$\overline{CAS}$	Input	Latches column addresses on the positive going edge of the CK with $\overline{CAS}$ low. Enables column access.
$\overline{WE}$	Input	Enables write operation and row precharge. Latches data in starting from $\overline{CAS}$, $\overline{WE}$ active.
DQS	Input/Output	Data input and output are synchronized with both edge of DQS.
DM_0 ~ DM_3	Input	Data In mask. Data In is masked by DM Latency=0 when DM is high in burst write. DM_0 for DQ_0 ~ DQ_7, DM_1 for DQ_8 ~ DQ_{15}, DM_2 for DQ_{16} ~ DQ_{23}, DM_3 for DQ_{24} ~ DQ_{31}.
DQ_0 ~ DQ_{31}	Input/Output	Data inputs/Outputs are multiplexed on the same pins.
BA_0, BA_1	Input	Selects which bank is to be active.
A_0 ~ A_{11}	Input	Row/Column addresses are multiplexed on the same pins. Row addresses : RA_0 ~ RA_{11}, Column addresses : CA_0 ~ CA_7. Column address CA_8 is used for auto precharge.
V_{DD}/V_{SS}	Power Supply	Power and ground for the input buffers and core logic.
V_{DDQ}/V_{SSQ}	Power Supply	Isolated power supply and ground for the output buffers to provide improved noise immunity.
V_{REF}	Power Supply	Reference voltage for inputs, used for SSTL interface.
MCL	Must Connect Low	Must connect Low

*1 : The timing reference point for the differential clocking is the cross point of CK and $\overline{CK}$.
For any applications using the single ended clocking, apply V_{REF} to $\overline{CK}$ pin.

BLOCK DIAGRAM (1Mbit x 32I/O x 4 Bank)



FUNCTIONAL DESCRIPTION

• Power-Up Sequence

DDR SDRAMs must be powered up and initialized in a predefined manner to prevent undefined operations.

1. Apply power and keep CKE at low state (All other inputs may be undefined)
   - Apply VDD before VDDQ .
   - Apply VDDQ before VREF & VTT
2. Start clock and maintain stable condition for minimum 200us.
3. The minimum of 200us after stable power and clock(CK,$\overline{CK}$), apply NOP and take CKE to be high.
4. Issue precharge command for all banks of the device.
5. Issue a EMRS command to enable DLL

*1 6. Issue a MRS command to reset DLL. The additional 200 clock cycles are required to lock the DLL.

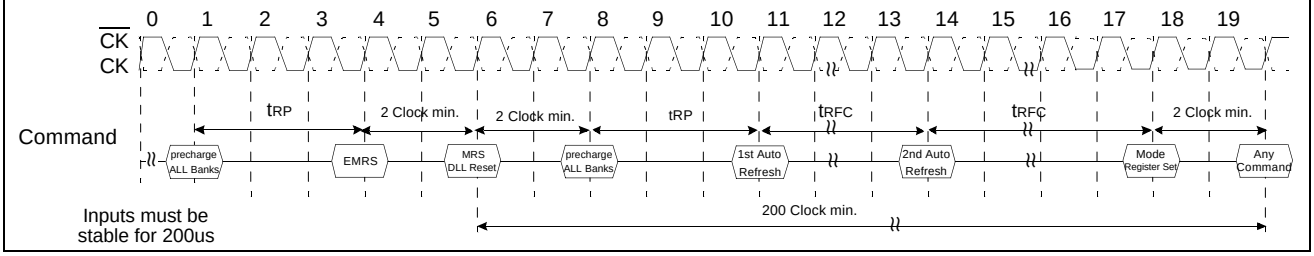
*1,2 7. Issue precharge command for all banks of the device.

8. Issue at least 2 or more auto-refresh commands.
9. Issue a mode register set command with A8 to low to initialize the mode register.

*1 The additional 200cycles of clock input is required to lock the DLL after enabling DLL.

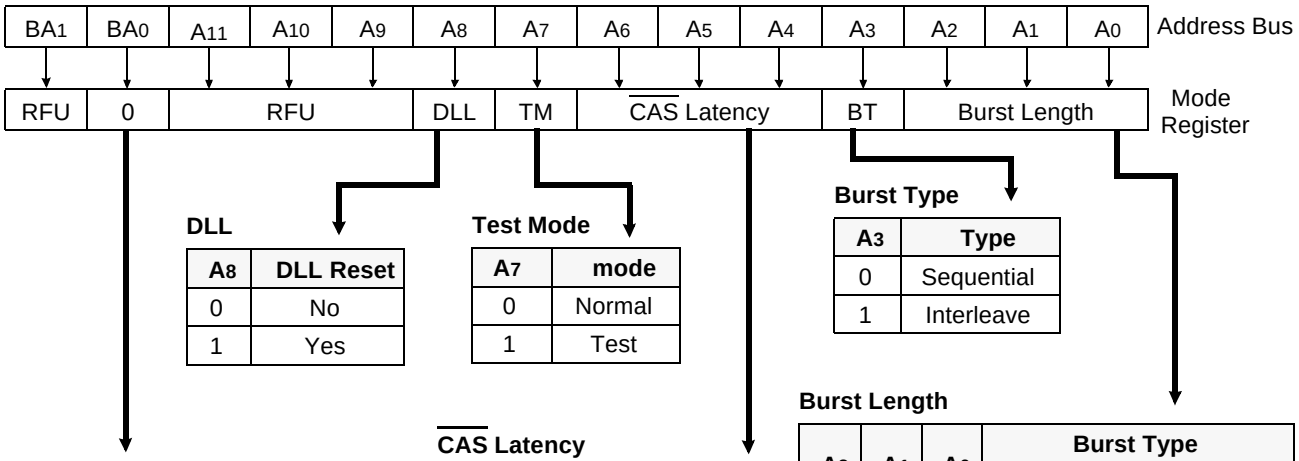
*2 Sequence of 6&7 is regardless of the order.

Power up & Initialization Sequence



MODE REGISTER SET(MRS)

The mode register stores the data for controlling the various operating modes of DDR SDRAM. It programs $\overline{CAS}$ latency, addressing mode, burst length, test mode, DLL reset and various vendor specific options to make DDR SDRAM useful for variety of different applications. The default value of the mode register is not defined, therefore the mode register must be written after EMRS setting for proper operation. The mode register is written by asserting low on $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$(The DDR SDRAM should be in active mode with CKE already high prior to writing into the mode register). The state of address pins A_0 ~ A_{11} and BA_0, BA_1 in the same cycle as $\overline{CS}$, $\overline{RAS}$, $\overline{CAS}$ and $\overline{WE}$ going low is written in the mode register. Minimum two clock cycles are requested to complete the write operation in the mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. The mode register is divided into various fields depending on functionality. The burst length uses A_0 ~ A_2, addressing mode uses A_3, $\overline{CAS}$ latency(read latency from column address) uses A_4 ~ A_6. A_7 is used for test mode. A_8 is used for DLL reset. A_7,A_8, BA_0 and BA_1 must be set to low for normal MRS operation. Refer to the table for specific codes for various burst length, addressing modes and $\overline{CAS}$ latencies.



DLL

A_8	DLL Reset
0	No
1	Yes

Test Mode

A_7	mode
0	Normal
1	Test

Burst Type

A_3	Type
0	Sequential
1	Interleave

BA_0	A_n ~ A_0
0	MRS
1	EMRS

* RFU(Reserved for future use) should stay "0" during MRS cycle.

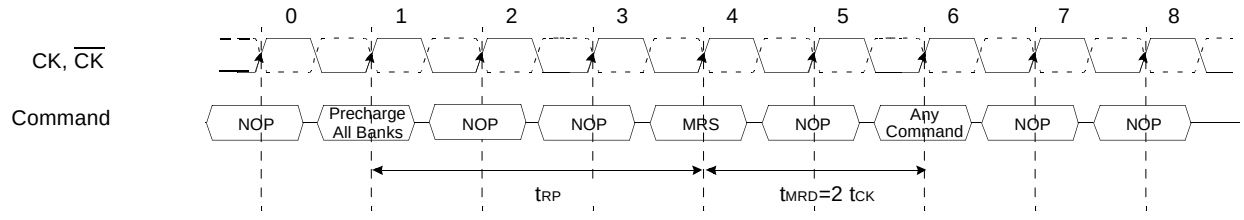
$\overline{CAS}$ Latency

A_6	A_5	A_4	Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	Reserved
0	1	1	3
1	0	0	4
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

Burst Length

A_2	A_1	A_0	Burst Type	
			Sequential	Interleave
0	0	0	Reserve	Reserve
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserve	Reserve
1	0	1	Reserve	Reserve
1	1	0	Reserve	Reserve
1	1	1	Full page	Reserve

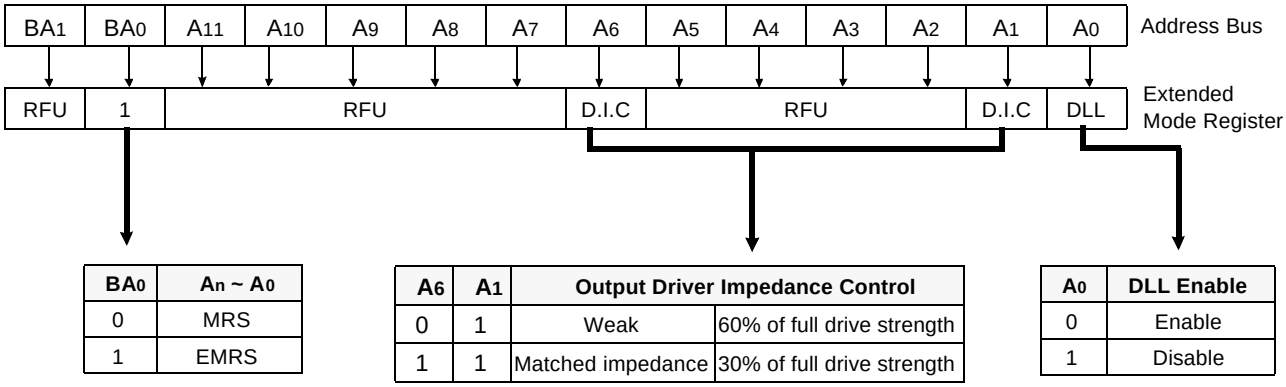
MRS Cycle



*1: MRS can be issued only at all banks precharge state.
*2: Minimum t_{RP} is required to issue MRS command.

EXTENDED MODE REGISTER SET(EMRS)

The extended mode register stores the data for enabling or disabling DLL and selecting output driver strength. The default value of the extended mode register is not defined, therefore the extend mode register must be written after power up for enabling or disabling DLL. The extended mode register is written by asserting low on CS, RAS, CAS, WE and high on BA0(The DDR SDRAM should be in all bank precharge with CKE already high prior to writing into the extended mode register). The state of address pins A0, A2 ~ A5, A7 ~ A11 and BA1 in the same cycle as CS, RAS, CAS and WE going low are written in the extended mode register. A1 and A6 are used for setting driver strength to weak or matched impedance. Two clock cycles are required to complete the write operation in the extended mode register. The mode register contents can be changed using the same command and clock cycle requirements during operation as long as all banks are in the idle state. A0 is used for DLL enable or disable. "High" on BA0 is used for EMRS. All the other address pins except A0,A1,A6 and BA0 must be set to low for proper EMRS operation. Refer to the table for specific codes.



BA_0	A_n ~ A_0
0	MRS
1	EMRS

A_6	A_1	Output Driver Impedance Control	
0	1	Weak	60% of full drive strength
1	1	Matched impedance	30% of full drive strength

A_0	DLL Enable
0	Enable
1	Disable

* RFU(Reserved for future use) should stay "0" during EMRS cycle.

Figure 7. Extend Mode Register set

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Voltage on any pin relative to Vss	V_{IN}, V_{OUT}	-0.5 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DD}	-1.0 ~ 3.6	V
Voltage on V_{DD} supply relative to Vss	V_{DDQ}	-0.5 ~ 3.6	V
Storage temperature	T_{STG}	-55 ~ +150	°C
Power dissipation	P_D	2.0	W
Short circuit current	I_{OS}	50	mA

Note : Permanent device damage may occur if ABSOLUTE MAXIMUM RATINGS are exceeded.
Functional operation should be restricted to recommended operating condition.
Exposure to higher than recommended voltage for extended periods of time could affect device reliability.

POWER & DC OPERATING CONDITIONS(SSTL_2 In/Out)

Recommended operating conditions(Voltage referenced to V_{SS}=0V, T_A=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Device Supply voltage	V_{DD}	2.375	2.50	2.625	V	1
Output Supply voltage	V_{DDQ}	2.375	2.50	2.625	V	1
Reference voltage	V_{REF}	0.49*V_{DDQ}	-	0.51*V_{DDQ}	V	2
Termination voltage	Vtt	V_{REF}-0.04	V_{REF}	V_{REF}+0.04	V	3
Input logic high voltage	V_{IH}	V_{REF}+0.15	-	V_{DDQ}+0.30	V	4
Input logic low voltage	V_{IL}	-0.30	-	V_{REF}-0.15	V	5
Output logic high voltage	V_{OH}	Vtt+0.76	-	-	V	I_{OH}=-15.2mA
Output logic low voltage	V_{OL}	-	-	Vtt-0.76	V	I_{OL}=+15.2mA
Input leakage current	I_{IL}	-5	-	5	uA	6
Output leakage current	I_{OL}	-5	-	5	uA	6

Note : 1. Under all conditions V_{DDQ} must be less than or equal to V_{DD}.
2. V_{REF} is expected to equal 0.50*V_{DDQ} of the transmitting device and to track variations in the DC level of the same. Peak to peak noise on the V_{REF} may not exceed ± 2% of the DC value. Thus, from 0.50*V_{DDQ}, V_{REF} is allowed ± 25mV for DC error and an additional ± 25mV for AC noise.
3. V_{tt} of the transmitting device must track V_{REF} of the receiving device.
4. V_{IH}(max.)= V_{DDQ} +1.5V for a pulse and it which can not be greater than 1/3 of the cycle rate.
5. V_{IL}(min.)= -1.5V for a pulse width and it can not be greater than 1/3 of the cycle rate.
6. For any pin under test input of 0V ≤ V_{IN} ≤ V_{DD} is acceptable. For all other pins that are not under test V_{IN}=0V.

DC CHARACTERISTICS

Recommended operating conditions Unless Otherwise Noted, T_A=0 to 65°C)

Parameter	Sym-bol	Test Condition	Version				Unit	Note
			-45*	-50	-55	-60		
Operating Current (One Bank Active)	I_{CC1}	Burst Lenth=2 $t_{RC} \geq t_{RC}$(min) I_{OL}=0mA, t_{CC}= t_{CC}(min)	310	260	260	260	mA	1
Precharge Standby Current in Power-down mode	I_{CC2P}	CKE ≤ V_{IL}(max), t_{CC}= t_{CC}(min)	90	80			mA	
Precharge Standby Current in Non Power-down mode	I_{CC2N}	CKE ≥ V_{IH}(min), $\overline{CS}$ ≥ V_{IH}(min), t_{CC}= t_{CC}(min).	155	135	130	125	mA	
Active Standby Current power-down mode	I_{CC3P}	CKE ≤ V_{IL}(max), t_{CC}= t_{CC}(min)	105	95			mA	
Active Standby Current in in Non Power-down mode	I_{CC3N}	CKE ≥ VIH(min), $\overline{CS}$ ≥ VIH(min), t_{CC}= t_{CC}(min) .	190	160	150	140	mA	
Operating Current (Burst Mode)	I_{CC4}	I_{OL}=0mA ,t_{CC}= t_{CC}(min), Page Burst, All Banks activated.	660	550	500	460	mA	
Refresh Current	I_{CC5}	$t_{RC} \geq t_{RFC}$(min)	380	330	320	320	mA	2
Self Refresh Current	I_{CC6}	CKE ≤ 0.2V	5	4			mA	

Note: 1. Measured with outputs open.
2. Refresh period is 32ms.

AC INPUT OPERATING CONDITIONS

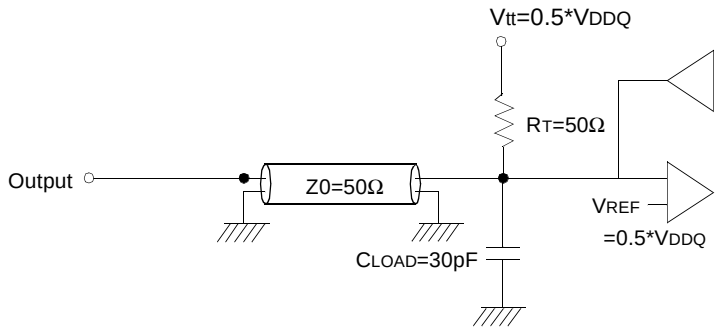
Recommended operating conditions(Voltage referenced to V_{SS}=0V, V_{DD}/ V_{DDQ}=2.5V± 5%, T_A=0 to 65°C)

Parameter	Symbol	Min	Typ	Max	Unit	Note
Input High (Logic 1) Voltage; DQ	V_{IH}	V_{REF}+0.35	-	-	V	
Input Low (Logic 0) Voltage; DQ	V_{IL}	-	-	V_{REF}-0.35	V	
Clock Input Differential Voltage; CK and $\overline{CK}$	V_{ID}	0.7	-	V_{DDQ}+0.6	V	1
Clock Input Crossing Point Voltage; CK and $\overline{CK}$	V_{IX}	0.5*V_{DDQ}-0.2	-	0.5*V_{DDQ}+0.2	V	2

Note : 1. V_{ID} is the magnitude of the difference between the input level on CK and the input level on $\overline{CK}$
2. The value of V_{IX} is expected to equal 0.5*V_{DDQ} of the transmitting device and must track variations in the DC level of the same

AC OPERATING TEST CONDITIONS (V_{DD}/ V_{DDQ}=2.5V± 5% , T_A= 0 to 65°C)

Parameter	Value	Unit	Note
Input reference voltage for CK(for single ended)	0.50*V_{DDQ}	V	
CK and $\overline{CK}$ signal maximum peak swing	1.5	V	
CK signal minimum slew rate	1.0	V/ns	
Input Levels(V_{IH}/V_{IL})	V_{REF}+0.35/V_{REF}-0.35	V	
Input timing measurement reference level	V_{REF}	V	
Output timing measurement reference level	V_{tt}	V	
Output load condition	See Fig.1		



(Fig. 1) Output Load Circuit

CAPACITANCE (V_{DD}=2.5V, T_A= 25°C, f=1MHz)

Parameter	Symbol	Min	Max	Unit
Input capacitance(CK, $\overline{CK}$)	C_{IN1}	1.0	5.0	pF
Input capacitance(A_0~A_{10}, BA_0~BA_1)	C_{IN2}	1.0	4.0	pF
Input capacitance (CKE, $\overline{CS}$, $\overline{RAS}$,$\overline{CAS}$, $\overline{WE}$)	C_{IN3}	1.0	4.0	pF
Data & DQS input/output capacitance(DQ_0~DQ_{31})	C_{OUT}	1.0	6.0	pF
Input capacitance(DM0 ~ DM3)	C_{IN4}	1.0	6.0	pF

DECOUPLING CAPACITANCE GUIDE LINE

Recommended decoupling capacitance added to power line at board.

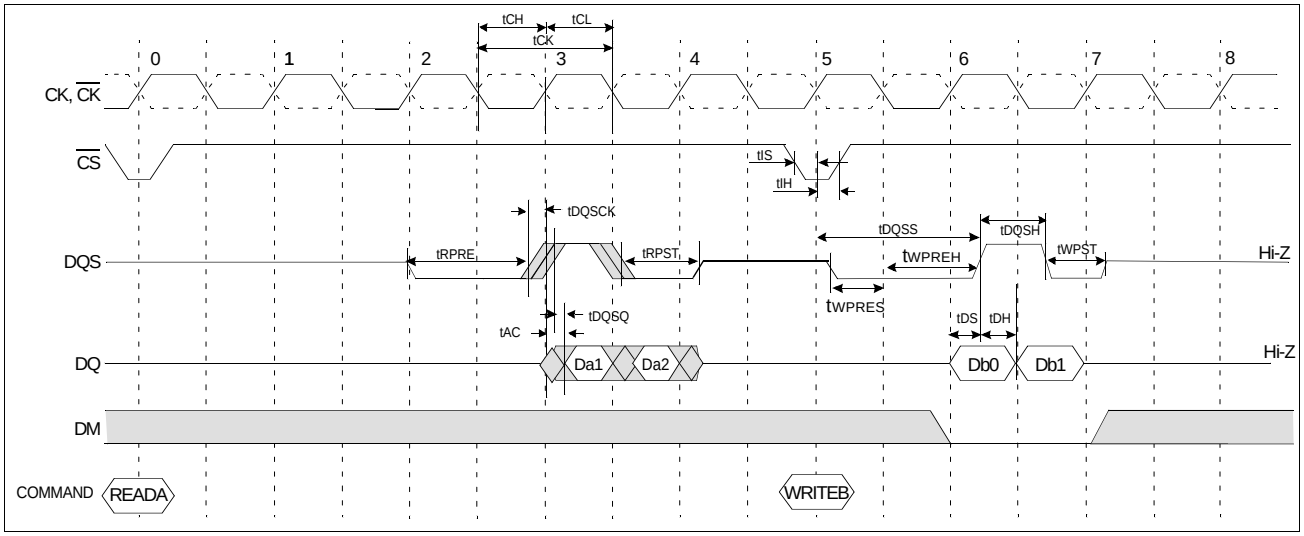
Parameter	Symbol	Value	Unit
Decoupling Capacitance between V_{DD} and V_{SS}	C_{DC1}	0.1 + 0.01	uF
Decoupling Capacitance between V_{DDQ} and V_{SSQ}	C_{DC2}	0.1 + 0.01	uF

Note : 1. V_{DD} and V_{DDQ} pins are separated each other.
All V_{DD} pins are connected in chip. All V_{DDQ} pins are connected in chip.
2. V_{SS} and V_{SSQ} pins are separated each other
All V_{SS} pins are connected in chip. All V_{SSQ} pins are connected in chip.

AC CHARACTERISTICS

Parameter		Symbol	-45*		-50		-55		-60		Unit	Note
			Min	Max	Min	Max	Min	Max	Min	Max		
CK cycle time	CL=3	tCK	-	10	5.0	10	5.5	10	6.0	10	ns	
	CL=4		4.5								ns	
CK high level width		tCH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
CK low level width		tCL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK	
DQS out access time from CK		tDQSCK	-0.7	+0.7	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Output access time from CK		tAC	-0.7	+0.7	-0.7	+0.7	-0.75	+0.75	-0.75	+0.75	ns	
Data strobe edge to Dout edge		tDQSQ	-	+0.45	-	+0.45	-	+0.5	-	+0.5	ns	1
Read preamble		tRPRE	0.9	1.1	0.9	1.1	0.9	1.1	0.9	1.1	tCK	
Read postamble		tRPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
CK to valid DQS-in		tDQSS	0.8	1.2	0.8	1.2	0.75	1.25	0.75	1.25	tCK	
DQS-In setup time		tWPRES	0	-	0	-	0	-	0	-	ns	
DQS-in hold time		tWPREH	0.25	-	0.25	-	0.25	-	0.25	-	tCK	
DQS write postamble		tWPST	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-In high level width		tDQSH	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
DQS-In low level width		tDQSL	0.4	0.6	0.4	0.6	0.4	0.6	0.4	0.6	tCK	
Address and Control input setup		tIS	1.0	-	1.0	-	1.1	-	1.1	-	ns	
Address and Control input hold		tIH	1.0	-	1.0	-	1.1	-	1.1	-	ns	
DQ and DM setup time to DQS		tDS	0.45	-	0.45	-	0.5	-	0.5	-	ns	
DQ and DM hold time to DQS		tDH	0.45	-	0.45	-	0.5	-	0.5	-	ns	
Clock half period		tHP	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	tCLmin or tCHmin	-	ns	1
Data output hold time from DQS		tQH	tHP-0.45	-	tHP-0.45	-	tHP-0.5	-	tHP-0.5	-	ns	1

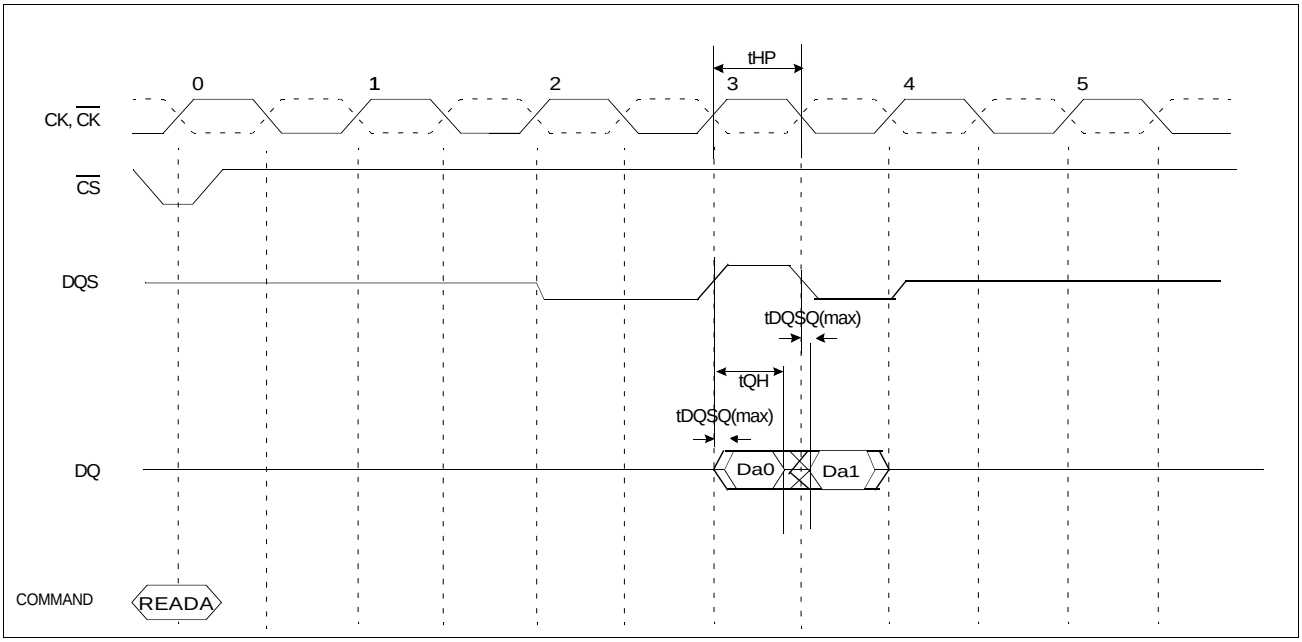
Simplified Timing @ BL=2, CL=3



Note 1 :

- The JEDEC DDR specification currently defines the output data valid window(tDV) as the time period when the data strobe and all data associated with that data strobe are coincidentally valid.
- The previously used definition of tDV(=0.35tCK) artificially penalizes system timing budgets by assuming the worst case output valid window even then the clock duty cycle applied to the device is better than 45/55%
- A new AC timing term, tQH which stands for data output hold time from DQS is defined to account for clock duty cycle variation and replaces tDV
- tQHmin = tHP-X where
  . tHP=Minimum half clock period for any given cycle and is defined by clock high or clock low time(tCH,tCL)
  . X=A frequency dependent timing allowance account for tDQSQmax

tQH Timing (CL3, BL2)



AC CHARACTERISTICS (I)

Parameter	Symbol	-45*		-50		-55		-60		Unit	Note
		Min	Max	Min	Max	Min	Max	Min	Max		
Row cycle time	t_{RC}	13	-	12	-	12	-	10	-	tCK	
Refresh row cycle time	t_{RFC}	15	-	14	-	14	-	12	-	tCK	
Row active time	t_{RAS}	9	100K	8	100K	8	100K	7	100K	tCK	
$\overline{RAS}$ to $\overline{CAS}$ delay for Read	t_{RCDRD}	4	-	4	-	4	-	3	-	tCK	
$\overline{RAS}$ to $\overline{CAS}$ delay for Write	t_{RCDWR}	2		2		2	-	2	-	tCK	
Row precharge time	t_{RP}	4	-	4	-	4	-	3	-	tCK	
Row active to Row active	t_{RRD}	2	-	2	-	2	-	2	-	tCK	
Last data in to Row precharge	t_{WR}	2	-	2	-	2	-	2	-	tCK	1
Last data in to Read com- mand	t_{CDLR}	2	-	2	-	2	-	2	-	tCK	1
Col. address to Col. address	t_{CCD}	1	-	1	-	1	-	1	-	tCK	
Mode register set cycle time	t_{MRD}	2	-	2	-	2	-	2	-	tCK	
Auto precharge write recovery + Precharge	t_{DAL}	6	-	6	-	6	-	5	-	tCK	
Exit self refresh to read com-	t_{XSR}	200	-	200	-	200	-	200	-	tCK	
Power down exit time	t_{PDEX}	1tCK+tIS	-	1tCK+tIS	-	1tCK+tIS	-	1tCK+tIS	-	ns	
Refresh interval time	t_{REF}	7.8	-	7.8	-	7.8	-	7.8	-	us	

Note :1 For normal write operation, even numbers of Din are to be written inside DRAM

(Unit : Number of Clock)

AC CHARACTERISTICS (II)

K4D263238M-QC45*

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	Unit
222MHz (4.5ns)	4	13	15	9	4	2	4	2	tCK
200MHz (5.0ns)	3	12	14	8	4	2	4	2	tCK
183MHz (5.5ns)	3	12	14	8	4	2	4	2	tCK
166MHz (6.0ns)	3	10	12	7	3	2	3	2	tCK
143MHz (7.0ns)	3	9	11	6	3	2	3	2	tCK

K4D263238M-QC50

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	Unit
200MHz (5.0ns)	3	12	14	8	4	2	4	2	tCK
183MHz (5.5ns)	3	12	14	8	4	2	4	2	tCK
166MHz (6.0ns)	3	10	12	7	3	2	3	2	tCK
143MHz (7.0ns)	3	9	11	6	3	2	3	2	tCK

K4D263238M-QC55

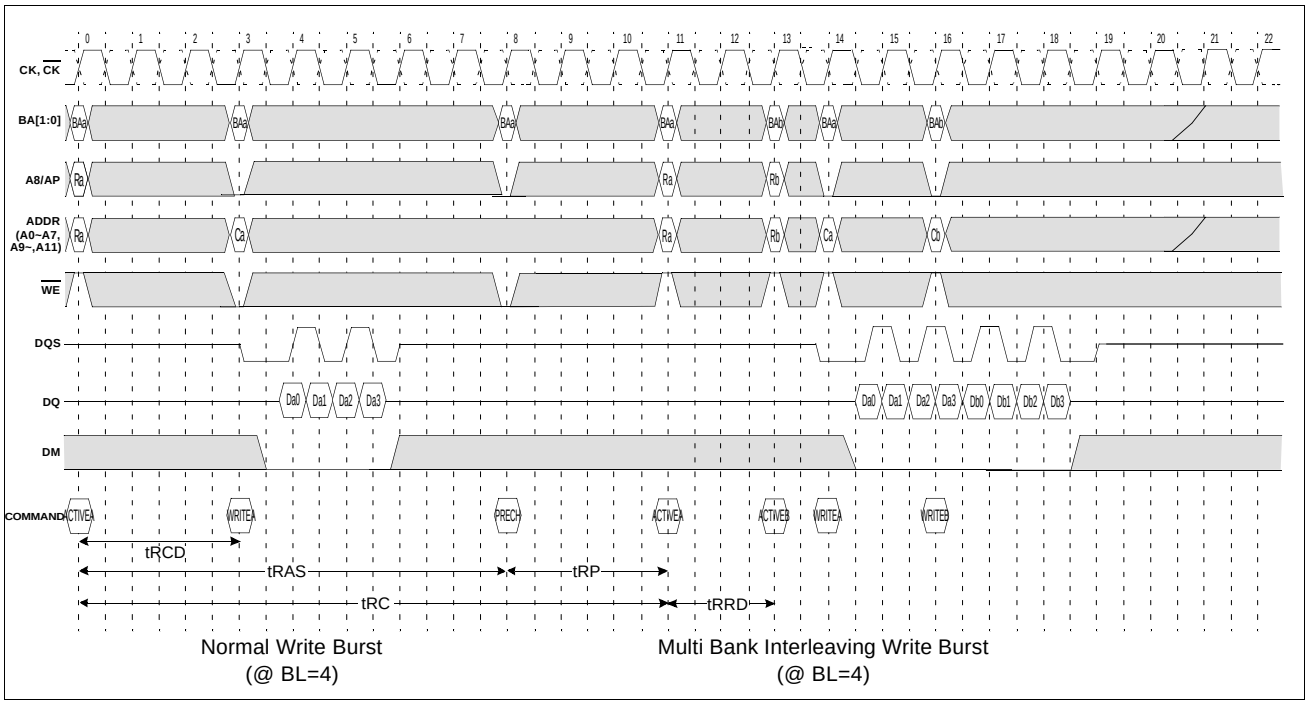
Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	Unit
183MHz (5.5ns)	3	12	14	8	4	2	4	2	tCK
166MHz (6.0ns)	3	10	12	7	3	2	3	2	tCK
143MHz (7.0ns)	3	9	11	6	3	2	3	2	tCK

K4D263238M-QC60

Frequency	Cas Latency	tRC	tRFC	tRAS	tRCDRD	tRCDWR	tRP	tRRD	Unit
166MHz (6.0ns)	3	10	12	7	3	2	3	2	tCK
143MHz (7.0ns)	3	9	11	6	3	2	3	2	tCK

*

Simplified Timing(2) @ BL=4, CL=3



PACKAGE DIMENSIONS (TQFP)

Dimensions in Millimeters

