AN2526NFH

Automotive LCD TV signal processor IC

■ Overview

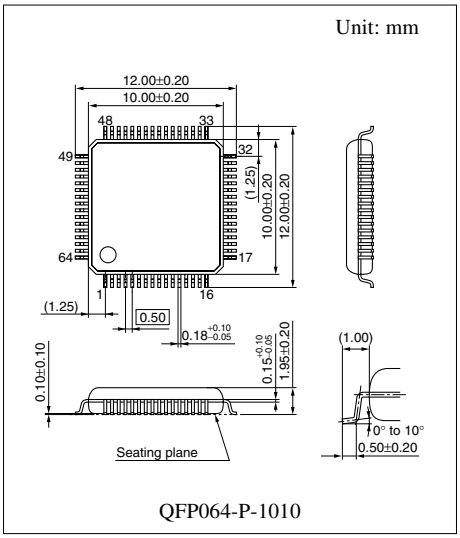
The AN2526NFH is a video signal processing IC with an LCD's 5 V-source driving power supply for TFT color LCD (normally white type), and it supports NTSC and PAL systems. The main circuitry of this IC includes video-signal processing circuit, color signal processing circuit, interface circuit, synchronizing circuit and many color quality adjusting circuits. This IC converts the composite video signal or separated Y/C signal or RGB signals into RGB signals available for TFT color LCD.

■ Features

- Supply voltage: 5 V/7.5 V
- Built-in LCD's 5 V-source driving power supply
- Low consumption power (typ. 260 mW)
- Supporting NTSC and PAL
- Supporting composite, component and color differential signal input
- Video signal, analog RGB (2 systems)
  One is for OSD (analog/digital).
- Each mode setting is possible with 3-wire or I^2C Bus control.
- Electronic volume (D/A converter) built in
- Contrast/Brightness/γ correction circuit built in
- Horizontal and vertical display position adjustment are possible by serial control.
- Package: QFP-64HP10L (10 × 10 × 1.95 mm)
- Difference from the AN2526FH
  Compared to the AN2526FH, the sync. system gain is increased in no signal input. This may cause the picture on the screen to be swaying horizontally. So we cannot recommend this IC to be used in the set with no-signal input mode.

■ Applications

- 4 inches to 7 inches middle size TFT LCD equipment of normally white, of such as in-car TV, an LCD monitor for car navigation system.

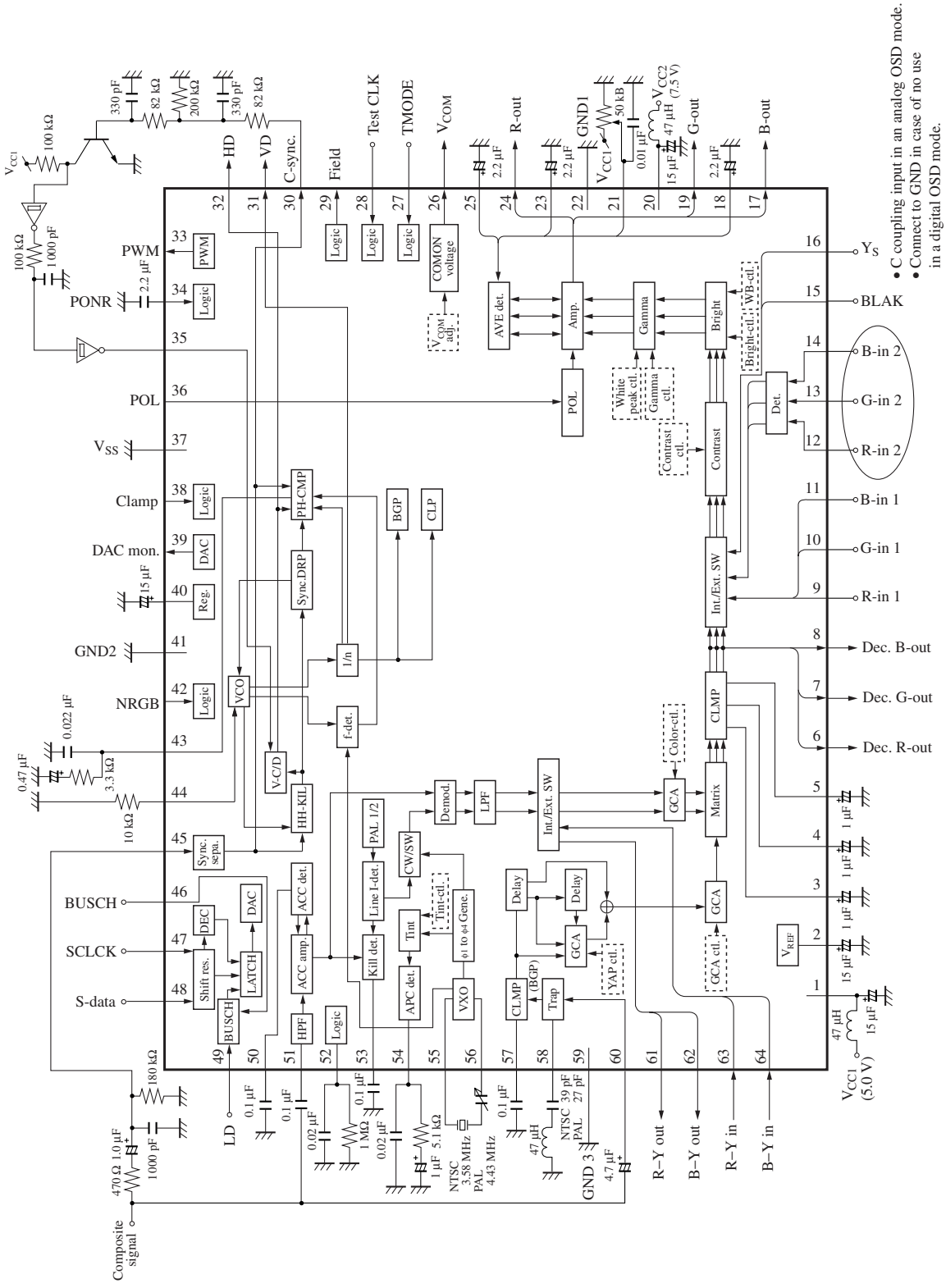


QFP064-P-1010

Note) The package of this product will be changed to lead-free type (QFP064-P-1010A). See the new package dimensions section later of this datasheet.

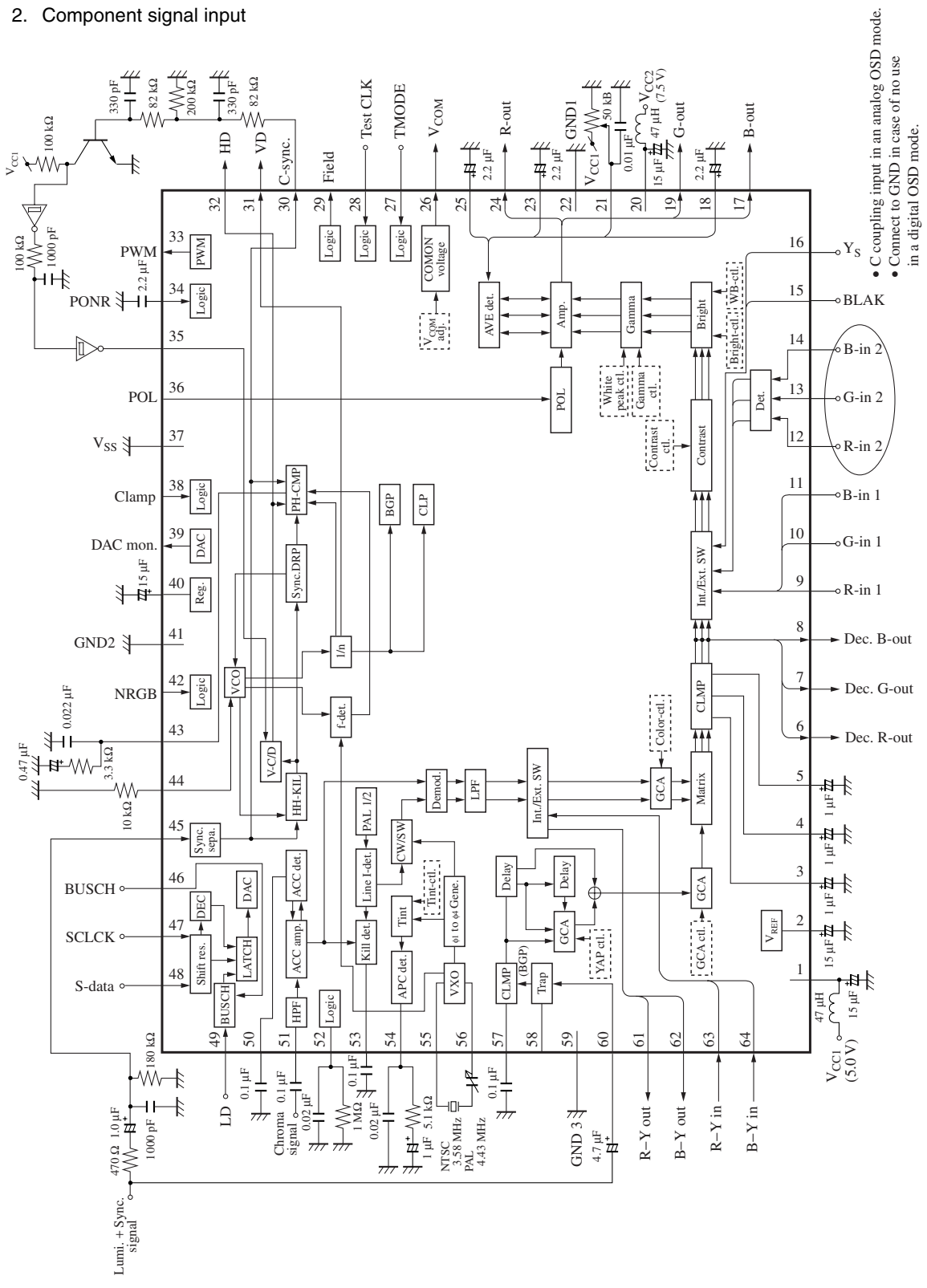
■ Application Circuit Examples

1. Composite signal input



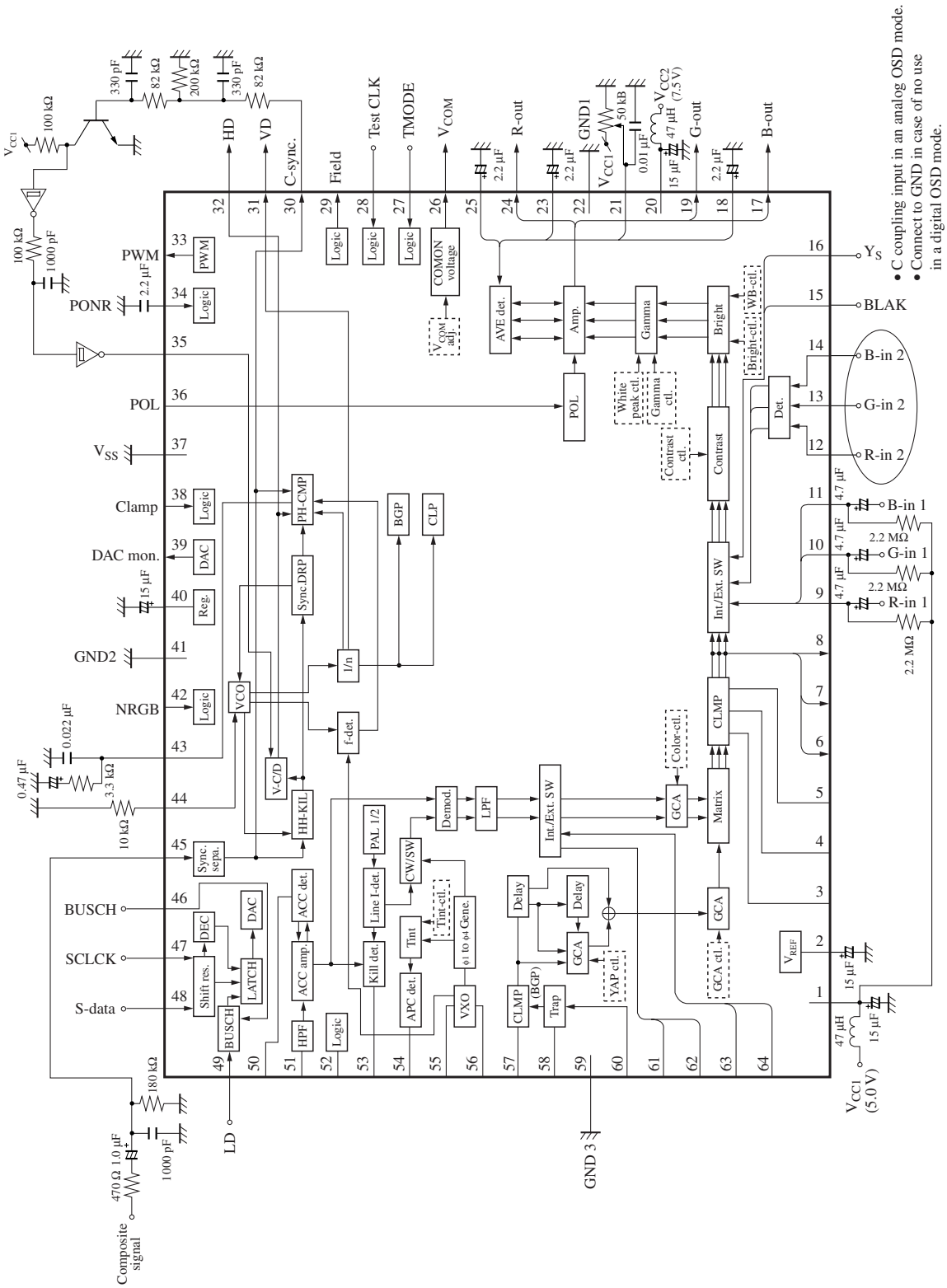
■ Application Circuit Examples (continued)

2. Component signal input



■ Application Circuit Examples (continued)

3. Analog RGB signal input



■ Pin Descriptions

Pin No.	Description	Pin No.	Description
1	V_{CC1} (5.0 V)	33	PWM output pin
2	Reference voltage pin	34	Power-on reset detection pin
3	R-ch. clamp detection pin	35	Vertical synchronous signal input pin
4	G-ch. clamp detection pin	36	1H reverse signal input pin
5	B-ch. clamp detection pin	37	Clock-system GND (V_{SS})
6	R-ch. decoder output pin	38	Clamp pulse input pin
7	G-ch. decoder output pin	39	DAC monitor pin
8	B-ch. decoder output pin	40	Clock-system power supply (3.0 V)
9	R-ch. analog signal input pin	41	GND 2
10	G-ch. analog signal input pin	42	Analog imposing control signal input pin
11	B-ch. analog signal input pin	43	AFC loop filter connecting pin
12	R-ch. analog/character signal input pin	44	VCO frequency adjustment pin
13	G-ch. analog/character signal input pin	45	Synchronous signal input pin
14	B-ch. analog/character signal input pin	46	Serial/I^2C Bus switching pin
15	Black level indication control signal input pin	47	Serial data shift clock input pin
16	Character picking up pulse input pin	48	Serial data input pin
17	B-ch. output pin	49	Serial data write pulse input pin
18	B-ch. output DC feedback detection pin	50	ACC detection pin
19	G-ch. output pin	51	ACC input pin
20	V_{CC2} (7.5 V)	52	Horizontal clock detection pin
21	Drive output reference potential input pin	53	Chroma killer detection pin
22	GND 1	54	APC detection pin
23	G-ch. output DC feedback detection pin	55	VXO input pin
24	R-ch. output pin	56	VXO output pin
25	R-ch. output DC feedback detection pin	57	Y-system clamp detection pin
26	Common reverse signal output pin	58	Chroma trap filter connection pin
27	Testing pulse input pin	59	GND 3
28	Testing clock input pin	60	Luminance signal input pin
29	Field identification signal output pin	61	R-Y output pin
30	Composite synchronous signal output pin	62	B-Y output pin
31	Vertical synchronous signal output pin	63	R-Y input pin
32	Horizontal synchronous signal output pin	64	B-Y input pin

■ Absolute Maximum Ratings

Parameter	Symbol	Rating	Unit
Supply voltage	V_{CC1}	5.5	V
	V_{CC2}	8.5	
Supply current	I_{CC}	—	mA
Power dissipation *2	P_D	423	mW
Operating ambient temperature *1	T_{opr}	−30 to +85	°C
Storage temperature *1	T_{stg}	−55 to +150	°C

Note) ∗1: Except for the operating ambient temperature and storage temperature, all ratings are for T_a = 25°C.
∗2: The power dissipation shown is the value in free air for T_{opr} = 85°C.

■ Recommended Operating Range

Parameter	Symbol	Range	Unit
Supply voltage	V_{CC1}	4.7 to 5.3	V
	V_{CC2}	7.0 to 8.0	

■ Electrical Characteristics at T_a = 25°C

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
DC						
V_{CC1}-system current consumption	I_{TOTAL1}	—	29	—	43	mA
V_{CC2}-system current consumption	I_{TOTAL2}	—	6.0	—	14.0	mA
Pin 2 voltage	V_2	—	1.8	—	2.2	V
Pin 40 voltage	V_{40}	—	2.7	—	3.3	V
Chroma system						
R-Y standard gain	G_{RY}	SG3 (Y_y = −17 dB, Y_s = 0 V[p-p], NTSC), ch.1 = "C0"	9.5	—	14.5	dB
R-Y/G-Y relative gain	G_{RYGY}	SG3 (Y_y = −17 dB, Y_s = 0 V[p-p], NTSC), ch.1 = "C0"	−8.0	—	−4.0	dB
B-Y standard gain	G_{BY}	SG3 (Y_y = −17 dB, Y_s = 0 V[p-p], NTSC), ch.1 = "C0"	9.5	—	14.5	dB
B-Y/G-Y relative gain	G_{BYGY}	SG3 (Y_y = −17 dB, Y_s = 0 V[p-p], NTSC), ch.1 = "C0"	−20.5	—	−12.5	dB
High-level APC pull-in	AP_H	SG5 (4.43 MHz + 520 Hz, PAL)	500	—	540	Hz
Low-level APC pull-in	AP_L	SG5 (4.43 MHz − 520 Hz, PAL)	−540	—	−500	Hz
ACC output characteristic 1	G_{ACC1}	SG5 (0 dB, 6 dB, NTSC), ch.1 = "80"	−1.0	—	1.0	dB
ACC output characteristic 2	G_{ACC2}	SG5 (0 dB, 6 dB, NTSC), ch.1 = "80"	−1.0	—	1.0	dB
Chroma killer characteristic 1	V_{KILL1}	SG5 (−30 dB, NTSC) ch.1 = "80", ch.2 = "80", ch.5 = "FF"	400	—	—	mV[p-p]
Chroma killer characteristic 2	V_{KILL2}	SG5 (−50 dB, NTSC) ch.1 = "80", ch.2 = "80", ch.5 = "FF"	—	—	600	mV[p-p]

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system						
Sharpness control characteristic	G_{SH}	SG1 (2 MHz, NTSC) ch.1 = "80", ch.9 = "80"/"FF"	1.0	—	—	dB
Sharpness frequency characteristic 1	f_{SH1}	SG1 (100 kHz/2 MHz, NTSC) ch.1 = "80"	3.5	—	—	dB
R-ch. contrast adjustment range 1	CTR_{R1}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment ch.15 = "C0"/"FF"	1.5	—	—	dB
G-ch. contrast adjustment range 1	CTR_{G1}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment ch.15 = "C0"/"FF"	1.5	—	—	dB
B-ch. contrast adjustment range 1	CTR_{B1}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment ch.15 = "C0"/"FF"	1.5	—	—	dB
R-ch. contrast adjustment range 2	CTR_{R2}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment ch.15 = "C0"/"80"	—	—	–5.2	dB
G-ch. contrast adjustment range 2	CTR_{G2}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment ch.15 = "C0"/"80"	—	—	–5.2	dB
B-ch. contrast adjustment range 2	CTR_{B2}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment ch.15 = "C0"/"80"	—	—	–5.2	dB
R-ch. pedestal amplitude minimum	$V_{PEDRmin}$	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment, ch.8 = "FF" ch.15 = "C0"	—	—	2.0	V[p-p]
G-ch. pedestal amplitude minimum	$V_{PEDGmin}$	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment, ch.8 = "FF" ch.15 = "C0"	—	—	2.0	V[p-p]
B-ch. pedestal amplitude minimum	$V_{PEDBmin}$	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment, ch.8 = "FF" ch.15 = "C0"	—	—	2.0	V[p-p]

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system (continued)						
R-ch. pedestal amplitude maximum	$V_{PEDRmax}$	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment, ch.8 = "00" ch.15 = "C0"	3.0	—	—	V[p-p]
G-ch. pedestal amplitude maximum	$V_{PEDGmax}$	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment, ch.8 = "00" ch.15 = "C0"	3.0	—	—	V[p-p]
B-ch. pedestal amplitude maximum	$V_{PEDBmax}$	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12/13/14 = "FF" ch.8/10/11 adjustment, ch.8 = "00" ch.15 = "C0"	3.0	—	—	V[p-p]
G-ch. output DC voltage	V_{GDC}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11 adjustment, ch.15 = "C0"	2.2	—	2.5	V[p-p]
R-ch. gamma characteristic 1	G_{GAMR1}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment	−8.5	—	−3.5	dB
G-ch. gamma characteristic 1	G_{GAMG1}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment	−8.5	—	−3.5	dB
B-ch. gamma characteristic 1	G_{GAMB1}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment	−8.5	—	−3.5	dB
R-ch. gamma characteristic 2	G_{GAMR2}	SG3 (NTSC), ch.1 = "E0", ch.4 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.13 = "80"/"FF"	−8.2	—	—	dB
G-ch. gamma characteristic 2	G_{GAMG2}	SG3 (NTSC), ch.1 = "E0", ch.4 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.13 = "80"/"FF"	−8.2	—	—	dB
B-ch. gamma characteristic 2	G_{GAMB2}	SG3 (NTSC), ch.1 = "E0", ch.4 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.13 = "80"/"FF"	−8.2	—	—	dB
R-ch. gamma characteristic 3	G_{GAMR3}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.13 = "80"/"60"	−3.5	—	0.5	dB

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system (continued)						
G-ch. gamma characteristic 3	G_{GAMG3}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.13 = "80"/"60"	−3.5	—	0.5	dB
B-ch. gamma characteristic 3	G_{GAMB3}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.13 = "80"/"60"	−3.5	—	0.5	dB
R-ch. white limiter low-level	V_{WRRL}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "00", ch.14 = "40" ch.8/10/11/15 adjustment ch.15 = "FF"	—	—	3.0	V[p-p]
G-ch. white limiter low-level	V_{WRGL}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "00", ch.14 = "40" ch.8/10/11/15 adjustment ch.15 = "FF"	—	—	3.0	V[p-p]
B-ch. white limiter low-level	V_{WRBL}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "00", ch.14 = "40" ch.8/10/11/15 adjustment ch.15 = "FF"	—	—	3.0	V[p-p]
R-ch. white limiter high-level	V_{WRRH}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.15 = "FF"	3.2	—	—	V[p-p]
G-ch. white limiter high-level	V_{WRGH}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.15 = "FF"	3.2	—	—	V[p-p]
B-ch. white limiter high-level	V_{WRBH}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment ch.15 = "FF"	3.2	—	—	V[p-p]
R-ch. black limiter low-level	V_{BRRL}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.7 = "80", ch.12 = "FF" ch.14 = "40", ch.8/10/11/15 adjustment ch.8 = "00"	3.0	—	—	V
G-ch. black limiter low-level	V_{BRGL}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.7 = "80", ch.12 = "FF" ch.14 = "40", ch.8/10/11/15 adjustment ch.8 = "00"	3.0	—	—	V

■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system (continued)						
B-ch. black limiter low-level	V_{BRBL}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.7 = "80", ch.12 = "FF" ch.14 = "40", ch.8/10/11/15 adjustment ch.8 = "00"	3.0	—	—	V
R-ch. black limiter high-level	V_{BRRH}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF" ch.8/10/11/15 adjustment, ch.7 = "FF" ch.8 = "00", ch.14 = "40"	—	—	1.2	V
G-ch. black limiter high-level	V_{BRGH}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF" ch.8/10/11/15 adjustment, ch.7 = "FF" ch.8 = "00", ch.14 = "40"	—	—	1.2	V
B-ch. black limiter high-level	V_{BRBH}	SG3 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF" ch.8/10/11/15 adjustment, ch.7 = "FF" ch.8 = "00", ch.14 = "40"	—	—	1.2	V
R-ch. Y_S threshold 1	V_{tYSR1}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 16 = 1 V	0.8	—	—	V[p-p]
G-ch. Y_S threshold 1	V_{tYSG1}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 16 = 1 V	0.8	—	—	V[p-p]
B-ch. Y_S threshold 1	V_{tYSB1}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 16 = 1 V	0.8	—	—	V[p-p]
R-ch. Y_S threshold 2	V_{tYSR2}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 16 = 2.2 V	—	—	0.5	V[p-p]
G-ch. Y_S threshold 2	V_{tYSG2}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 16 = 2.2 V	—	—	0.5	V[p-p]
B-ch. Y_S threshold 2	V_{tYSB2}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 16 = 2.2 V	—	—	0.5	V[p-p]
R-ch. black level	CHR_{RB}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 16 = SG7	– 0.6	—	0.6	V
G-ch. black level	CHR_{GB}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 16 = SG7	– 0.6	—	0.6	V
B-ch. black level	CHR_{BB}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 16 = SG7	– 0.6	—	0.6	V

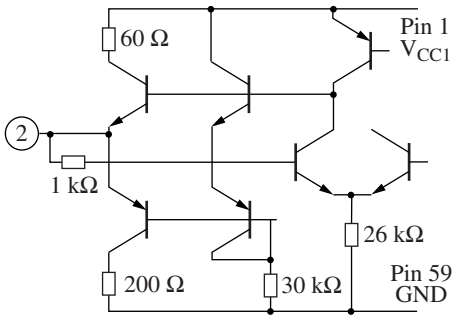
■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system (continued)						
R-ch. black level width	$WCHR_{RB}$	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 16 = SG7	2.25	—	3.75	µs
G-ch. black level width	$WCHR_{GB}$	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 16 = SG7	2.25	—	3.75	µs
B-ch. black level width	$WCHR_{BB}$	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 16 = SG7	2.25	—	3.75	µs
R-ch. CHR threshold 1	V_{tCHR1}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 12 = 1 V	1.5	—	—	V[p-p]
G-ch. CHR threshold 1	V_{tCHG1}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 13 = 1 V	1.5	—	—	V[p-p]
B-ch. CHR threshold 1	V_{tCHB1}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 14 = 1 V	1.5	—	—	V[p-p]
R-ch. CHR threshold 2	V_{tCHR2}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 12 = 2.2 V	3.0	—	—	V[p-p]
G-ch. CHR threshold 2	V_{tCHG2}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 13 = 2.2 V	3.0	—	—	V[p-p]
B-ch. CHR threshold 2	V_{tCHB2}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 14 = 2.2 V	3.0	—	—	V[p-p]
R-ch. white level	CHR_{RW}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 12 = SG7	2.0	—	—	V[p-p]
G-ch. white level	CHR_{GW}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 13 = SG7	2.0	—	—	V[p-p]
B-ch. white level	CHR_{BW}	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 14 = SG7	2.0	—	—	V[p-p]
R-ch. white level width	$WCHR_{RW}$	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 12 = SG7	2.25	—	3.75	µs
G-ch. white level width	$WCHR_{GW}$	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 13 = SG7	2.25	—	3.75	µs

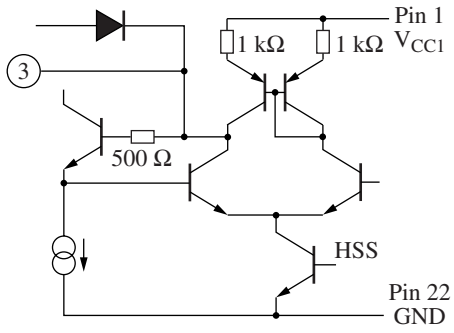
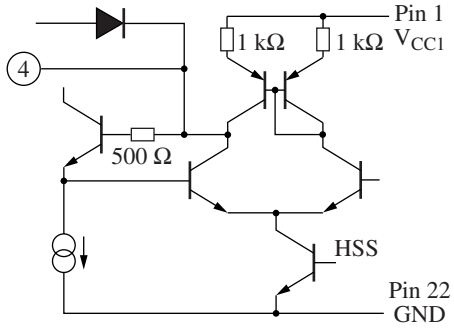
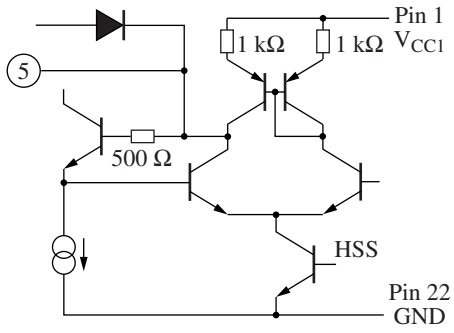
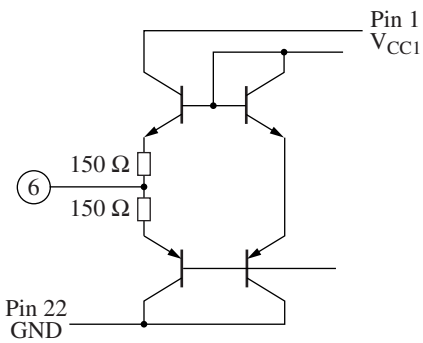
■ Electrical Characteristics at T_a = 25°C (continued)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Y-system (continued)						
B-ch. white level width	$WCHR_{BW}$	SG2 (NTSC), ch.1 = "E0", ch.2 = "40" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, Pin 14 = SG7	2.25	—	3.75	µs
R-ch. RGB2 relative amplitude	V_{RGB2R}	SG2 (NTSC), ch.1 = "A0" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, ch.3 = "40" ch.6 = "40", Pin 42 = 2.2 V	– 0.45	—	0.45	V[p-p]
B-ch. RGB2 relative amplitude	V_{RGB2B}	SG2 (NTSC), ch.1 = "A0" ch.5 = "80", ch.12 = "FF", ch.14 = "40" ch.8/10/11/15 adjustment, ch.3 = "40" ch.6 = "40", Pin 42 = 2.2 V	– 0.45	—	0.45	V[p-p]
Synchronous system						
Horizontal sync. pulse low-level	V_{HDL}	—	—	—	0.4	V
Horizontal sync. pulse amplitude	V_{HD}	—	4.0	—	—	V[p-p]
Horizontal sync. pulse width	t_{HD}	—	4.86	—	6.86	µs
Vertical sync. pulse low-level	V_{VDL}	—	—	—	0.4	V
Vertical sync. pulse amplitude	V_{VD}	—	4.0	—	—	V[p-p]
Horizontal sync. separation pulse high-level	V_{HSSH}	SG2 (NTSC)	4.0	—	—	V
Horizontal sync. separation pulse amplitude	V_{HSS}	SG2 (NTSC)	4.0	—	—	V[p-p]
Horizontal sync. separation pulse width	t_{HSS}	SG2 (NTSC)	3.8	—	5.8	µs
Horizontal sync. pulse free-run frequency	f_{HD}		15.434	—	16.034	kHz

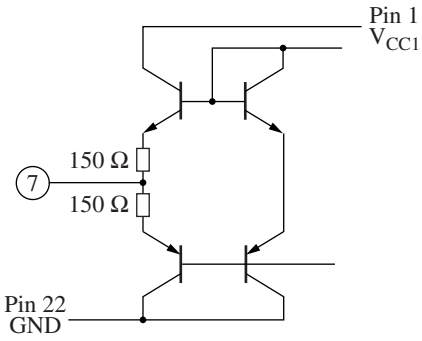
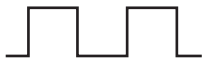
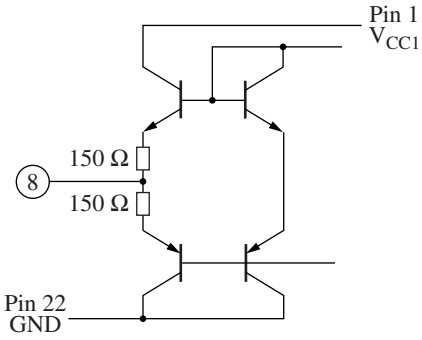
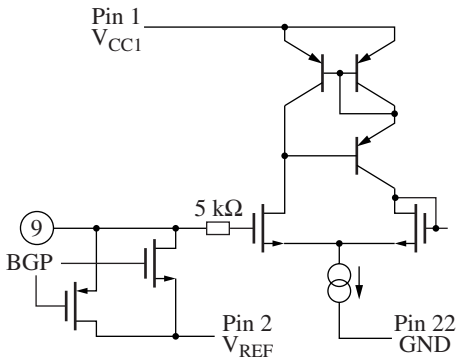
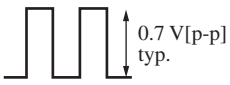
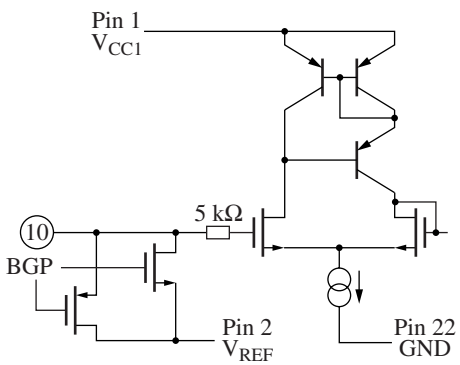
■ Terminal Equivalent Circuits

Pin No.	Equivalent circuit	Description	Voltage · Waveform
1	—	V_{CC1}: 5.0 V-system power supply pin Supply current 40 mA typ.	—
2		V_{REF}: Reference voltage output pin 2.0 V typ.	—

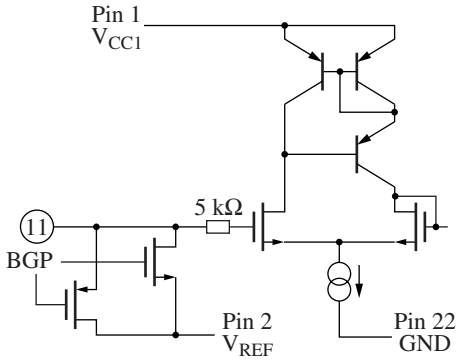
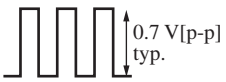
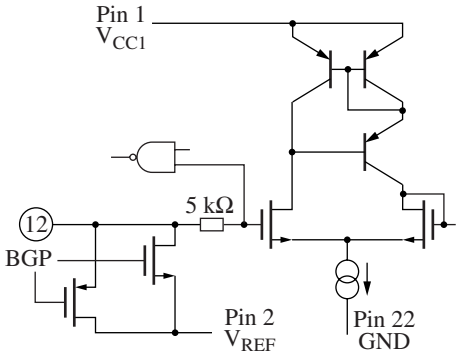
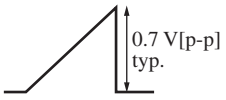
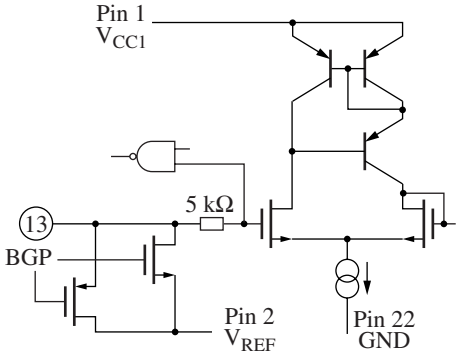
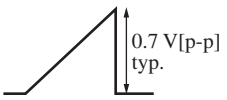
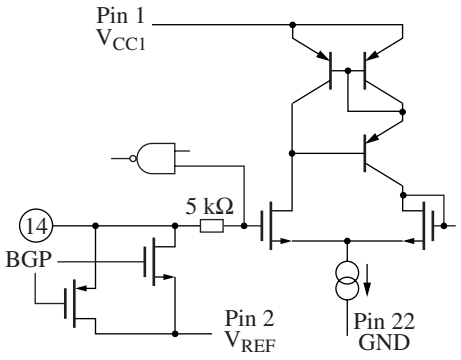
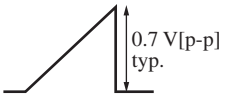
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
3		R-ch. det.: R-ch. clamping capacitor coupling pin	—
4		G-ch. det.: G-ch. clamping capacitor coupling pin	—
5		B-ch. det.: B-ch. clamping capacitor coupling pin	—
6		Dec.R-out: Output pin of R signal demodulated from video signal	

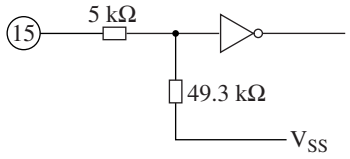
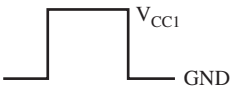
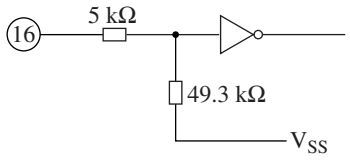
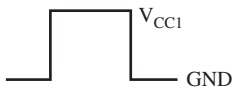
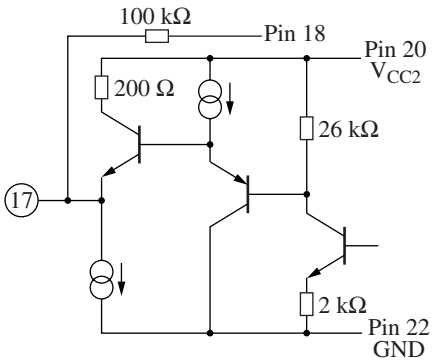
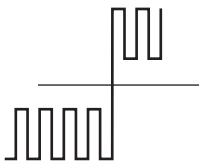
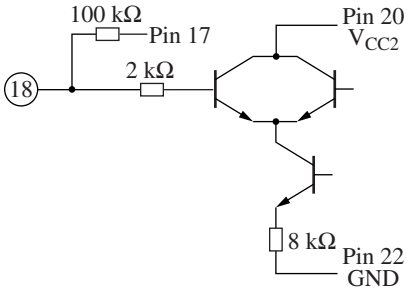
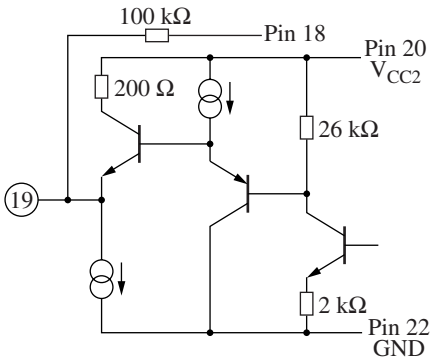
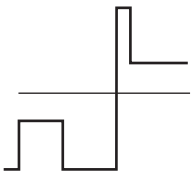
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
7		Dec.G-out: Output pin of G signal demodulated from video signal	
8		Dec.B-out: Output pin of B signal demodulated from video signal	
9		R-in 1: Analog R signal input	Analog R signal 
10		G-in 1: Analog G signal input	Analog G signal 

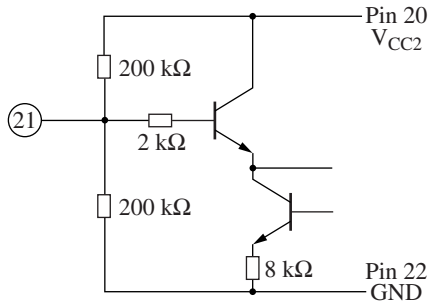
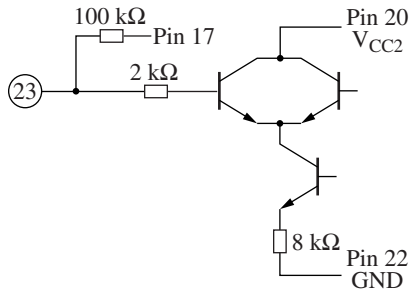
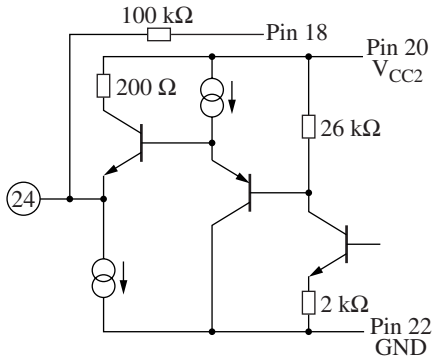
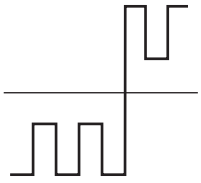
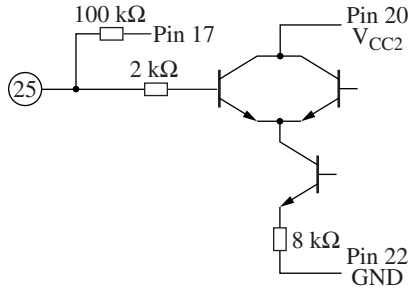
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
11		B-in 1: Analog B signal input	Analog B signal 
12		R-in 2: Character insertion signal input for R-ch., supporting analog and digital OSD.	Analog OSD  Digital OSD 
13		G-in 2: Character insertion signal input for G-ch., supporting analog and digital OSD.	Analog OSD  Digital OSD 
14		B-in 2: Character insertion signal input for B-ch., supporting analog and digital OSD.	Analog OSD  Digital OSD 

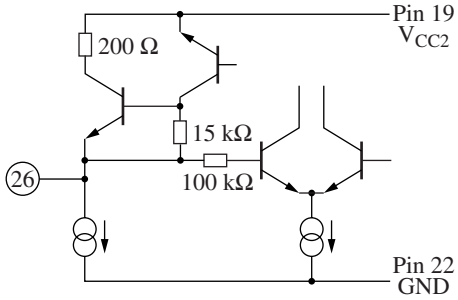
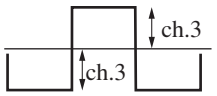
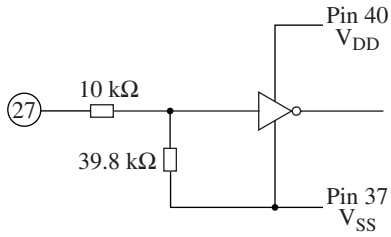
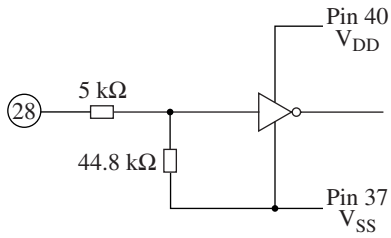
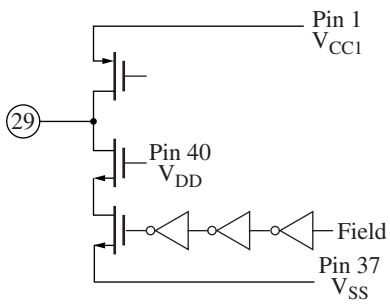
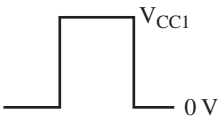
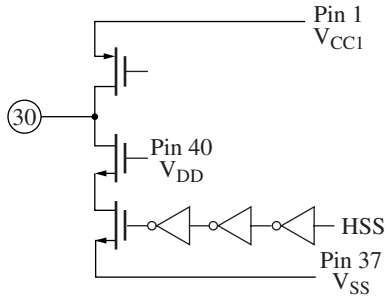
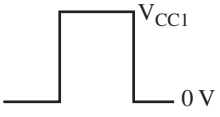
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
15		BLAK: Black level indication control signal input pin	
16		Y_S: Character picking up signal input	
17		B-out: B signal output pin	
18		B-ch.AVE det.: B-ch. output DC feedback detection pin	—
19		G-out: G signal output pin	
20	—	V_{CC2}: 7.5 V system power supply Supply current 12 mA typ.	—

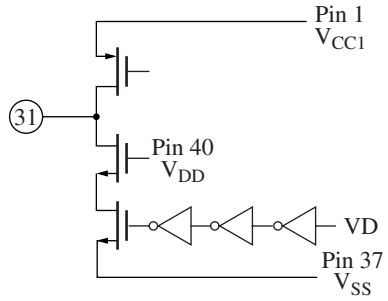
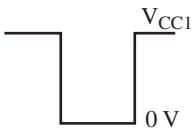
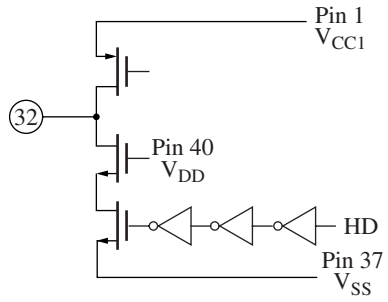
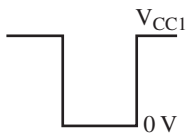
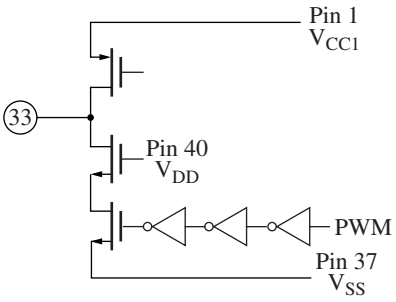
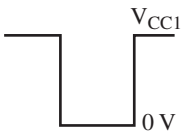
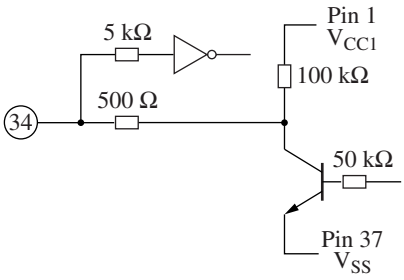
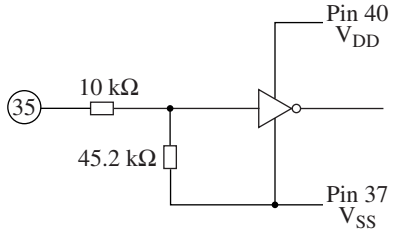
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
21		AVE: R,G,B output DC reference voltage pin	—
22	—	GND 2: Drive circuit system GND	—
23		G-ch.AVE det.: G-ch. output DC feedback detection pin	—
24		R-out: R signal output pin	
25		R-ch.AVE det.: R-ch. output DC feedback detection pin	—

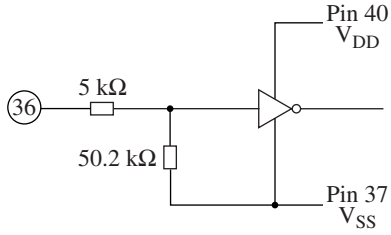
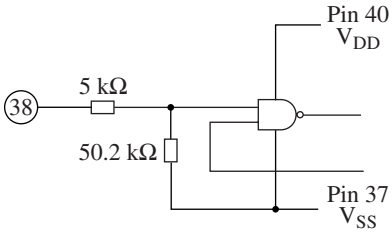
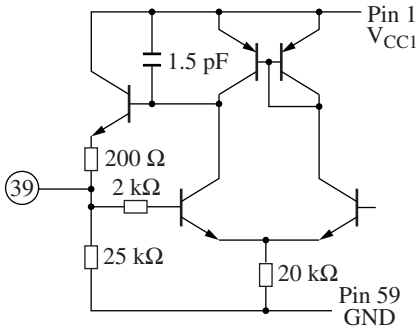
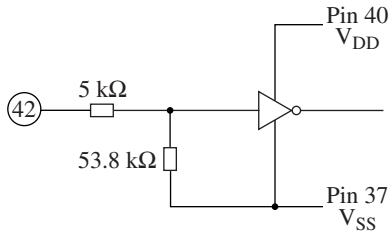
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
26		Common out: Voltage output pin for common. Output impedance; Approx. 150 Ω	
27		Test mode: Logic test mode start signal input pin; "Open" or "GND" normally	High or Low
28		Test CLK: Logic test pulse input pin; "Open" or "GND" normally	High or Low
29		Field: Field identifying signal output pin	Output waveform 
30		HSS: Composite synchronous signal output pin	Output waveform 

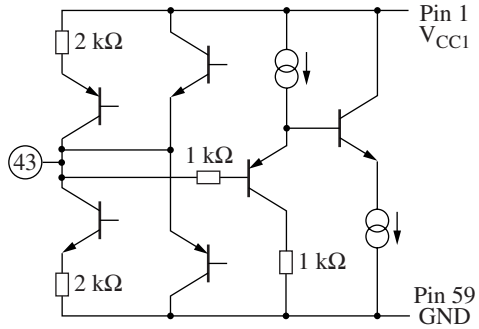
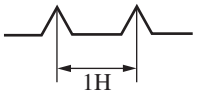
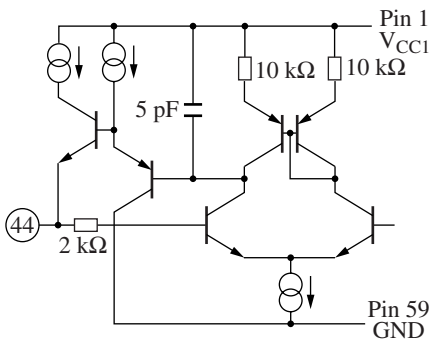
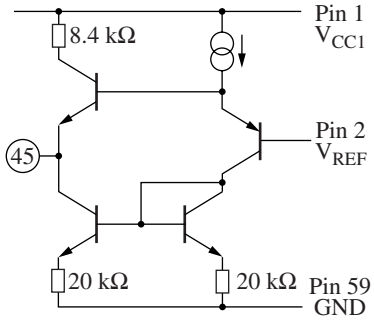
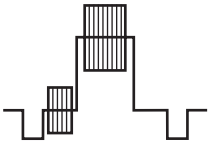
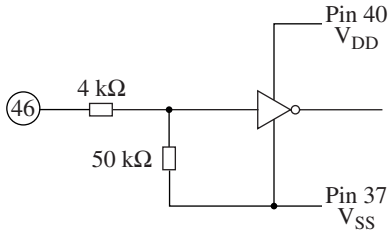
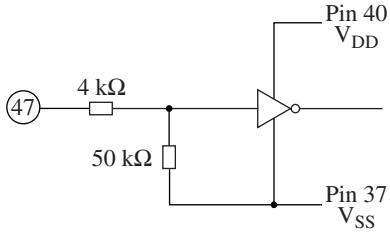
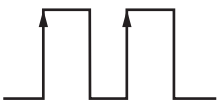
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
31		VD: Vertical synchronous signal output pin	Output waveform 
32		HD : Horizontal synchronous signal output pin	Output waveform 
33		PWM: PWM signal output pin	Output waveform 
34		RST: Capacitor coupling pin for power-on reset	—
35		VDB in: Vertical synchronous pulse input pin	High or Low

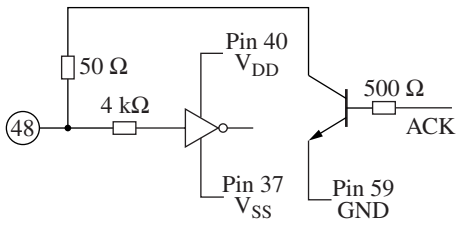
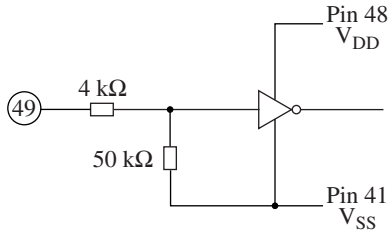
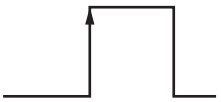
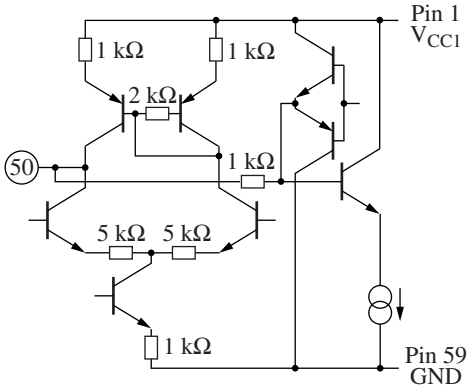
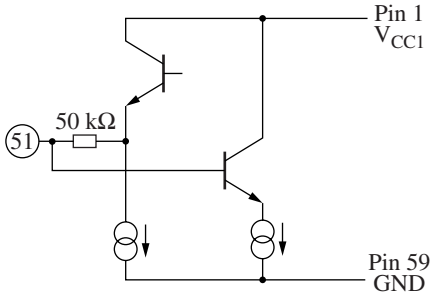
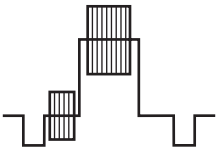
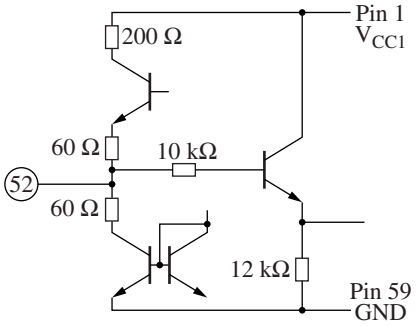
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
36		Ext. pol.: 1H reverse signal input pin	High or Low
37	—	V_{SS} : MOS system GND	—
38		Clamp in: Clamp pulse input pin Valid only in the external clamp mode. Positive polarity input.	High or Low
39		DAC mon.: DAC DC voltage output pin	DC
40	—	V_{DD}: Capacitor connection pin for MOS part power supply. 3.0 V typ.	—
41	—	GND 3: Pulse system GND	—
42		PRGB: Analog OSD signal input Mode start-up signal input pin Valid only in the analog OSD mode High = Analog OSD start up	High or Low

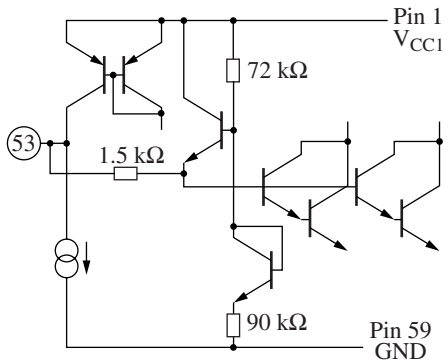
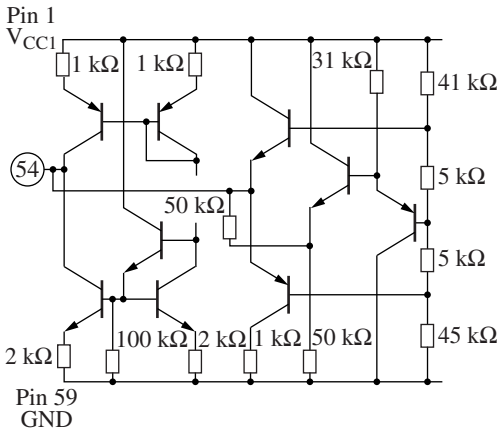
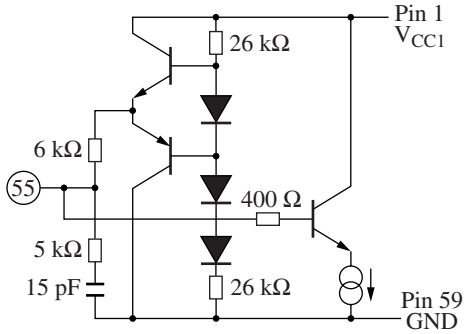
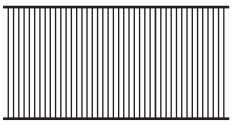
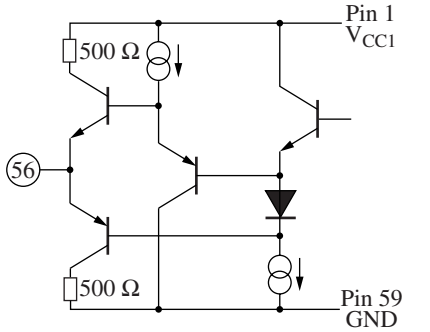
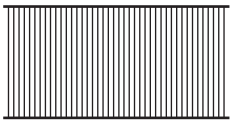
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
43		AFC det.: AFC filter connection pin Input impedance; 100 kΩ or more	
44		H f_O: VCO oscillation frequency adjusting resistor connection pin	—
45		HSS in: H-sync. input pin Separates a sync signal from luminance signal (video signal)	Input signal example: Video signal 
46		Bus-ch: Switching pin for serial three-wire control/I^2C Bus control High = I^2C Bus Open or Low = Serial three-wire control	High or Low
47		DAC: Serial clock input pin	

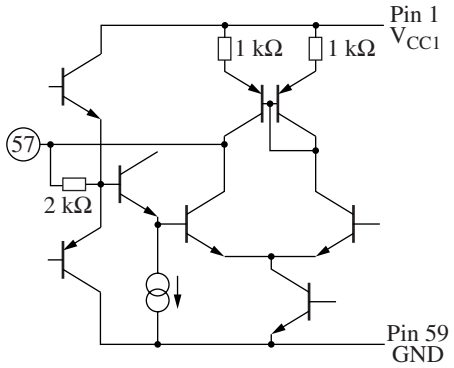
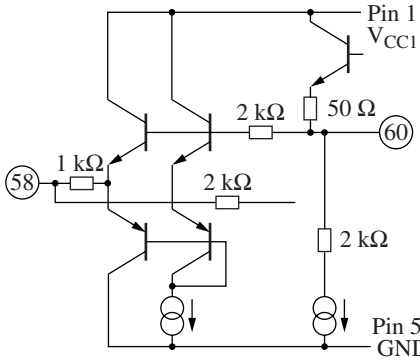
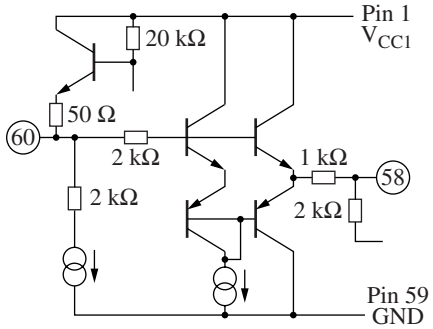
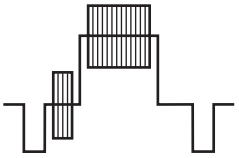
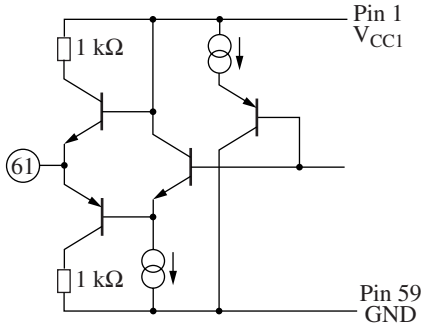
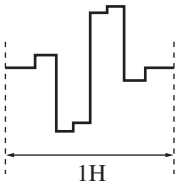
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
48		DAT: Serial data input pin	
49		LEN: Load pulse input pin, also works as the slave address conversion pin in the I^2C mode. High = "88" Low = "8A"	High or Low 
50		ACC det.: ACC capacitor connecting pin, adjusting the amplitude of a burst signal automatically	—
51		C in: Chroma signal input pin Input chroma signal (video signal)	Input signal example: Video signal 
52		L.det.: Capacitor coupling pin for the horizontal unlock detecting circuit	—

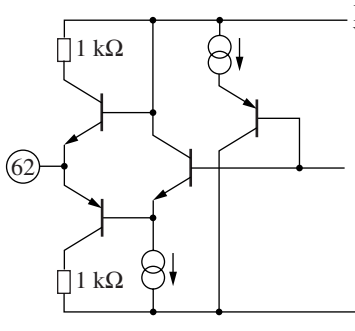
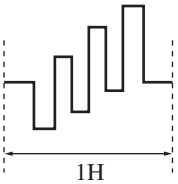
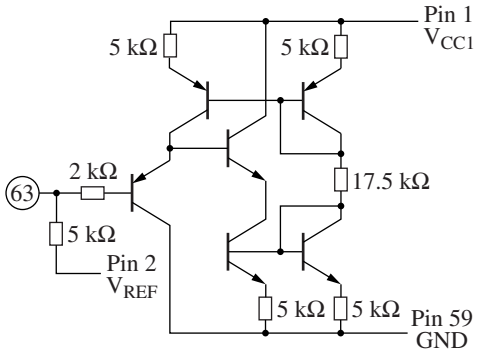
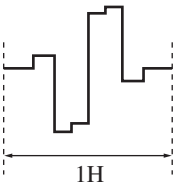
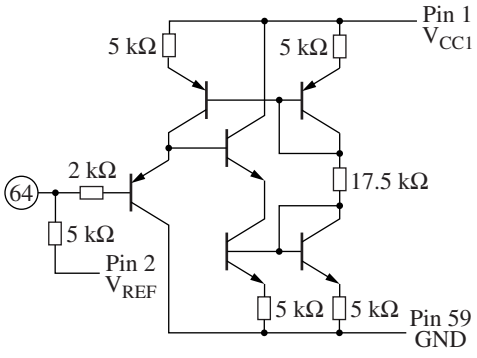
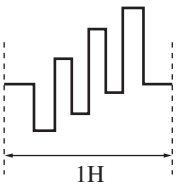
■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
53		Kill det.: Killer capacitor coupling pin. To prevent degradation of image in a small amplitude of a burst signal, this pin stops a chroma signal and the mode changes to black and white mode.	—
54		APC det.: APC capacitor coupling pin. Matching the phase of a crystal oscillation to that of burst signal.	—
55		VXOI : Xtal connecting pin The pair with pin 56	NTSC 3.58 MHz PAL 4.43 MHz 
56		VXOO : Xtal connecting pin The pair with pin 55 Output impedance; Approximately 100 Ω	NTSC 3.58 MHz PAL 4.43 MHz 

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
57		Y-det.: Capacitor coupling pin for luminance signal clamping	—
58		Trap: Trap connecting pin Trapping a chroma signal by connecting external inductor and capacitor. Not necessary in case that an input signal is a component.	—
59	—	GND 3: GND for chroma and luminance signal process blocks	—
60		Y-in: Luminance signal input pin Input luminance signal (video signal)	Input signal example: Video signal 
61		R-Y out: R-Y signal output pin, demodulated from a video signal	R-Y signal 

■ Terminal Equivalent Circuits (continued)

Pin No.	Equivalent circuit	Description	Voltage · Waveform
62		B-Y out : B-Y signal output pin, demodulated from a video signal	B-Y signal 
63		R-Y in: R-Y signal input pin in a color difference mode and standard PAL.	R-Y signal 
64		B-Y in : B-Y signal input pin in a color difference mode and standard PAL.	B-Y signal 

■ Usage Notes

- You are required to study adequately before using it in PAL.
- If the duty of PWM output is set to other than 0% to 100%, the jitter of the HD out put increases. So, confirm the horizontal jitter amount on the screen of the set you introduce the PWM function into.

■ Technical Data

Serial data control

In addition to its serial control by the conventional three-wire method, the AN2526NFH can be controlled by the I^2C Bus. The transmission method is selected by the voltage to be applied to Pin 46.

Three-wire control mode: Pin 46 = Low-level (connect to GND)

I^2C Bus mode: Pin 46 = High-level (Pin 41: connect to V_{DD})

It is recommended that the serial data is transferred during a vertical blanking period.

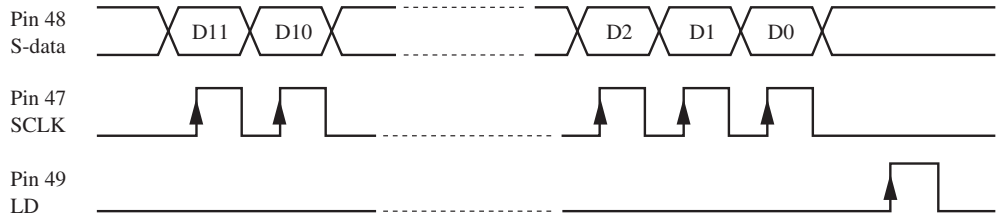
1. Three-wire control mode

A serial data is of three-line system transmitting three kinds of signals of data, shift clock and load pulse independently. The data to be transmitted is made up by 12 bits in total of address (4 bits) and data (8 bits). The DAC is composed of four blocks of serial-parallel conversion, address decoder, data latch and ladder resistors, enabling to control 16 channels in total. Further, the mode setting such as the input signal switching is done by a serial data to reduce the pin count.

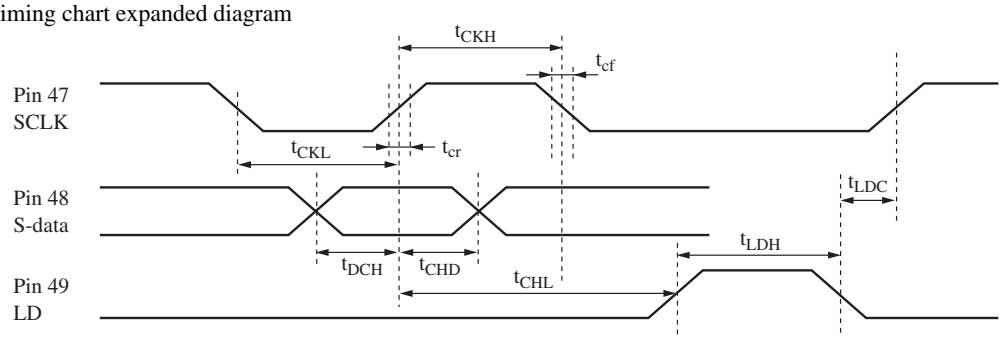
1) Serial data format

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
Address block				Data block							

2) Serial data input timing chart



Timing chart expanded diagram



■ Technical Data (continued)

1. Three-wire control mode (continued)

2) Serial data input timing chart (continued)

Parameter	Symbol	Min	Max	Unit
Clock low-level pulse width	t_{CKL}	500	—	ns
Clock high-level pulse width	t_{CKH}	500	—	ns
Clock rise time	t_{cr}	—	20	ns
Clock fall time	t_{cf}	—	20	ns
Data setup time	t_{DCH}	30	—	ns
Data hold time	t_{CHD}	60	—	ns
Load setup time	t_{CHL}	200	—	ns
Load hold time	t_{LDC}	100	—	ns
Load high-level pulse width	t_{LDH}	500	—	ns

3) Serial-data control contents

D11	D10	D9	D8	Selection-ch.	EVR control function	Number of bit
0	0	0	0	0	Vertical sync. signal output position	3
1	0	0	0	1	Horizontal sync. signal output position	5
0	1	0	0	2	PWM duty	6
1	1	0	0	3	Common pulse amplitude	7
0	0	1	0	4	Y-gain	8
1	0	1	0	5	Color gain	7
0	1	1	0	6	Hue	7
1	1	1	0	7	Black-limiter level	8
0	0	0	1	8	Bright	8
1	0	0	1	9	Y-aperture gain	8
0	1	0	1	10	R-ch. sub brightness	8
1	1	0	1	11	B-ch. sub brightness	8
0	0	1	1	12	White peak limiter level	8
1	0	1	1	13	Gamma-1 Knee level	8
0	1	1	1	14	Gamma-2 Knee level	8
1	1	1	1	15	RGB contrast	7

A variety of mode-settings for the channel for 8 bits or less is made by using the data stored in the data block.
The contents of each mode setting are shown next.

■ Technical Data (continued)

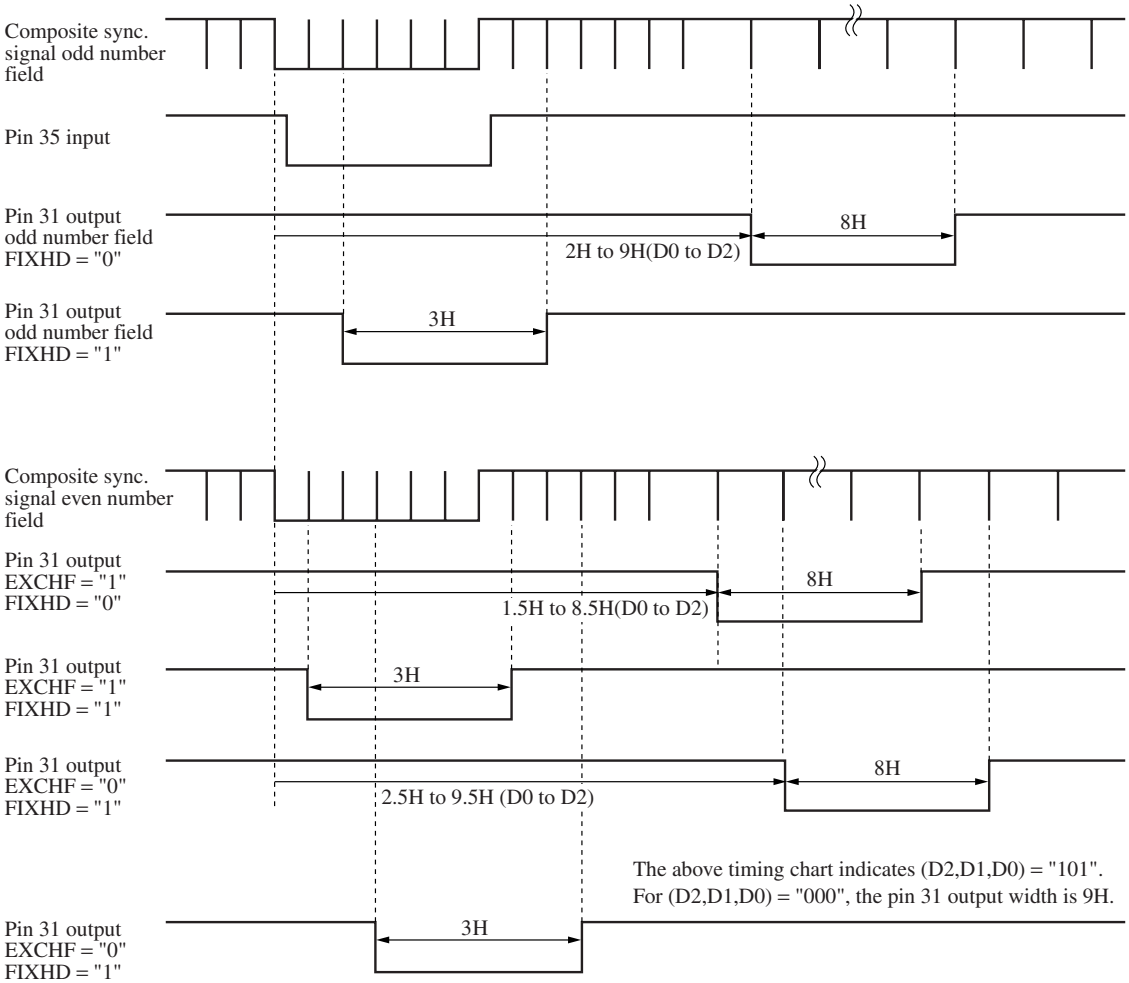
1. Three-wire control mode (continued)

4) Mode setup channel bit-map.

- ch.0: Vertical sync. output position adjustment

D11	D10	D9	D8	D7	D6	D5	D4 to D3	D2	D1	D0
				EXCHF	FIXHD	BOSC	Hor. PLL start position adjustment			
0	0	0	0	—	—	0	Automatic switching			
				—	—	1	263H/313H fixed (NTSC/PAL)			
				—	0	HD/VD output timing is serially variable				
				—	1	HD/VD output timing fixed				
				0	Odd number field: Advanced phase					
				1	Even number field: Advanced phase					

- Vertical sync. output timing adjusting range



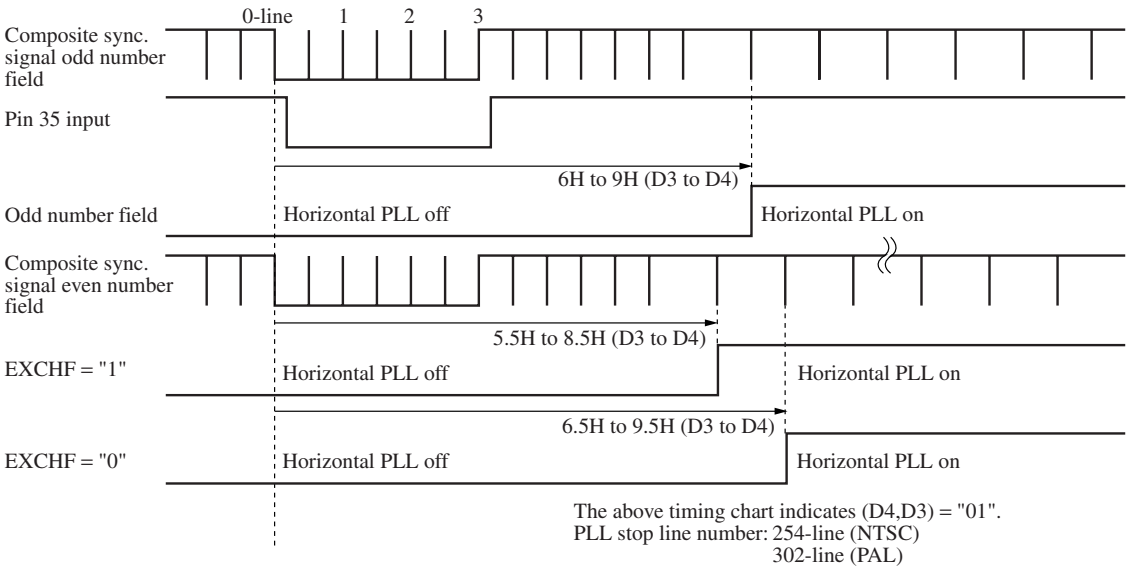
The pin 31 timing is synchronous with the pin 35 input timing.
The above timing chart is just for your reference.

■ Technical Data (continued)

1. Three-wire control mode (continued)

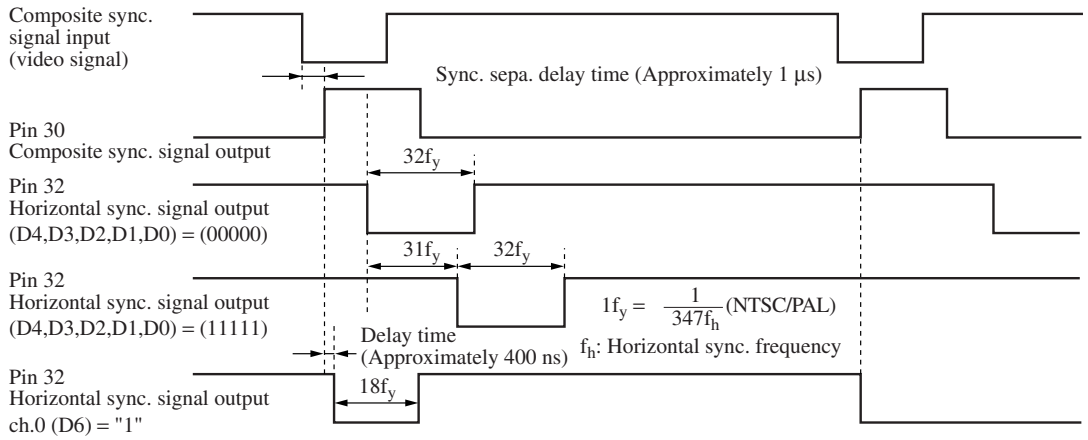
4) Mode setup channel bit-map. (continued)

- Horizontal PLL start position adjustment range



- ch.1: Horizontal sync. output position adjustment

D11	D10	D9	D8	D7 V Mode	D6 YUV	D5 RGB	D4	D3	D2	D1	D0
1	0	0	0	—	—	0	Video signal input display mode				
				—	—	1	Analog RGB input display mode				
				—	0	Chroma signal input mode					
				—	1	Color-difference signal input mode					
				0	PAL						
				1	NTSC						



The delay time of pin 30 output to video signal is likely to vary according to an external constant connected to pin 45. For an external constant, you are required to evaluate adequately the characteristics in weak electric field. Though the horizontal sync signal output adjustment range is designed by referring to the center of pin 30 output pulse, there would be some error according to VCO free-run frequency.

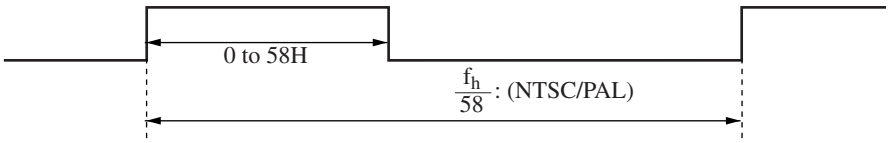
■ Technical Data (continued)

1. Three-wire control mode (continued)

4) Mode setup channel bit-map. (continued)

• ch.2: PWM duty adjustment

D11	D10	D9	D8	D7 P mode	D6 YC mode	D5	D4	D3	D2	D1	D0
0	1	0	0	—	0	Composite input mode					
				—	1	Component input mode					
				0	STD PAL mode						
				1	Quasi PAL/NTSC mode						



Note that adjustment characteristics come to discontinuation around max. Duty.

(D5,D4,D3,D2,D1,D0) = (000000): t_w = 1H
= (000001): t_w = 3H
= (000010): t_w = 4H
= (110110): t_w = 56H
= (110111): t_w = 56H
= (111000): t_w = 0H
= (111001): t_w = 58H

• ch.3: Common pulse amplitude adjustment

D11	D10	D9	D8	D7 OSD	D6	D5	D4	D3	D2	D1	D0
1	1	0	0	0	Analog OSD signal input mode						
				1	Digital OSD signal input mode						

• ch.5: Color gain adjustment

D11	D10	D9	D8	D7 HTS	D6	D5	D4	D3	D2	D1	D0
1	0	1	0	0	1H reverse inhibit mode						
				1	1H reverse mode						

• ch.6: Hue adjustment

D11	D10	D9	D8	D7 CP	D6	D5	D4	D3	D2	D1	D0
0	1	1	0	0	External clamp pulse input mode						
				1	Internal clamp (pedestal) mode						

■ Technical Data (continued)

1. Three-wire control mode (continued)

4) Mode setup channel bit-map. (continued)

• ch.9: Y-aperture gain adjustment

D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
1	0	0	1	00h, 01h: Test mode							

• ch.15: RGB contrast adjustment

D11	D10	D9	D8	D7 POL mode	D6	D5	D4	D3	D2	D1	D0
1	1	1	1	0	Internal POL 1H reverse mode						
				1	External POL 1H reverse mode						

2. I²C control mode

A serial data is capable of transferring 9-bit unit of 8-bit transfer data and 1-bit answering data using two kinds of signal lines of data and shift clock.

When a slave address after setting a start condition matches the address on the IC side, you can receive the data to be transmitted from then. Once the stop condition is set up, the next transmitting data will be ignored until the start condition is set up.

There are two kinds of transfer mode: an auto-increment mode which does not transmit sub-address, and data upgrade mode which transmits sub-address + data by 2 bites.

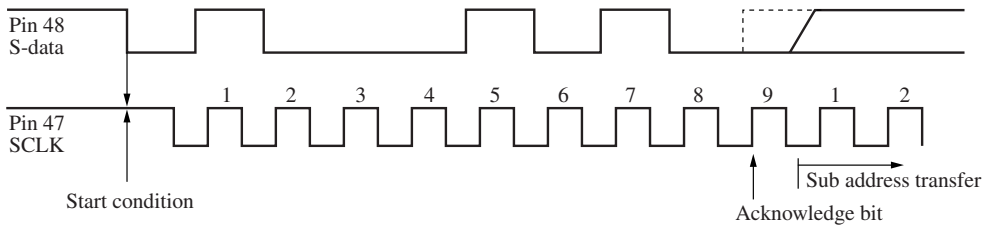
The typical models of transmitting sequence are shown below:

1) Start condition

When the S data changes from high-level to low-level at SCLK = high-level, a data receiving mode becomes available.

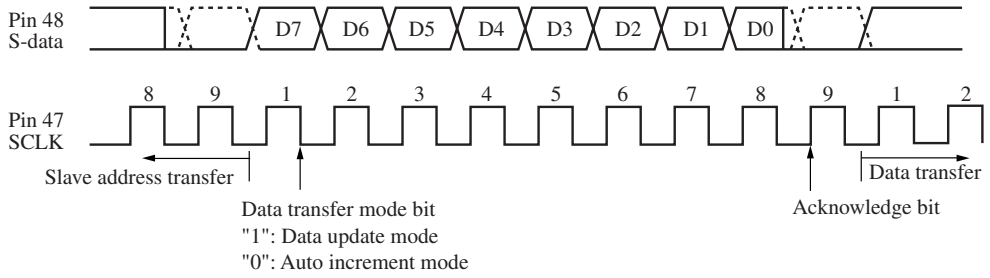
2) Slave address transfer

The slave address of the AN2526NFH is 88h at pin 49 = high-level and 8Ah at pin 49 = low-level.



3) Sub address transfer

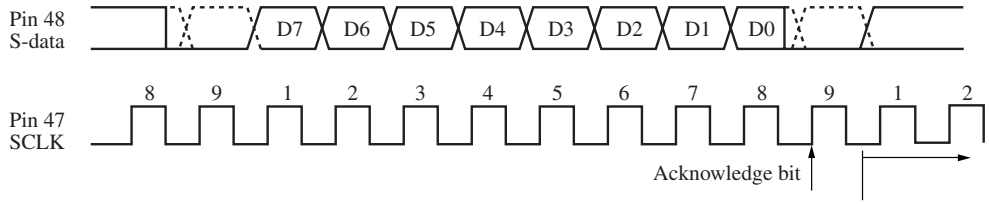
When a data transfer mode bit is 0, all the serial data columns transferred until a stop condition is set is regarded as the data block.



■ Technical Data (continued)

2. I²C control mode (continued)

4) Data transfer



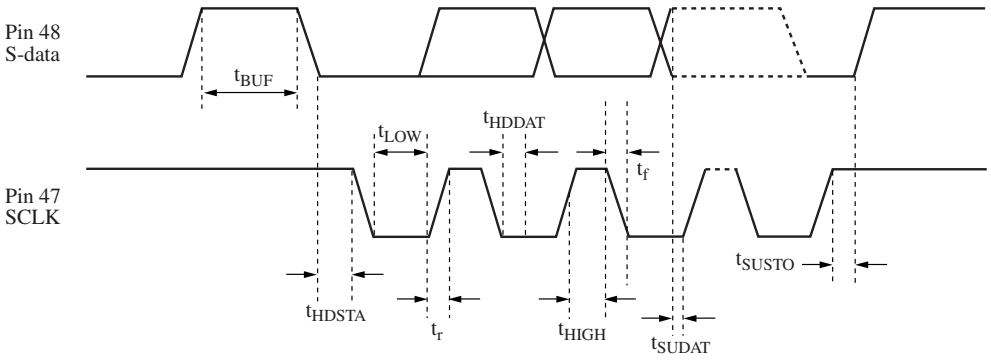
At auto increment mode: Data transfer
At data update mode: Sub address transfer

5) Stop condition

When S-data changes from low-level to high-level at SCLK = high-level, data reception is halted.

6) Pulse timing

Timing chart expanded diagram



Parameter	Symbol	Min	Typ	Max	Unit
SCLK clock frequency	t_{SCL}	0	—	400	kHz
Bus free-time for stop condition and start condition	t_{BUF}	1.3	—	—	µs
Hold time start condition	t_{HDSTA}	0.6	—	—	µs
SCLK clock low-state hold time	t_{LOW}	1.3	—	—	µs
SCLK clock high-state hold time	t_{HIGH}	0.6	—	—	µs
Data hold time	t_{HDDAT}	0	—	—	µs
Data setup time	t_{SUDAT}	100	—	—	ns
S-data, SCLK signal rise time	t_r	—	—	300	ns
S-data, SCLK signal fall time	t_f	—	—	300	ns
Stop condition setup time	t_{SUSTO}	0.6	—	—	µs

■ Technical Data (continued)

2. I²C control mode (continued)

6) Pulse timing (continued)

D7	D6 to D4	D3	D2	D1	D0	Selection channel	EVR control function	Number of bit
Mode	Don't Care	0	0	0	0	0	Vertical sync. signal output position	3
		0	0	0	1	1	Horizontal sync. signal output position	5
		0	0	1	0	2	PWM duty	6
		0	0	1	1	3	Common pulse amplitude	7
		0	1	0	0	4	Y-gain	8
		0	1	0	1	5	Color gain	7
		0	1	1	0	6	Hue	7
		0	1	1	1	7	Black-limiter level	8
		1	0	0	0	8	Bright	8
		1	0	0	1	9	Y-aperture gain	8
		1	0	1	0	10	R-ch. sub bright	8
		1	0	1	1	11	B-ch. sub bright	8
		1	1	0	0	12	White peak limiter	8
		1	1	0	1	13	Gamma-1 Knee level	8
		1	1	1	0	14	Gamma-2 Knee level	8
		1	1	1	1	15	RGB contrast	7

In case that the ch. has 8 bits or less of data bit number, the data in the data block is used to set various modes.
The content of each mode setting is same as three-wire control mode

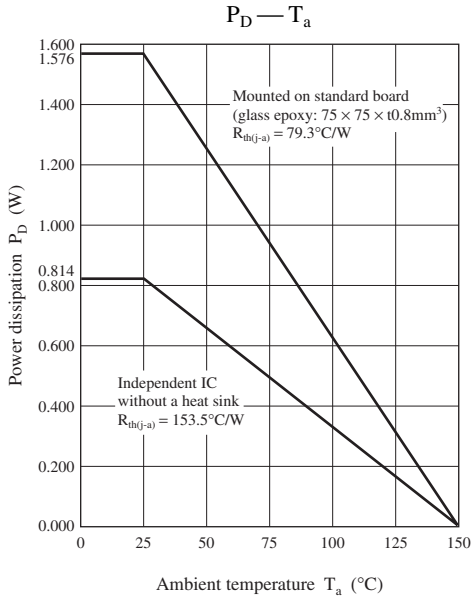
3. Recommended Operating Conditions

Parameter	Symbol	Range	Min	Typ	Max	Unit
Composite video input signal	Y_{IN}	Sync. chip - white	0.9	1.0	1.1	V[p-p]
Y-input signal voltage	Y_{IN}	Pedestal - white	0.6	0.7	0.8	V[p-p]
C-input signal voltage	C_{IN}	Burst signal amplitude	200	300	400	mV[p-p]
MOS input signal low-level voltage	V_{MOSL}		0	—	0.8	V
MOS input signal high-level voltage	V_{MOSH}		2.3	—	*1	V
Synchronous signal input	H_{SYNC}	Pedestal - sync. chip	0.2	0.3	0.4	V[p-p]
Serial data transfer frequency	f_{SD}		—	—	1.0	MHz
Analog RGB input signal	RGB_{IN}	Pedestal - white	0.6	0.7	0.8	V[p-p]

Note) *: Set it lower than V_{CC1} (Pin 1 voltage).

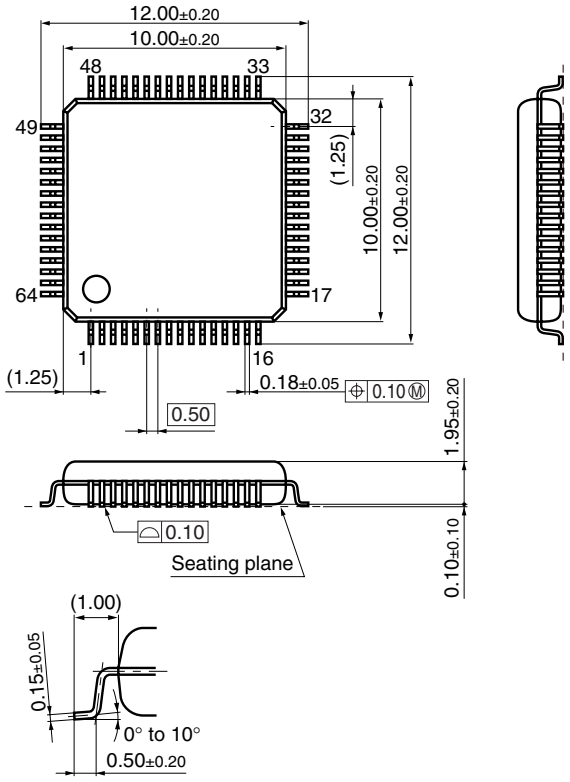
■ Technical Data (continued)

4. P_D — T_a curves of QFP064-P-1010



■ New Package Dimensions (Unit: mm)

• QFP064-P-1010A (Lead-free package)



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