

N-Channel Enhancement-Mode Vertical DMOS FET

Features

- Free from secondary breakdown
- ► Low power drive requirement
- Ease of paralleling
- ► Low C_{iss} and fast switching speeds
- Excellent thermal stability
- Integral source-drain diode
- ► High input impedance and high gain

Applications

- Motor controls
- Converters
- Amplifiers
- Switches
- Power supply circuits
- Drivers (relays, hammers, solenoids, lamps, memories, displays, bipolar transistors, etc.)

General Description

This enhancement-mode (normally-off) transistor utilizes a vertical DMOS structure and Supertex's well-proven, silicongate manufacturing process. This combination produces a device with the power handling capabilities of bipolar transistors and the high input impedance and positive temperature coefficient inherent in MOS devices. Characteristic of all MOS structures, this device is free from thermal runaway and thermally-induced secondary breakdown.

Supertex's vertical DMOS FETs are ideally suited to a wide range of switching and amplifying applications where very low threshold voltage, high breakdown voltage, high input impedance, low input capacitance, and fast switching speeds are desired.

Ordering Information

Device	Package	BV _{DSS} /BV _{DGS}	R _{DS(ON)}	l _{D(ON)}	
Device	TO-92	(V)	(max) (Ω)	(min) (mA)	
VN10K	VN10KN3-G	60	5.0	750	

For packaged products, -G indicates package is RoHS compliant ('Green'). Consult factory for die / wafer form part numbers.

Refer to Die Specification VF21 for layout and dimensions.

Absolute Maximum Ratings

Parameter	Value
Drain-to-source voltage	BV _{DSS}
Drain-to-gate voltage	BV _{DGS}
Gate-to-source voltage	±30V
Operating and storage temperature	-55°C to +150°C

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied. Continuous operation of the device at the absolute rating level may affect device reliability. All voltages are referenced to device ground.

Pin Configuration



Product Marking

SIVN 10K YYWW

YY = Year Sealed WW = Week Sealed ____ = "Green" Packaging

Package may or may not include the following marks: Si or

TO-92 (N3)

Thermal Characteristics

Package	I _D (continuous) [†] (mA)	I _D (pulsed) (A)	Power Dissipation @T _c = 25°C (W)	θ _{jc} (°C/W)	θ _{ja} (°C/W)	_{DR} † (mA)	I _{DRM} (A)
TO-92	310	1.0	1.0	125	170	310	1.0

Notes:

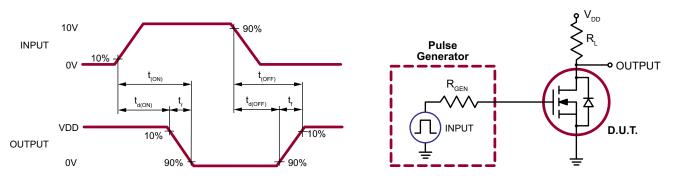
Electrical Characteristics (T_A = 25°C unless otherwise specified)

Sym	Parameter	Min	Тур	Max	Units	Conditions	
BV _{DSS}	Drain-to-source breakdown voltage	60	-	-	V	$V_{GS} = 0V, I_{D} = 100 \mu A$	
$V_{\rm GS(th)}$	Gate threshold voltage	0.8	-	2.5	V	$V_{GS} = V_{DS}$, $I_{D} = 1.0$ mA	
$\Delta V_{GS(th)}$	Change in V _{GS(th)} with temperature	-	-3.8	-	mV/°C	$V_{GS} = V_{DS}$, $I_{D} = 1.0$ mA	
I _{GSS}	Gate body leakage	-	-	100	nA	$V_{GS} = 15V, V_{DS} = 0V$	
		-	-	10		$V_{GS} = 0V, V_{DS} = 45V$	
I _{DSS}	Zero gate voltage drain current		-	500	μA	$V_{GS} = 0V, V_{DS} = 45V,$ $T_{A} = 125^{\circ}C$	
I _{D(ON)}	On-state drain current	0.75	-	-	Α	$V_{GS} = 10V, V_{DS} = 10V$	
D	Static drain to course an atota registeres	-	-	7.5	Ω	$V_{GS} = 5.0V, I_{D} = 200mA$	
R _{DS(ON)}	Static drain-to-source on-state resistance		-	5.0	12	$V_{GS} = 10V, I_{D} = 500mA$	
$\Delta R_{DS(ON)}$	Change in R _{DS(ON)} with temperature	-	0.7	-	%/°C	$V_{GS} = 10V, I_{D} = 500mA$	
G _{FS}	Forward transductance	100	-	-	mmho	$V_{DS} = 10V, I_{D} = 500mA$	
C _{ISS}	Input capacitance	-	48	60		V _{GS} = 0V,	
C _{oss}	Common source output capacitance	-	16	25	pF	$V_{DS} = 25V$,	
C _{RSS}	Reverse transfer capacitance	-	2.0	5.0		f = 1.0MHz	
t _(ON)	Turn-on time	-	-	10	ns	V _{DD} = 15V, I _D = 600mA,	
t _(OFF)	Turn-off time	-	-	10	113	$R_{GEN} = 25\Omega$	
V _{SD}	Diode forward voltage drop	-	8.0	-	V	$V_{GS} = 0V$, $I_{SD} = 500$ mA	
t _{rr}	Reverse recovery time	-	160	-	ns	$V_{GS} = 0V, I_{SD} = 500mA$	

Notes:

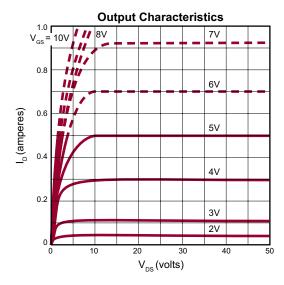
- 1. All D.C. parameters 100% tested at 25°C unless otherwise stated. (Pulse test: 300µs pulse, 2% duty cycle.)
- 2. All A.C. parameters sample tested.

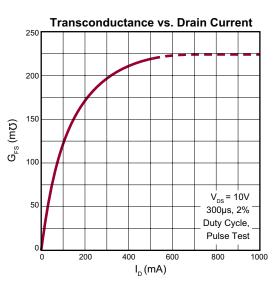
Switching Waveforms and Test Circuit

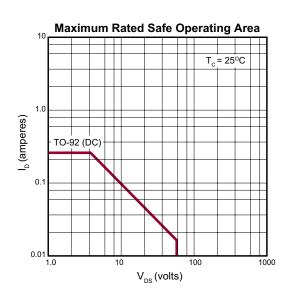


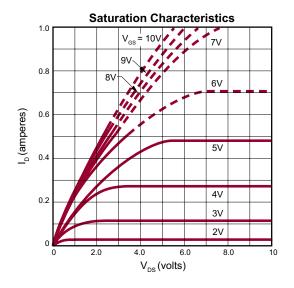
 $[\]dagger$ I_D (continuous) is limited by max rated T_i. (VN0106N3 can be used if an I_D (continuous) of 500mA is needed.)

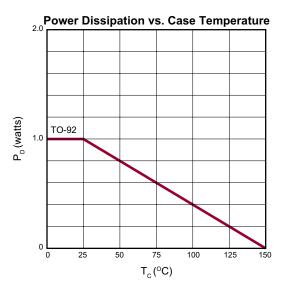
Typical Performance Curves

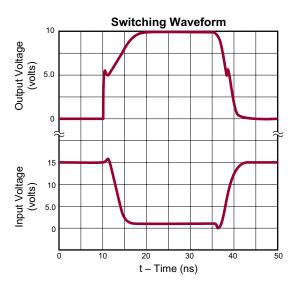




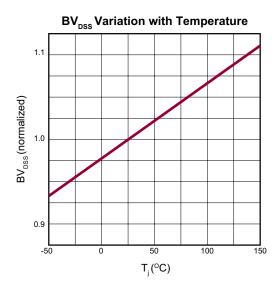


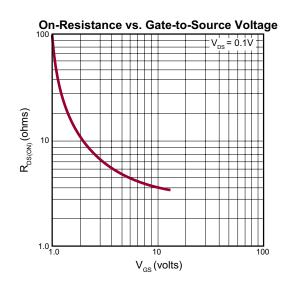


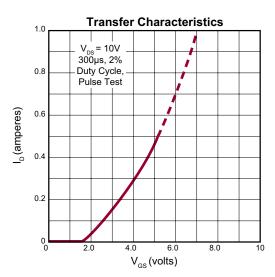


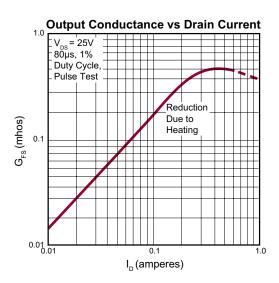


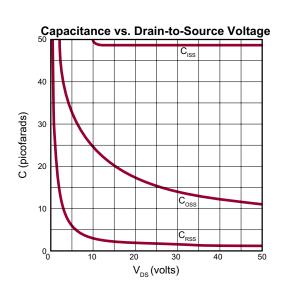
Typical Performance Curves (cont.)

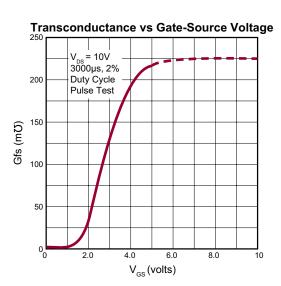




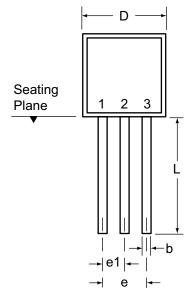


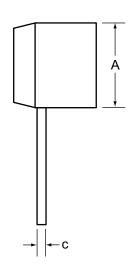






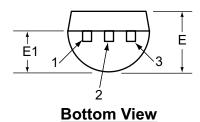
3-Lead TO-92 Package Outline (N3)





Front View

Side View



Symbol		Α	b	С	D	E	E1	е	e1	L
Dimensions (inches)	MIN	.170	.014 [†]	.014 [†]	.175	.125	.080	.095	.045	.500
	NOM	-	-	-	-	-	-	-	-	-
	MAX	.210	.022 [†]	.022 [†]	.205	.165	.105	.105	.055	.610*

JEDEC Registration TO-92.

Drawings not to scale.

Supertex Doc.#: DSPD-3TO92N3, Version E041009.

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to http://www.supertex.com/packaging.html.)

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^{*} This dimension is not specified in the JEDEC drawing.

[†] This dimension differs from the JEDEC drawing.

Mouser Electronics

Authorized Distributor

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Supertex:

<u>VN10KN3-P002-G</u> <u>VN10KN3-P014-G</u> <u>VN10KN3-G</u> <u>VN10KN3-P003</u> <u>VN10KN3-P002</u> <u>VN10KN3-P013</u> <u>VN10KN3-P013</u> <u>VN10KN3-P013</u> <u>VN10KN3-P003-G</u>