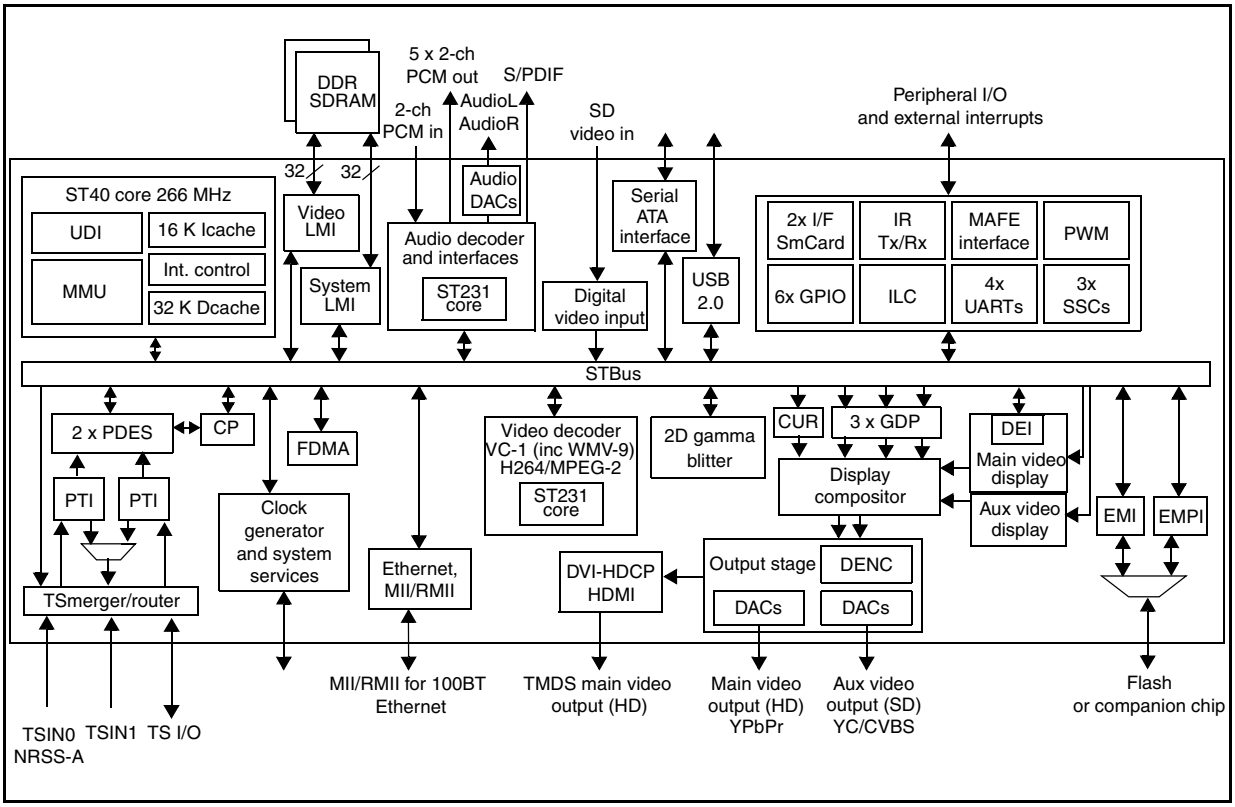
STi7109

Low-cost HDTV set-top box decoder for H.264 and Microsoft WMA9

Data Brief

Features

- The STi7109 is a single-chip, high-definition video decoder including:
  - Microsoft® VC-1, WMA9 and H.264 support
  - Linux®, Windows® CE and OS21 compatible ST40 CPU core: 266 MHz
  - transport filtering and descrambling
  - video decoder: VC-1 (including WMA 9), H.264 (MPEG-4 part 10) and MPEG-2
  - SVP compliant
  - Windows® DRM support
  - graphics engine and dual display: standard and high-definition
  - audio decoder: including Windows Media® Audio 9 (WMA-9) and WMA-9 Pro
  - DVD data retrieval and decryption
- The STi7109 also features the following embedded interfaces:
  - USB 2.0 host controller/PHY interface
  - DVI/HDMI™ output
  - digital audio and video auxiliary inputs
  - low-cost modem
  - 100BT ethernet controller with integrated MAC and MII/RMII interface for external PHY
  - serial ATA (SATA)



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1 Description

The STi7109 is a new generation, high-definition set-top box / DVD decoder chip, and provides very high performance for low-cost HD systems. STi7109 includes both Windows Media Video 9 and H.264 video decoders for new, low bit rate applications.

Based on the Omega2 (STBus) architecture, this system-on-chip is a full back-end processor for digital terrestrial, satellite, cable, DSL and IP client high-definition set-top boxes, compliant with ATSC, SMPTE VC-1, DVB, DIRECTV, DCII, OpenCable and ARIB BS4 specifications. It includes all processing for DVD applications.

The STi7109 demultiplexes, decrypts and decodes HD or SD video streams with associated multichannel audio. Video is output to two independently formatted displays: a full resolution display intended for a TV monitor, and a downsampled display intended for a VCR or DVD-R. Connection to a TV or display panel can be analog through the DACs, or digital through a copy protected DVI/HDMI. Composite outputs are provided for connection to the VCR with Macrovision protection. Audio is output with optional PCM mixing to an S/PDIF interface, PCM interface, or through integrated stereo audio DACs.

Digitized analog programs can also be input to the STi7109 for reformatting and display.

The STi7109 includes a graphics rendering and display capability with a 2D graphics accelerator, three graphics planes and a cursor plane. A dual display compositor provides mixing of graphics and video with independent composition for each of the TV and VCR/DVD-R outputs.

The STi7109 includes a stream merger to allow seven different transport streams from different sources to be merged and processed concurrently. Applications include DVR time-shifted viewing of a terrestrial program, while acquiring an EPG/data stream from a satellite or cable front end.

The flexible descrambling engine is compatible with required standards including DVB, DES, AES and Multi2.

The STi7109 embeds a 266 MHz ST40-202 CPU for applications and device control. A dual DDR1 SDRAM memory interface is used for higher performance, to allow the video decoder the required memory bandwidth for VC-1/HD H.264 and sufficient bandwidth for the CPU and the rest of the system. A second memory bus is also provided for flash memory, storing resident software, and for connection of peripherals. This bus also has a high speed synchronous mode that can be used to exchange data between two STi7109 devices. This can be used to connect a second STi7109 as a co-decoder for a dual TV STB application.

A hard-disk drive (HDD) can be connected either to the serial ATA interface, or as an expansion drive through the USB 2.0 port.

For IP-TV applications, the integrated 100BT Ethernet controller and MII/RMII interface can be used for generic Ethernet delivery, as shown in *Figure 4: Low-cost HD IP-TV set-top box with HDD on page 4*.

The USB or Ethernet interfaces can also be used to connect to a DOCSIS 2.0 CM gateway for interactive cable applications.

The STi7109 is supported by STMicroelectronics' STAPI software, and is compatible with the STx7100 and STi7710.

Figure 1. Low-cost satellite HD set-top box

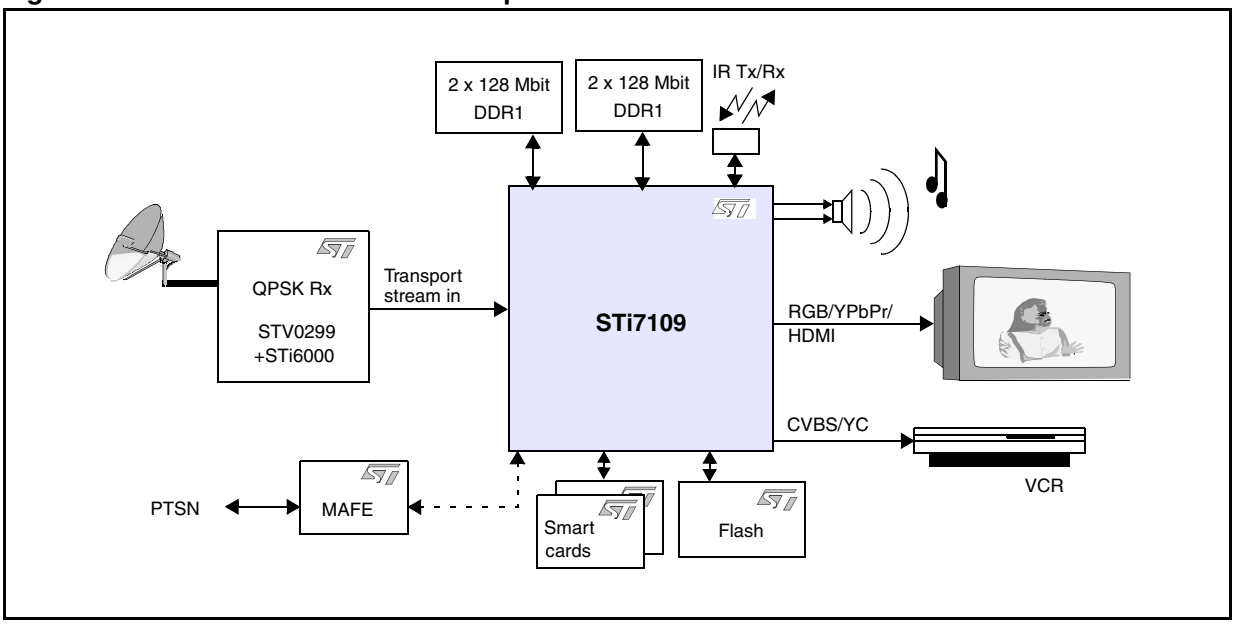


Figure 2. Low-cost cable HD set-top box with return channel

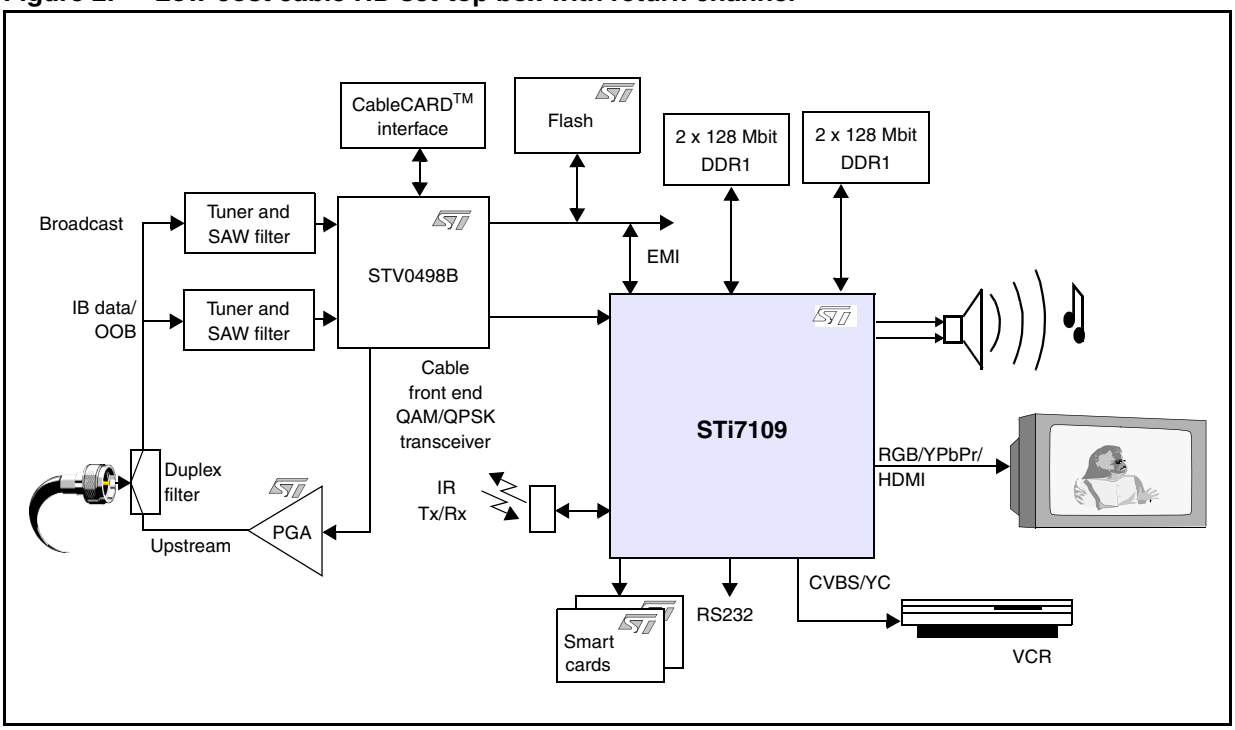


Figure 3. Low-cost dual satellite and terrestrial HD set-top box with HDD and DVD

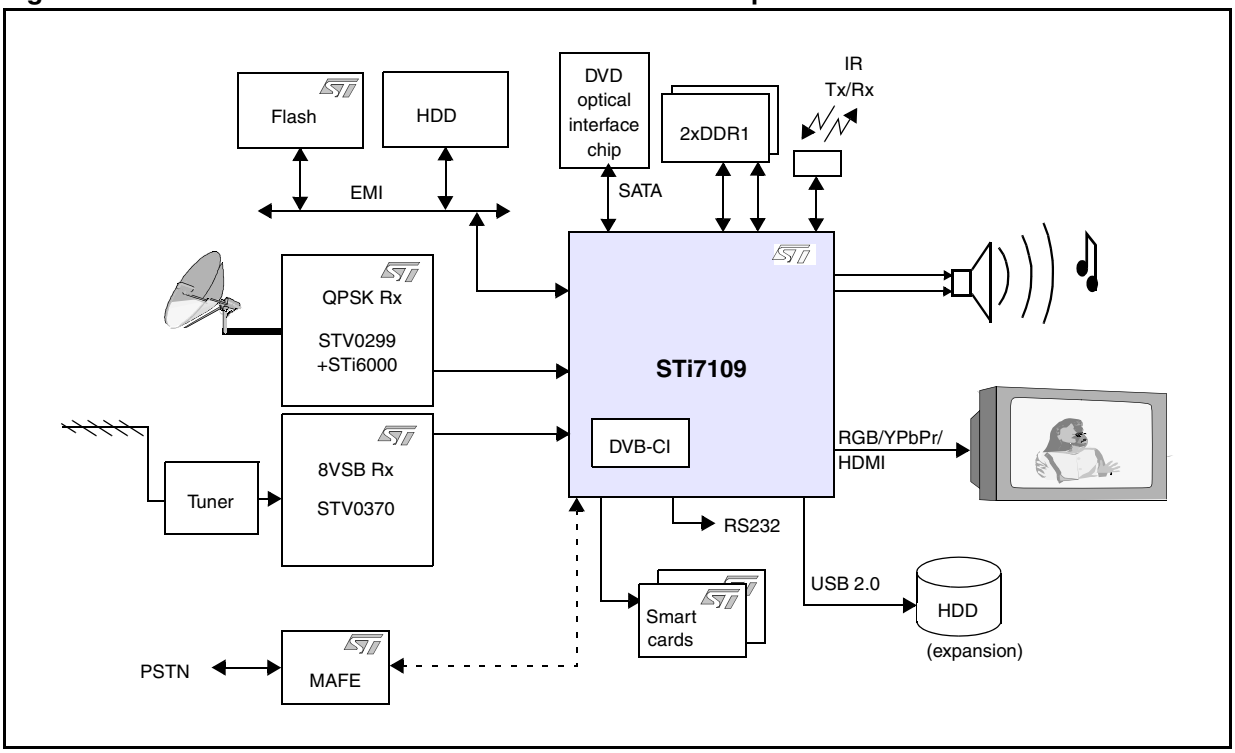
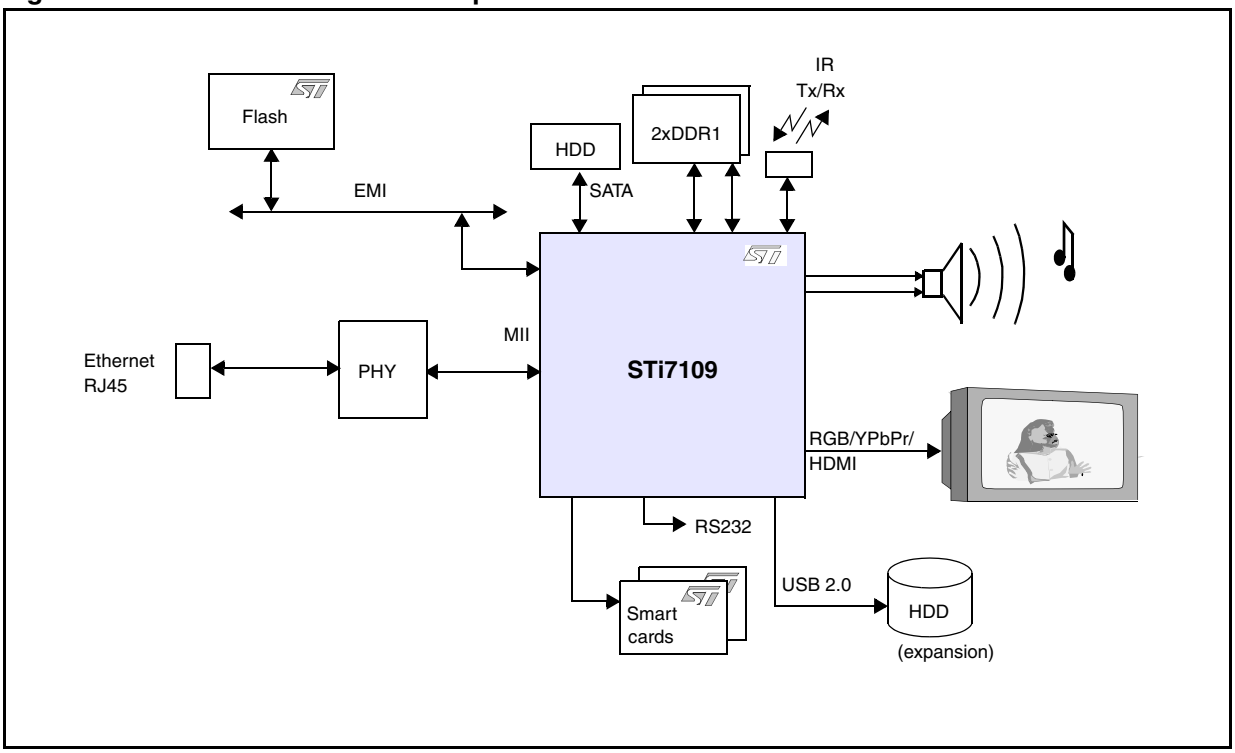


Figure 4. Low-cost HD IP-TV set-top box with HDD



1.1 Detailed features list

1.1.1 Processor subsystem

- ST40 32-bit superscaler RISC CPU
  - 266 MHz, 2-way set associative 16-Kbyte ICache, 32-Kbyte DCache, MMU
  - 5-stage pipeline, delayed branch support
  - floating point unit, matrix operation support
  - debug port, interrupt controller

1.1.2 Transport subsystem

- TS merger/router
  - 2 serial/parallel inputs
  - 1 bidirectional interface
  - merging of 3 external transport streams
  - transport streams from memory support
  - NRSS-A module interface
  - TS routing for DVB-CI and CableCARD™ modules
- Programmable transport interfaces (PTIs)
  - two programmable transport interfaces
  - two transport stream demultiplexers: DVB, DIRECTV®, ATSC, ARIB, OpenCable, DCII
  - integrated DES, AES, DVB and Multi2 descramblers
  - NDS random access scrambled stream protocol (RASP) compliant
  - NDS ICAM CA
  - support for VGS, Passage and DVS042 residue handling

1.1.3 Video/graphics subsystem

- Microsoft VC-1 MP@HL (WMV 9) and AP@L3/H.264(MPEG-4 part 10) main and high profile level 4.1/MPEG-2 MP@HL video decoder
  - advanced error concealment and trick mode support
  - dual MPEG-2 MP@HL decode
- SD (standard package) or HD/SD (extended package) digital video input
- Displays
  - one HD display multi format capable (1080I, 720P, 480P/576P, 480I/576I)
    - analog HD output RGB or YPbPr
    - HDMI encoded output
  - one standard-definition display
    - analog SD output: YPbPr or YC and CVBS
- Gamma 2D/3D graphics processor
  - triple source 2D gamma blitter engine
  - alpha blending and logical operations
  - color space and format conversion

  - fast color fill
  - arbitrary resizing with high quality filters
  - acceleration of direct drawing by CPU
- Gamma compositor and video processor
  - 7-channel mixer for high definition output
  - independent 2-channel mixer for SD output
  - 3 graphic display planes
  - high-quality video scaler
  - motion and detail adaptive deinterlacer
  - linear resizing and format conversions
  - horizontal and vertical filtering
- Copy protection
  - HDMI/HDCP copy protection hardware
  - SVP compliant
  - Macrovision® copy protection for 480I, 480P, 576I, 576P outputs
  - DTCP-IP
  - AWG-based DCS analog copy protection

1.1.4 Audio subsystem

- Digital audio decoder
  - support for all the most popular audio standards including WMA-9, WMA-9 Pro, MPEG-1 layer I/II, MPEG-2 layer II, MPEG-2 AAC, MPEG-4 AAC LC 2-channel/5.1 channel MPEG-4 AAC+SBR 2-channel/5.1 channel, Dolby® Digital EX, Pro Logic® II, MLP™ and DTS®
  - PCM mixing with internal or external source and sample rate conversion
  - 6- to 2-channel downmixing
  - PCM audio input
  - independent multichannel PCM output, S/PDIF output and analog output
- Stereo 24-bit audio DAC for analog output
- IEC958/IEC1937 digital audio output interface (S/PDIF)
- CSS/CPxM copy protection hardware

1.1.5 Interfaces

- External memory interface (EMI)
  - 16-bit interface supporting ROM, flash, SFlash, SRAM, peripherals
  - access in 5 banks
  - high speed synchronous mode for interconnecting two STi7109 devices
- External microprocessor interface (EMPI)
  - 32-bit MPX satellite, target-only interface,
  - synchronous operation at MPX clock speed, capable of 100 MHz,
- Dual local memory interface (LMI)
  - dual interface (2 x 32-bit) for DDR1 200-MHz (DDR400) memories, supports 128-, 256- and 512-Mbit devices
- USB 2.0 host controller/PHY interface
- Serial ATA hard-disk drive support
  - record and playback with trick modes
  - pause and time shifting, watch and record
- 100BT Ethernet controller, MAC and MII/RMII
- On-chip peripherals
  - 4 ASCs (UARTs) with Tx and Rx FIFOS, two of which can be used in smartcard interfaces
  - 2 smartcard interfaces and clock generators (improved to reduce external circuitry)
  - 3 SSCs for I²C/SPI master slaves interfaces
  - serial communications interface (SCIF)
  - 2 PWM outputs
  - teletext serializer and DMA module
  - 6 banks of general purpose I/O, 3.3 V tolerant
  - SiLabs line-side (DAA) interface
  - modem analog front end (MAFE) interface
  - infrared transmitter/receiver supporting RC5, RC6 and RECS80 codes
  - UHF remote receiver input interface
  - interrupt level controller and external interrupts, 3.3 V tolerant
  - low power/RTC/watchdog controller
  - integrated VCXO
  - DiSEqC 2.0 interface
  - PWM capture/compare functions
- Flexible multi-channel DMA

1.1.6 Services and package

- JTAG/TAP interface, ST40 toolset support, ST231 toolset support
- Two package options
  - 35 x 35 PBGA, 580 + 100 balls (standard version)
  - 35 x 35 PBGA 708 + 84 balls (extended version)

2 Revision history

Table 1. Document revision history

Date	Revision	Changes
19-Dec-2006	2	Rewritten to include latest information and corrected product code.
10-Sep-2005	1	Initial release.

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