128Kx32 SSRAM/4Mx32 SDRAM

*Advanced**

External Memory Solution for Texas Instruments TMS320C6000 DSP

FEATURES

- Clock speeds:
  - SSRAM: 200, 166,150, and 133 MHz
  - SDRAMs: 125 and 100 MHz
- DSP Memory Solution
  - Texas Instruments TMS320C6201
  - Texas Instruments TMS320C6701
- Packaging:
  - 153 pin BGA, JEDEC MO-163
- 3.3V Operating supply voltage
- Direct control interface to both the SSRAM and SDRAM ports on the "C6x"
- Common address and databus
- 65% space savings vs. monolithic solution
- Reduced system inductance and capacitance

DESCRIPTION

The WED9LC6416VxxBC is a 3.3V, 128K x 32 Synchronous Pipeline SRAM and a 4Mx32 Synchronous DRAM array constructed with one 128K x 32 SBSRAM and two 4Mx16 SDRAM die mounted on a multilayer laminate substrate. The device is packaged in a 153 lead, 14mm by 22mm, BGA.

The WED9LC6416VxxBC provides a total memory solution for the Texas Instruments TMS320C6201 and the TMS320C6701 DSPs

The Synchronous Pipeline SRAM is available with clock speeds of 200, 166,150, and 133 MHz, allowing the user to develop a fast external memory for the SSRAM interface port .

The SDRAM is available in clock speeds of 125 and 100 MHz, allowing the user to develop a fast external memory for the SDRAM interface port .

The WED9LC6416V is available in both commercial and industrial temperature ranges.

* This data sheet describes a product that may or may not be under development and is subject to change or cancellation without notice.

FIG. 1 PIN CONFIGURATION

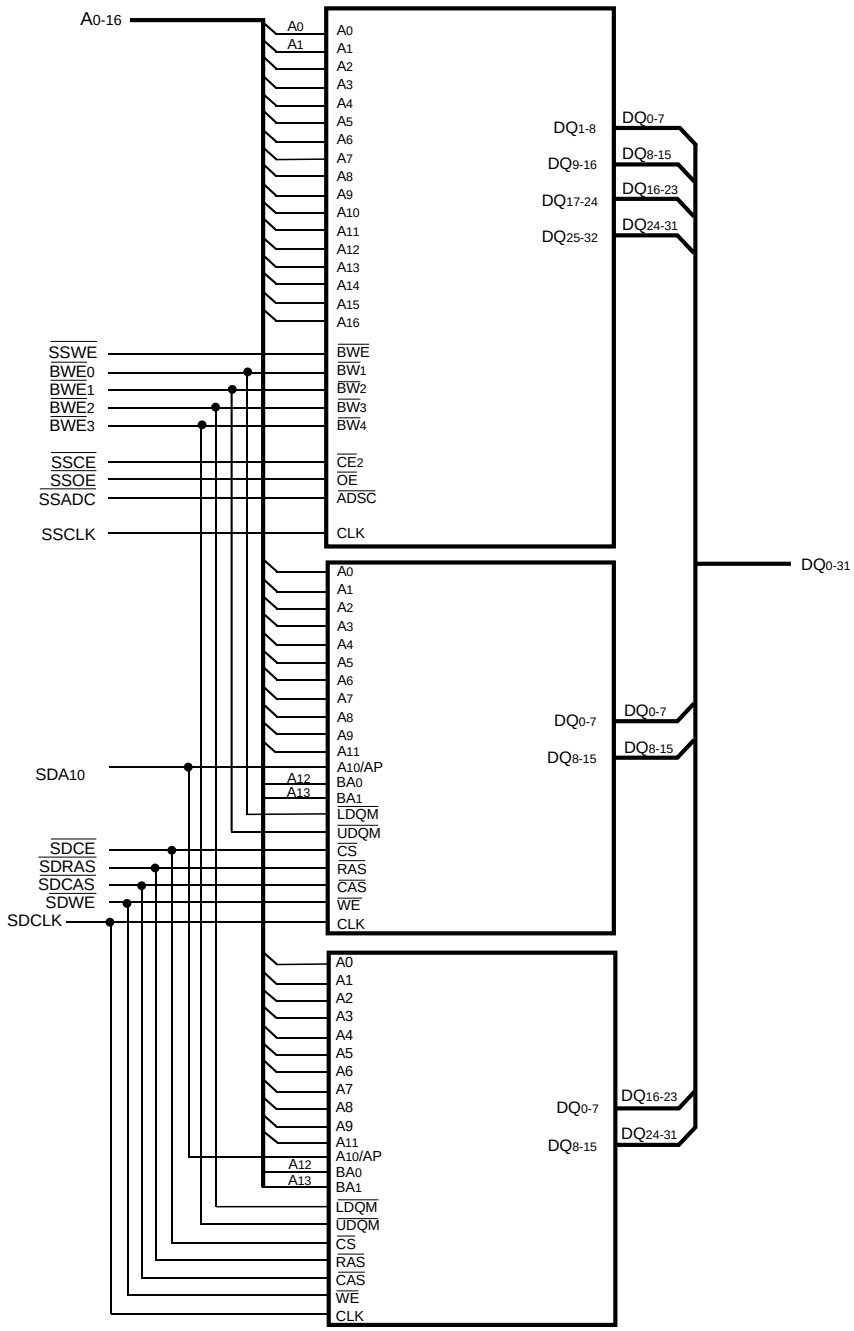
TOP VIEW

	1	2	3	4	5	6	7	8	9	
A	DQ_{19}	DQ_{23}	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	DQ_{24}	DQ_{28}	A
B	DQ_{18}	DQ_{22}	V_{CC}	V_{SS}	$\overline{SDCE}$	V_{SS}	V_{CC}	DQ_{25}	DQ_{29}	B
C	V_{CCQ}	V_{CCQ}	V_{CC}	$\overline{SDWE}$	SDA_{10}	NC	V_{CC}	V_{CCQ}	V_{CCQ}	C
D	DQ_{17}	DQ_{21}	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	DQ_{26}	DQ_{30}	D
E	DQ_{16}	DQ_{20}	V_{CC}	V_{SS}	SDCLK	V_{SS}	V_{CC}	DQ_{27}	DQ_{31}	E
F	V_{CCQ}	V_{CCQ}	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	V_{CCQ}	V_{CCQ}	F
G	NC	NC	NC	$\overline{SDRAS}$	$\overline{SDCAS}$	V_{SS}	A_2	A_4	A_5	G
H	NC	NC	A_8	V_{SS}	V_{SS}	NC	A_1	A_3	A_{10}	H
J	A_6	A_7	A_9	V_{SS}	V_{SS}	NC	A_0	A_{11}	A_{12}	J
K	NC / A_{17}	NC / A_{18}	NC / A_{19}	V_{SS}	V_{SS}	NC	NC	A_{13}	A_{14}	K
L	NC	NC	NC	$\overline{BWE_2}$	$\overline{BWE_3}$	NC	NC	A_{15}	A_{16}	L
M	V_{CCQ}	V_{CCQ}	V_{CC}	$\overline{BWE_0}$	$\overline{BWE_1}$	NC	V_{CC}	V_{CCQ}	V_{CCQ}	M
N	DQ_{12}	DQ_{11}	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	DQ_4	DQ_0	N
P	DQ_{13}	DQ_{10}	V_{CC}	V_{SS}	SSCLK	V_{SS}	V_{CC}	DQ_5	DQ_1	P
R	V_{CCQ}	V_{CCQ}	V_{CC}	V_{SS}	V_{SS}	V_{SS}	V_{CC}	V_{CCQ}	V_{CCQ}	R
T	DQ_{14}	DQ_9	V_{CC}	$\overline{SSADC}$	$\overline{SSWE}$	NC	V_{CC}	DQ_6	DQ_2	T
U	DQ_{15}	DQ_8	V_{CC}	$\overline{SSOE}$	$\overline{SSCE}$	NC	V_{CC}	DQ_7	DQ_3	U
	1	2	3	4	5	6	7	8	9	

PIN DESCRIPTION

$A_{0\text{-}16}$	Address Bus
$DQ_{0\text{-}31}$	Data Bus
SSCLK	SSRAM Clock
$\overline{SSADC}$	SSRAM Address Status Control
$\overline{SSWE}$	SSRAM Write Enable
$\overline{SSOE}$	SSRAM Output Enable
SDCLK	SDRAM Clock
$\overline{SDRAS}$	SDRAM Row Address Strobe
$\overline{SDCAS}$	SDRAM Column Address Strobe
$\overline{SDWE}$	SDRAM Write Enable
SDA_{10}	SDRAM Address 10/auto precharge
$\overline{BWE}_{0\text{-}3}$	SSRAM Byte Write Enables SDRAM SDQM 0 - 3
$\overline{SSCE}$	Chip Enable SSRAM Device
$\overline{SDCE}$	Chip Enable SDRAM Device
V_{CC}	Power Supply pins, 3.3V
V_{CCQ}	Data Bus Power Supply pins, 3.3V (2.5V future)
V_{SS}	Ground
NC	No Connect

FIG. 2 BLOCK DIAGRAM



OUTPUT FUNCTIONAL DESCRIPTIONS

Symbol	Type	Signal	Polarity	Function
SSCLK	Input	Pulse	Positive Edge	The system clock input. All of the SSRAM inputs are sampled on the rising edge of the clock.
$\overline{\text{SSADS}}$ $\overline{\text{SSOE}}$ $\overline{\text{SSWE}}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{\text{SSADS}}$, $\overline{\text{SSOE}}$, and $\overline{\text{SSWE}}$ define the operation to be executed by the SSRAM.
$\overline{\text{SSCE}}$	Input	Pulse	Active Low	$\overline{\text{SSCE}}$ disable or enable SSRAM device operation.
SDCLK	Input	Pulse	Positive Edge	The system clock input. All of the SDRAM inputs are sampled on the rising edge of the clock.
SDCE	Input	Pulse	Active Low	SDCE disable or enable device operation by masking or enabling all inputs except SDCLK and BWE_{0-3}.
$\overline{\text{SDRAS}}$ $\overline{\text{SDCAS}}$ $\overline{\text{SDWE}}$	Input	Pulse	Active Low	When sampled at the positive rising edge of the clock, $\overline{\text{SDCAS}}$, $\overline{\text{SDRAS}}$, and $\overline{\text{SDWE}}$ define the operation to be executed by the SDRAM.
A_{0-16}, SDA_{10}	Input	Level	—	Address bus for SSRAM and SDRAM A_0 and A_1 are the burst address inputs for the SSRAM During a Bank Active command cycle, A_{0-11}, SDA_{10} defines the row address (RA_{0-10}) when sampled at the rising clock edge. During a Read or Write command cycle, A_{0-7} defines the column address (CA_{0-7}) when sampled at the rising clock edge. In addition to the row address, SDA_{10} is used to invoke Autoprecharge operation at the end of the Burst Read or Write Cycle. If SDA_{10} is high, autoprecharge is selected and A_{12} and A_{13} define the bank to be precharged. If SDA_{10} is low, autoprecharge is disabled. During a Precharge command cycle, SDA_{10} is used in conjunction with A_{12} and A_{13} to control which bank(s) to precharge. If SDA_{10} is high, all banks will be precharged regardless of the state of A_{12} and A_{13}. If SDA_{10} is low, then A_{12} and A_{13} are used to define which bank to precharge.
DQ_{0-31}	Input Output	Level	—	Data Input/Output are multiplexed on the same pins.
BWE_{0-3}	Input	Pulse		BWE_{0-3} perform the byte write enable function for the SSRAM and DQM function for the SDRAM. BWE_0 is associated with DQ_{0-7}, BWE_1 with DQ_{8-15}, BWE_2 with DQ_{16-23} and BWE_3 with DQ_{24-31}.
Vcc, Vss	Supply			Power and ground for the input buffers and the core logic.
V_{CCQ}	Supply			Data base power supply pins, 3.3V (2.5V future).

ABSOLUTE MAXIMUM RATINGS

Voltage on Vcc Relative to Vss	-0.5V to +4.6V
Vin (DQx)	-0.5V to Vcc +0.5V
Storage Temperature (BGA)	-55°C to +125°C
Junction Temperature	+175°C
Short Circuit Output Current	100 mA

*Stress greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions greater than those indicated in operational sections of this specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

RECOMMENDED DC OPERATING CONDITIONS

(V_{CC} = 3.3V -5% / +10% unless otherwise noted;
0°C ≤ T_A ≤ 70°C, Commercial; -40°C ≤ T_A ≤ 85°C, Industrial)

Parameter	Symbol	Min	Max	Units
Supply Voltage (1)	V_{CC}	3.135	3.6	V
Input High Voltage (1,2)	V_{IH}	2.0	V_{CC} +0.3	V
Input Low Voltage (1,2)	V_{IL}	-0.3	0.8	V
Input Leakage Current 0 ≤ V_{IN} ≤ Vcc	I_{LI}	-10	10	µA
Output Leakage (Output Disabled) 0 ≤ V_{IN} ≤ Vcc	I_{LO}	-10	10	µA
Output High (I_{OH} = -4mA) (1)	V_{OH}	2.4	—	V
Output Low (I_{OL} = 8mA) (1)	V_{OL}	—	0.4	V

NOTES:
1. All voltages referenced to Vss (GND).
2. Overshoot: V_{IH} ≤ +6.0V for t ≤ t_{KC}/2
   Underershoot: V_{IL} ≥ -2.0V for t ≤ t_{KC}/2

DC ELECTRICAL CHARACTERISTICS

(V_{CC} = 3.3V -5% / +10% unless otherwise noted; 0°C ≤ T_A ≤ 70°C, Commercial; -40°C ≤ T_A ≤ 85°C, Industrial)

Description	Conditions	Symbol	Frequency	Typ	Max	Units
Power Supply Current: Operating (1,2,3)	SSRAM Active / DRAM Auto Refresh	I_{CC1}	133MHz	400	550	mA
			150MHz	450	580	
			166MHz	500	625	
			200MHz	550	700	
Power Supply Current Operating (1,2,3)	SSRAM Active / DRAM Idle	I_{CC2}	133MHz	300	450	mA
			150MHz	350	480	
			166MHz	400	525	
			200MHz	450	585	
Power Supply Current Operating (1,2,3)	SDRAM Active / SSRAM Idle	I_{CC3}	83MHz	220	240	mA
			100MHz	235	250	
			125MHz	255	280	
CMOS Standby	$\overline{SSCE}$ and $\overline{SDCE}$ ≤ Vcc -0.2V, All other inputs at Vss +0.2 ≤ V_{IN} or V_{IN} ≤ Vcc -0.2V, Clk frequency = 0	I_{SB1}		20.0	40.0	mA
TTL Standby	$\overline{SSCE}$ and $\overline{SDCE}$ ≤ V_{IH} min All other inputs at V_{IL} max ≤ V_{IN} or V_{IN} ≤ Vcc -0.2V, Clk frequency = 0	I_{SB2}		30.0	55.0	mA
Auto Refresh		I_{CC5}		190	250	mA

NOTES:
1. I_{CC} (operating) is specified with no output current. I_{CC} (operating) increases with faster cycle times and greater output loading.
2. "Device idle" means device is deselected ($\overline{CE}$ ≥ V_{IH}) Clock is running at max frequency and Addresses are switching each cycle.
3. Typical values are measured at 3.3V, 25°C. I_{CC} (operating) is specified at specified frequency.

BGA CAPACITANCE

Description	Conditions	Symbol	Typ	Max	Units
Address Input Capacitance (1)	T_A = 25°C; f = 1MHz	C_I	5	8	pF
Input/Output Capacitance (DQ) (1)	T_A = 25°C; f = 1MHz	C_O	8	10	pF
Control Input Capacitance (1)	T_A = 25°C; f = 1MHz	C_A	5	8	pF
Clock Input Capacitance (1)	T_A = 25°C; f = 1MHz	C_{CK}	4	6	pF

NOTE:
1. This parameter is sampled.

SSRAM AC CHARACTERISTICS

(V_{CC} = 3.3V -5% / +10% unless otherwise noted; 0°C ≤ T_A ≤ 70°C, Commercial; -40°C ≤ T_A ≤ 85°C, Industrial)

Parameter	Symbol	200MHz		166MHz		150MHz		133MHz		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Cycle Time	t_{KHKH}	5		6		7		8		ns
Clock HIGH Time	t_{KLKH}	1.6		2.4		2.6		2.8		ns
Clock LOW Time	t_{KHKL}	1.6		2.4		2.6		2.8		ns
Clock to output valid	t_{KHQV}		2.5		3.5		3.8		4.0	ns
Clock to output invalid	t_{KHQX}	1.5		1.5		1.5		1.5		ns
Clock to output on Low-Z	t_{KQLZ}	0		0		0		0		ns
Clock to output in High-Z	t_{KQHZ}	1.5	3	1.5	3.5	1.5	3.8	1.5	4.0	ns
Output Enable to output valid	t_{OELQV}		2.5		3.5		3.8		4.0	ns
Output Enable to output in Low-Z	t_{OELZ}	0		0		0		0		ns
Output Enable to output in High-Z	t_{OEHZ}		3.0		3.5		3.5		3.8	ns
Address, Control, Data-in Setup Time to Clock	t_S	1.5		1.5		1.5		1.5		ns
Address, Control, Data-in Hold Time to Clock	t_H	0.5		0.5		0.5		0.5		ns

SSRAM OPERATION TRUTH TABLE

Operation	Address Used	$\overline{SSCE}$	$\overline{SSADS}$	$\overline{SSWE}$	$\overline{SSOE}$	DQ
Deselected Cycle, Power Down	None	H	L	X	X	High-Z
WRITE Cycle, Begin Burst	External	L	L	L	X	D
READ Cycle, Begin Burst	External	L	L	H	L	Q
READ Cycle, Begin Burst	External	L	L	H	H	High-Z
READ Cycle, Suspend Burst	Current	X	H	H	L	Q
READ Cycle, Suspend Burst	Current	X	H	H	H	High-Z
READ Cycle, Suspend Burst	Current	H	H	H	L	Q
READ Cycle, Suspend Burst	Current	H	H	H	H	High-Z
WRITE Cycle, Suspend Burst	Current	X	H	L	X	D
WRITE Cycle, Suspend Burst	Current	H	H	L	X	D

NOTE:

1. X means “don’t care”, H means logic HIGH. L means logic LOW.
2. All inputs except $\overline{SSOE}$ must meet setup and hold times around the rising edge (LOW to HIGH) of SSCLK.
3. Suspending burst generates wait cycle
4. For a write operation following a read operation, $\overline{SSOE}$ must be HIGH before the input data required setup time plus High-Z time for $\overline{SSOE}$ and staying HIGH though out the input data hold time.
5. This device contains circuitry that will ensure the outputs will be in High-Z during power-up.

SSRAM PARTIAL TRUTH TABLE

Function	$\overline{SSWE}$	$\overline{BWE_0}$	$\overline{BWE_1}$	$\overline{BWE_2}$	$\overline{BWE_3}$
READ	H	X	X	X	X
WRITE one Byte (DQ0-7)	L	L	H	H	H
WRITE all Bytes	L	L	L	L	L

FIG. 3 SSRAM READ TIMING

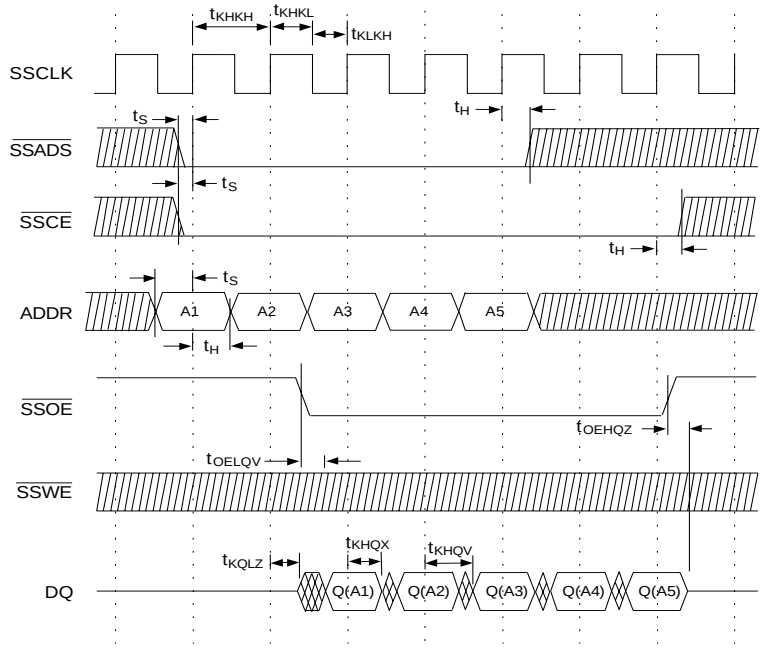
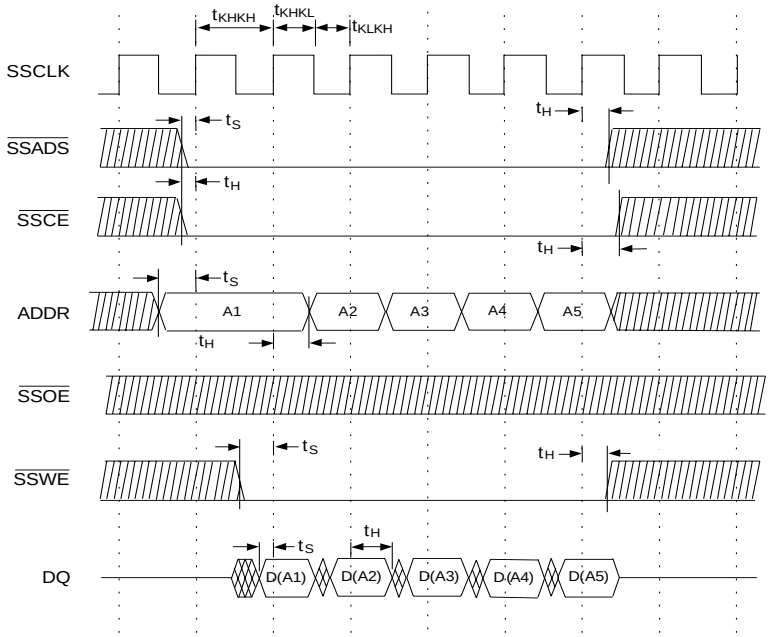


FIG. 4 SSRAM WRITE TIMING



SDRAM AC CHARACTERISTICS

(V_{CC} = 3.3V -5% / +10% unless otherwise noted; 0°C ≤ T_A ≤ 70°C, Commercial; -40°C ≤ T_A ≤ 85°C, Industrial)

Parameter		Symbol	125MHz		100MHz		83MHz		Units
			Min	Max	Min	Max	Min	Max	
Clock Cycle Time (1)	CL = 3	t_{CC}	8	1000	10	1000	12	1000	ns
	CL = 2	t_{CC}	10	1000	12	1000	15	1000	
Clock to valid Output delay (1,2)		t_{SAC}		6		7		8	ns
Output Data Hold Time (2)		t_{OH}	3		3		3		ns
Clock HIGH Pulse Width (3)		t_{CH}	3		3		3		ns
Clock LOW Pulse Width (3)		t_{CL}	3		3		3		ns
Input Setup Time (3)		t_{SS}	2		2		2		ns
Input Hold Time (3)		t_{SH}	1		1		1		ns
CLK to Output Low-Z (2)		t_{SLZ}	2		2		2		ns
CLK to Output High-Z		t_{SHZ}		7		7		8	ns
Row Active to Row Active Delay (4)		t_{RRD}	20		20		24		ns
RAS\ to CAS\ Delay (4)		t_{RCD}	20		20		24		ns
Row Precharge Time (4)		t_{RP}	20		20		24		ns
Row Active Time (4)		t_{RAS}	50	10,000	50	10,000	60	10,000	ns
Row Cycle Time - Operation (4)		t_{RC}	70		80		90		ns
Row Cycle Time - Auto Refresh (4,8)		t_{RFC}	70		80		90		ns
Last Data in to New Column Address Delay (5)		t_{CDL}	1		1		1		CLK
Last Data in to Row Precharge (5)		t_{RDL}	1		1		1		CLK
Last Data in to Burst Stop (5)		t_{BDL}	1		1		1		CLK
Column Address to Column Address Delay (6)		t_{CCD}	1.5		1.5		1.5		CLK
Number of Valid Output Data (7)			2		2		2		ea
			1		2		1		

NOTES:

1. Parameters depend on programmed CAS latency.
2. If clock rise time is longer than 1ns (t_{rise}/2 -0.5)ns should be added to the parameter.
3. Assumed input rise and fall time = 1ns. If t_{rise} of t_{fall} are longer than 1ns. [(t_{rise} = t_{fall})/2] - 1ns should be added to the parameter.
4. The minimum number of clock cycles required is detemined by dividing the minimum time required by the clock cycle time and then rounding up to the next higher integer.
5. Minimum delay is required to complete write.
6. All devices allow every cycle column address changes.
7. In case of row precharge interrupt, auto precharge and read burst stop.
8. A new command may be given t_{RFC} after self-refresh exit.

CLOCK FREQUENCY AND LATENCY PARAMETERS - 125MHz SDRAM

(Unit = number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	50ns	20ns	20ns	20ns	10ns	10ns	10ns
125MHz (8.0ns)	3	9	6	3	2	3	1	1	1
100MHz (10.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	4	2	2	2	1	1	1

CLOCK FREQUENCY AND LATENCY PARAMETERS - 100MHz SDRAM

(Unit = number of clock)

Frequency	CAS Latency	t_{RC}	t_{RAS}	t_{RP}	t_{RRD}	t_{RCD}	t_{CCD}	t_{CDL}	t_{RDL}
		70ns	50ns	20ns	20ns	20ns	10ns	10ns	10ns
100MHz (12.0ns)	3	7	5	2	2	2	1	1	1
83MHz (12.0ns)	2	6	5	2	2	2	1	1	1

REFRESH CYCLE PARAMETERS

Parameter	Symbol	-10 Min	-10 Max	-12 Min	-12 Max	Units
Refresh Period (1,2)	t_{REF}	—	64	—	64	ms

NOTES:

1. 4096 cycles
2. Any time that the Refresh Period has been exceeded, a minimum of two Auto (CBR) Refresh commands must be given to "wake-up" the device.

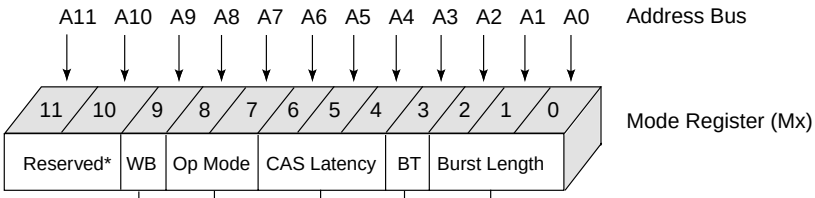
SDRAM COMMAND TRUTH TABLE

Function		$\overline{SDCE}$	$\overline{SDRAS}$	$\overline{SDCAS}$	$\overline{SDWE}$	BWE	A_{12}, A_{13}	SDA_{10} A_{11-0}	Notes
Mode Register Set		L	L	L	L	X	OP CODE		
Auto Refresh (CBR)		L	L	L	H	X	X	X	
Precharge	Single Bank	L	L	H	L	X	BA	L	2
	Precharge all Banks	L	L	H	L	X	X	H	
Bank Activate		L	L	H	H	X	BA	Row Address	2
Write		L	H	L	L	X	BA	L	2
Write with Auto Precharge		L	H	L	L	X	BA	H	2
Read		L	H	L	L	X	BA	L	2
Read with Auto Precharge		L	H	L	H	X	BA	H	2
Burst Termination		L	H	H	L	X	X	X	3
No Operation		L	H	H	H	X	X	X	
Device Deselect		H	X	X	X	X	X	X	
Data Write/Output Disable		X	X	X	X	L	X	X	4
Data Mask/Output Disable		X	X	X	X	H	X	X	4

NOTES:

1. All of the SDRAM operations are defined by states of SDCE\, SDWE\, SDRAS\, SDCAS\, and BWE_{0-3} at the positive rising edge of the clock.
2. Bank Select (BA), if A_{12} (BA_0) and A_{13} (BA_1) select between different banks.
3. During a Burst Write cycle there is a zero clock delay, for a Burst Read cycle the delay is equal to the CAS latency.
4. The BWE has two functions for the data DQ Read and Write operations. During a Read cycle, when BWE goes high at a clock timing the data outputs are disabled and become high impedance after a two clock delay. BWE also provides a data mask function for Write cycles. When it activates, the Write operation at the clock is prohibited (zero clock latency).

MODE REGISTER SET TABLE



*Should program
M11, M10 = "0, 0"
to ensure compatibility
with future devices.

			Burst Length	
M2	M1	M0	M3 = 0	M3 = 1
0	0	0	1	1
0	0	1	2	2
0	1	0	4	4
0	1	1	8	8
1	0	0	Reserved	Reserved
1	0	1	Reserved	Reserved
1	1	0	Reserved	Reserved
1	1	1	Full Page	Reserved

M3	Burst Type
0	Sequential
1	Interleaved

M2	M1	M0	CAS Latency
0	0	0	Reserved
0	0	1	Reserved
0	1	0	2
0	1	1	3
1	0	0	Reserved
1	0	1	Reserved
1	1	0	Reserved
1	1	1	Reserved

M8	M7	M6-M0	Operating Mode
0	0	Defined	Standard Operation
---	---	---	All other states reserved

M9	Write Burst Mode
0	Programmed Burst Length
1	Single Location Access

SDRAM CURRENT STATE TRUTH TABLE

Current State	Command							Action	Notes
	$\overline{SDCE}$	$\overline{SDRAS}$	$\overline{SDCAS}$	$\overline{SDWE}$	A_{12} & A_{13} (BA)	A_{11}-A_0	Description		
Idle	L	L	L	L	OP Code		Mode Register Set	Set the Mode Register	1
	L	L	L	H	X	X	Auto or Self Refresh	Start Auto	1
	L	L	H	L	X	X	Precharge	No Operation	
	L	L	H	H	BA	Row Address	Bank Activate	Activate the specified bank and row	
	L	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	2
	L	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	1
	L	H	H	L	X	X	Burst Termination	No Operation	1
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
Row Active	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Precharge	3
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	1
	L	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	4,5
	L	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	4,5
	L	H	H	L	X	X	Burst Termination	No Operation	
	L	H	H	H	X	X	No Operation	No Operation	
	H	X	X	X	X	X	Device Deselect	No Operation	
Read	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write	Terminate Burst; Start the Write cycle	5,6
	L	H	L	H	BA	Column	Read	Terminate Burst; Start a new Read cycle	5,6
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Write	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	Terminate Burst; Start the Precharge	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write	Terminate Burst; Start a new Write cycle	5,6
	L	H	L	H	BA	Column	Read	Terminate Burst; Start the Read cycle	5,6
	L	H	H	L	X	X	Burst Termination	Terminate the Burst	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Read with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	2
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	

SDRAM CURRENT STATE TRUTH TABLE (cont.)

Current State	Command							Action	Notes
	$\overline{SDCE}$	$\overline{SDRAS}$	$\overline{SDCAS}$	$\overline{SDWE}$	A_{12} & A_{13} (BA)	A_{11}-A_0	Description		
Write with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	2
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	Continue the Burst	
	H	X	X	X	X	X	Device Deselect	Continue the Burst	
Precharging	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	No Operation; Bank(s) idle after t_{RP}	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write w/o Precharge	ILLEGAL	2
	L	H	L	H	BA	Column	Read w/o Precharge	ILLEGAL	20
	L	H	H	L	X	X	Burst Termination	No Operation; Bank(s) idle after t_{RP}	
	L	H	H	H	X	X	No Operation	No Operation; Bank(s) idle after t_{RP}	
	H	X	X	X	X	X	Device Deselect	No Operation; Bank(s) idle after t_{RP}	
Row Activating	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	2
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write	ILLEGAL	2
	L	H	L	H	BA	Column	Read	ILLEGAL	2
	L	H	H	L	X	X	Burst Termination	No Operation; Row active after t_{RCD}	
	L	H	H	H	X	X	No Operation	No Operation; Row active after t_{RCD}	
	H	X	X	X	X	X	Device Deselect	No Operation; Row active after t_{RCD}	
Write Recovering	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	2
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write	Start Write; Determine if Auto Precharge	6
	L	H	L	H	BA	Column	Read	Start Read; Determine if Auto Precharge	6
	L	H	H	L	X	X	Burst Termination	No Operation; Row active after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Row active after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Row active after t_{DPL}	
Write Recovering with Auto Precharge	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto orSelf Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	2
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	2
	L	H	L	L	BA	Column	Write	ILLEGAL	2,6
	L	H	L	H	BA	Column	Read	ILLEGAL	2,6
	L	H	H	L	X	X	Burst Termination	No Operation; Precharge after t_{DPL}	
	L	H	H	H	X	X	No Operation	No Operation; Precharge after t_{DPL}	
	H	X	X	X	X	X	Device Deselect	No Operation; Precharge after t_{DPL}	

SDRAM CURRENT STATE TRUTH TABLE (cont.)

Current State	Command							Action	Notes
	$\overline{SDCE}$	$\overline{SDRAS}$	$\overline{SDCAS}$	$\overline{SDWE}$	A_{12} & A_{13} (BA)	A_{11}-A_0	Description		
Refreshing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	No Operation; Idle after t_{RC}	
	L	H	H	H	X	X	No Operation	No Operation; Idle after t_{RC}	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after t_{RC}	
Mode Register Accessing	L	L	L	L	OP Code		Mode Register Set	ILLEGAL	
	L	L	L	H	X	X	Auto or Self Refresh	ILLEGAL	
	L	L	H	L	X	X	Precharge	ILLEGAL	
	L	L	H	H	BA	Row Address	Bank Activate	ILLEGAL	
	L	H	L	L	BA	Column	Write	ILLEGAL	
	L	H	L	H	BA	Column	Read	ILLEGAL	
	L	H	H	L	X	X	Burst Termination	ILLEGAL	
	L	H	H	H	X	X	No Operation	No Operation; Idle after two clock cycles	
	H	X	X	X	X	X	Device Deselect	No Operation; Idle after two clock cycles	

NOTES:

1. Both Banks must be idle otherwise it is an illegal action.
2. The Current State refers only refers to one of the banks, if BA selects this bank then the action is illegal. If BA selects the bank not being referenced by the Current State then the action may be legal depending on the state of that bank.
3. The minimum and maximum Active time (t_{RAS}) must be satisfied.
4. The $\overline{RAS}$ to $\overline{CAS}$ Delay (t_{RCD}) must occur before the command is given.
5. Address SDA_{10} is used to determine if the Auto Precharge function is activated.
6. The command must satisfy any bus contention, bus turn around, and/or write recovery requirements.

The command is illegal if the minimum bank to bank delay time (t_{RRD}) is not satisfied.

FIG. 5 SDRAM SINGLE BIT READ-WRITE-READ CYCLE (SAME PAGE) @ CAS LATENCY = 3, BURST LENGTH = 1

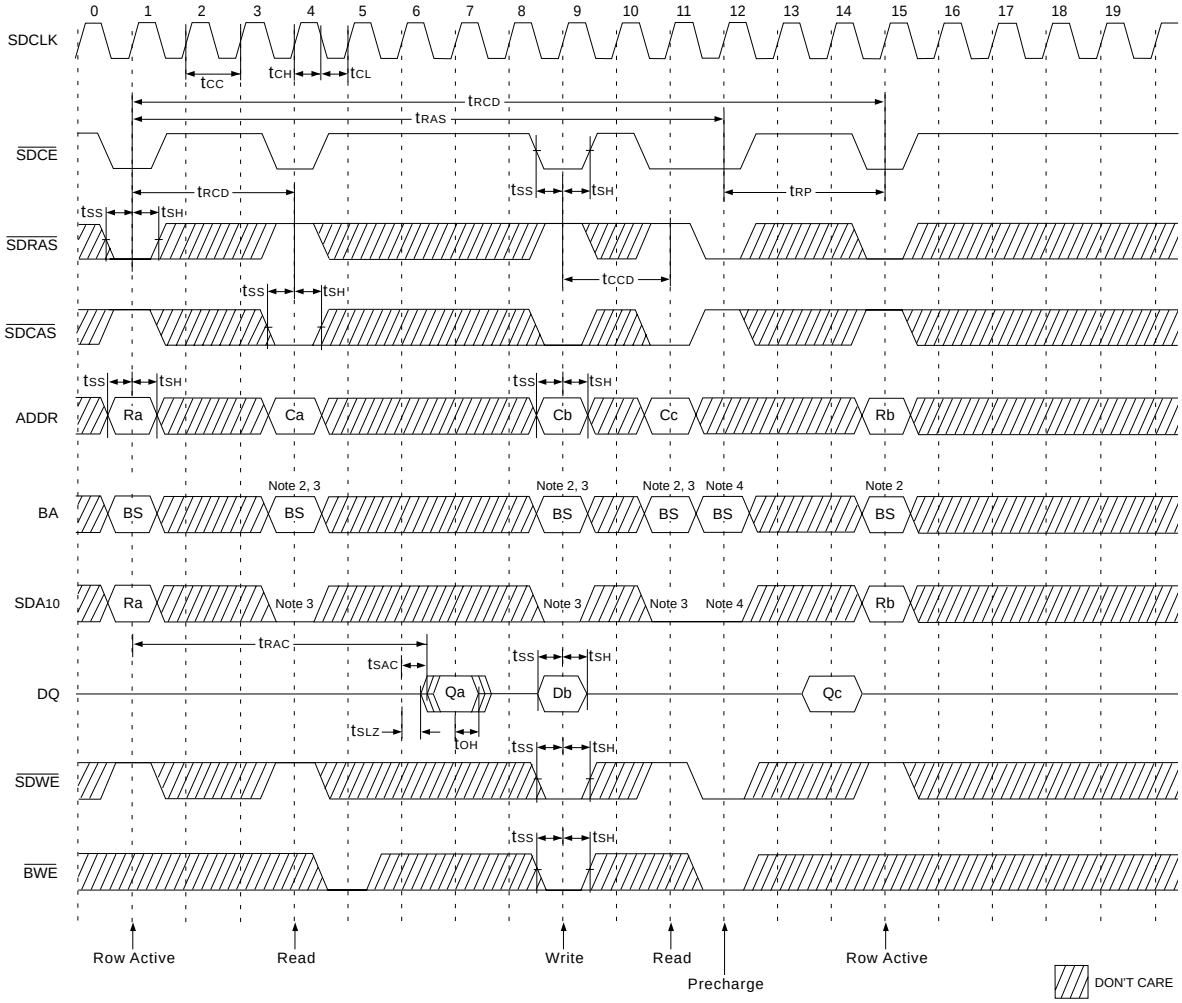


FIG. 6 SDRAM POWER UP SEQUENCE

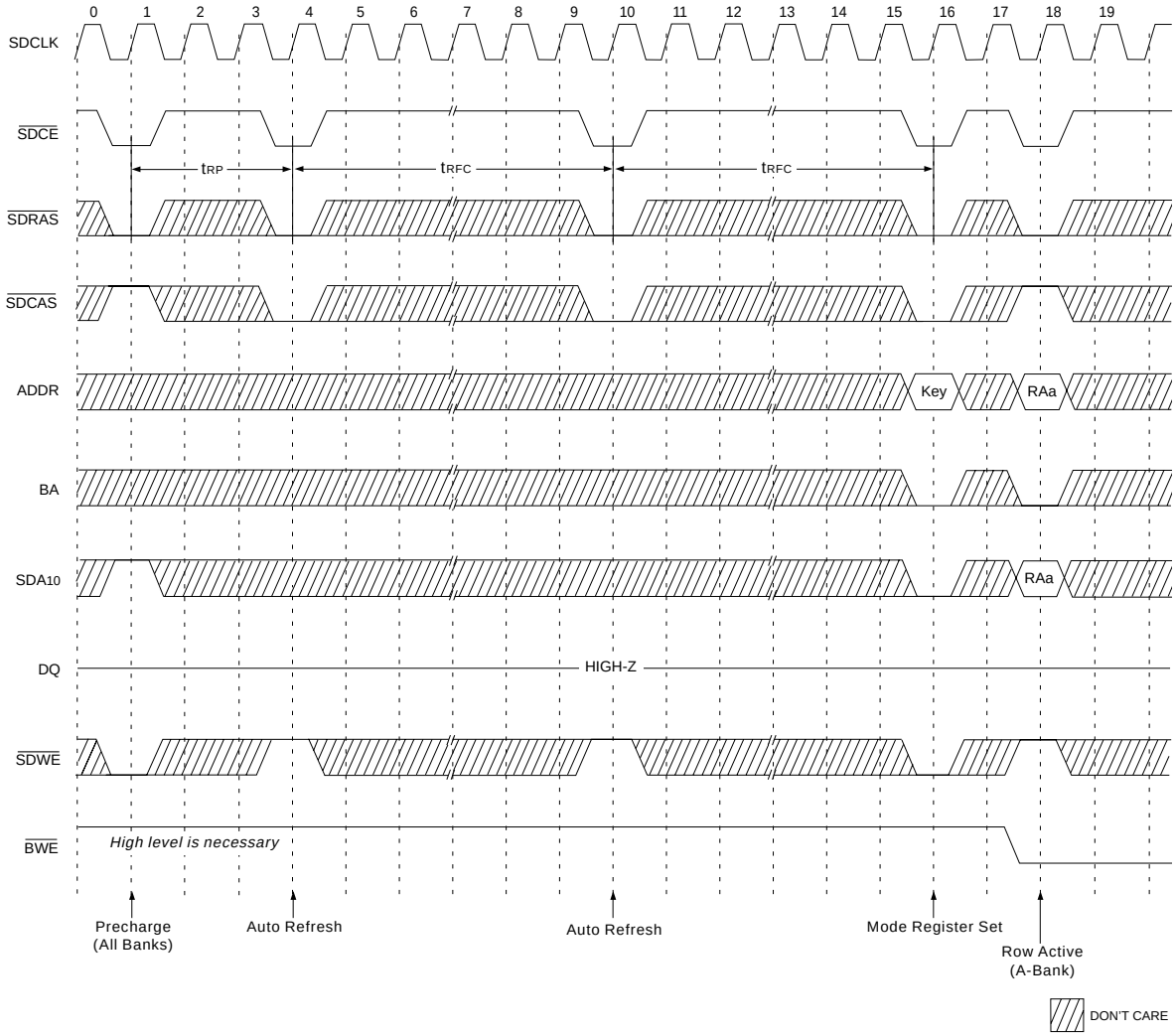
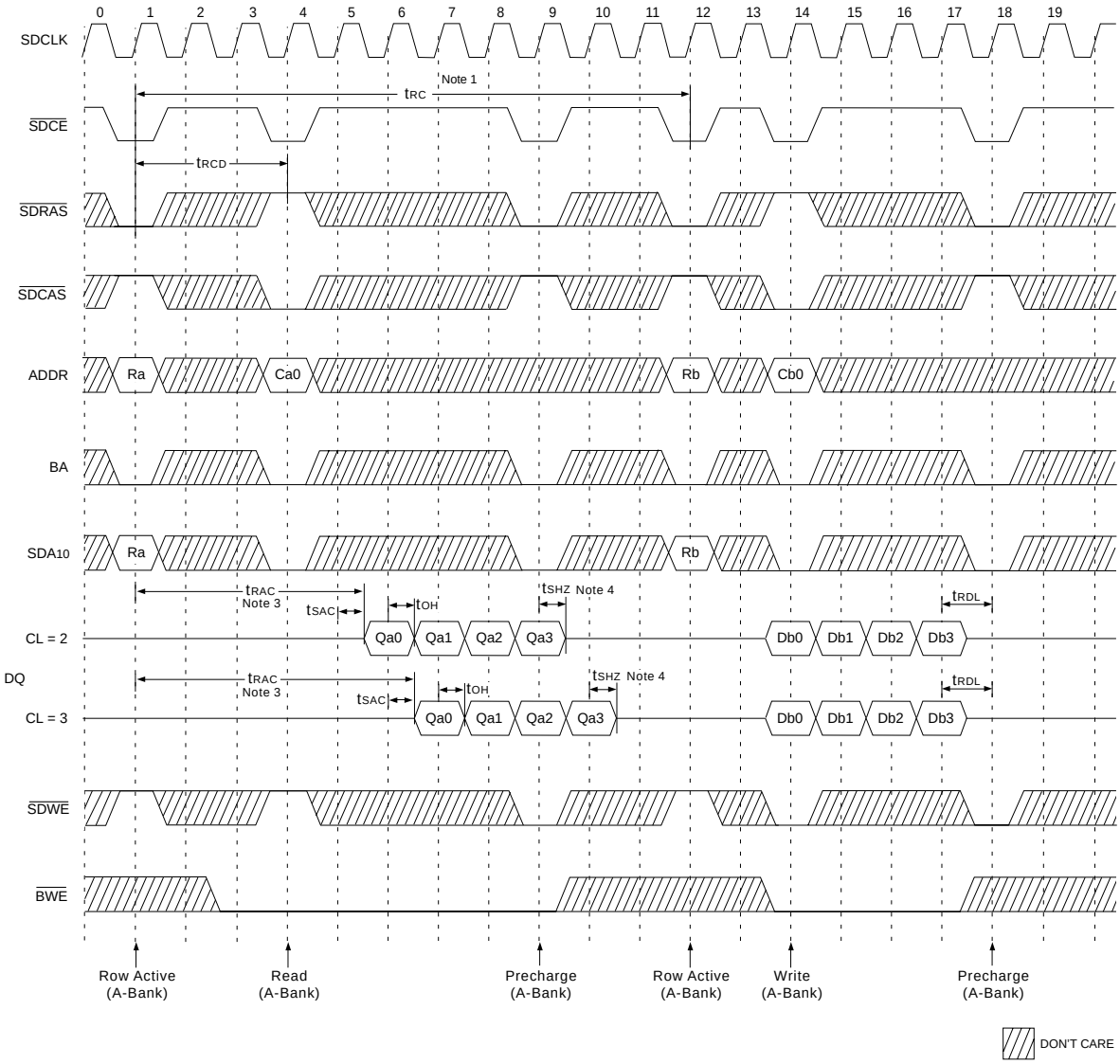


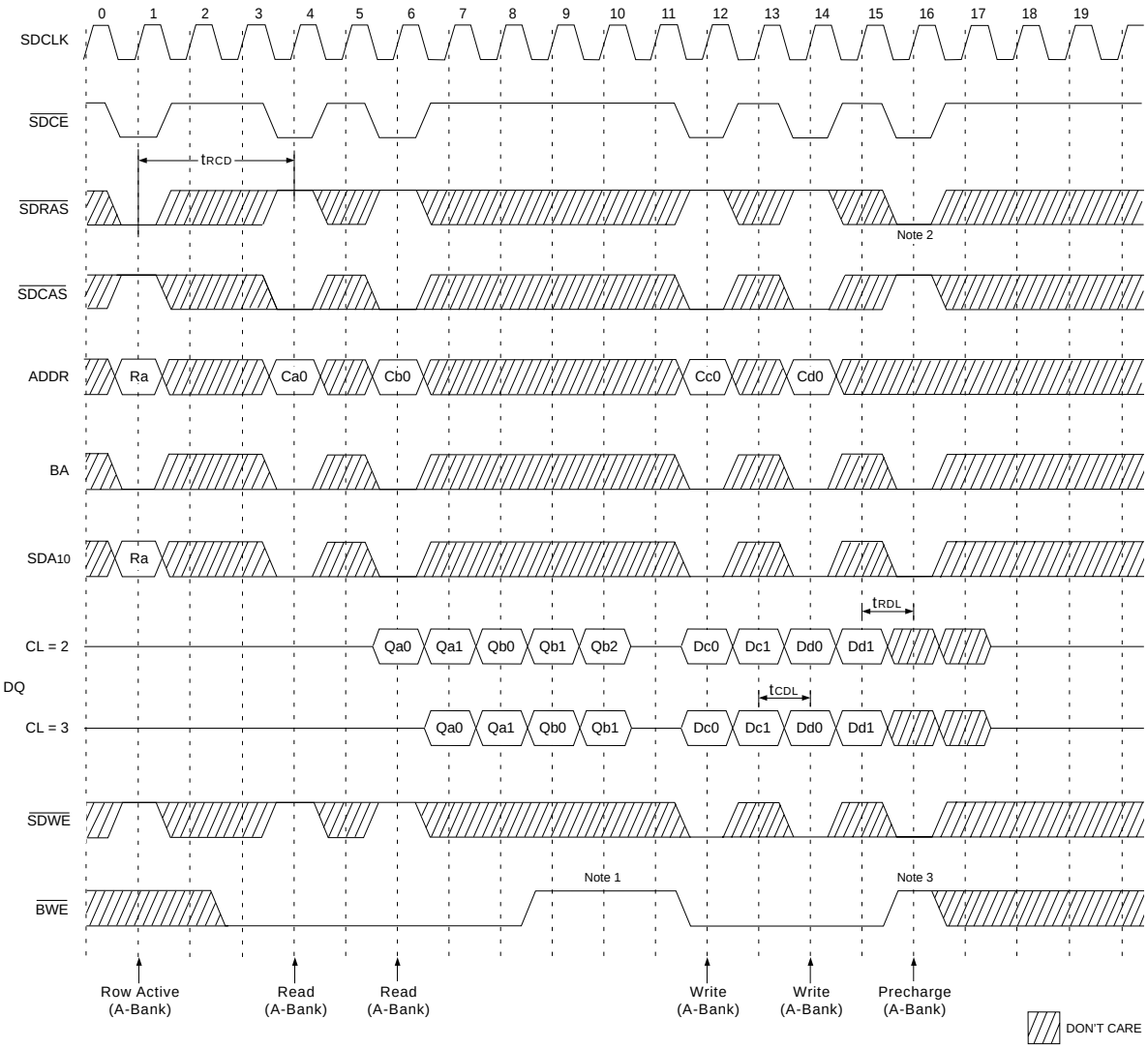
FIG. 7 SDRAM READ & WRITE CYCLE AT SAME BANK @ BURST LENGTH = 4



NOTES:

1. Minimum row cycle times are required to complete internal DRAM operation.
2. Row precharge can interrupt burst on any cycle. (CAS Latency - 1) number of valid output data is available after Row precharge. Last valid output will be Hi-Z (t_{SHZ}) after the clock.
3. Access time from Row active command. t_{CC} *(t_{RCD} + CAS Latency - 1) + t_{SAC}.
4. Output will be Hi-Z after the end of burst. (1, 2, 4, 8 & Full page bit burst)

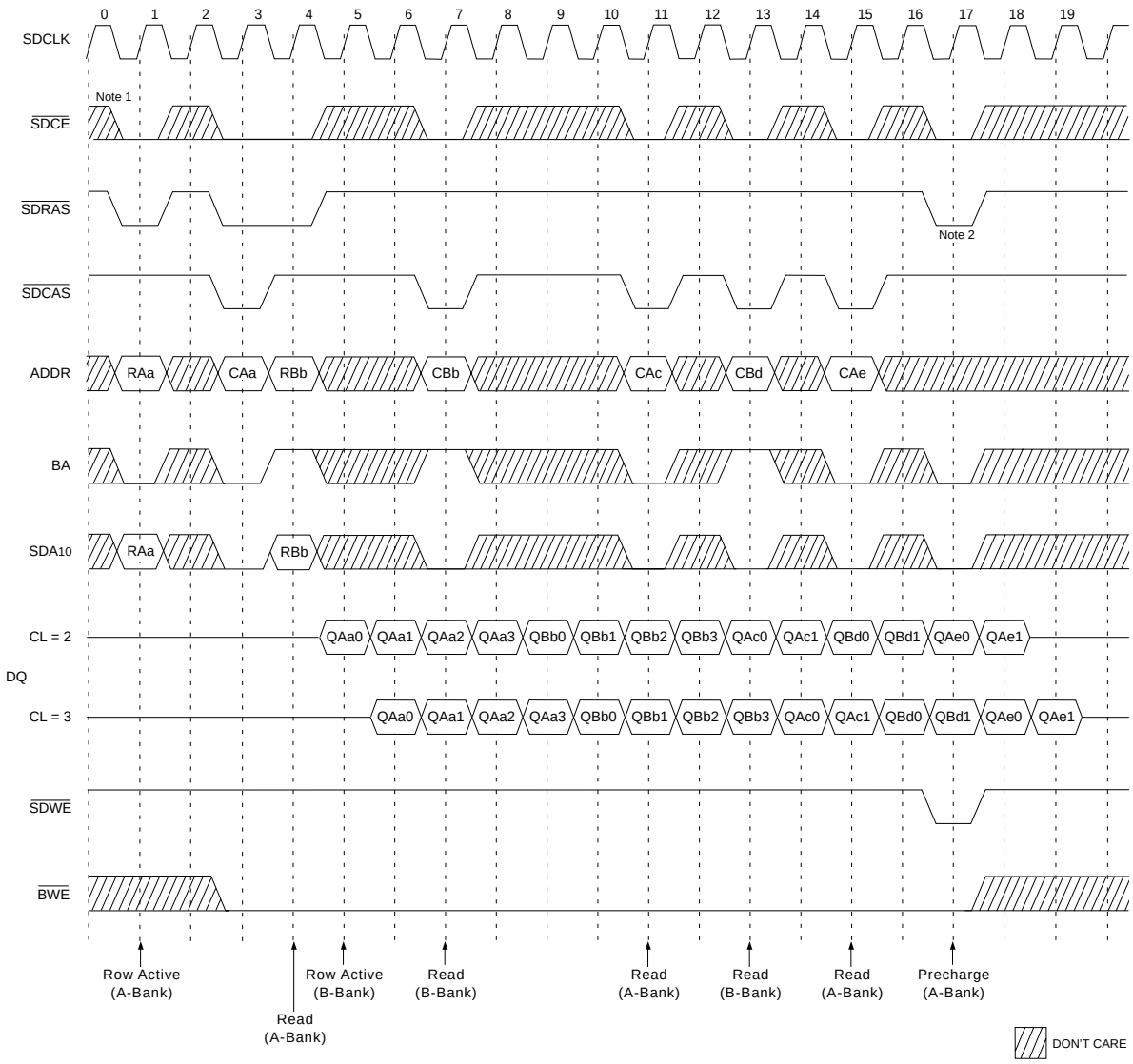
FIG. 8 SDRAM PAGE READ & WRITE CYCLE AT SAME BANK @ BURST LENGTH = 4



NOTES:

1. To write data before burst read ends. $\overline{BWE}$ should be asserted three cycle prior to write command to avoid bus contention.
2. Row precharge will interrupt writing. Last data input, t_{RDL} before Row precharge will be written.
3. $\overline{BWE}$ should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.

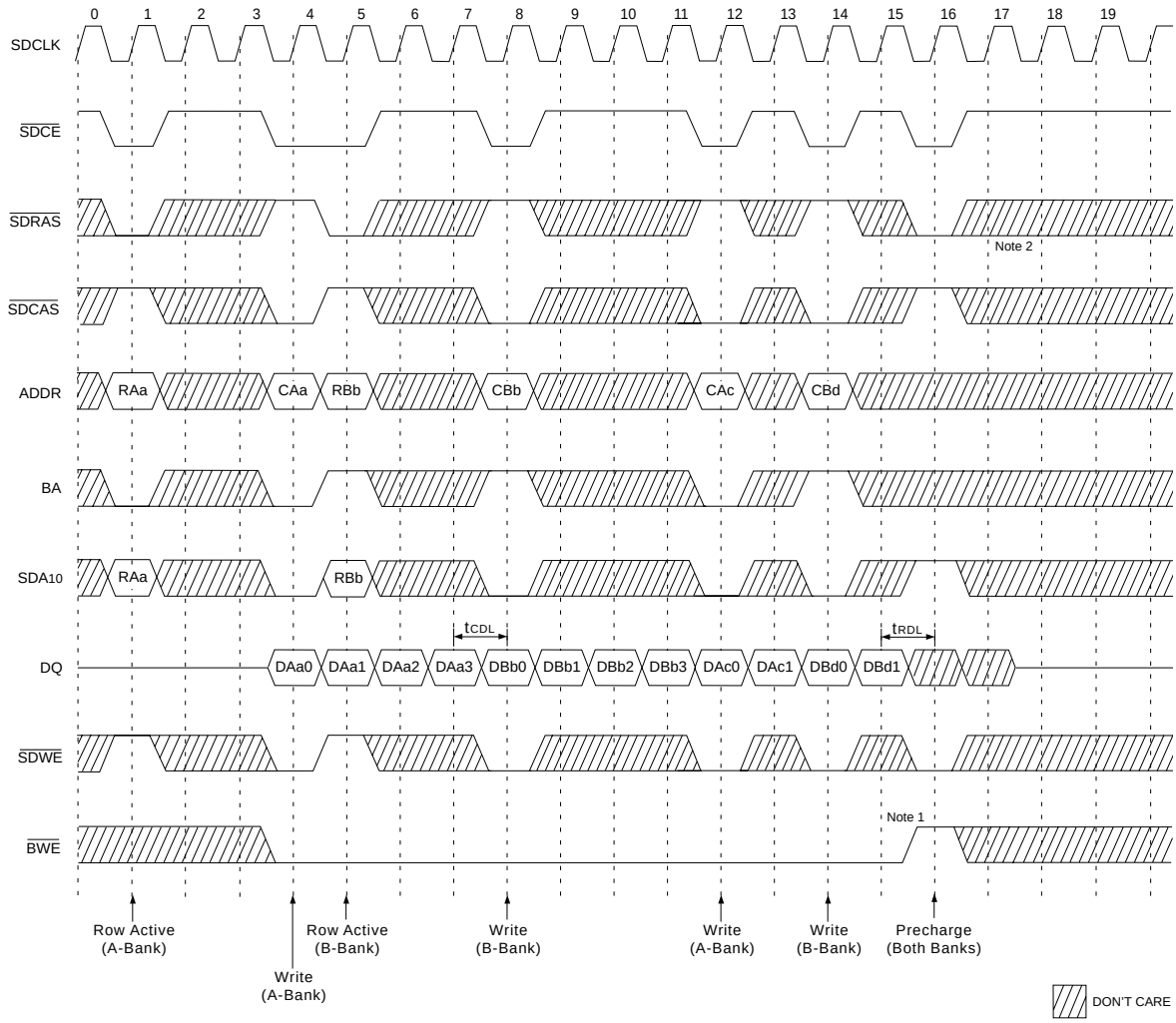
FIG. 9 SDRAM PAGE READ CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4



NOTES:

1. $\overline{\text{SDCE}}$ can be "don't care" when $\overline{\text{SDRAS}}$, $\overline{\text{SDCAS}}$ and $\overline{\text{SDWE}}$ are high at the clock going high edge.
2. To interrupt a burst read by Row precharge, both the read and the precharge banks must be the same.

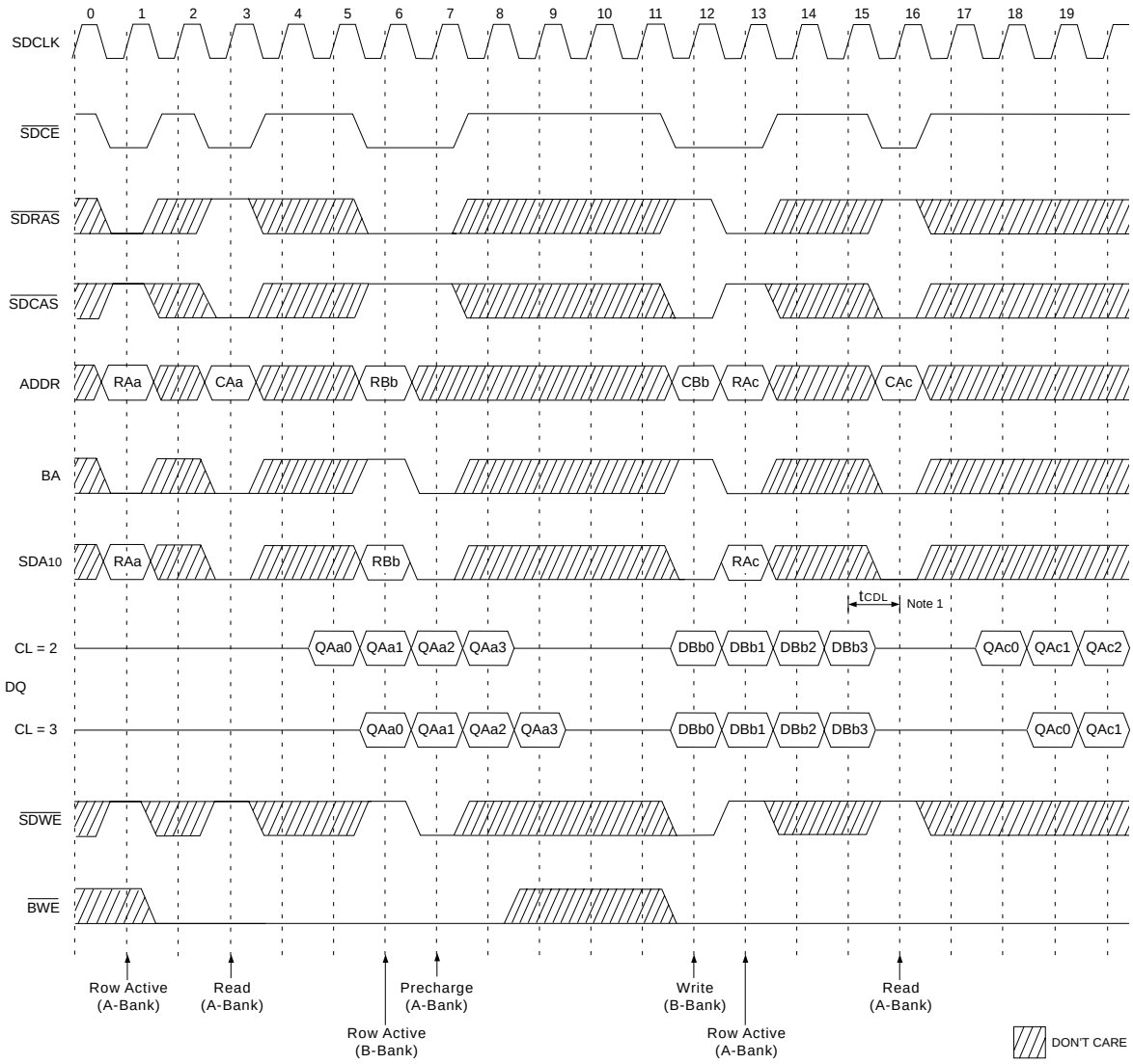
FIG. 10 SDRAM PAGE WRITE CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4



NOTES:

1. To interrupt burst write by Row precharge, $\overline{BWE}$ should be asserted to mask invalid input data.
2. To interrupt a burst read by Row precharge, both the read and the precharge banks must be the same.

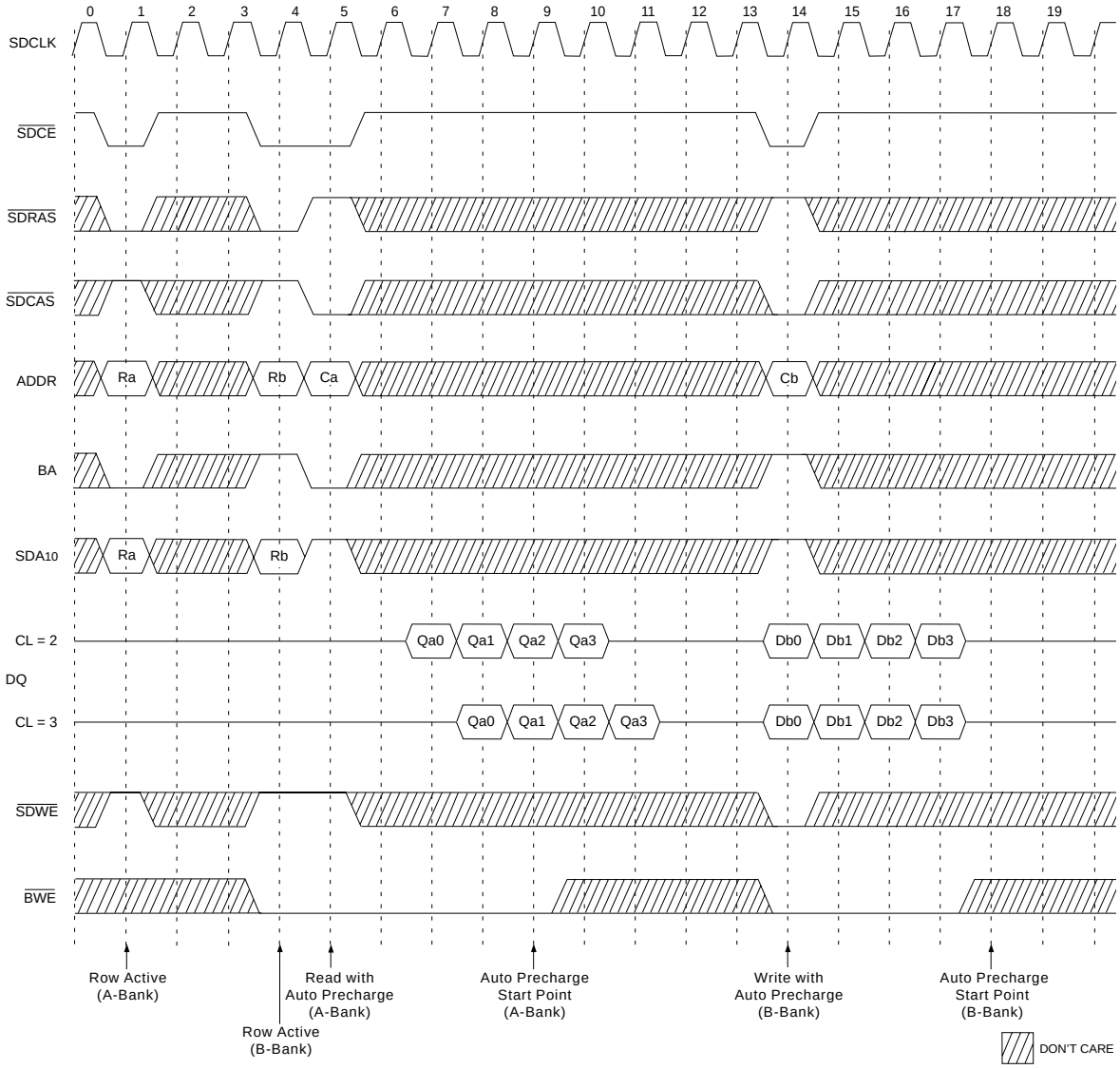
FIG. 11 SDRAM READ & WRITE CYCLE AT DIFFERENT BANK @ BURST LENGTH = 4



NOTES:

1. t_{CDL} should be met to complete write.

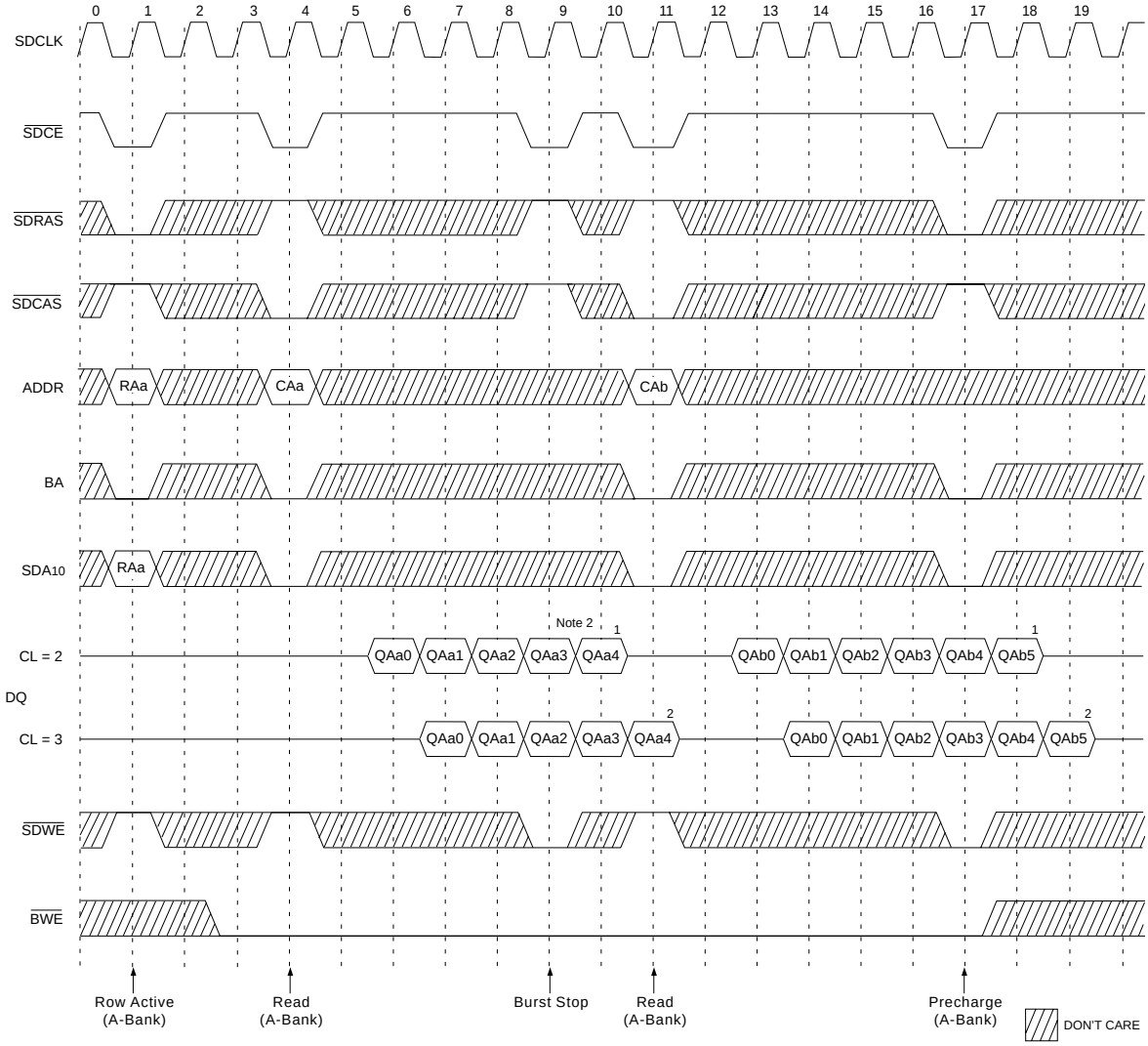
FIG. 12 SDRAM READ & WRITE CYCLE WITH AUTO PRECHARGE @ BURST LENGTH = 4



NOTES:

1. t_{CDL} should be controlled to meet minimum t_{RAS} before internal precharge start. (In the case of Burst Length = 1 & 2 and BRSW mode)

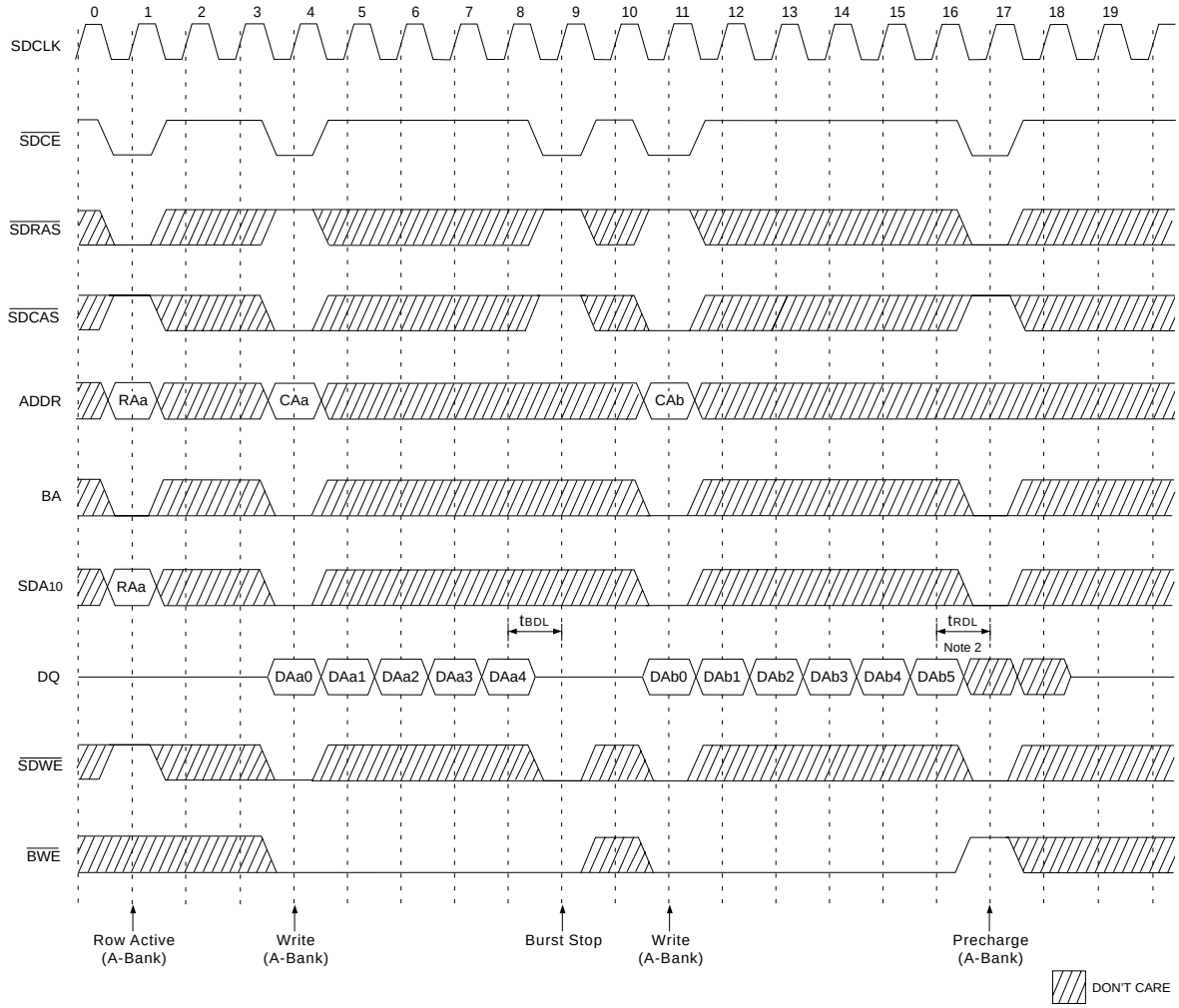
FIG. 13 SDRAM READ INTERRUPTED BY PRECHARGE COMMAND & READ BURST STOP @ BURST LENGTH = FULL PAGE



NOTES:

1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. About the valid DQs after burst stop, it is the same as the case of $\overline{\text{SDRAS}}$ interrupt. Both cases are illustrated in the above timing diagram. See the label 1, 2 on each of them. But at burst write, burst stop and $\overline{\text{SDRAS}}$ interrupt should be compared carefully. Refer to the timing diagram of "Full page write burst stop cycle".
3. Burst stop is valid at every burst length.

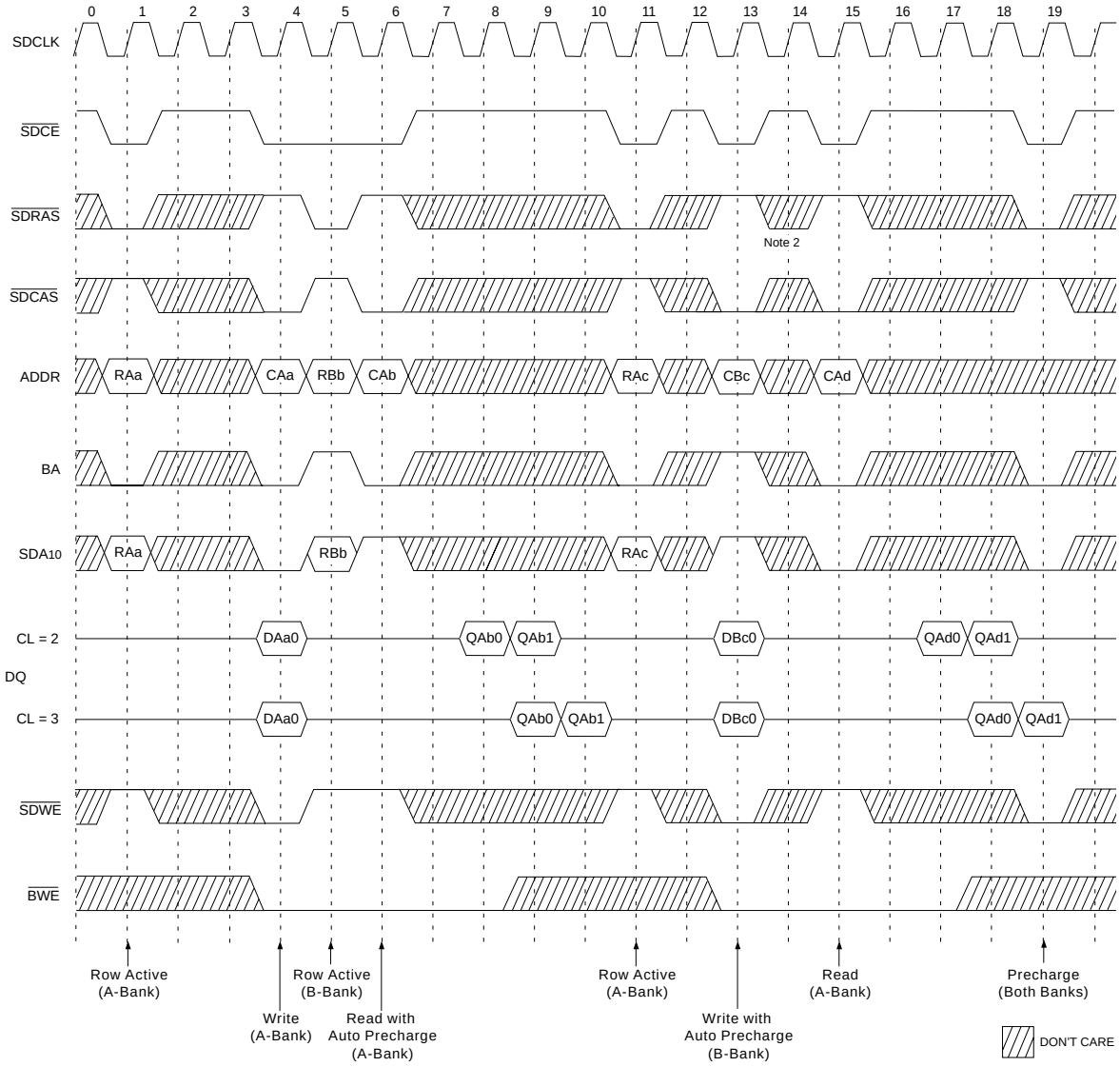
FIG. 14 SDRAM WRITE INTERRUPTED BY PRECHARGE COMMAND & WRITE BURST STOP @ BURST LENGTH = FULL PAGE



NOTES:

1. At full page mode, burst is end at the end of burst. So auto precharge is possible.
2. Data-in at the cycle of interrupted by precharge can not be written into the corresponding memory cell. It is defined by AC parameter of t_{RDL}.
   $\overline{BWE}$ at write interrupt by precharge command is needed to prevent invalid write.
   $\overline{BWE}$ should mask invalid input data on precharge command cycle when asserting precharge before end of burst. Input data after Row precharge cycle will be masked internally.
3. Burst stop is valid at every burst length.

FIG. 15 SDRAM BURST READ SINGLE BIT WRITE CYCLE @ BURST LENGTH = 2

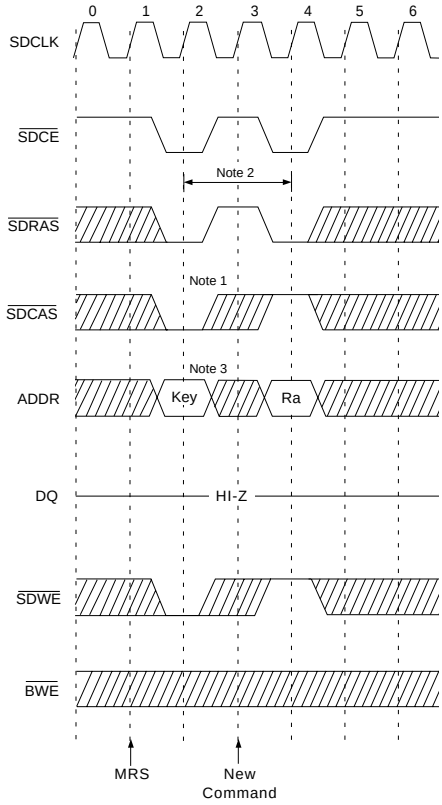


NOTES:

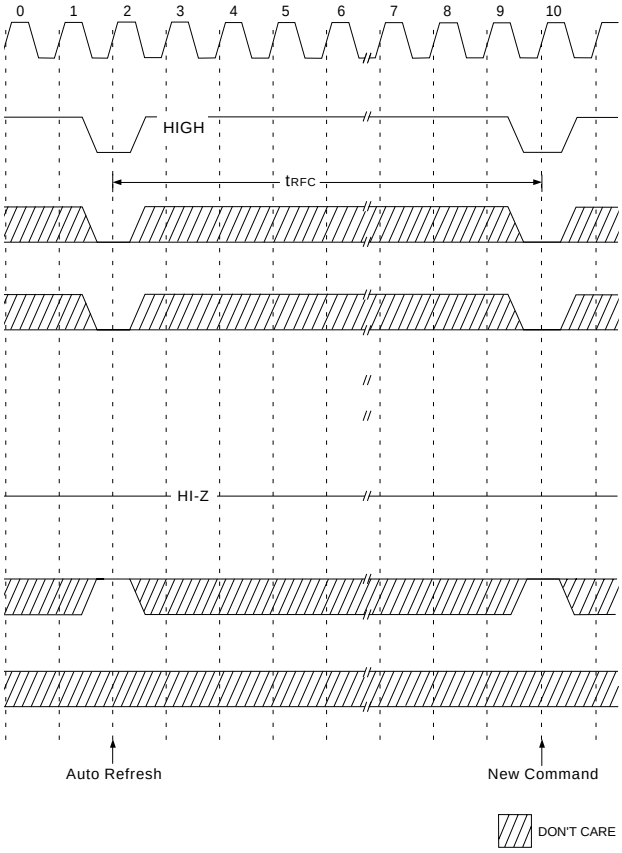
1. BRSW modes enabled by setting A9 "High" at MRS (Mode Register Set).
   At the BRSW Mode, the burst length at Write is fixed to "1" regardless of programmed burst length.
2. When BRSW write command with auto precharge is executed, keep it in mind that t_{RAS} should not be violated. Auto precharge is executed at the burst-end cycle, so in the case of BRSW write command, the next cycle starts the precharge.

FIG. 16

SDRAM MODE REGISTER SET CYCLE



SDRAM AUTO REFRESH CYCLE



*Both banks precharge should be completed before Mode Register Set cycle and Auto refresh cycle.

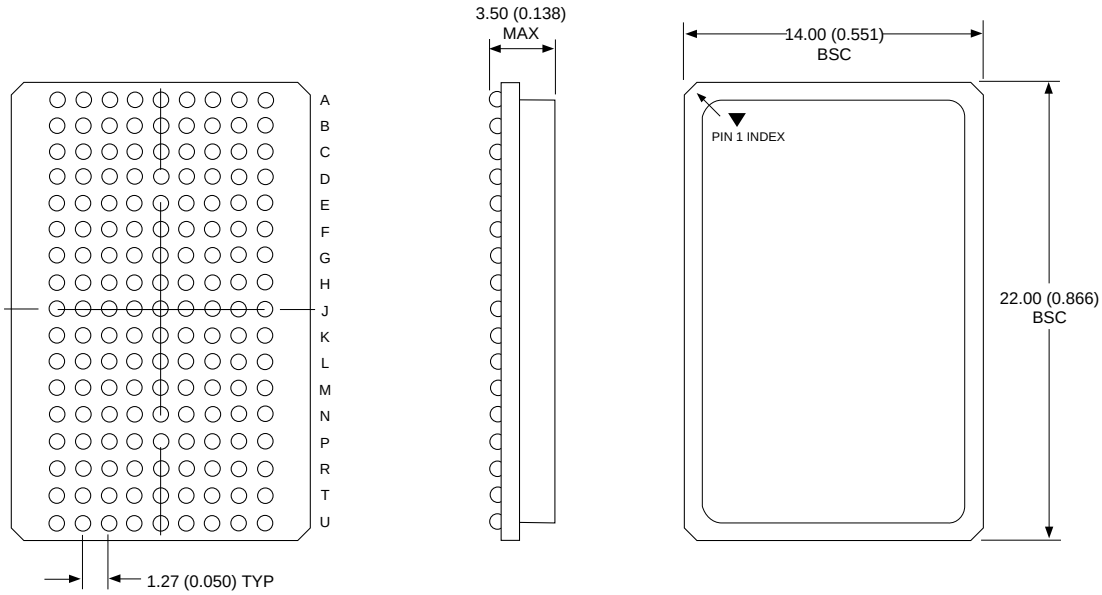
NOTES:

MODE REGISTER SET CYCLE

1. $\overline{SDCE}$, $\overline{SDRAS}$, $\overline{SDCAS}$ & $\overline{SDWE}$ activation at the same clock cycle with address key will set internal mode register.
2. Minimum 2 clock cycles should be met before new $\overline{SDRAS}$ activation.
3. Please refer to Mode Register Set Table.

PACKAGE DESCRIPTION: 153 LEAD BGA (17 x 9 BALL ARRAY)

JEDEC MO-163



ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

ORDERING INFORMATION

COMMERCIAL ($0^{\circ}C \leq T_A \leq 70^{\circ}C$)

Part Number	SSRAM Access	SDRAM Access
WED9LC6416V2012BC	200MHz	125MHz
WED9LC6416V2010BC	200MHz	100MHz
WED9LC6416V1612BC	166MHz	125MHz
WED9LC6416V1610BC	166MHz	100MHz
WED9LC6416V1512BC	150MHz	125MHz
WED9LC6416V1510BC	150MHz	100MHz
WED9LC6416V1312BC	133MHz	125MHz
WED9LC6416V1310BC	133MHz	100MHz

INDUSTRIAL ($-40^{\circ}C \leq T_A \leq 85^{\circ}C$)

Part Number	SSRAM Access	SDRAM Access
WED9LC6416V2012BI	200MHz	125MHz
WED9LC6416V2010BI	200MHz	100MHz
WED9LC6416V1612BI	166MHz	125MHz
WED9LC6416V1610BI	166MHz	100MHz
WED9LC6416V1512BI	150MHz	125MHz
WED9LC6416V1510BI	150MHz	100MHz
WED9LC6416V1312BI	133MHz	125MHz
WED9LC6416V1310BI	133MHz	100MHz

FIG. 17
INTERFACING THE TEXAS INSTRUMENTS TMS320C6x WITH THE WED9LC6416V (128Kx32 SSRAM/4Mx32 SDRAM)

