

MAATCC0011
V3

Digital Attenuator
31.5 dB, 6-Bit, TTL Driver, DC-4.0 GHz
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Electrical Specifications: $T_A = +25^\circ\text{C}$

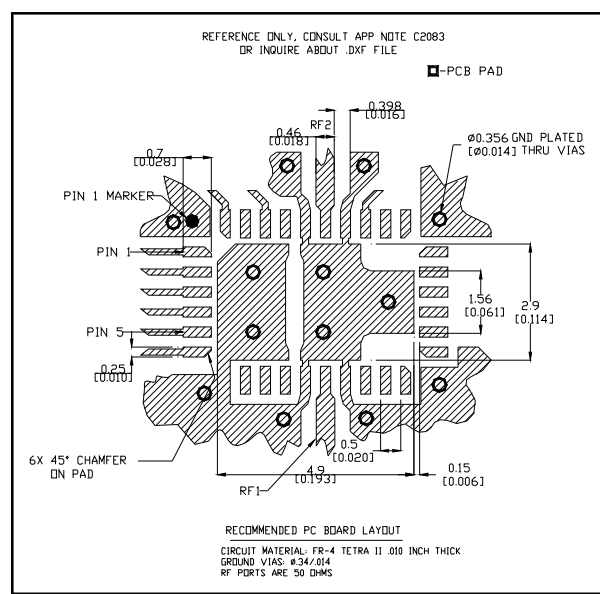
Parameter	Test Conditions	Frequency	Units	Min	Typ	Max
Insertion Loss	—	DC - 4.0 GHz	dB	—	4.5	5.1
Attenuation Accuracy	Individual Bits 0.5-1-2-4-8-16 dB Any Combination of Bits 1 to 31.5 dB	DC - 4.0 GHz DC - 4.0 GHz	dB dB	— —	— —	$\pm(.3 + 7\%$ of atten setting) $\pm(.5 + 8\%$ of atten setting)
VSWR	Full Range	DC - 4.0 GHz	Ratio	—	2.0:1	2.2:1
Switching Speed	50% Cntl to 90%/10% RF 10% to 90% or 90% to 10%	— —	nS nS	— —	75 20	— —
1 dB Compression	— —	50 MHz 0.5 - 4.0 GHz	dBm dBm	— —	+21 +24	— —
Input IP_3	Two-tone inputs up to +5 dBm	50 MHz 0.5-4.0 GHz	dBm dBm	— —	+35 +48	— —
V_{CC}	—	—	V	4.75	5.0	5.25
V_{IL} V_{IH}	LOW-level input voltage HIGH-level input voltage	— —	V V	0.0 2.0	— —	0.8 5.0
I_{in} (Input Leakage Current)	$V_{in} = V_{CC}$ or GND	—	μA	-1.0	—	1.0
I_{CC}^4	V_{CC} min to max, Logic "0" or "1"	—	mA	—	6	10
Turn-on Current ⁵	For guaranteed start-up	—	mA	—	—	125
ΔI_{CC} (Additional Supply Current Per TTL Input Pin)	$V_{CC} = \text{Max}$, $V_{ctrl} = V_{CC} - 2.1 \text{ V}$	—	mA	—	—	1.0
Switching Noise	Generated from DC-DC Converter with recommended capacitors	3.5 MHz	dBm	—	-93	—
Thermal Resistance θ_{jc}	—	—	$^\circ\text{C/W}$	—	15	—

- During turn-on, the device requires an initial "Turn-on Current". Once operational, I_{CC} will drop to the specified levels.
- The DC-DC converter is guaranteed to start in 100 μs as long as the power supplies can provide a minimum of 100 mA "Turn-on Current".

Absolute Maximum Ratings^{6,7}

Parameter	Absolute Maximum
Max. Input Power 0.05 GHz 0.5 - 4.0 GHz	+27 dBm +34 dBm
V_{CC}	$-0.5 \text{ V} \leq V_{CC} \leq +6.0 \text{ V}$
V_{in}^8	$-0.5 \text{ V} \leq V_{in} \leq V_{CC} + 0.5 \text{ V}$
Operating Temperature	-40°C to $+85^\circ\text{C}$
Storage Temperature	-65°C to $+125^\circ\text{C}$

- Exceeding any one or combination of these limits may cause permanent damage to this device.
- M/A-COM does not recommend sustained operation near these survivability limits.
- Standard CMOS TTL interface, latch-up will occur if logic signal is applied prior to power supply.

Recommended PCB Configuration⁹


9. Application Note S2083 is available on line at www.macom.com

- North America** Tel: 800.366.2266 / Fax: 978.366.2266
- Europe** Tel: 44.1908.574.200 / Fax: 44.1908.574.300
- Asia/Pacific** Tel: 81.44.844.8296 / Fax: 81.44.844.8298

Visit www.macom.com for additional data sheets and product information.

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Handling Procedures

Please observe the following precautions to avoid damage:

Static Sensitivity

Gallium Arsenide Integrated Circuits are sensitive to electrostatic discharge (ESD) and can be damaged by static electricity. Proper ESD control techniques should be used when handling these devices.

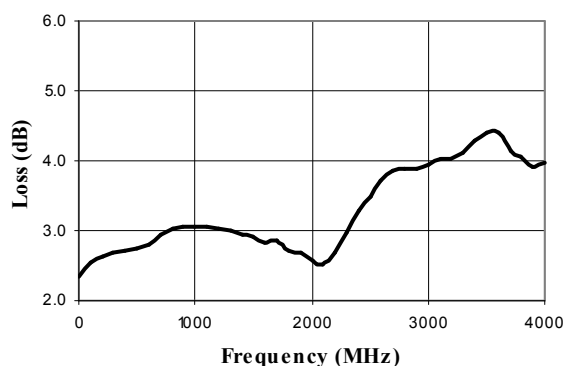
Truth Table (Digital Attenuator)

C16	C8	C4	C2	C1	C0	Attenuation
0	0	0	0	0	0	Loss, Reference
0	0	0	0	0	1	0.5 dB
0	0	0	0	1	0	1.0 dB
0	0	0	1	0	0	2.0 dB
0	0	1	0	0	0	4.0 dB
0	1	0	0	0	0	8.0 dB
1	0	0	0	0	0	16.0 dB
1	1	1	1	1	1	31.5 dB

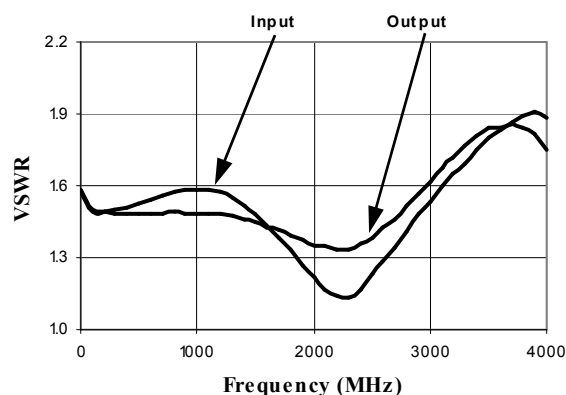
0 = TTL Low; 1 = TTL High

Typical Performance Curves

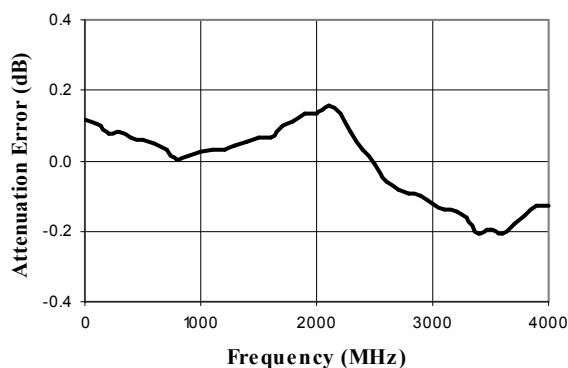
Insertion Loss



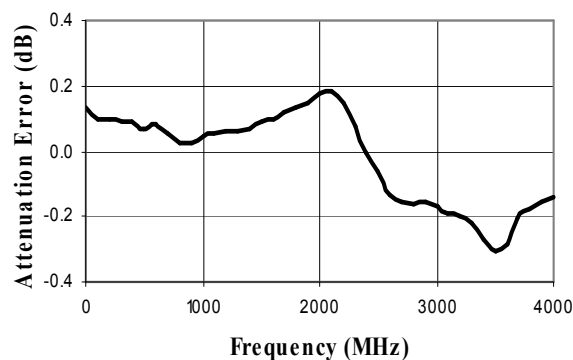
VSWR @ Insertion Loss



Attenuation Error, 0.5 dB Bit



Attenuation Error, 1 dB Bit

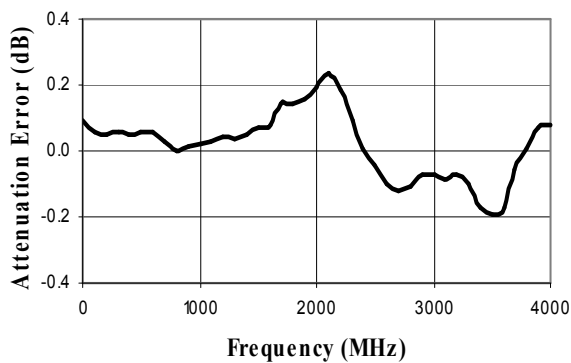


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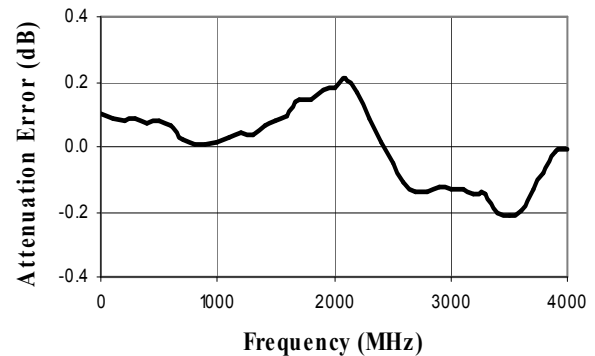
MAATCC0011
V3

Typical Performance Curves

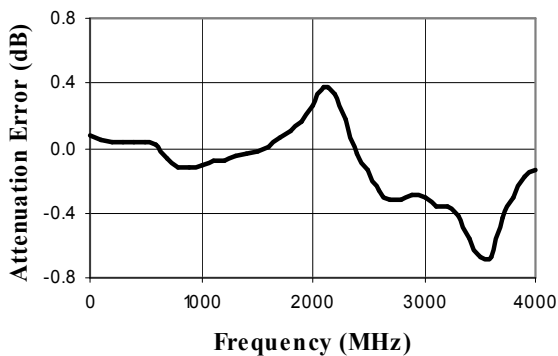
Attenuation Error, 2 dB Bit



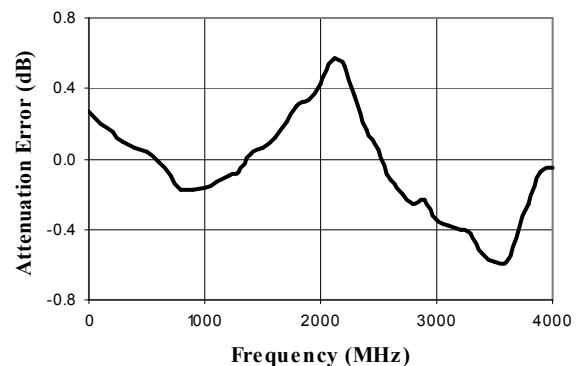
Attenuation Error, 4 dB Bit



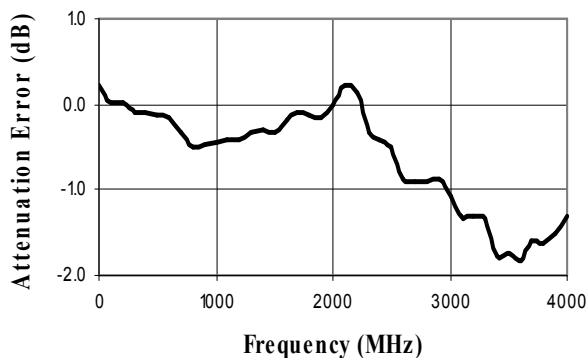
Attenuation Error, 8 dB Bit



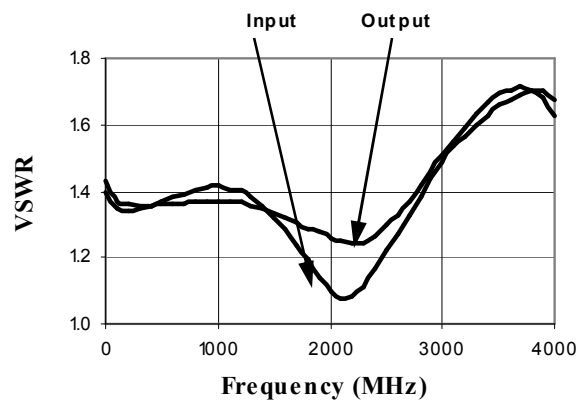
Attenuation Error, 16 dB Bit



Attenuation Error, Max. Attenuation



VSWR, 0.5 dB Bit

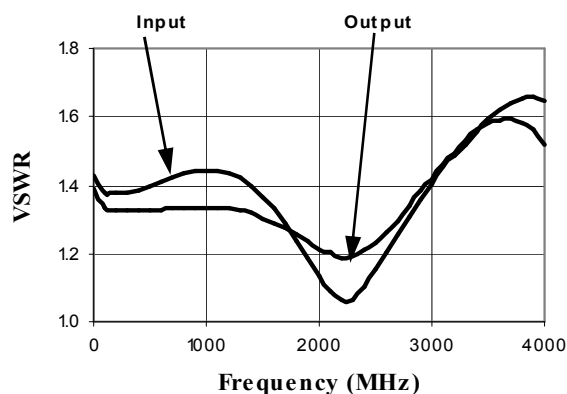


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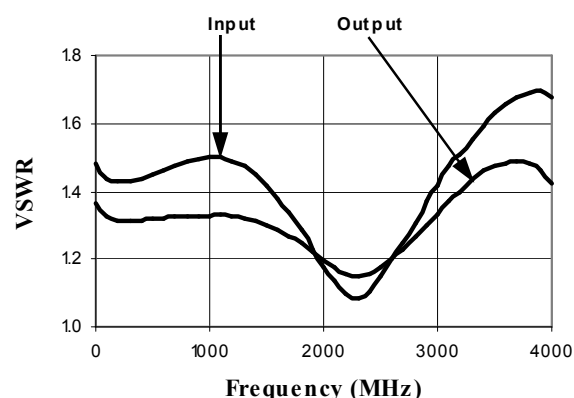
MAATCC0011
V3

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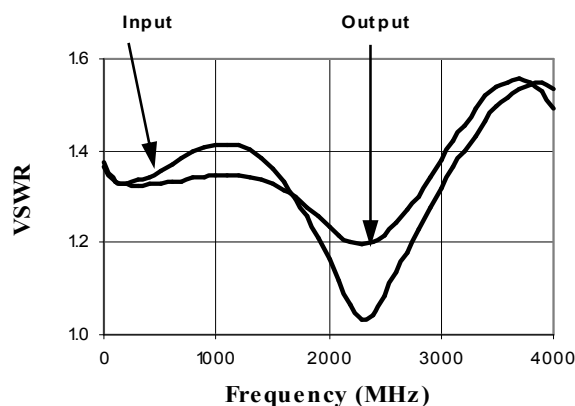
VSWR, 1 dB Bit



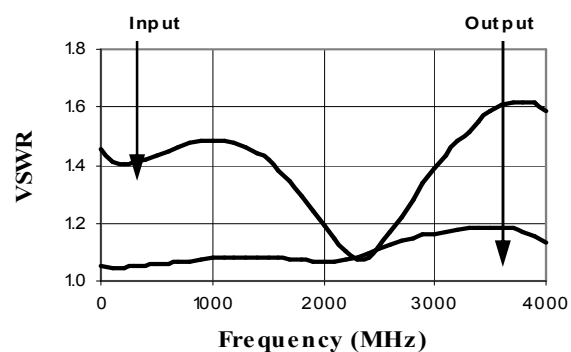
VSWR, 2 dB Bit



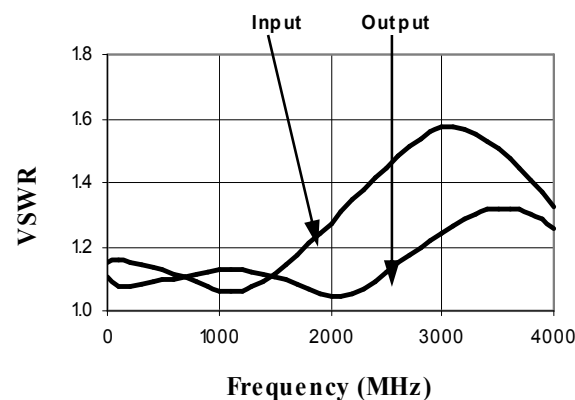
VSWR, 4 dB Bit



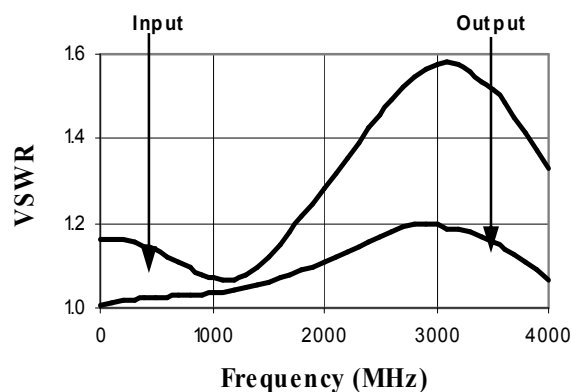
VSWR, 8 dB Bit



VSWR, 16 dB Bit



VSWR, Max. Attenuation

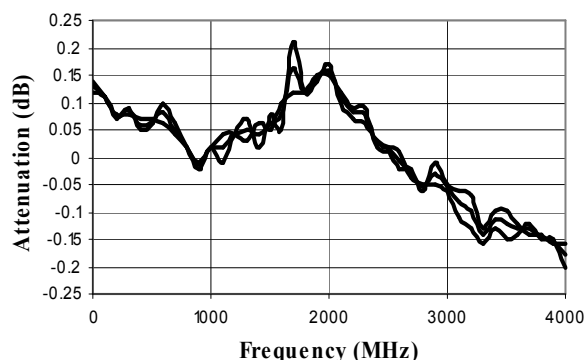


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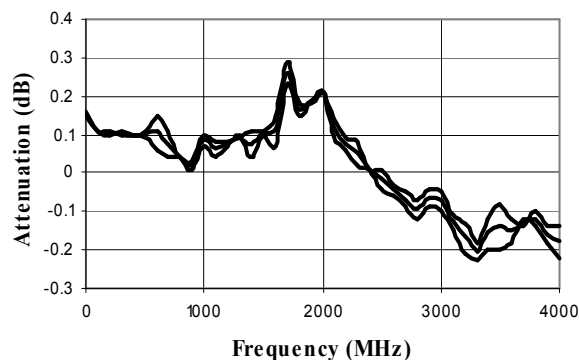
MAATCC0011
V3

Typical Performance Curves

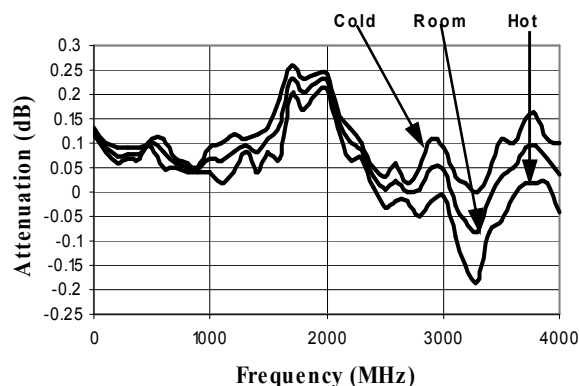
Typical Attenuation Deviation vs. Temperature for 0.5 dB Bit



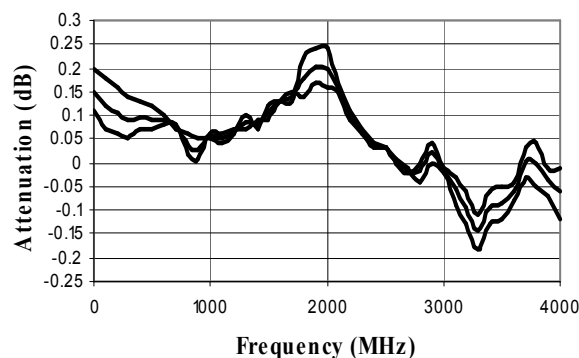
Typical Attenuation Deviation vs. Temperature for 1 dB Bit



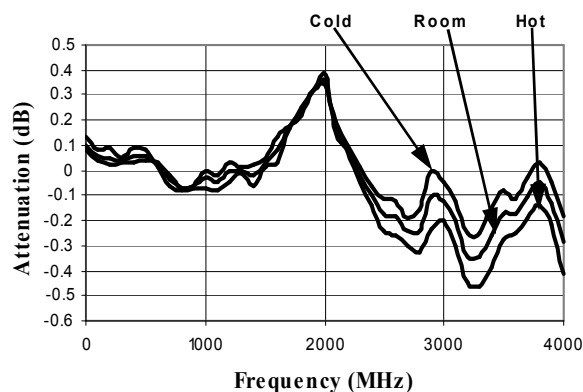
Typical Attenuation Deviation vs. Temperature for 2 dB Bit



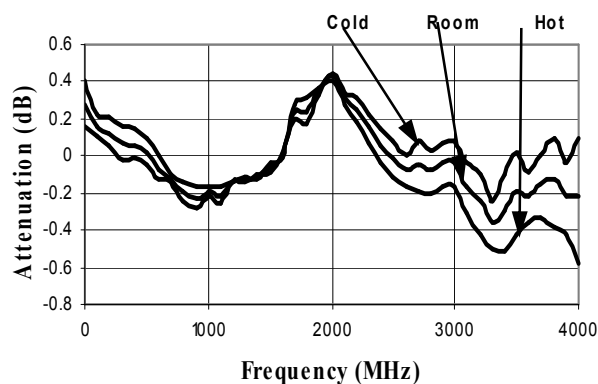
Typical Attenuation Deviation vs. Temperature for 4 dB Bit



Typical Attenuation Deviation vs. Temperature for 8 dB Bit



Typical Attenuation Deviation vs. Temperature for 16 dB Bit

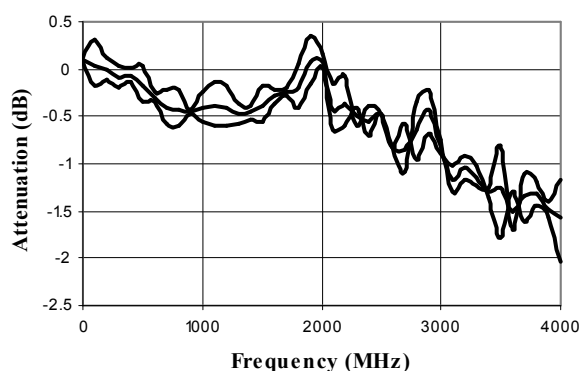


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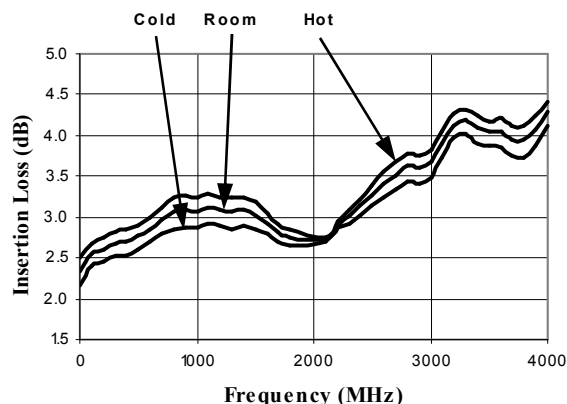
MAATCC0011
V3

Typical Performance Curves

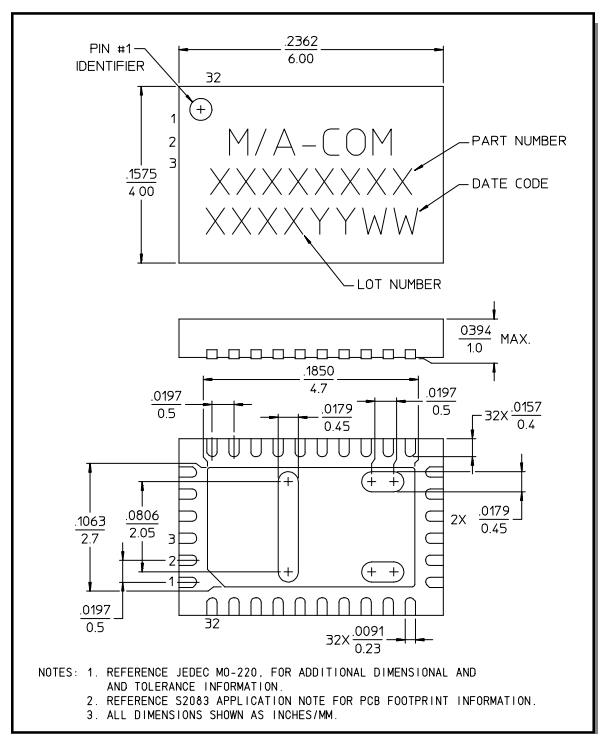
Typical Attenuation Deviation vs. Temperature at Maximum Attenuation



Insertion Loss vs. Temperature



CSP-1, Lead-Free 4 x 6 mm, 32-lead
PQFN†



† Reference Application Note M538 for lead-free solder reflow recommendations.