256-TAPS DUAL CHANNEL DIGITAL POTENTIOMETER WITH NON-VOLATILE MEMORY

Check for Samples: TPL0102

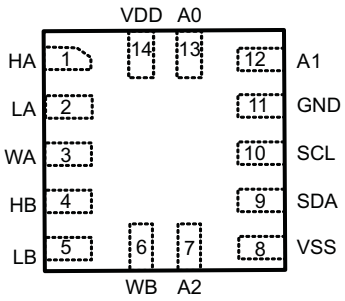
FEATURES

- **Dual Channel, 256-Position Resolution**
- **Non-volatile Memory Stores Wiper Settings**
- **2mm x 2mm, 14-pin MicroQFN or 14-pin TSSOP Packages**
- **100 kΩ End-to-End Resistance (TPL0102-100)**
- **Fast Power-up Response Time to Wiper Setting: <100µs**
- **±0.5 LSB INL, ±0.25 LSB DNL (Voltage-Divider Mode)**
- **4 ppm/°C Ratiometric Temperature Coefficient**
- **I²C-compatible Serial Interface**
- **2.7 V to 5.5 V Single-Supply Operation**
- **±2.25 V to ±2.75 V Dual-Supply Operation**
- **Operating Temperature Range From -40°C to +85°C**
- **ESD Performance Tested Per JESD 22**
  - **2000-V Human Body Model (A114-B, Class II)**

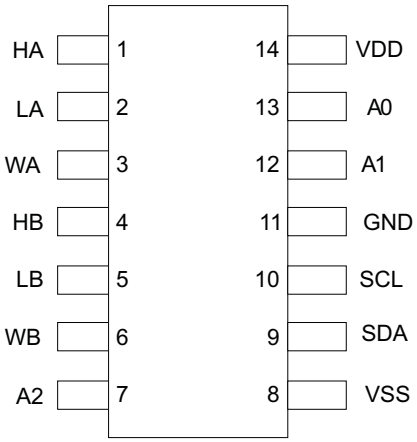
APPLICATIONS

- **Adjustable Gain Amplifiers and Offset Trimming**
- **Adjustable Power Supplies**
- **Precision Calibration of Set Point Thresholds**
- **Sensor Trimming and Calibration**
- **Mechanical Potentiometer Replacement**

MicroQFN - RUC PACKAGE
(TOP VIEW)



TSSOP - PW PACKAGE
(TOP VIEW)



DESCRIPTION

The TPL0102 is a two channel, linear-taper digital potentiometer with 256 wiper positions. Each potentiometer can be used as a three-terminal potentiometer or as a two-terminal rheostat. The TPL0102-100 has an end-to-end resistance of 100kΩ.

The TPL0102 has non-volatile memory (EEPROM) which can be used to store the wiper position. The internal registers of the TPL0102 can be accessed using the I²C interface.

The TPL0102 is available in a 14-pin MicroQFN and 14-pin TSSOP package with a specified temperature range of -40°C to +85°C.

ORDERING INFORMATION

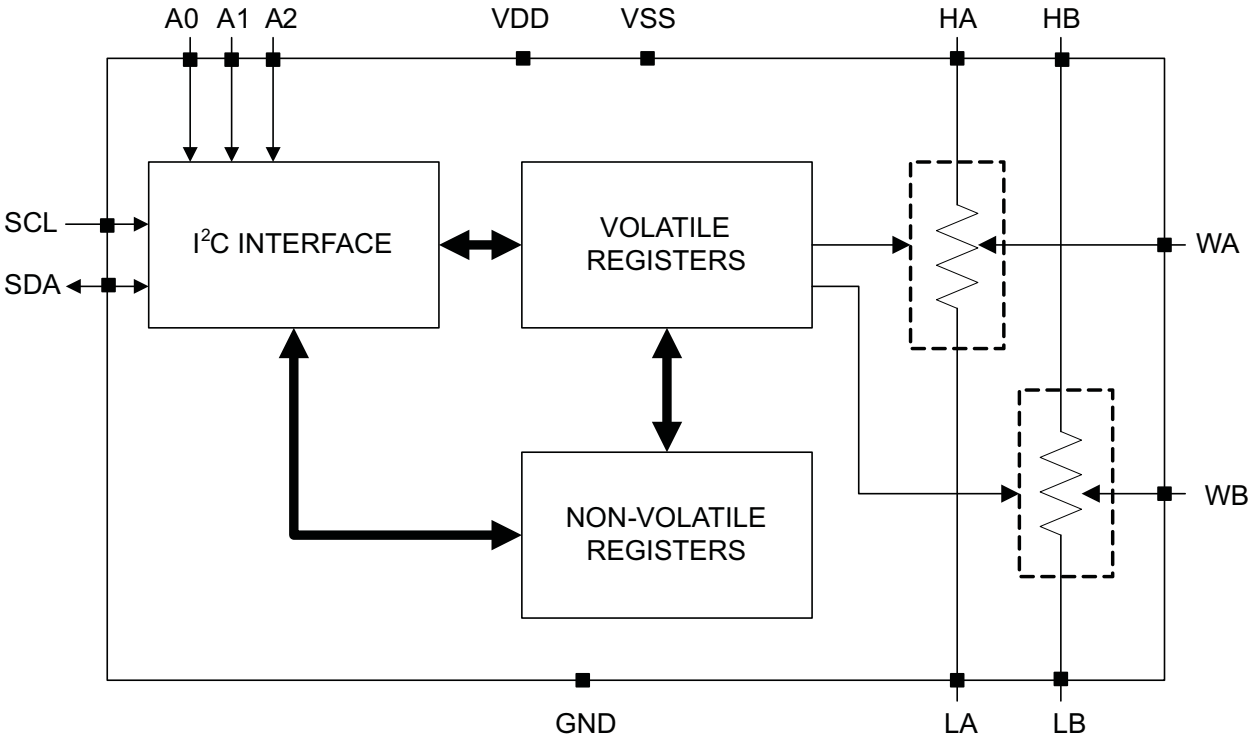
T_A	PACKAGE (1) (2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – PW	Tape and reel	TPL0102-100PWR	EL-100
	MicroQFN-RUC		TPL0102-100RUCR	6N

(1) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
(2) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI website at www.ti.com.

Table 1. Summary of Features

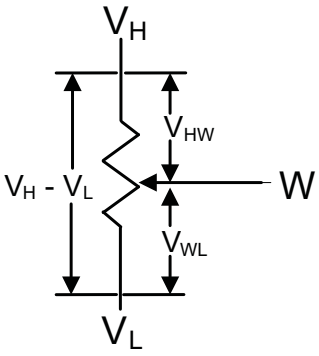
Feature	TPL0102-100
# of Potentiometers	2
Digital Interface	I^2C
Steps	256
Wiper Memory	Non-Volatile
Taper	Linear
End-to-end Resistance	100kΩ
End-to-end Resistance Tolerance	20%
Wiper Resistance	25 Ω (typ)
Smallest Package Size	MicroQFN (RUC): 4 mm^2

FUNCTIONAL BLOCK DIAGRAM



DIGITAL POTENTIOMETER CONFIGURATIONS

VOLTAGE DIVIDER MODE

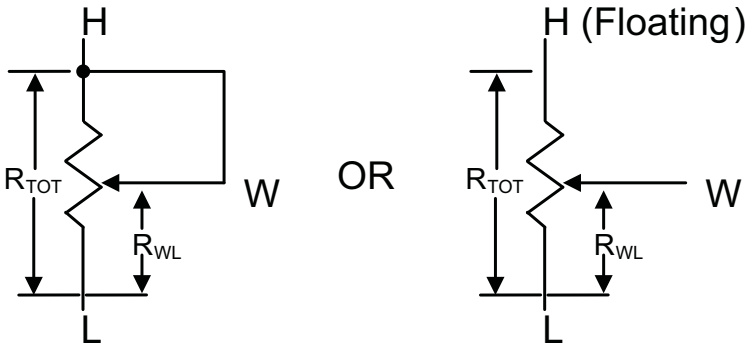


$V_{HW} = (V_H – V_L) \times (1 – (D/256))$

$V_{WL} = (V_H – V_L) \times D/256$

Where D = Decimal Value of Wiper Code

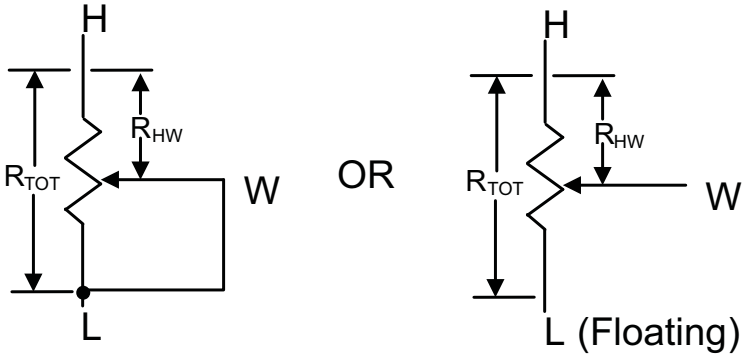
RHEOSTAT MODE A



$R_{WL} = R_{TOT} \times D/256$

Where D = Decimal Value of Wiper Code

RHEOSTAT MODE B



$R_{HW} = R_{TOT} \times (1 – (D/256))$

Where D = Decimal Value of Wiper Code

Figure 1. DPOT Configurations

Table 2. PIN DESCRIPTION TABLE

14 RUC/14 PW	PIN NAME	TYPE	DESCRIPTION
1	HA	I/O	High terminal of Potentiometer A
2	LA	I/O	Low terminal of Potentiometer A
3	WA	I/O	Wiper terminal of Potentiometer A
4	HB	I/O	High terminal of Potentiometer B
5	LB	I/O	Low terminal of Potentiometer B
6	WB	I/O	Wiper terminal of Potentiometer B
7	A2	Input	Address Bit 2
8	VSS	Power	Negative or GND Power Supply Pin
9	SDA	I/O	I^2C Data I/O
10	SCL	Input	I^2C Clock Input
11	GND	Ground	Ground
12	A1	Input	Address Bit 1
13	A0	Input	Address Bit 0
14	VDD	Power	Positive Power Supply Pin

ABSOLUTE MAXIMUM RATINGS(1)(2)(3)

			MIN	MAX	UNIT
V_{DD} to GND	Supply voltage range		–0.3	7	V
V_{SS} to GND			–7	0.3	V
V_{DD} to V_{SS}				7	V
V_H, V_L, V_W	Voltage at resistor terminals		V_{SS} – 0.3	V_{DD} + 0.3	V
V_I	Digital input voltage range		–0.3	V_{DD} + 0.3	V
I_H, I_L, I_W	Pulse Current			±20	mA
	Continuous Current			±2	mA
θ_{JA}	Package thermal impedance(4)	PW package		88	°CW
		RUC package		216.7	
T_{stg}	Storage temperature range		–65	150	°C

(1) Stresses above these ratings may cause permanent damage. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.
(2) The algebraic convention, whereby the most negative value is a minimum and the most positive value is a maximum.
(3) All voltages are with respect to ground, unless otherwise specified.
(4) The package thermal impedance is calculated in accordance with JESD 51-7.

ELECTRICAL CHARACTERISTICS

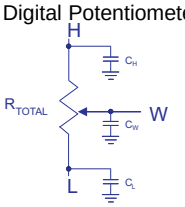
V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, V_H= V_{DD}, V_L= GND, T_A = –40°C to 85°C (unless otherwise noted). Typical values are at V_{DD}= 5V, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
R_{TOT}	End-to-end Resistance (Between H and L Terminals)	TPL0102-100		80	100	120	kΩ
R_H, R_L	Terminal resistance				60	200	Ω
R_W	Wiper resistance				25	100	Ω
C_H, C_L (1)(2)	Terminal capacitance				22		pF
C_W (1)(2)	Wiper capacitance				16		pF
I_{LKG}	Terminal Leakage Current	V_H = V_{SS} to V_{DD}, V_L = Floating OR V_L = V_{SS} to V_{DD}, V_H = Floating			0.1	1	µA
TC_R	Resistance temperature coefficient	Input Code = 0x80h			92		ppm/°C
$R_{TOT,MATCH}$	Channel-to-channel resistance match				0.1		%
Voltage Divider Mode							
INL (3)(4)	Integral non-linearity			–0.5		0.5	LSB
DNL (3)(5)	Differential non-linearity			–0.25		0.25	LSB
ZS_{ERROR} (6)(7)	Zero-scale error			0	0.1	2	LSB
FS_{ERROR} (6)(8)	Full-scale error			–2	–0.1	0	LSB
V_{MATCH} (6)(9)	Channel-to-Channel matching	Wiper at the same tap position, same voltage at all H and same voltage at all L terminals		–2		2	LSB
TC_V	Ratiometric temperature coefficient	Wiper set at mid-scale			4		ppm/°C
BW	Bandwidth	TPL0102-100	Wiper set at mid-scale C_{LOAD} = 10 pF		229		kHz
T_{SW}	Wiper setting time	TPL0102-100			3.6		µS
THD	Total harmonic distortion	V_H = 1 V_{RMS} at 1 kHz, V_L = (V_{DD} – V_{SS})/2, Measurement at W	TPL0102-100		0.03		%
X_{TALK}	Cross talk	f_H = 1 kHz, V_L = GND, Measurement at W			–82		dB

(1) Terminal and Wiper Capacitance extracted from self admittance of three port network measurement

$$Y_{ii} = \frac{I_i}{V_i}\Big|_{V_k=0 \text{ for } k\neq i}$$

(2) Digital Potentiometer Macromodel



(3) LSB = ($V_{MEAS[code\ 255]}$ – $V_{MEAS[code\ 0]}$) / 255
(4) INL = (($V_{MEAS[code\ x]}$ – $V_{MEAS[code\ 0]}$) / LSB) - [code x]
(5) DNL = (($V_{MEAS[code\ x]}$ – $V_{MEAS[code\ x-1]}$) / LSB) – 1
(6) IDEAL_LSB = (V_H-V_L) / 256
(7) ZS_{ERROR} = $V_{MEAS[code\ 0]}$ / IDEAL_LSB
(8) FS_{ERROR} = [($V_{MEAS[code\ 255]}$ – (V_H-V_L)) / IDEAL_LSB] + 1
(9) V_{MATCH} = ($V_{MEAS\_A[code\ x]}$ – $V_{MEAS\_B[code\ x]}$) / IDEAL_LSB

ELECTRICAL CHARACTERISTICS (continued)

V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, V_H= V_{DD}, V_L= GND, T_A = –40°C to 85°C (unless otherwise noted). Typical values are at V_{DD}= 5V, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS		MIN	TYP	MAX	UNIT
RHEOSTAT MODE (Measurements between W and L with H not connected, or between W and H with L not connected)							
RINL (10)(11)	Integral non-linearity			–1		1	LSB
RDNL (10)(12)	Differential non-linearity			–0.5		0.5	LSB
R_{OFFSET} (13)(14)	Offset			0	0.2	2	LSB
R_{MATCH} (13)(15)	Channel-to-Channel matching			–2		2	LSB
RBW	Bandwidth	Code = 0x00h, L Floating, Input applied to W, Measure at H, C_{LOAD} = 10 pF	TPL0102-100		54		kHz

(10) RLSB = ($R_{MEAS[code\ 255]}$ – $R_{MEAS[code\ 0]}$) / 255
(11) RINL =(($R_{MEAS[code\ x]}$ – $R_{MEAS[code\ 0]}$) / RLSB) - [code x]
(12) RDNL =(($R_{MEAS[code\ x]}$ – $R_{MEAS[code\ x-1]}$) / RLSB)– 1
(13) IDEAL_RLSB = R_{TOT} / 256
(14) R_{OFFSET} = $R_{MEAS[code\ 0]}$ / IDEAL_RLSB
(15) R_{MATCH} = ($R_{MEAS\_A[code\ x]}$ – $R_{MEAS\_B[code\ x]}$) / IDEAL_RLSB

OPERATING CHARACTERISTICS

V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, V_H = V_{DD}, V_L = GND, T_A= –40°C to 85°C (unless otherwise noted). Typical values are at V_{DD} = 5V, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$I_{DD(STBY)}$	V_{DD} standby current	V_{DD} = 2.75 V, V_{SS} = –2.75, I^2C interface in standby mode		0.2	1	µA
$I_{SS(STBY)}$	V_{SS} standby current	V_{DD} = 2.75 V, V_{SS} = –2.75, I^2C interface in standby mode	–1	–0.2		µA
$I_{DD(SHUTDOWN)}$	V_{DD} shutdown current	V_{DD} = 2.75 V, V_{SS} = –2.75, I^2C interface in standby mode		0.2	1	µA
$I_{SS(SHUTDOWN)}$	V_{SS} shutdown current	V_{DD} = 2.75 V, V_{SS} = –2.75, I^2C interface in standby mode	–1	–0.2		µA
I_{DD}	V_{DD} current during non-volatile write	V_{DD} = 2.75 V, V_{SS} = –2.75		200	µA	
I_{SS}	V_{SS} current during non-volatile write	V_{DD} = 2.75 V, V_{SS} = –2.75	-200			µA
$I_{LKG-DIG}$	Digital pins leakage current (A0, A1, A2, SDA, and SCL)		–1		1	µA
V_{POR}	Power-on recall voltage	Minimum V_{DD} at which memory recall occurs		2		V
EEPROM Specification						
	EEPROM endurance			100,000		Cycles
	EEPROM retention	T_A = 85°C		100		Years
t_{WC}	Non-volatile write cycle time			20		ms
Wiper Timing Characteristics						
t_{WRT}	Wiper response time	SCL falling edge of last bit of wiper data byte to wiper new position		600		ns
$t_{SHUTDOWNREC}$	Wiper position recall time from shut-down mode	SCL falling edge of last bit of ACR data byte to wiper stored position and H connection		800		ns
t_D	Power-up delay	V_{DD} above V_{POR}, to wiper initial value register recall completed, and I^2C interface in standby mode		35	100	µs
C_{IN}	Pin capacitance	A0, A1, A2, SDA SCL pins		7		pF

OPERATING CHARACTERISTICS (continued)

V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, V_H = V_{DD}, V_L = GND, T_A= –40°C to 85°C (unless otherwise noted). Typical values are at V_{DD} = 5V, T_A = 25°C (unless otherwise noted).

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
I²C Interface Specifications						
V_{IH}	Input high voltage		0.7 x V_{DD}		5.5	V
V_{IL}	Input low voltage		0		0.3 x V_{DD}	V
V_{OL}	Output low voltage	SDA pin, I_{OL} = 4 mA			0.4	V
C_{IN}	Pin capacitance	A0, A1, A2, SDA SCL pins		7		pF

TIMING REQUIREMENTS

V_{DD} = 2.7V to 5.5V, V_{SS} = 0V, V_H = V_{DD}, V_L = GND, T_A = –40°C to 85°C (unless otherwise noted). Typical values are at V_{DD} = 5V, T_A = 25°C (unless otherwise noted).

		STANDARD MODE I²C BUS		FAST MODE I²C BUS		UNIT
		MIN	MAX	MIN	MAX	
I²C Interface Timing Requirements						
f_{SCL}	I²C clock frequency	0	100	0	400	kHz
t_{SCH}	I²C clock high time	4		0.6		µs
t_{SCL}	I²C clock low time	4.7		1.3		µs
tsp	I²C spike time	0	50	0	50	ns
t_{SDS}	I²C serial data setup time	250		100		ns
t_{SDH}	I²C serial data hold time	0		0		ns
t_{ICR}	I²C input rise time		1000	20 + 0.1C_b (1)	300	ns
t_{ICF}	I²C input fall time		300	20 + 0.1C_b (1)	300	ns
t_{ICF}	I²C output fall time, 10 pF to 400 pF bus		300	20 + 0.1C_b (1)	300	ns
t_{BUF}	I²C bus free time between stop and start	4.7		1.3		µs
t_{STS}	I²C start or repeater start conditions setup time	4.7		1.3		µs
t_{STH}	I²C start or repeater start condition hold time	4		0.6		µs
t_{SPS}	I²C stop condition setup time	4		0.6		µs
$t_{VD(DATA)}$	Valid data time, SCL low to SDA output valid		1		1	µs
$t_{VD(DATA)}$	Valid data time of ACK condition, ACK signal from SCL low to SDA (out) low		1		1	µs

(1) C_b = total capacitance of one bus line in pF

REGISTER DESCRIPTION

Slave Address

Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 2	Bit 0 (LSB)
1	0	1	0	A2	A1	A0	R/W

TPL0102 Register Map

REGISTER ADDRESS (HEX)	NON-VOLATILE	VOLATILE
0	IVRA	WRA
1	IVRB	WRB
2	General purpose	N/A
3	General purpose	N/A
4	General purpose	N/A
5	General purpose	N/A
6	General purpose	N/A
7	General purpose	N/A
8	General purpose	N/A
9	General purpose	N/A
A	General purpose	N/A
B	General purpose	N/A
C	General purpose	N/A
E	General purpose	N/A
D	General purpose	N/A
F	Reserved	
10	N/A	ACR

IVRA (Initial Value Register for Potentiometer A)

- Register Address: 00H
- Factory Programmed Value: 80H
- Type: Non-volatile Write/Read

NAME	SIZE (BITS)	DESCRIPTION
IVRA	8	Non-volatile register to store wiper position for potentiometer A

WRA (Wiper Resistance Register for Potentiometer A)

- Register Address: 00H
- Reset Value: Same as IVRA
- Type: Volatile Write/Read

NAME	SIZE (BITS)	DESCRIPTION
WRA	8	Volatile register to change wiper position for potentiometer A

IVRB (Initial Value Register for Potentiometer B)

- Register Address: 01H
- Factory Programmed Value: 80H
- Type: Non-volatile Write/Read

NAME	SIZE (BITS)	DESCRIPTION
IVRB	8	Non-volatile register to store wiper position for potentiometer B

WRB (Wiper Resistance Register for Potentiometer B)

- Register Address: 01H
- Reset Value: Same as IVRB
- Type: Volatile Write/Read

NAME	SIZE (BITS)	DESCRIPTION
WRB	8	Volatile register to change wiper position for potentiometer B

ACR (Access Control Register)

- Register Address: 00H
- Reset Value: 40H
- Type: Non-volatile Write/Read

NAME	SIZE (BITS)	DESCRIPTION							
IVRA	8	Non-volatile register to store wiper position for potentiometer A							
ACR	8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
		VOL	$\overline{\text{SHDN}}$	WIP	0	0	0	0	0
Default Value		0	1	0	0	0	0	0	0

NAME	SIZE (BITS)	DESCRIPTION
VOL	1	0: Non-volatile registers (IVRA, IVRB) are accessible. Value written to IVRi register is also written to the corresponding WRi.
		1: Only Volatile Registers (WRi) are accessible.
$\overline{\text{SHDN}}$	1	0: Shut-down mode is enabled. Potentiometers are in shut-down mode. (see Figure 2)
		1: Shut-down mode is disabled
WIP (Read-only bit)	1	0: Non-volatile write operation is not in progress
		1: Non-volatile write operation is in progress (it is not possible to write to the WRi or ACR while WIP = 1)

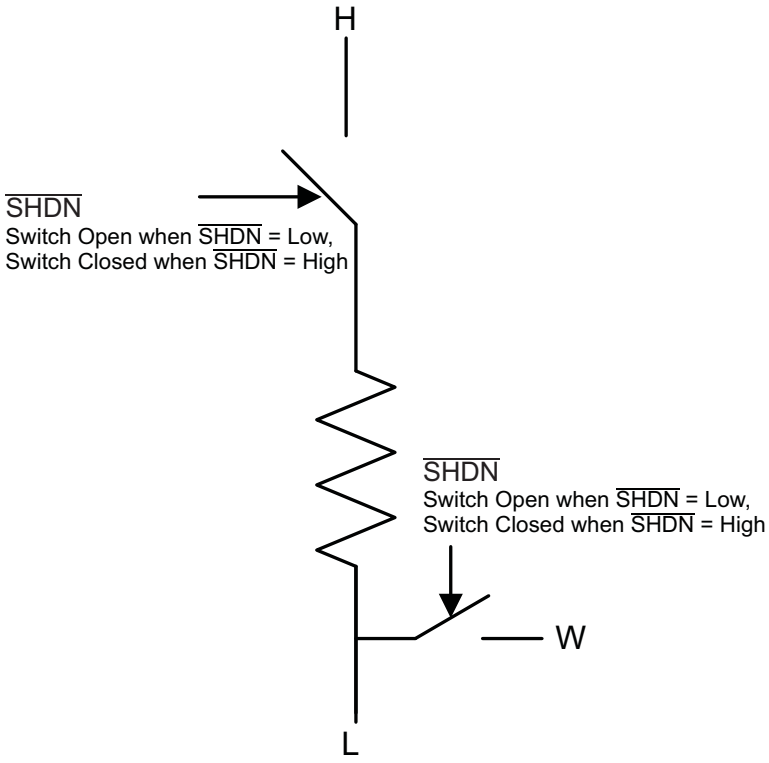


Figure 2. Potentiometer in Shut-Down Mode

PRINCIPLES OF OPERATION

The TPL0102 is a two channel, linear-taper digital potentiometer with 256 wiper positions. Each potentiometer can be used as a three-terminal potentiometer or as a two-terminal rheostat. The TPL0102-100 has an end-to-end resistance of 100kΩ.

The TPL0102 has non-volatile memory (EEPROM) which can be used to store the wiper position. When the device is powered down, the last value stored in the IVR register will be maintained in the non-volatile memory. When power is restored, the contents of the IVR register are recalled and loaded into the corresponding WR register to set the wipers to the initial position. The internal registers of the TPL0102 can be accessed using the I^2C interface.

The position of the wiper terminal is controlled by the value in the WR 8-bit register. When the WR contains all zeroes, the wiper terminal W is closest to its L (Low) terminal. As the value of the WR increases from all zeroes to all ones (255 decimal), the wiper moves monotonically from the position closest to L to the position closest to H. At the same time, the resistance between W and L increases monotonically, whereas the resistance between W and H decreases monotonically.

Potentiometer Pin Description

HA,HB,LA,LB

The high (HA, HB) and low (LA, LB) terminals of the TPL0102 are equivalent to the fixed terminals of a mechanical potentiometer. The H and L terminals do not have any polarity restrictions, i.e. H can be at a higher voltage than L, or L can be at a higher voltage than H. The WA and WB terminals are the wipers and equivalent to the movable terminal of a mechanical potentiometer. The position of the wiper is set using the WR register. With the WR register set to 255 decimal, the wiper is closest to the H terminal, and with the WR register set to 0, the wiper is closest to the L terminal.

SDA, SCL

SDA is a bi-directional serial data input/output pin for I^2C communication. SDA is an open drain output and requires an external pull-up resistor.

SCL is the serial clock input for I^2C communication. SCL requires an external pull-up resistor.

A0, A1, A2

These inputs are used to set the last three bits of the I^2C address of the device. By using different values for A0, A1, A2, up to eight TPL0102 devices can be used on the same I^2C bus.

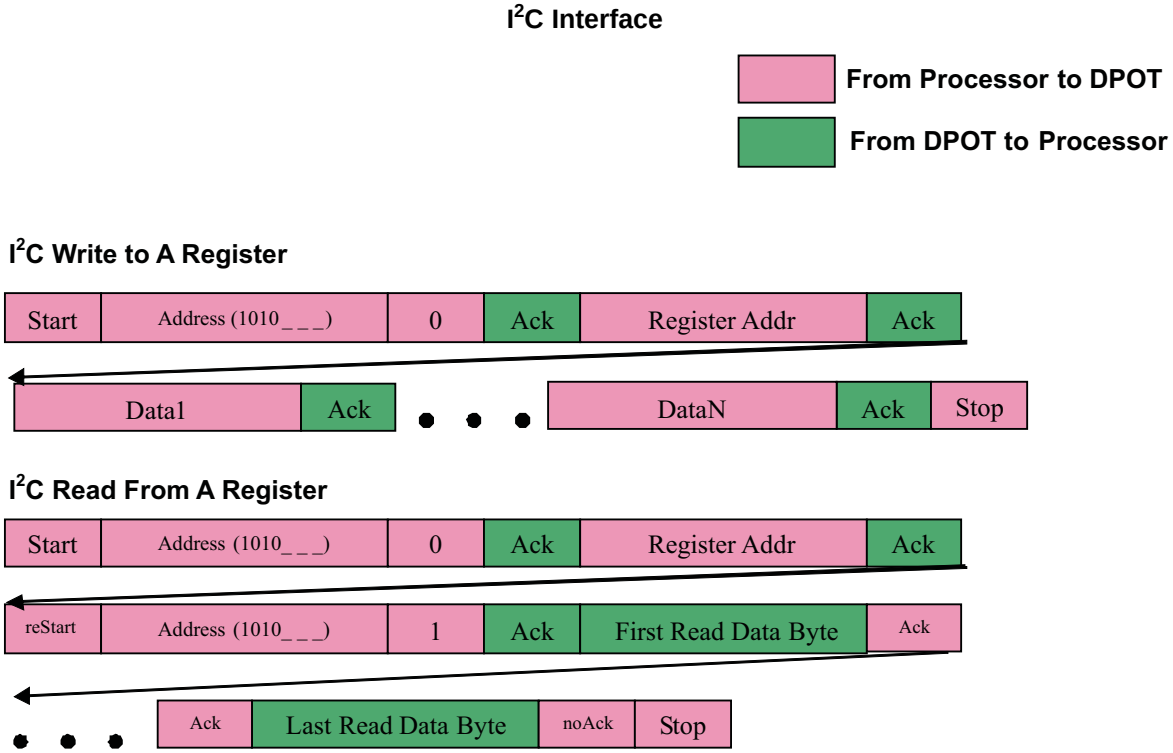
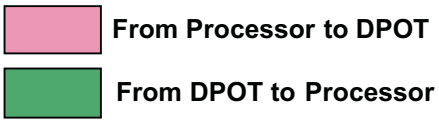
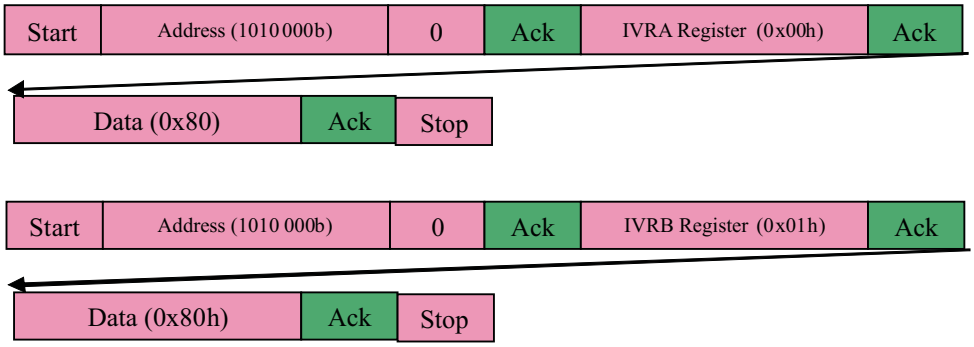


Figure 3. I²C Interface

Following is a sample sequence to set wipers of both potentiometers at mid-scale. Assume A0, A1, and A2 are zero and device has just been powered up.



Method 1: First Write 0x80 to IVRA and then write 0x80 to IVRB Register



Method 2: Perform a multi byte write to IVRA and IVRB Register

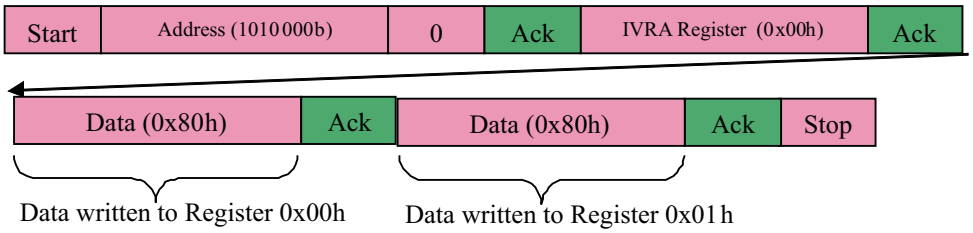


Figure 4. I^2C Interface Example

Standard I²C Interface Details

The bidirectional I²C bus consists of the serial clock (SCL) and serial data (SDA) lines. Both lines must be connected to a positive supply via a pullup resistor when connected to the output stages of a device. Data transfer may be initiated only when the bus is not busy.

I²C communication with this device is initiated by the master sending a start condition, a high-to-low transition on the SDA input/output while the SCL input is high (see Figure 5). After the start condition, the device address byte is sent, MSB first, including the data direction bit (R/W). This device does not respond to the general call address. After receiving the valid address byte, this device responds with an ACK, a low on the SDA input/output during the high of the ACK-related clock pulse

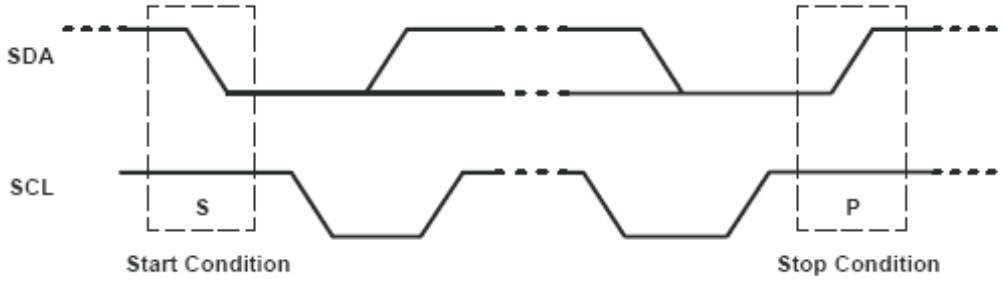


Figure 5. Definition of Start and Stop Conditions

The data byte follows the address ACK. The R/W bit is kept low for transfer from the master to the slave. The data byte is followed by an ACK sent from this device. Data are output only if complete bytes are received and acknowledged. The output data is valid at time (tpv) after the low-to-high transition of SCL, during the clock cycle for the ACK. On the I²C bus, only one data bit is transferred during each clock pulse. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as control commands (start or stop) (see Figure 6).

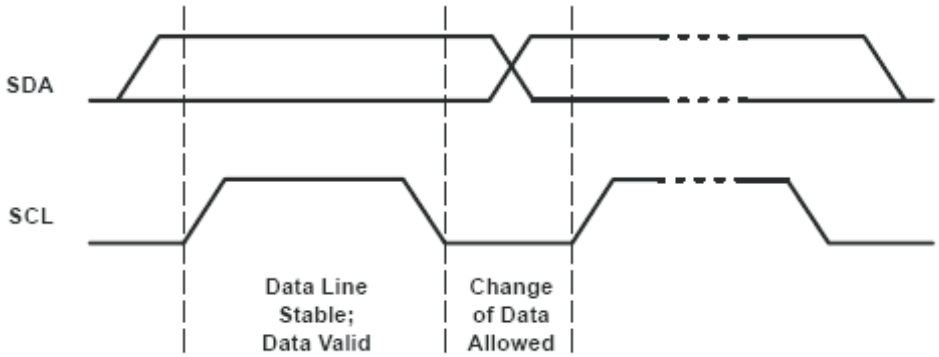


Figure 6. Bit Transfer

A stop condition, a low-to-high transition on the SDA input/output while the SCL input is high, is sent by the master (see Figure 5).

The number of data bytes transferred between the start and the stop conditions from transmitter to receiver is not limited. Each byte of eight bits is followed by one ACK bit. The transmitter must release the SDA line before the receiver can send an ACK bit.

A slave receiver that is addressed must generate an ACK after the reception of each byte. The device that acknowledges has to pull down the SDA line during the ACK clock pulse so that the SDA line is stable low during the high pulse of the ACK-related clock period (see Figure 7). Setup and hold times must be taken into account.

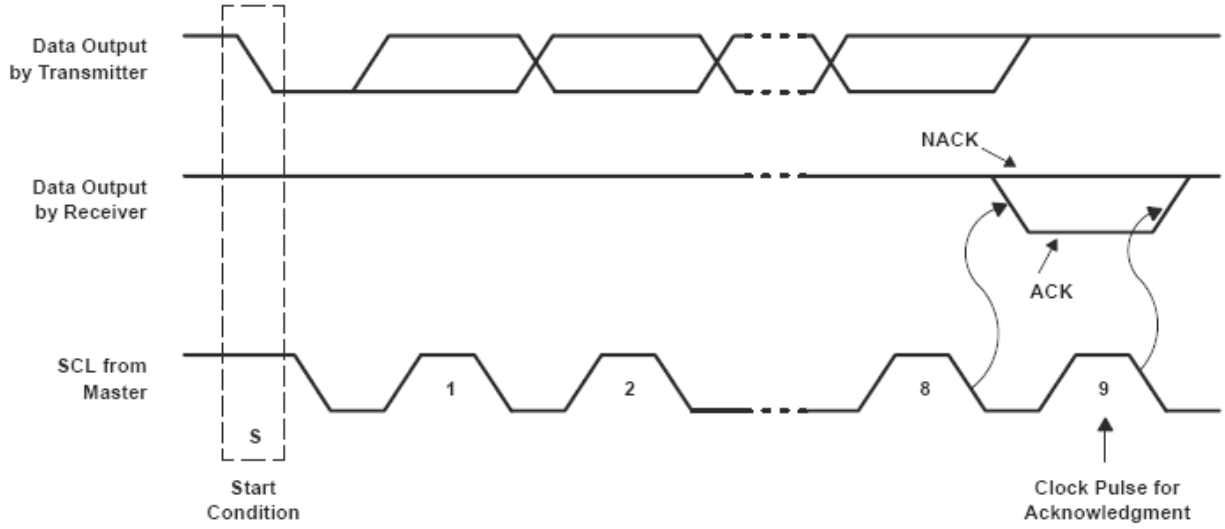


Figure 7. Acknowledgment on the I^2C Bus

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Peak Temp (3)	Samples (Requires Login)
TPL0102-100PWR	PREVIEW	TSSOP	PW	14	2000	TBD	Call TI	Call TI	
TPL0102-100RUCR	ACTIVE	QFN	RUC	14	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	

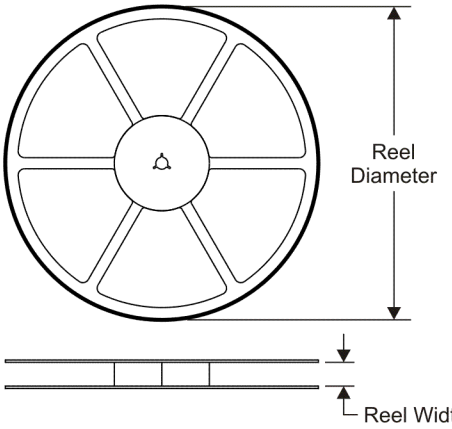
(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

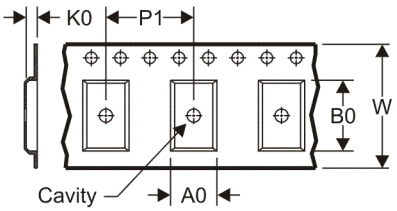
(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

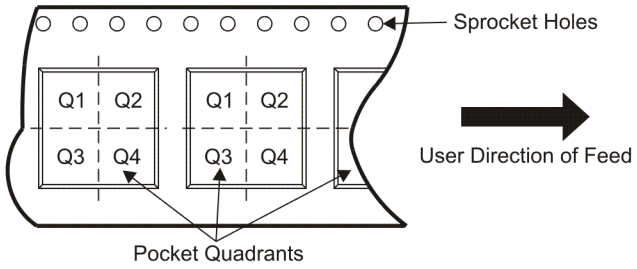


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

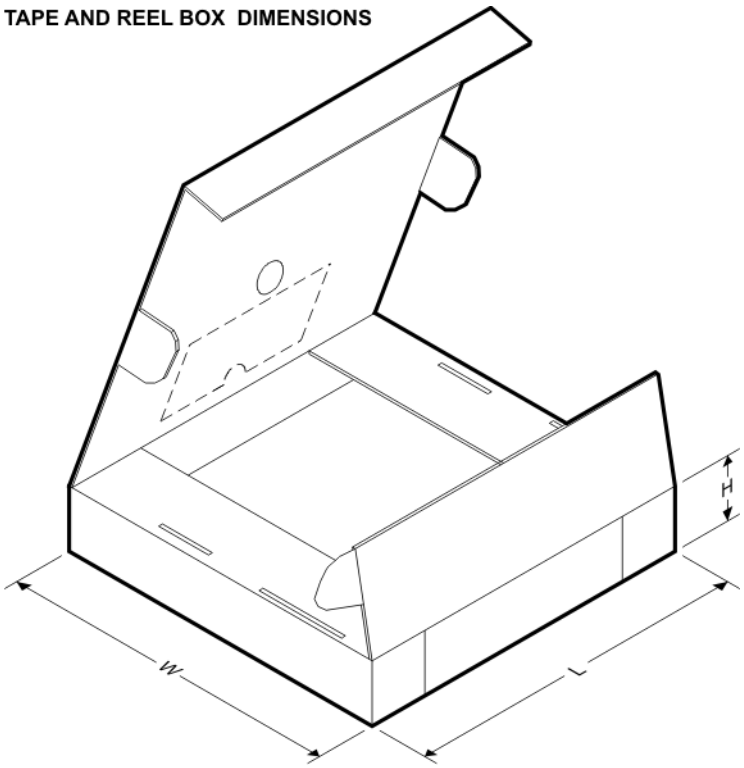
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPL0102-100RUCR	QFN	RUC	14	3000	180.0	8.4	2.3	2.3	0.55	4.0	8.0	Q2

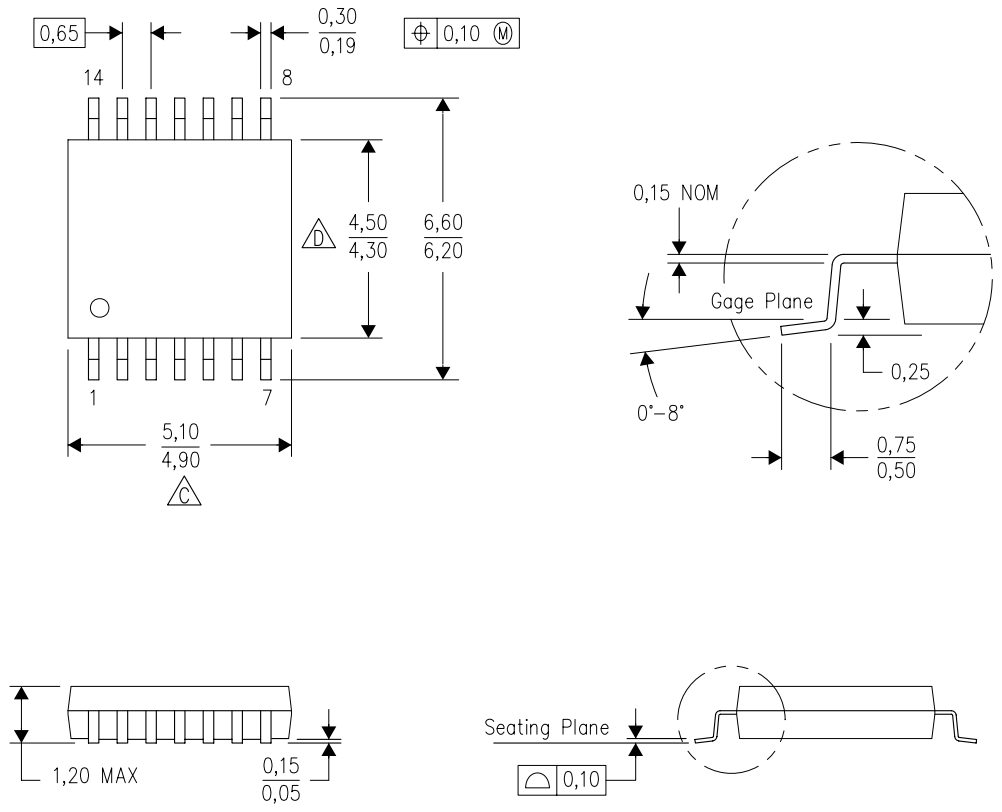
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPL0102-100RUCR	QFN	RUC	14	3000	202.0	201.0	28.0

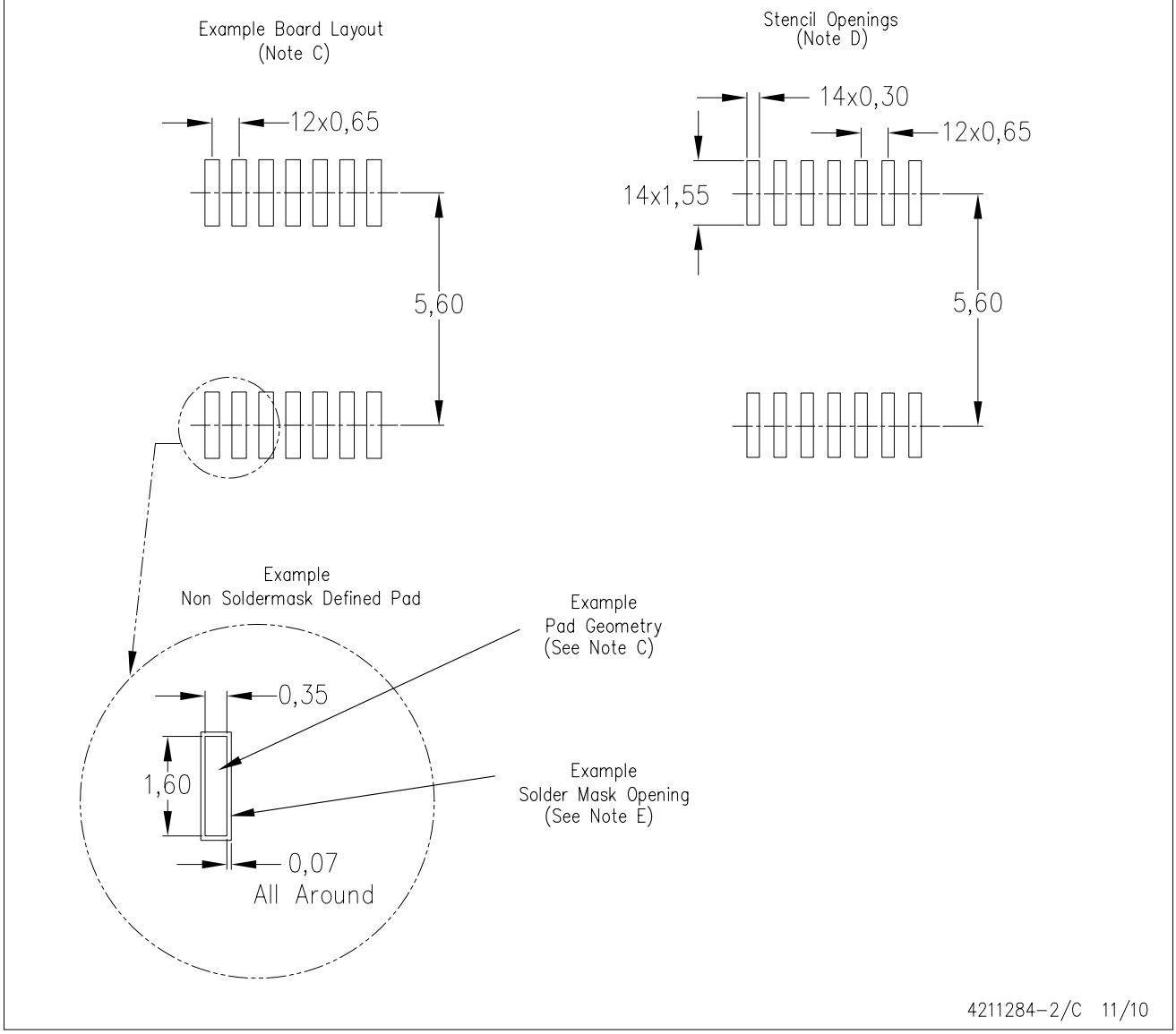
PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



4040064–3/G 02/11

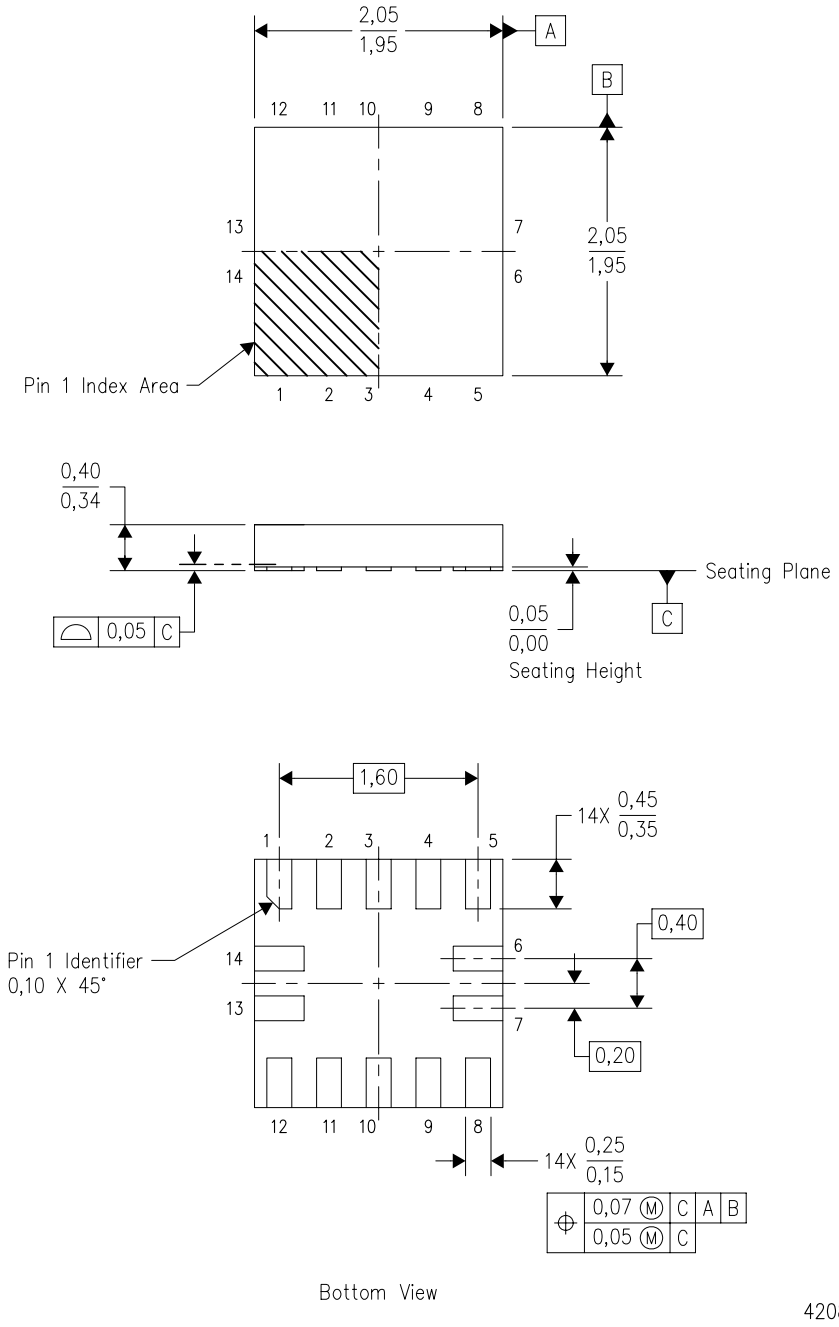
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G14) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

RUC (S–PX2QFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

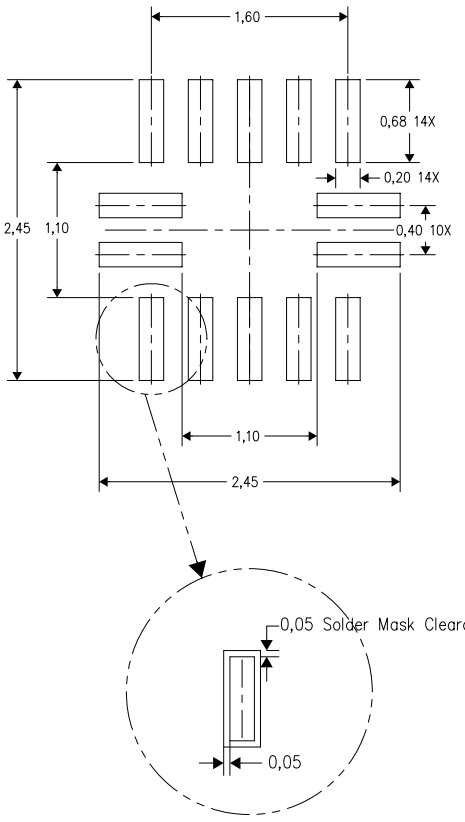


4208447/C 08/2008

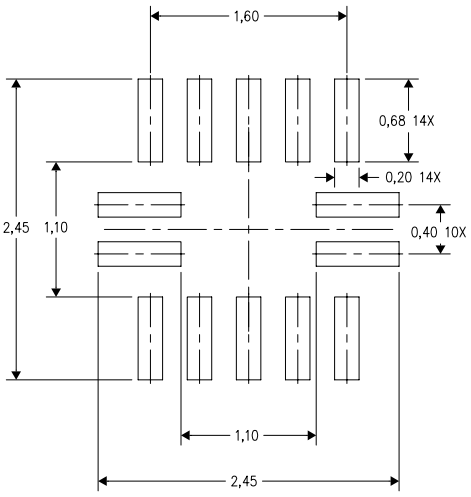
NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. QFN (Quad Flatpack No–lead) package configuration.
D. This package complies to JEDEC MO–288 variation X2GFE.

RUC (S–PX2QFN–N14) PLASTIC QUAD FLATPACK NO–LEAD

Example Board Layout



Example Stencil Design
(Note E)



Note D

4211124/A 06/10

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Customers should contact their board fabrication site for minimum solder mask web tolerances between signal pads.
E. Maximum stencil thickness 0,127 mm (5 mils). All linear dimensions are in millimeters.
F. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
G. Side aperture dimensions over–print land for acceptable area ratio > 0.66. Customer may reduce side aperture dimensions if stencil manufacturing process allows for sufficient release at smaller opening.

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