Single Channel, 16-Bit, Serial Input, Current Source DAC

Preliminary Technical Data

AD5420

FEATURES

16-Bit Resolution and Monotonicity
Current Output Ranges: 4–20mA, 0–20mA or 0–24mA
0.1% typ Total Unadjusted Error (TUE)
5ppm/°C Output Drift
Flexible Serial Digital Interface
On-Chip Output Fault Detection
On-Chip Reference (10 ppm/°C Max)
Asynchronous CLEAR Function
Power Supply (AV_{DD}) Range
10.8V to 60 V; AD5420BCPZ
10.8V to 40V; AD5420BREZ
Output Loop Compliance to AV_{DD} – 2.5 V
Temperature Range: -40°C to +85°C
TSSOP and LFCSP Packages

APPLICATIONS

Process Control
Actuator Control
PLC

GENERAL DESCRIPTION

The AD5420 is a low-cost, precision, fully integrated 16-bit converter offering a programmable current source output designed to meet the requirements of industrial process control applications.

The output current range is programmable to 4mA to 20 mA, 0mA to 20mA or an over range function of 0mA to 24mA. The output is open circuit protected and can drive inductive loads of 1H. The device is specified to operate with a power supply range from 10.8 V to 40V (AD5420BREZ) or 10.8V to 60V (AD5420BCPZ). Output loop compliance is 0 V to AV_{DD} – 2.5 V.

The flexible serial interface is SPI and MICROWIRE compatible and can be operated in 3-wire mode to minimize the digital isolation required in isolated applications.

The device also includes a power-on-reset function ensuring that the device powers up in a known state and an asynchronous CLEAR pin which sets the output to the low end of the selected current range.

The total output error is typically ±0.1% FSR.

Table 1. Related Devices

Part Number	Description
AD5422	Single Channel, 16-Bit, Serial Input Current Source and Voltage Output DAC
AD5412	Single Channel, 12-Bit, Serial Input Current Source and Voltage Output DAC
AD5410	Single Channel, 12-Bit, Serial Input Current Source DAC

Rev. PrD
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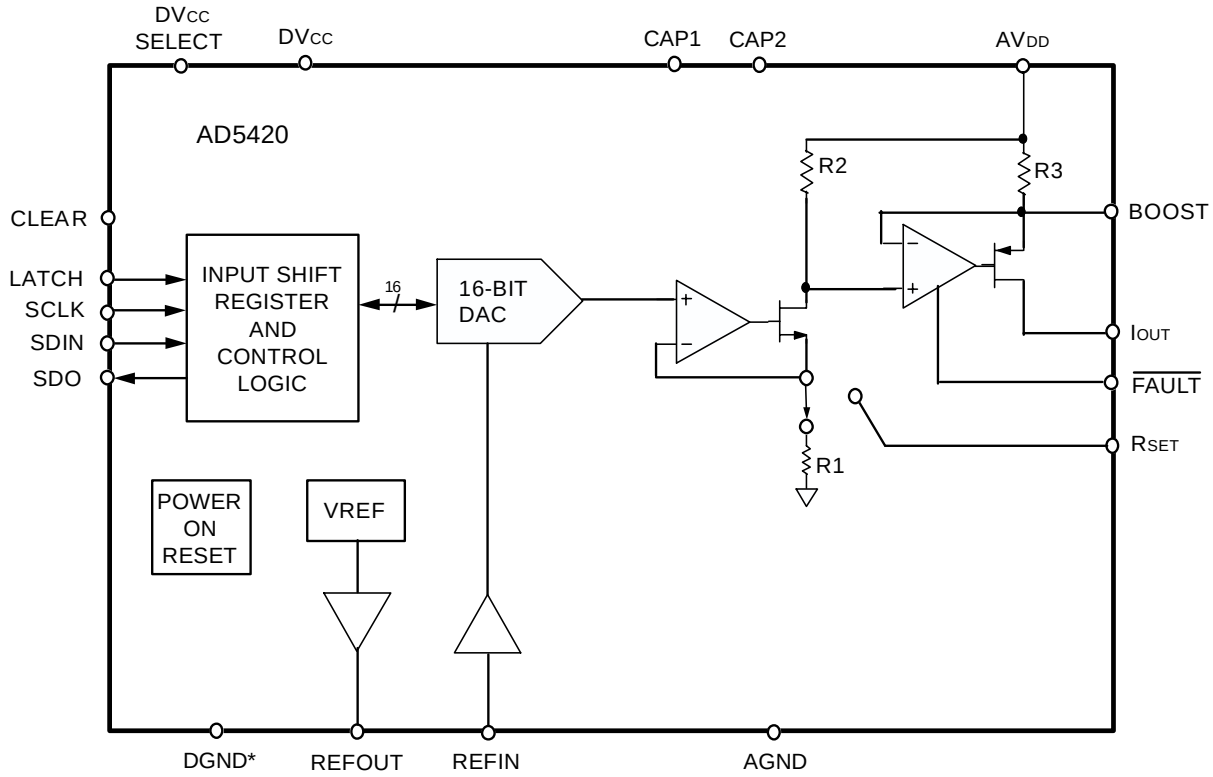
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REVISION HISTORY

PrD – Preliminary Version.

FUNCTIONAL BLOCK DIAGRAM



*LFCSP Package

Figure 1.

SPECIFICATIONS

AV_{DD} = 10.8V to 40V/60V[1], AGND = DGND = 0 V, REFIN= +5 V external; DV_{CC} = 2.7 V to 5.5 V, R_L = 300Ω, H_L = 50mH; all specifications T_{MIN} to T_{MAX}, 0 to 24 mA range unless otherwise noted.

Table 2.

Parameter	Value[2]	Unit	Test Conditions/Comments
Output Current Ranges	0 to 24	mA	
	0 to 20	mA	
	4 to 20	mA	
ACCURACY			
Resolution	16	Bits	
Total Unadjusted Error (TUE)	±0.3	% FSR max	Over temperature, supplies, and time, typically 0.1% FSR
TUE TC[3]	±5	ppm/°C typ	
Relative Accuracy (INL)	±0.012	% FSR max	
Differential Nonlinearity (DNL)	±1	LSB max	Guaranteed monotonic
Offset Error	±0.05	% FSR max	
Offset Error Drift	±5	µv/°C typ	
Gain Error	±0.02	% FSR max	@ 25°C, error at other temperatures obtained using gain TC
Gain TC[3]	±8	ppm FSR/°C max	
Full-Scale Error	0.05	% FSR max	@ 25°C, error at other temperatures obtained using gain TC
Full-Scale TC[3]	±8	ppm FSR/°C	
OUTPUT CHARACTERISTICS[3]			
Current Loop Compliance Voltage	AVDD - 2.5	V max	
Output Current Drift vs. Time	TBD	ppm FSR/500 hr typ	
	TBD	ppm FSR/1000 hr typ	
Resistive Load	TBD	Ω max	
Inductive Load	1	H max	
DC PSRR	10	µA/V max	
Output Impedance	50	MΩ typ	
REFERENCE INPUT/OUTPUT			
Reference Input[3]			
Reference Input Voltage	5	V nom	±1% for specified performance
DC Input Impedance	30	kΩ min	Typically 40 kΩ
Reference Range	4 to 5	V min to V max	
Reference Output			
Output Voltage	4.998 to 5.002	V min to V max	@ 25°C
Reference TC	±10	ppm/°C max	
Output Noise (0.1 Hz to 10 Hz)[3]	18	µV p-p typ	
Noise Spectral Density[3]	120	nV/√Hz typ	@ 10 kHz
Output Voltage Drift vs. Time[3]	±40	ppm/500 hr typ	
	±50	ppm/1000 hr typ	
Capacitive Load	TBD	nF max	
Load Current	5	mA typ	
Short Circuit Current	7	mA typ	
Line Regulation[3]	10	ppm/V typ	
Load Regulation[3]	TBD	ppm/mA	
Thermal Hysteresis[3]	TBD	ppm	
DIGITAL INPUTS[3]			DV_{CC} = 2.7 V to 5.5 V, JEDEC compliant
V_{IH}, Input High Voltage	2	V min	
V_{IL}, Input Low Voltage	0.8	V max	
Input Current	±1	µA max	Per pin
Pin Capacitance	10	pF typ	Per pin

Parameter	Value[2]	Unit	Test Conditions/Comments
DIGITAL OUTPUTS [3]			
SDO			
V_{OL}, Output Low Voltage	0.4	V max	sinking 200 µA
V_{OH}, Output High Voltage	DV_{CC} – 0.5	V min	sourcing 200 µA
High Impedance Leakage Current	±1	µA max	
High Impedance Output Capacitance	5	pF typ	
$\overline{FAULT}$			
V_{OL}, Output Low Voltage	0.4	V max	10kΩ pull-up resistor to DV_{CC}
V_{OL}, Output Low Voltage	0.6	V typ	@ 2.5 mA
V_{OH}, Output High Voltage	3.6	V min	10kΩ pull-up resistor to DV_{CC}
POWER REQUIREMENTS			
AV_{DD}	10.8 to 60	V min to V max	AD5420BCPZ
	10.8 to 40	V min to V max	AD5420BREZ
DV_{CC}			
Input Voltage	2.7 to 5.5	V min to V max	Internal supply disabled
Output Voltage	4.5	V typ	DV_{CC} can be overdriven up to 5.5V
Output Load Current	5	mA typ	
Short Circuit Current	20	mA typ	
AI_{DD}	TBD	mA	
DI_{CC}	1	mA max	$V_{IH} = DV_{CC}$, V_{IL} = GND, TBD mA typ
Power Dissipation	TBD	mW typ	AV_{DD} = 40V
	TBD	mW typ	AV_{DD} = 60V
	TBD	mW typ	AV_{DD} = 15V

[1] Maximum supply for the AD5420BREZ is 40V, Maximum supply for the AD5420BCPZ is 60V
[2] Temperature range: -40°C to +85°C; typical at +25°C.
[3] Guaranteed by design and characterization, not production tested.

AC PERFORMANCE CHARACTERISTICS

AV_{DD} = 10.8V to 40V/60V[1], AGND = DGND = 0 V, REFIN= +5 V external; DV_{CC} = 2.7 V to 5.5 V, R_L = 300Ω, H_L = 50mH; all specifications T_{MIN} to T_{MAX}, 0 to 24 mA range unless otherwise noted.

Table 3.

Parameter[2]		Unit	Test Conditions/Comments
DYNAMIC PERFORMANCE			
Output Current Settling Time	TBD	µs typ	To 0.1% FSR , L = 1H
	TBD	µs typ	To 0.1% FSR , L < 1mH

[1] Maximum supply for the AD5420BREZ is 40V, Maximum supply for the AD5420BCPZ is 60V
[2] Guaranteed by design and characterization, not production tested.

TIMING CHARACTERISTICS

AV_{DD} = 10.8V to 40V/60V[1], AGND = DGND = 0 V, REFIN= +5 V external; DV_{CC} = 2.7 V to 5.5 V, R_L = 300Ω, H_L = 50mH; all specifications T_{MIN} to T_{MAX}, 0 to 24 mA range unless otherwise noted.

Table 4.

Parameter[2, 3, 4]	Limit at T_{MIN}, T_{MAX}	Unit	Description
Write Mode			
t_1	33	ns min	SCLK cycle time
t_2	13	ns min	SCLK low time
t_3	13	ns min	SCLK high time
t_4	13	ns min	LATCH delay time
t_5	40	ns min	LATCH high time
t_5	5	µs min	LATCH high time (After a write to the CONTROL register)
t_6	5	ns min	Data setup time
t_7	5	ns min	Data hold time
t_8	40	ns min	LATCH low time
t_9	20	ns min	CLEAR pulsewidth
t_{10}	5	µs max	CLEAR activation time
Readback Mode			
t_{11}	82	ns min	SCLK cycle time
t_{12}	33	ns min	SCLK low time
t_{13}	33	ns min	SCLK high time
t_{14}	13	ns min	LATCH delay time
t_{15}	40	ns min	LATCH high time
t_{16}	5	ns min	Data setup time
t_{17}	5	ns min	Data hold time
t_{18}	40	ns min	LATCH low time
t_{19}	40	ns max	Serial output delay time ($C_{L\,SDO}$[5] = 15pF)
t_{20}	33	ns max	LATCH rising edge to SDO tri-state
Daisychain Mode			
t_{21}	82	ns min	SCLK cycle time
t_{22}	33	ns min	SCLK low time
t_{23}	33	ns min	SCLK high time
t_{24}	13	ns min	LATCH delay time
t_{25}	40	ns min	LATCH high time
t_{26}	5	ns min	Data setup time
t_{27}	5	ns min	Data hold time
t_{28}	40	ns min	LATCH low time
t_{29}	40	ns max	Serial output delay time ($C_{L\,SDO}$[5] = 15pF)

[1] Maximum supply for the AD5420BREZ is 40V, Maximum supply for the AD5420BCPZ is 60V
[2] Guaranteed by characterization. Not production tested.
[3] All input signals are specified with $t_R = t_F$ = 5 ns (10% to 90% of DV_{CC}) and timed from a voltage level of 1.2 V.
[4] See Figure 2, Figure 3, and Figure 4.
[5] $C_{L\,SDO}$ = Capacitive load on SDO output.

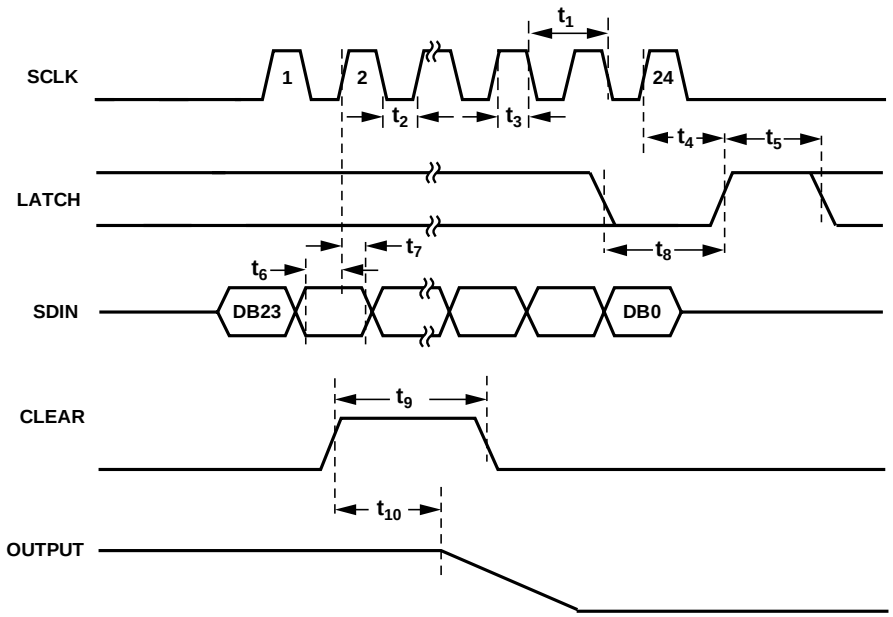


Figure 2. Write Mode Timing Diagram

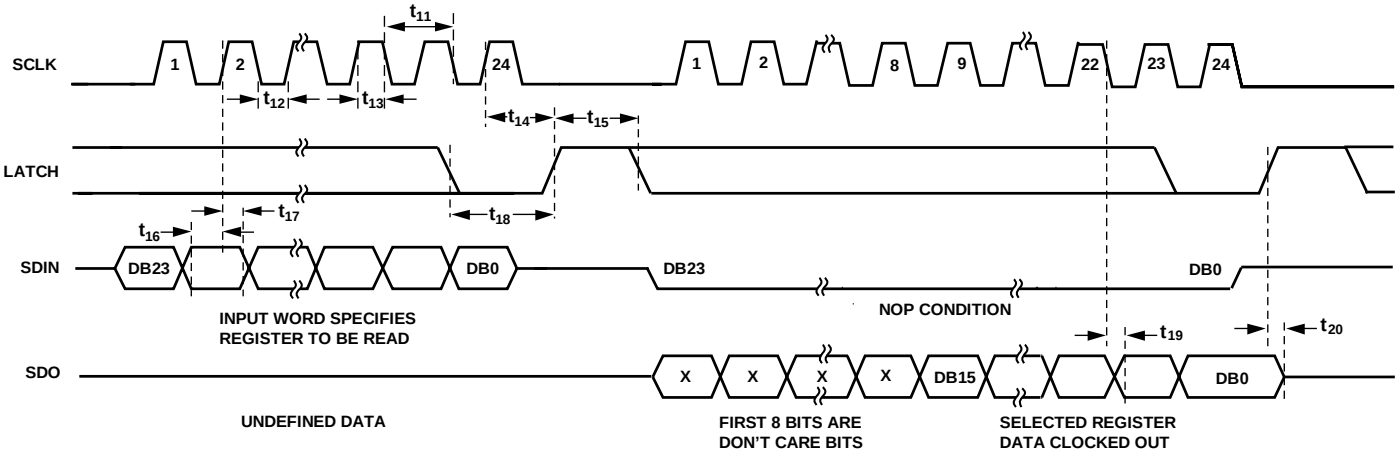


Figure 3. Readback Mode Timing Diagram

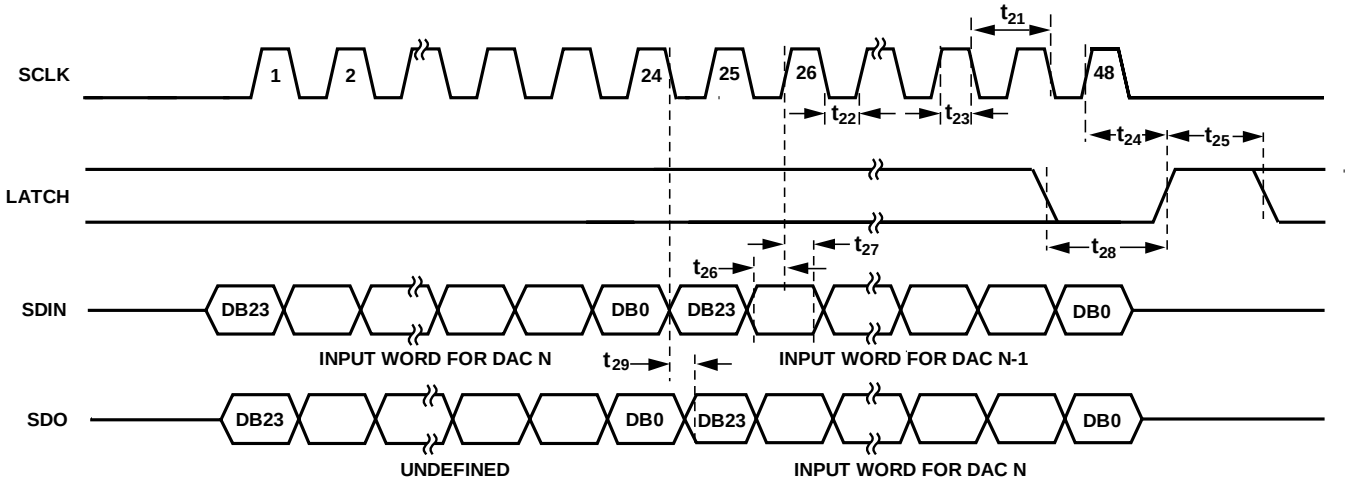


Figure 4. Daisychain Mode Timing Diagram

ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise noted.
Transient currents of up to 100 mA do not cause SCR latch-up.

Table 5.

Parameter	Rating
AV_{DD} to AGND, DGND	−0.3V to 60V
DV_{CC} to AGND, DGND	−0.3 V to +7 V
Digital Inputs to AGND, DGND	−0.3 V to DV_{CC} + 0.3 V or 7 V (whichever is less)
Digital Outputs to AGND, DGND	−0.3 V to DV_{CC} + 0.3 V or 7V (whichever is less)
REFIN/REFOUT to AGND, DGND	−0.3 V to +7 V
I_{OUT} to AGND, DGND	−0.3V to AV_{DD}
AGND to DGND	-0.3V to +0.3V
Operating Temperature Range	
Industrial	−40°C to +85[1]°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature (T_J max)	125°C
24-Lead TSSOP Package	
θ_{JA} Thermal Impedance	42°C/W
40-Lead LFCSP Package	
θ_{JA} Thermal Impedance	28°C/W
Power Dissipation	(T_J max – T_A)/ θ_{JA}
Lead Temperature	JEDEC Industry Standard
Soldering	J-STD-020

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

[1] Power dissipated on chip must be de-rated to keep junction temperature below 125°C. Assumption is max power dissipation condition is sourcing 24mA into Ground from AV_{DD} with a 3mA on-chip current.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

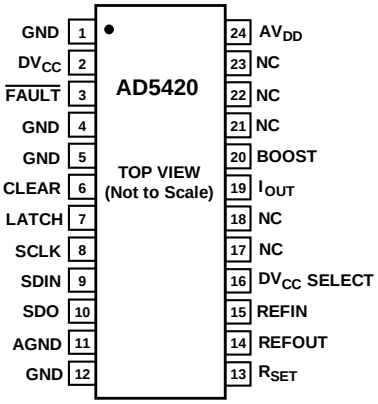


Figure 5. TSSOP Pin Configuration

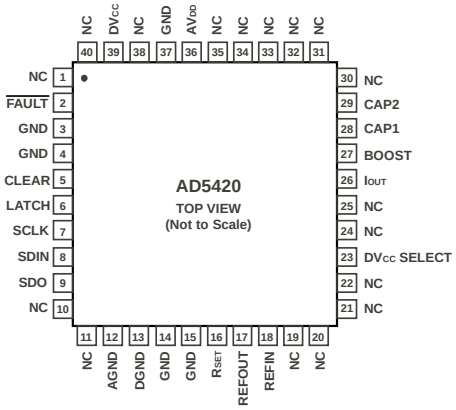


Figure 6. LFCSP Pin Configuration

Table 6. Pin Function Descriptions

TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Description
1,4,5,12	3,4,15,14,37	GND	These pins must be connected to 0V.
2	39	DV_{CC}	Digital Supply Pin. Voltage ranges from 2.7 V to 5.5 V.
3	2	$\overline{FAULT}$	Fault alert, This pin is asserted low when an open circuit is detected in current mode or an over temperature is detected. Open drain output, must be connected to a pull-up resistor.
17,18,21,22, 23	1,10,11,19, 20,21,22,24,25, 30,31,32,33,34, 35,38,40	NC	No Connection.
6	5	CLEAR	Active High Input. Asserting this pin will set the current output to the bottom of the selected range.
7	6	LATCH	Positive edge sensitive latch, a rising edge will parallel load the input shift register data into the DAC register, also updating the output.
8	7	SCLK	Serial Clock Input. Data is clocked into the shift register on the rising edge of SCLK. This operates at clock speeds up to 30 MHz.
9	8	SDIN	Serial Data Input. Data must be valid on the rising edge of SCLK.
10	9	SDO	Serial Data Output. Used to clock data from the serial register in daisy-chain or readback mode. Data is clocked out on the falling edge of SCLK. See Figure 3 and Figure 4.
11	12	AGND	Ground reference pin for analog circuitry.
N/A	13	DGND	Ground reference pin for digital circuitry. (AGND and DGND are internally connected in TSSOP package).
13	16	R_{SET}	An external, precision, low drift 15kΩ current setting resistor can be connected to this pin to improve the I_{OUT} temperature drift performance. Refer to Features section.
14	17	REFOUT	Internal Reference Voltage Output. REFOUT = 5 V ± 2 mV.
15	18	REFIN	External Reference Voltage Input. Reference input range is 4 V to 5 V. REFIN = 5 V for specified performance.
16	23	DV_{CC} SELECT	This pin when connected to GND disables the internal supply and an external supply must be connected to the DV_{CC} pin. Leave this pin unconnected to enable the internal supply. Refer to features section.
19	26	I_{OUT}	Current output pin.
20	27	BOOST	Optional external transistor connection. Connecting an external transistor will reduce the power dissipated in the AD5420. Refer to the features section.
N/A	28	CAP1	Connection for optional output filtering capacitor. Refer to Features section.
N/A	29	CAP2	Connection for optional output filtering capacitor. Refer to Features section.
24	36	AV_{DD}	Positive Analog Supply Pin. Voltage ranges from 10.8V to 40V/60V.

TSSOP Pin No.	LFCSP Pin No.	Mnemonic	Description
Paddle	Paddle	AGND	Ground reference for analog circuitry.

TYPICAL PERFORMANCE CHARACTERISTICS

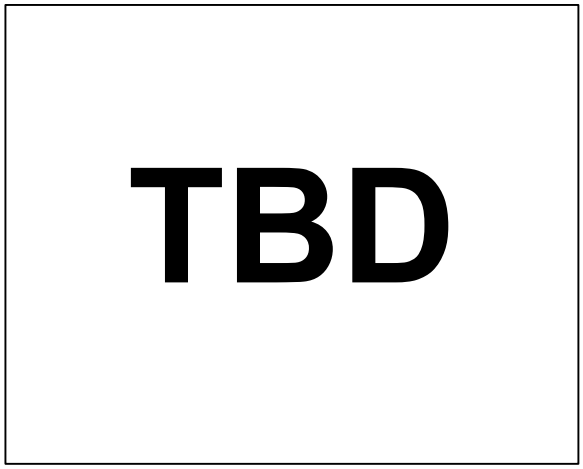


Figure 7. Integral Non Linearity vs. Code

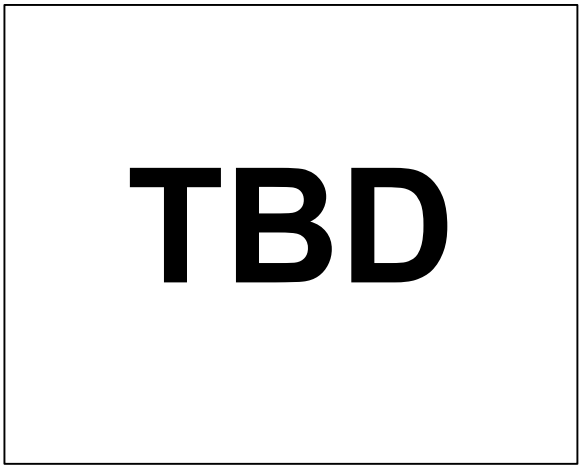


Figure 10. Integral Non Linearity vs. Temperature

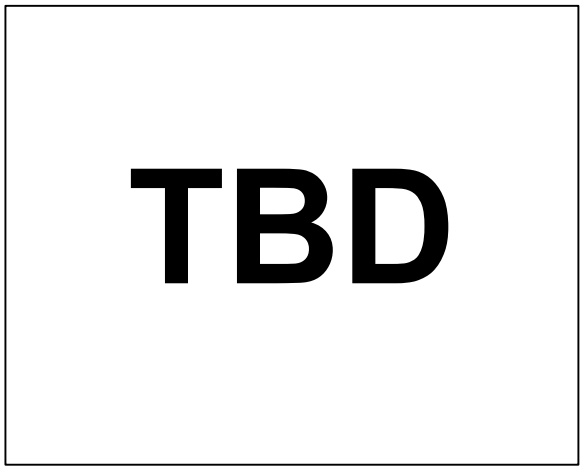


Figure 8.Differential Non Linearity vs. Code

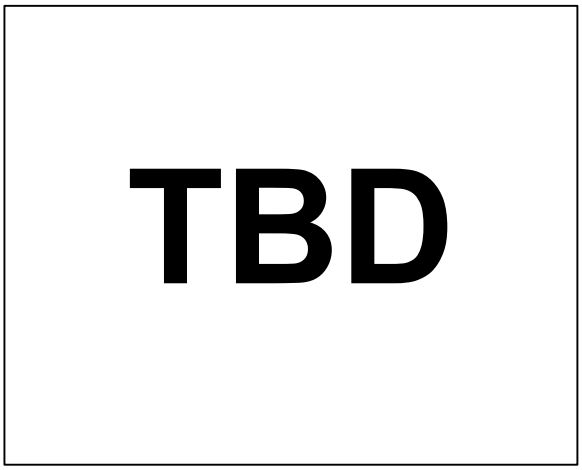


Figure 11. Differential Non Linearity vs. Temperature

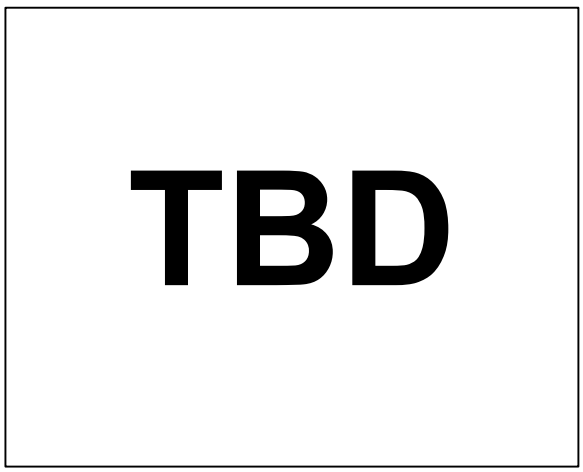


Figure 9. Total Unadjusted Error vs. Code

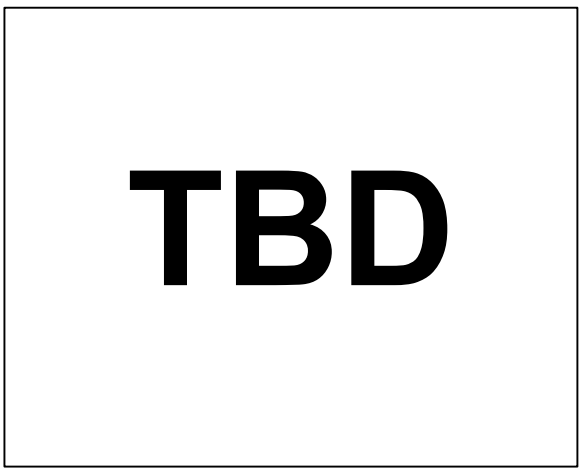


Figure 12. Integral Non Linearity vs. Supply

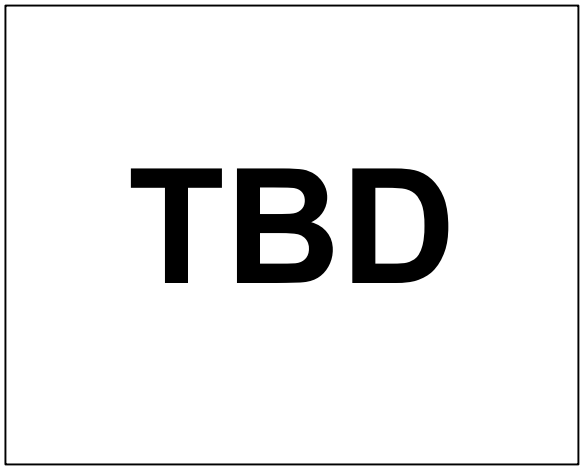


Figure 13. Differential Non Linearity vs. Supply Voltage

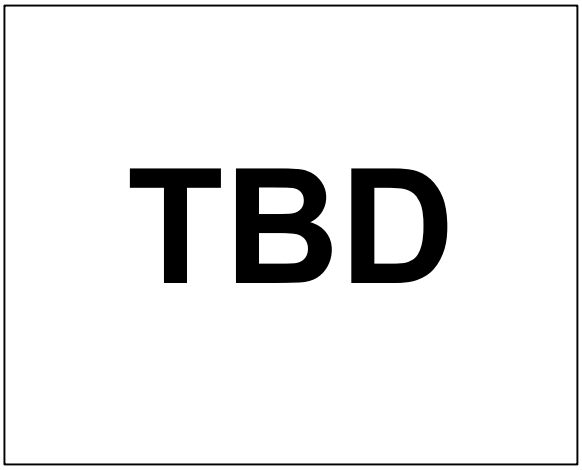


Figure 16. Total Unadjusted Error vs. Reference Voltage

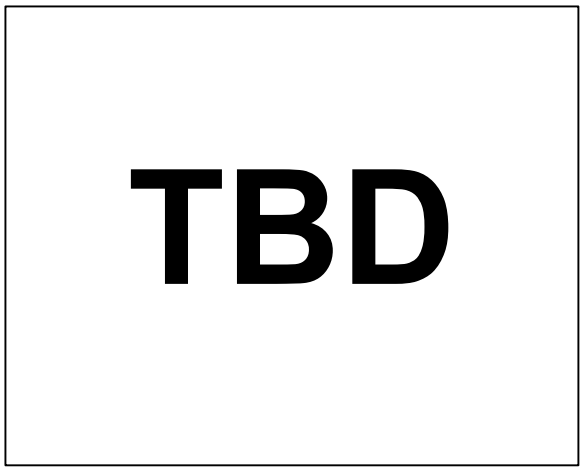


Figure 14. Integral Non Linearity vs. Reference Voltage

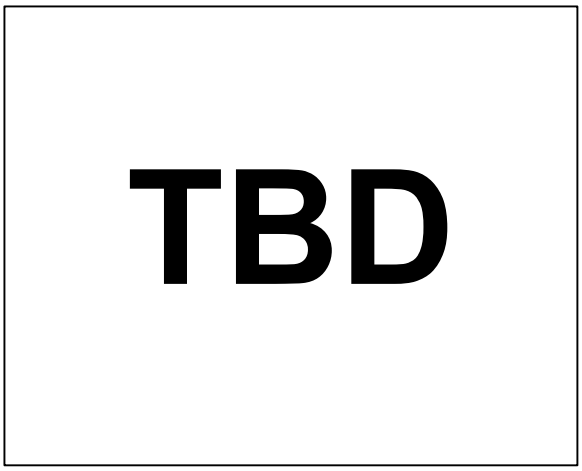


Figure 17. Total Unadjusted Error vs. Supply Voltage

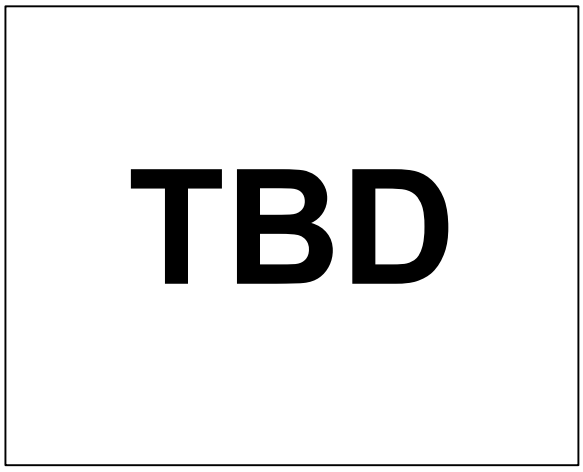


Figure 15. Differential Non Linearity vs. Reference Voltage

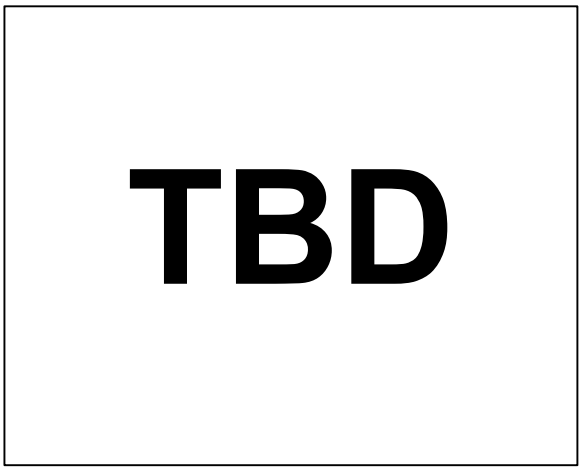


Figure 18. Offset Error vs. Temperature

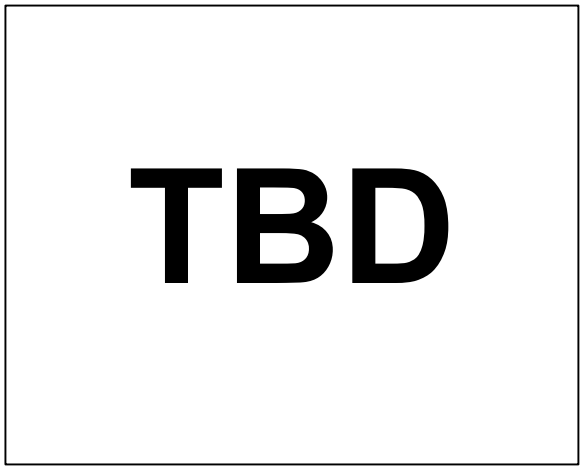


Figure 19. Gain Error vs. Temperature

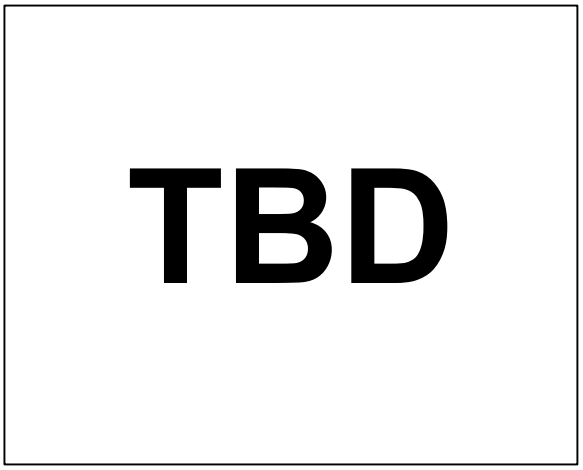


Figure 21. I_{OUT} vs. Time on Power-up

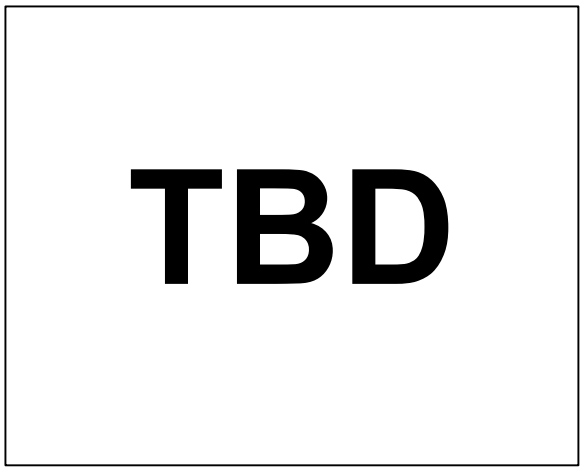


Figure 20. Voltage Compliance vs. Temperature

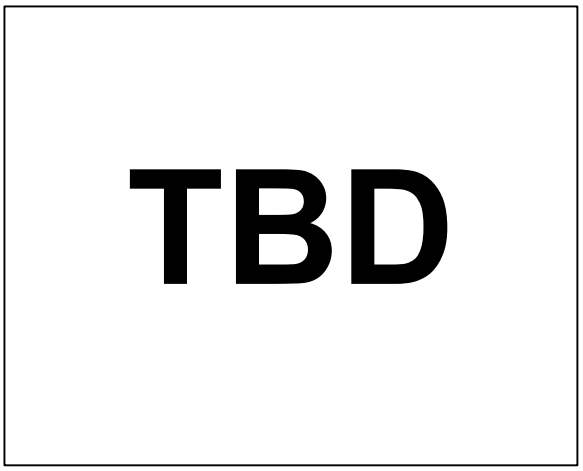


Figure 22. I_{OUT} vs. Time on Output Enabled

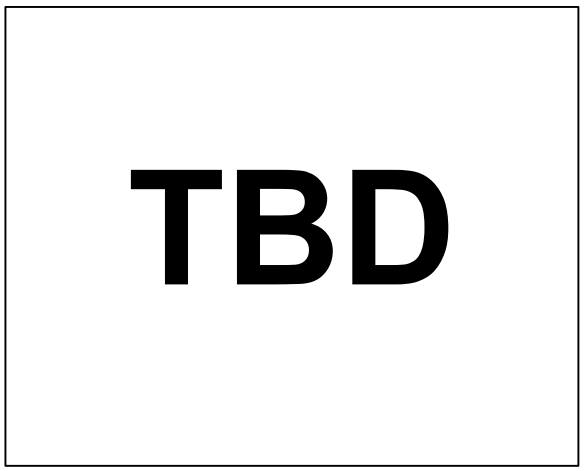


Figure 23. DI_{CC} vs.Logic Input Voltage

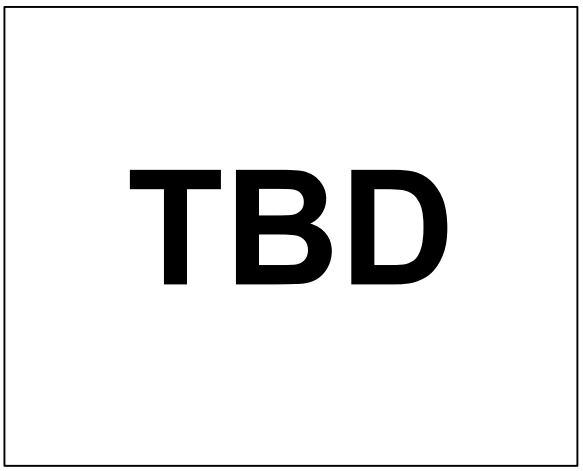


Figure 24. AI_{DD} vs AV_{DD}

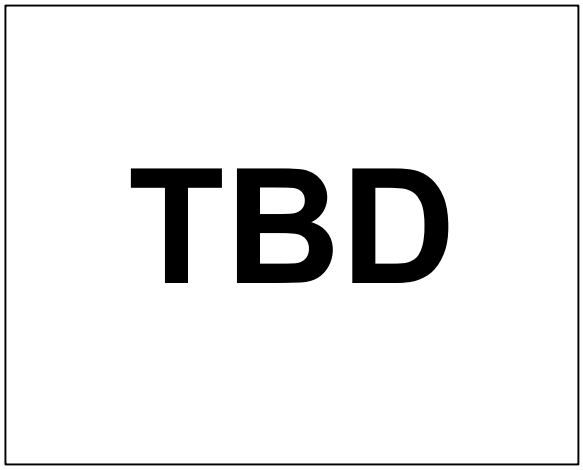


Figure 25. DV_{CC} Output Voltage vs. DI_{CC} Load Current

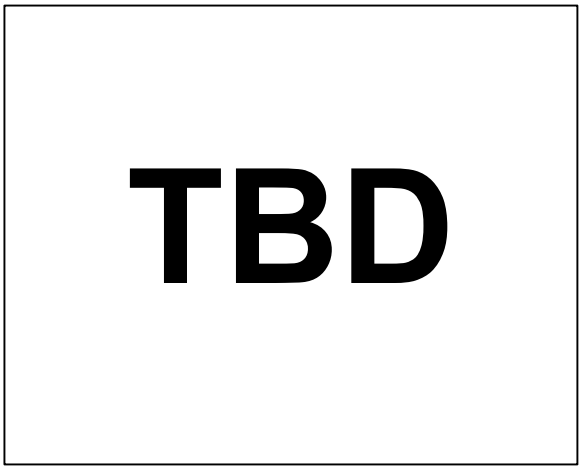


Figure 28. Refout Output Noise (100kHz Bandwidth)

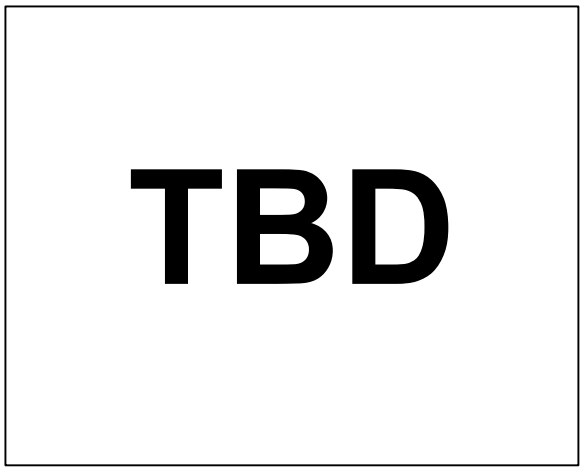


Figure 26. Refout Turn-on Transient

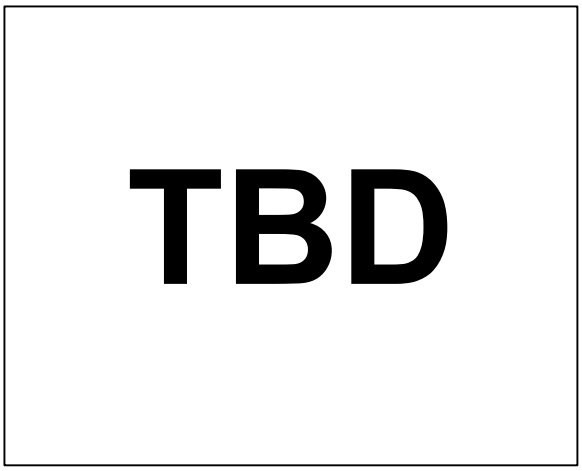


Figure 29. Refout Line Transient

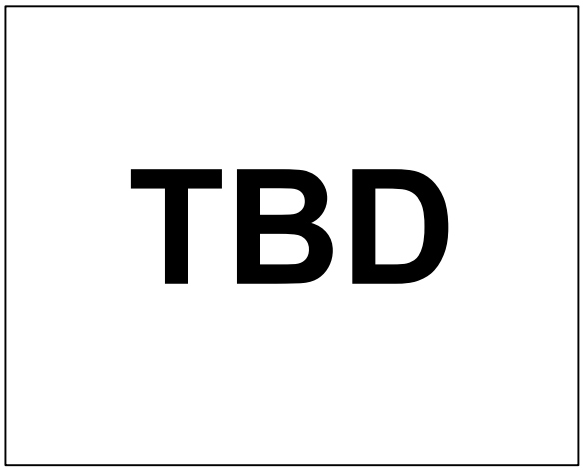


Figure 27. Refout Output Noise (0.1Hz to 10Hz Bandwidth)

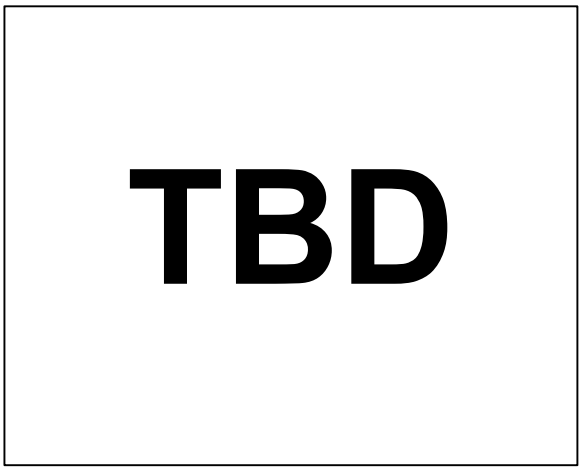


Figure 30. Refout Load Transient

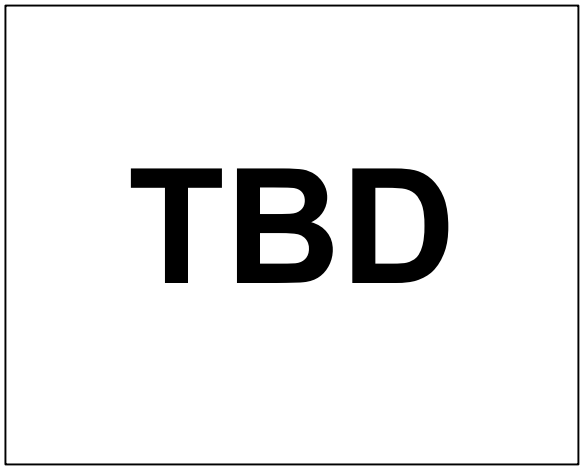


Figure 31. Refout Histogram of Thermal Hysteresis

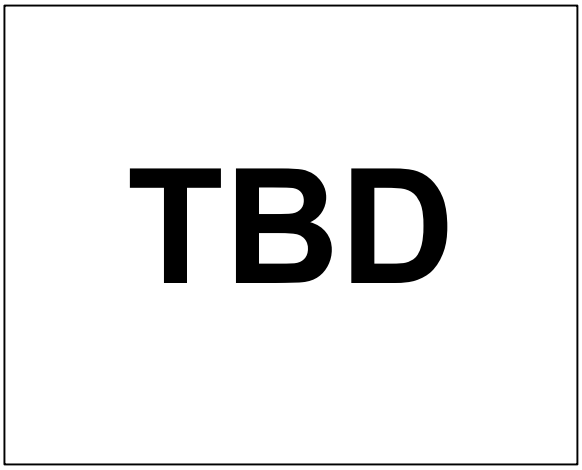


Figure 32. Refout Voltage vs. Load Current

TERMINOLOGY

Relative Accuracy or Integral Nonlinearity (INL)
For the DAC, relative accuracy, or integral nonlinearity (INL), is a measure of the maximum deviation, in LSBs, from a straight line passing through the endpoints of the DAC transfer function. A typical INL vs. code plot can be seen in Figure 7

Differential Nonlinearity (DNL)
Differential nonlinearity (DNL) is the difference between the measured change and the ideal 1 LSB change between any two adjacent codes. A specified differential nonlinearity of ±1 LSB maximum ensures monotonicity. This DAC is guaranteed monotonic by design. A typical DNL vs. code plot can be seen in Figure 8.

Monotonicity
A DAC is monotonic if the output either increases or remains constant for increasing digital input code. The AD5724R/ AD5734R/AD5754R are monotonic over their full operating temperature range.

Full-Scale Error
Full-Scale error is a measure of the output error when full-scale code is loaded to the DAC register. Ideally, the output should be full-scale − 1 LSB. Full-scale error is expressed in percent of full-scale range (% FSR).

Zero-Scale TC
This is a measure of the change in zero-scale error with a change in temperature. Zero-scale error TC is expressed in ppm FSR/°C.

Gain Error
This is a measure of the span error of the DAC. It is the deviation in slope of the DAC transfer characteristic from ideal expressed in % FSR. A plot of gain error vs. temperature can be seen in Table TBD

Gain TC
This is a measure of the change in gain error with changes in temperature. Gain Error TC is expressed in ppm FSR/°C.

Total Unadjusted Error
Total unadjusted error (TUE) is a measure of the output error taking all the various errors into account, namely INL error, offset error, gain error, and output drift over supplies, temperature, and time. TUE is expressed in % FSR.

Current Loop Voltage Compliance
The maximum voltage at the I_{OUT} pin for which the output currnet will be equal to the programmed value.

Power Supply Rejection Ratio (PSRR)
PSRR indicates how the output of the DAC is affected by changes in the power supply voltage.

Reference TC

Reference TC is a measure of the change in the reference output voltage with a change in temperature. It is expressed in ppm/°C.

Line Regulation

Line regulation is the change in reference output voltage due to a specified change in supply voltage. It is expressed in ppm/V.

Load Regulation

Load regulation is the change in reference output voltage due to a specified change in load current. It is expressed in ppm/mA.

Thermal Hysteresis

Thermal hysteresis is the change of reference output voltage after the device is cycled through temperatures from +25°C to −40°C to +85°C and back to +25°C. This is a typical value from a sample of parts put through such a cycle. See Table TBDfor a histogram of thermal hysteresis.

$$V_{O_HYS} = V_O(25°C) - V_{O_TC}$$

$$V_{O_HYS}(ppm) = \frac{V_O(25°C) - V_{O_TC}}{V_O(25°C)} \times 10^6$$

where:

$V_O(25°C)$ = V_O at 25°C
V_{O_TC} = V_O at 25°C after temperature cycle

THEORY OF OPERATION

The AD5420 is a precision digital to current loop output converter designed to meet the requirements of industrial process control applications. It provides a high precision, fully integrated, low cost single-chip solution for generating current loop outputs. The current ranges available are; 0 to 20mA, 0 to 24mA and 4 to 20mA, The desired output configuration is user selectable via the CONTROL register.

ARCHITECTURE

The DAC core architecture of the AD5420 consists of two matched DAC sections. A simplified circuit diagram is shown in Figure 33. The 4 MSBs of the 16-bit data word are decoded to drive 15 switches, E1 to E15. Each of these switches connects 1 of 15 matched resistors to either ground or the reference buffer output. The remaining 12 bits of the data-word drive switches S0 to S11 of a 12-bit voltage mode R-2R ladder network.

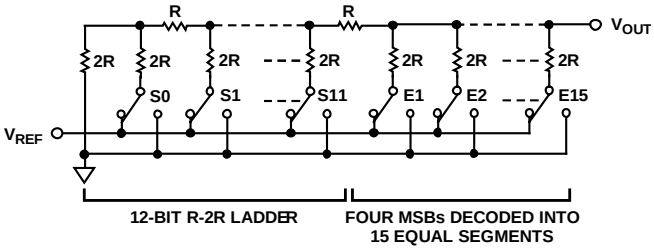


Figure 33. DAC Ladder Structure

The voltage output from the DAC core is converted to a current (see diagram, Figure 34) which is then mirrored to the supply rail so that the application simply sees a current source output with respect to ground.

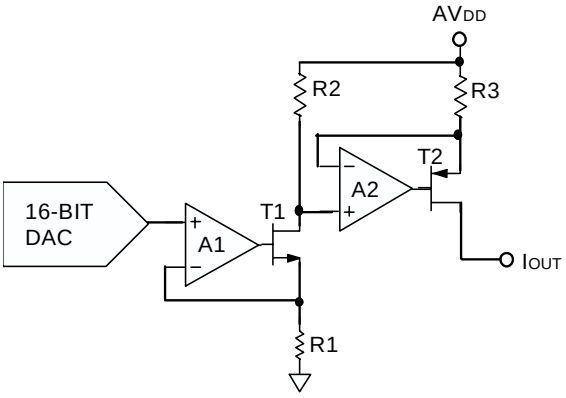


Figure 34. Voltage to Current conversion circuitry

Reference Buffers

The AD5420 can operate with either an external or internal reference. The reference input has an input range of 4 V to 5 V, 5 V for specified performance. This input voltage is then buffered before it is applied to the DAC.

SERIAL INTERFACE

The AD5420 is controlled over a versatile 3-wire serial interface that operates at clock rates up to 30 MHz. It is compatible with SPI®, QSPI™, MICROWIRE™, and DSP standards.

Input Shift Register

The input shift register is 24 bits wide. Data is loaded into the device MSB first as a 24-bit word under the control of a serial clock input, SCLK. Data is clocked in on the rising edge of SCLK. The input register consists of 8 control bits and 16 data bits as shown in Table 7. The 24 bit word is unconditionally latched on the rising edge of LATCH. Data will continue to be clocked in irrespective of the state of LATCH, on the rising edge of LATCH the data that is present in the input register will be latched, in other words the last 24 bits to be clocked in before the rising edge of LATCH will be the data that is latched. The timing diagram for this operation is shown in Figure 2.

Table 7. Input Shift Register Format

MSB																							LSB
D23	D22	D21	D20	D19	D18	D17	D16	D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
ADDRESS WORD								DATA WORD															

Table 8. Control Word Functions

Address Word	Function
00000000	No Operation (NOP)
00000001	DATA Register
00000010	Readback register value as per Read Address (See Table 10)
01010101	CONTROL Register
01010110	RESET Register

Standalone Operation

The serial interface works with both a continuous and noncontinuous serial clock. A continuous SCLK source can only be used if LATCH is taken high after the correct number of data bits have been clocked in. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and LATCH must be taken high after the final clock to latch the data. The first rising edge of SCLK that clocks in the MSB of the dataword marks the beginning ot the write cycle. Exactly 24 rising clock edges must be applied to SCLK before LATCH is brought high. If LATCH is brought high before the 24th rising SCLK edge, the data written will be invalid. If more than 24 rising SCLK edges are applied before LATCH is brought high, the input data will also be invalid.

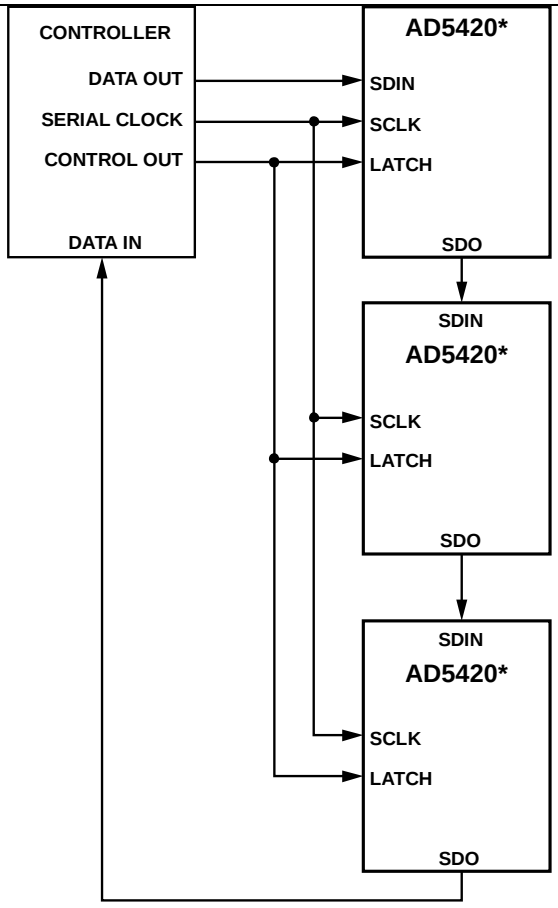


Figure 35. Daisy Chaining the AD5420

Daisy-Chain Operation

For systems that contain several devices, the SDO pin can be used to daisy chain several devices together as shown in Figure 35. This daisy-chain mode can be useful in system diagnostics and in reducing the number of serial interface lines. Daisychain mode is enabled by setting the DCEN bit of the CONTROL 1 register. The first rising edge of SCLK that clocks in the MSB of the dataword marks the beginning of the write cycle. SCLK is continuously applied to the input shift register. If more than 24 clock pulses are applied, the data ripples out of the shift register and appears on the SDO line. This data is clocked out on the falling edge of SCLK and is valid on the next rising edge. By connecting the SDO of the first device to the SDIN input of the next device in the chain, a multidevice interface is constructed. Each device in the system requires 24 clock pulses. Therefore, the total number of clock cycles must equal 24 × *N*, where *N* is the total number of AD5420 devices in the chain. When the serial transfer to all devices is complete, LATCH is taken high. This latches the input data in each device in the daisy chain. The serial clock can be a continuous or a gated clock.

A continuous SCLK source can only be used if LATCH is taken high after the correct number of clock cycles. In gated clock mode, a burst clock containing the exact number of clock cycles must be used, and LATCH must be taken high after the final clock to latch the data. See Figure 4 for a timing diagram.

Readback Operation

Readback mode is invoked by setting the control word and read address as shown in Table 9 and Table 10 when writing to the input register. The next write to the AD5420 should be a NOP command which will clock out the data from the previously addressed register as shown in Figure 3.
By default the SDO pin is disabled, after having addressed the AD5420 for a read operation, a rising edge on LATCH will enable the SDO pin in anticipation of data being clocked out, after the data has been clocked out on SDO, a rising edge on LATCH will disable (tri-state) the SDO pin once again.
To read back the data register for example, the following sequence should be implemented:

1. Write 0x020001 to the AD5420 input register. This configures the part for read mode with the data register selected.
2. Follow this with a second write, a NOP condition, 0x000000 During this write, the data from the register is clocked out on the SDO line.

Table 9. Input Shift Register Contents for a read operation

MSB																							LSB
D23	**D22**	**D21**	**D20**	**D19**	**D18**	**D17**	**D16**	**D15**	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	0	0	0	0	1	0	X	X	X	X	X	X	X	X	X	X	X	X	X	X	Read Address	

Table 10. Read Address Decoding

Read Address	Function
00	Read Status Register
01	Read Data Register
10	Read Control Register

DEFAULT CONFIGURATION

On initial power-up of the AD5420, the power-on-reset circuit ensures that all registers are loaded with zero-code, as such the default output range is 4mA to 20mA. The current output until a value is programmed is 0mA. An alternative current range may be selected via the CONTROL register.

TRANSFER FUNCTION

For the 0 to 20mA, 0 to 24mA and 4 to 20mA current output ranges the output current expressions are respectively given by;

$$I_{OUT} = \left[\frac{20mA}{2^N}\right] \times D$$

$$I_{OUT} = \left[\frac{24mA}{2^N}\right] \times D$$

$$I_{OUT} = \left[\frac{16mA}{2^N}\right] \times D + 4mA$$

where:

D is the decimal equivalent of the code loaded to the DAC.
N is the bit resolution of the DAC.

DATA REGISTER

The DATA register is addressed by setting the control word of the input shift register to 0x01. The data to be written to the DATA register is entered in positions D15 to D0 as shown in Table 11,

Table 11. Programming the Data Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
DATA WORD															

CONTROL REGISTER

The CONTROL register is addressed by setting the control word of the input shift register to 0x55. The data to be written to the CONTROL register is entered in positions D15 to D0 as shown in Table 12. The CONTROL register functions are shown in Table 13.

Table 12. Programming the CONTROL Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
0	0	REXT	OUTEN	SR CLOCK				SR STEP			SREN	DCEN	R2	R1	R0

Table 13. Control Register Functions

Option	Description
REXT	Setting this bit selects the external current setting resistor, Further details in Features section
OUTEN	Output enable. This bit must be set to enable the output.
SR CLOCK	See Features Section. Digital Slew Rate Control
SR STEP	See Features Section. Digital Slew Rate Control
SREN	Digital Slew Rate Control enable
DCEN	Daisychain enable
R2,R1,R0	Output range select. See Table 14

Table 14. Output Range Options

R2	R1	R0	Output Range Selected
1	0	1	4 to 20 mA Current Range
1	1	0	0 to 20 mA Current Range
1	1	1	0 to 24 mA Current Range

RESET REGISTER

The RESET register is addressed by setting the control word of the input shift register to 0x56. The data to be written to the RESET register is entered in positions D15 to D0 as shown in Table 15. The RESET register options are shown in Table 15 and Table 16.

Table 15. Programming the CONTROL 2 Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
															RESET

Table 16. Control 2 register Functions

Option	Description
RESET	Setting this bit performs a reset operation, restoring the AD5420 to its initial power on state

STATUS REGISTER

The STATUS register is a read only register. The STATUS register functionality is shown in Table 17 and Table 18.

Table 17. Decoding the STATUS Register

MSB															LSB
D15	**D14**	**D13**	**D12**	**D11**	**D10**	**D9**	**D8**	**D7**	**D6**	**D5**	**D4**	**D3**	**D2**	**D1**	**D0**
													I_{OUT} FAULT	SLEW ACTIVE	OVER TEMP

Table 18. STATUS Register Functions

Option	Description
I_{OUT} FAULT	This bit will be set if a fault is detected on the I_{OUT} pin.
SLEW ACTIVE	This bit will be set while the output value is slewing (slew rate control enabled)
OVER TEMP	This bit will be set if the AD5420 core temperature exceeds approx. 150°C.

FEATURES

FAULT ALERT

The AD5420 is equipped with a FAULT pin, this is an open-drain output allowing several AD5420 devices to be connected together to one pull-up resistor for global fault detection. The FAULT pin is forced active by any one of the following fault scenarios;

1) The Voltage at I_{OUT} attempts to rise above the compliance range, due to an open-loop circuit or insufficient power supply voltage. The I_{OUT} current is controlled by a PMOS transistor and internal amplifier as shown in Figure 34. The internal circuitry that develops the fault output avoids using a comparator with "window limits" since this would require an actual output error before the FAULT output becomes active. Instead, the signal is generated when the internal amplifier in the output stage has less than approxiamately one volt of remaining drive capability (when the gate of the output PMOS transistor nearly reaches ground). Thus the FAULT output activates slightly before the compliance limit is reached. Since the comparison is made within the feedback loop of the output amplifier, the output accuracy is maintained by its open-loop gain and an output error does not occur before the FAULT output becomes active.
2) If the core temperature of the AD5420 exceeds approx. 150°C.

The OPEN CCT and OVER TEMP bits of the STATUS register are used in conjunction with the FAULT pin to inform the user which one of the fault conditions caused the FAULT pin to be asserted. See Table 17 and Table 18.

ASYNCHRONOUS CLEAR (CLEAR)

CLEAR is an active high clear that clears the Current output to the bottom of its programmed range. It is necessary to maintain CLEAR high for a minimum amount of time (see Figure 2) to complete the operation. When the CLEAR signal is returned low, the output remains at the cleared value until a new value is programmed.

INTERNAL REFERENCE

The AD5420 contains an integrated +5V voltage reference with initial accuracy of ±2mV max and a temperature drift coefficient of ±10 ppm max. The reference voltage is buffered and externally available for use elsewhere within the system. See Figure 32 for a load regulation graph of the Integrated reference.

EXTERNAL CURRENT SETTING RESISTOR

Referring to Figure 34, R1 is an internal sense resistor as part of the voltage to current conversion circuitry. The stability of the output current over temperature is dependent on the stability of the value of R1. As a method of improving the stability of the output current over temperature an external precision 15kΩ low drift resistor can be connected to the R_{SET} pin of the AD5420 to be used instead of the internal resistor R1. The external resistor is selected via the CONTROL 1 register. See Table 12.

DIGITAL POWER SUPPLY

By default the DV_{CC} pin accepts a power supply of 2.7V to 5.5V, alternatively, via the DV_{CC} SELECT pin an internal 4.5V power supply may be output on the DV_{CC} pin for use as a digital power supply for other devices in the system or as a termination for pull-up resistors. This facility offers the advantage of not having to bring a digital supply across an isolation barrier. The internal power supply is enabled by leaving the DV_{CC} SELECT pin unconnected. To disable the internal supply DV_{CC} SELECT should be tied to 0V.

EXTERNAL BOOST FUNCTION

The addition of an external boost transistor as shown in Figure 36 will reduce the power dissipated in the AD5420 by reducing the current flowing in the on-chip output transistor (dividing it by the current gain of the external circuit). A discrete NPN transistor with a breakdown voltage, BV_{CEO}, greater than 60V can be used.

The external boost capability has been developed for those users who may wish to use the AD5420 at the extremes of the supply voltage, load current and temperature range. The boost transistor can also be used to reduce the amount of temperature induced drift in the part. This will minimise the temperature induced drift of the on-chip voltage reference, which improves drift and linearity.

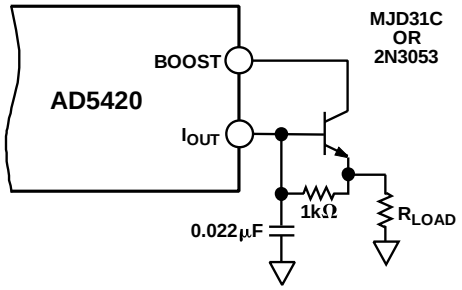


Figure 36. External Boost Configuration

DIGITAL SLEW RATE CONTROL

The Slew Rate Control feature of the AD5420 allows the user to control the rate at which the output current changes. With the slew rate control feature disabled the output currrent will change at a rate limited by the output drive circuitry and the attached load. If the user wishes to reduce the slew rate this can be achieved by enabling the slew rate control feature.With the feature enabled via the SREN bit of the CONTROL register, (See Table 12) the output, instead of slewing directly between two values, will step digitally at a rate defined by two parameters accessible via the CONTROL register as shown in Table 12. The parameters are SR CLOCK and SR STEP. SR CLOCK defines the rate at which the digital slew will be updated, e.g. if the selected update rate is 1MHz the output will update every 1µs, SR STEP defines by how much the output value will change at each update. Together both parameters define the rate of change of the output current.Table 19 and Table 20 outline the range of values for both the SR CLOCK and SR STEP parameters.

Table 19. Slew Rate Update Clock Options

SR CLOCK	Update Clock Frequency (Hz)
0000	1000000
0001	500000
0010	333333
0011	250000
0100	200000
0101	100000
0110	50000
0111	33333
1000	25000
1001	20000
1010	12500
1011	10000
1100	8333
1101	6666
1110	5000
1111	3921

Table 20. Slew Rate Step Size Options

SR STEP	Step Size (LSBs)
000	1
001	2
010	4
011	8
100	16
101	32
110	64
111	128

The following equation describes the slew rate as a function of the step size, the update clock frequency and the LSB size.

$$SlewRate = \frac{StepSize \times UpdateClockFrequency \times LSBSize}{1 \times 10^6}$$

Where:

Slew Rate is expressed in A/µs
LSBSize = Fullscale Range / 65536

When the slew rate control feature is enabled, all output changes will change at the programmed slew rate, i.e. if the CLEAR pin is asserted the output will slew to the clear value at the programmed slew rate. The output can be halted at its current value with a write to the CONTROL register. To avoid halting the output slew, the SLEW ACTIVE bit can be used to check that the slew has completed before writing to the AD5420 registers. See Table 17.

I_{OUT} FILTERING CAPACITORS

Two capacitors may be placed between the pins CAP1, CAP2 and AV_{DD} as shown in Figure 37. The capacitors form a filter on the current output circuitry reducing the bandwidth and the rate of change of the output current.

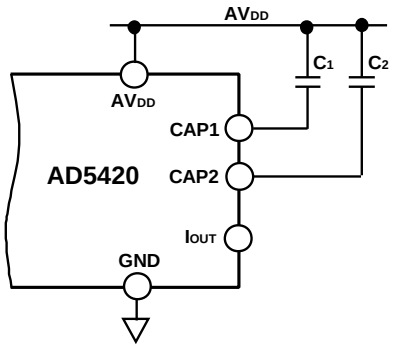


Figure 37. I_{OUT} Filtering Capacitors

APPLICATIONS INFORMATION

DRIVING INDUCTIVE LOADS

When driving inductive or poorly defined loads connect a 0.01µF capacitor between I_{OUT} and GND. This will ensure stability with loads beyond 50mH. There is no maximum capacitance limit. The capacitive component of the load may cause slower settling, though this may be masked by the settling time of the AD5420.

TRANSIENT VOLTAGE PROTECTION

The AD5420 contains ESD protection diodes which prevent damage from normal handling. The industrial control environment can, however, subject I/O circuits to much higher transients. In order to protect the AD5420 from excessively high voltage transients , external power diodes and a surge current limiting resistor may be required, as shown in Figure 38. The constraint on the resistor value is that during normal operation the output level at IOUT must remain within its voltage compliance limit of $AV_{DD} - 2.5V$ and the two protection diodes and resistor must have appropriate power ratings.

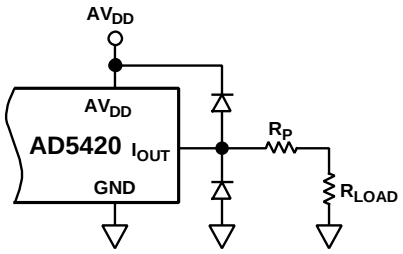


Figure 38. Output Transient Voltage Protection

LAYOUT GUIDELINES

In any circuit where accuracy is important, careful consideration of the power supply and ground return layout helps to ensure the rated performance. The printed circuit board on which the AD5420 is mounted should be designed so that the analog and digital sections are separated and confined to certain areas of the board. If the AD5420 is in a system where multiple devices require an AGND-to-DGND connection, the connection should be made at one point only. The star ground point should be established as close as possible to the device.

The AD5420 should have ample supply bypassing of 10 µF in parallel with 0.1 µF on each supply located as close to the package as possible, ideally right up against the device. The 10 µF capacitors are the tantalum bead type. The 0.1 µF capacitor should have low effective series resistance (ESR) and low effective series inductance (ESI) such as the common ceramic types, which provide a low impedance path to ground at high frequencies to handle transient currents due to internal logic switching.

The power supply lines of the AD5420 should use as large a trace as possible to provide low impedance paths and reduce the effects of glitches on the power supply line. Fast switching signals such as clocks should be shielded with digital ground to avoid radiating noise to other parts of the board and should never be run near the reference inputs. A ground line routed between the SDIN and SCLK lines helps reduce crosstalk between them (not required on a multilayer board that has a separate ground plane, but separating the lines helps). It is essential to minimize noise on the REFIN line because it couples through to the DAC output.

Avoid crossover of digital and analog signals. Traces on opposite sides of the board should run at right angles to each other. This reduces the effects of feed through the board. A microstrip technique is by far the best, but not always possible with a double-sided board. In this technique, the component side of the board is dedicated to ground plane, while signal traces are placed on the solder side.

GALVANICALLY ISOLATED INTERFACE

In many process control applications, it is necessary to provide an isolation barrier between the controller and the unit being controlled to protect and isolate the controlling circuitry from any hazardous common-mode voltages that might occur. The *i*Coupler® family of products from Analog Devices provides voltage isolation in excess of 2.5 kV. The serial loading structure of the AD5420 make it ideal for isolated interfaces because the number of interface lines is kept to a minimum. Figure 39 shows a 4-channel isolated interface to the AD5420 using an ADuM1400. For further information, visit http://www.analog.com/icouplers.

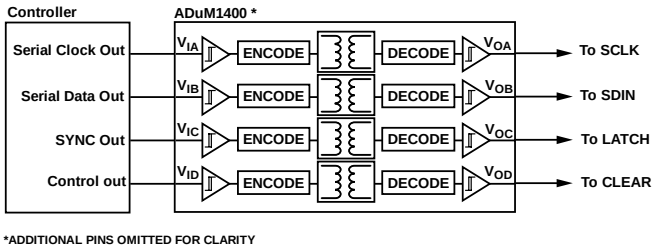


Figure 39. Isolated Interface

MICROPROCESSOR INTERFACING

Microprocessor interfacing to the AD5420 is via a serial bus that uses protocol compatible with microcontrollers and DSP processors. The communications channel is a 3-wire (minimum) interface consisting of a clock signal, a data signal, and a latch signal. The AD5420 require a 24-bit data-word with data valid on the rising edge of SCLK.

For all interfaces, the DAC output update is initiated on the rising edge of LATCH. The contents of the registers can be read using the readback function.

THERMAL AND SUPPLY CONSIDERATIONS

The AD5420 is designed to operate at a maximum junction temperature of 125°C. It is important that the device is not operated under conditions that will cause the junction temperature to exceed this value . Excessive junction temperature can occur if the AD5420 is operated from the maximum AV_{DD} and driving the maximum current (24mA) directly to ground. In this case the ambient temperature should be controlled or AV_{DD} should be reduced. The conditions will depend on the device and package.

At maximum ambient temperature of 85°C the AD5420BREZ (24-lead TSSOP) can dissipate 950mW and the AD5420BCPZ (40-lead LFCSP) can dissipate 1.42W.

To ensure the junction temperature does not exceed 125°C while driving the maximum current of 24mA directly into ground (also adding an on-chip current of 3mA), AV_{DD} should be reduced from the maximum rating to ensure the package is not required to dissipate more power than stated above. See Table 21, Figure 40 and Figure 41.

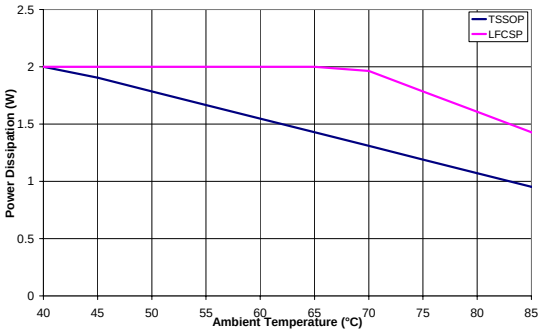


Figure 40. Maximum Power Dissipation Vs Ambient Temperature

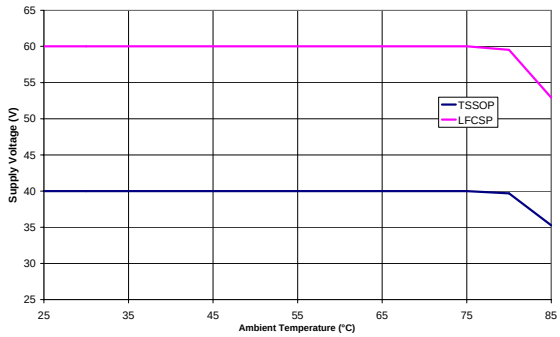
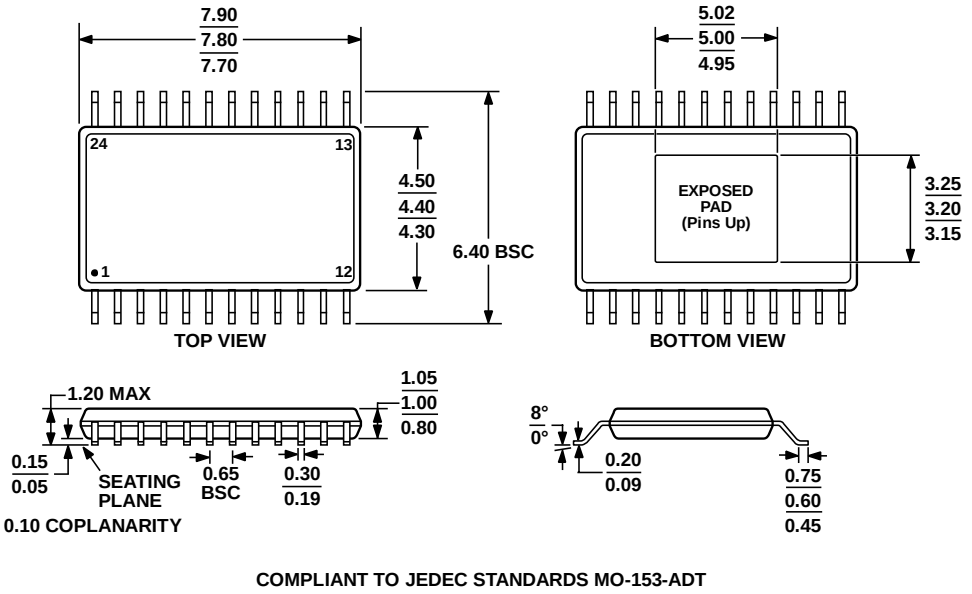


Figure 41. Maximum Supply Voltage Vs Ambient Temperature

Table 21. Thermal and Supply considerations for each package

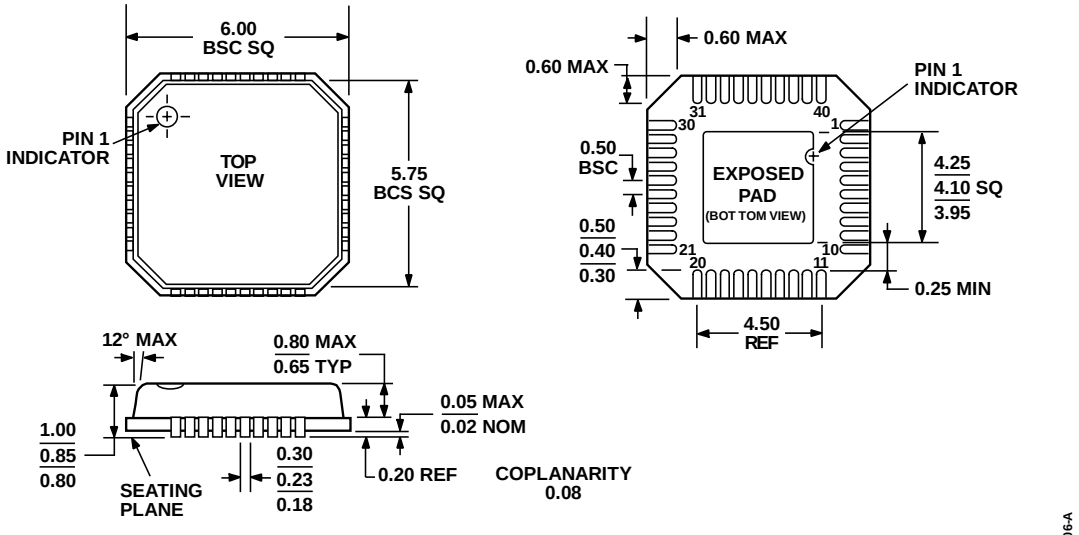
	TSSOP	LFCSP
Maximum allowed power dissipation when operating at an ambient temperature of 85°C	$\frac{T_J\ \max - T_A}{\Theta_{JA}} = \frac{125-85}{42} = 950mW$	$\frac{T_J\ \max - T_A}{\Theta_{JA}} = \frac{125-85}{28} = 1.42W$
Maximum allowed ambient temperature when operating from a supply of 40V/60V and driving 24mA directly to ground.	$T_J\ \max - P_D \times \Theta_{JA} = 125 - (40 \times 0.027) \times 42 = 79°C$	$T_J\ \max - P_D \times \Theta_{JA} = 125 - (60 \times 0.027) \times 28 = 79°C$
Maximum allowed supply voltage when operating at an ambient temperature of 85°C and driving 24mA directly to ground.	$\frac{T_J\ \max - T_A}{AI_{DD} \times \Theta_{JA}} = \frac{125-85}{0.027 \times 42} = 35V$	$\frac{T_J\ \max - T_A}{AI_{DD} \times \Theta_{JA}} = \frac{125-85}{0.027 \times 28} = 53V$

OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MO-153-ADT

Figure 42. 24-Lead Thin Shrink Small Outline Package, Exposed Pad [TSSOP_EP]
(RE-24)
Dimensions shown in millimeters



COMPLIANT TO JEDEC STANDARDS MO-220-VJJD-2

Figure 43. 40-Lead Lead Frame Chip Scale Package
(CP-40)
Dimensions shown in millimeters

ORDERING GUIDE

Model	AV_{DD} max	Temperature Range	Package Description	Package Option
AD5420BREZ	40V	-40°C to 85°C	24 Lead TSSOP_EP	RE-24
AD5420BCPZ	60V	-40°C to 85°C	40 Lead LFCSP	CP-40

NOTES

NOTES

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