25-35GHz Single Side Band Mixer Self biased

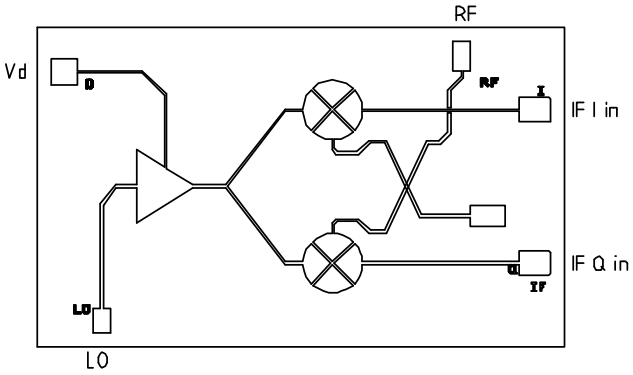
Preliminary

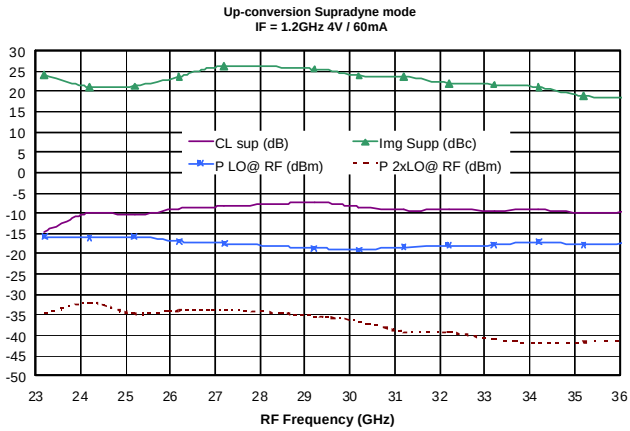
GaAs Monolithic Microwave IC

Description

The CHR2294 is a multifunction chip (MFC) which integrates a self biased LO buffer amplifier and a sub-harmonically balanced diodes mixer for 2LO suppression and image rejection. It is usable for both up-conversion and down-conversion. It is designed for a wide range of applications, typically commercial communication systems for broadband local access. The backside of the chip is both RF and DC grounded. This helps to simplify the assembly process.

The circuit is manufactured with a PM-HEMT process, 0.25µm gate length, via holes through the substrate, air bridges and electron beam gate lithography.
It is available in chip form.





Main Features

- Broadband performances : 25-35GHz
- 11dB conversion Loss
- 15dBc image rejection
- +9dBm LO input power
- +2.5dBm input power (1dB gain comp.)
- Low DC power consumption, 55mA@4V
- Chip size : 2.06 x 1.25 x 0.10 mm

Main Characteristics

Tamb. = 25°C

	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	25		35	GHz
F_{LO}	LO frequency range	11		19	GHz
F_{IF}	IF frequency range	DC		3	GHz
L_c	Conversion Loss		11		dB

ESD Protection : Electrostatic discharge sensitive device. Observe handling precautions !

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Electrical Characteristics for Broadband Operation

Preliminary

Tamb = +25°C

Symbol	Parameter	Min	Typ	Max	Unit
F_{RF}	RF frequency range	25		35	GHz
F_{LO}	LO frequency range	11		19	GHz
F_{IF}	IF frequency range	DC		3	GHz
L_c	Conversion Loss		11		dB
P_{LO}	LO Input power		+9		dBm
2xLO Leak	2xLO Leakage (for P_{LO}=+5dBm)		-35		dBm
Img Rej	Image Rejection (1)		15		dBc
P1dB	Input power at 1dB gain compression		+2.5		dBm
LO Match	LO VSWR		2.0:1		
RF Match	RF VSWR		2.0:1		
IF Match	IF VSWR		2.0:1		
Vd	Drain bias voltage		4		V
Id	Bias current		55		mA

(1) With external quadrature hybrid coupler (reference on request). The minimal value depends on the quality of the external quadrature combiner.

A bonding wire of typically 0.1 to 0.15 nH will improve the accesses matching.

Absolute Maximum Ratings

Tamb. = 25°C (1)

Symbol	Parameter	Values	Unit
Vd	Drain bias voltage	4.25	V
Id	Drain bias current	75	mA
Tj	Junction temperature	175	°C
Ta	Operating temperature range (chip backside)	-40 to +85	°C
Tstg	Storage temperature range	-55 to +125	°C

(1) Operation of this device above anyone of these parameters may cause permanent damage.

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united monolithic semiconductors

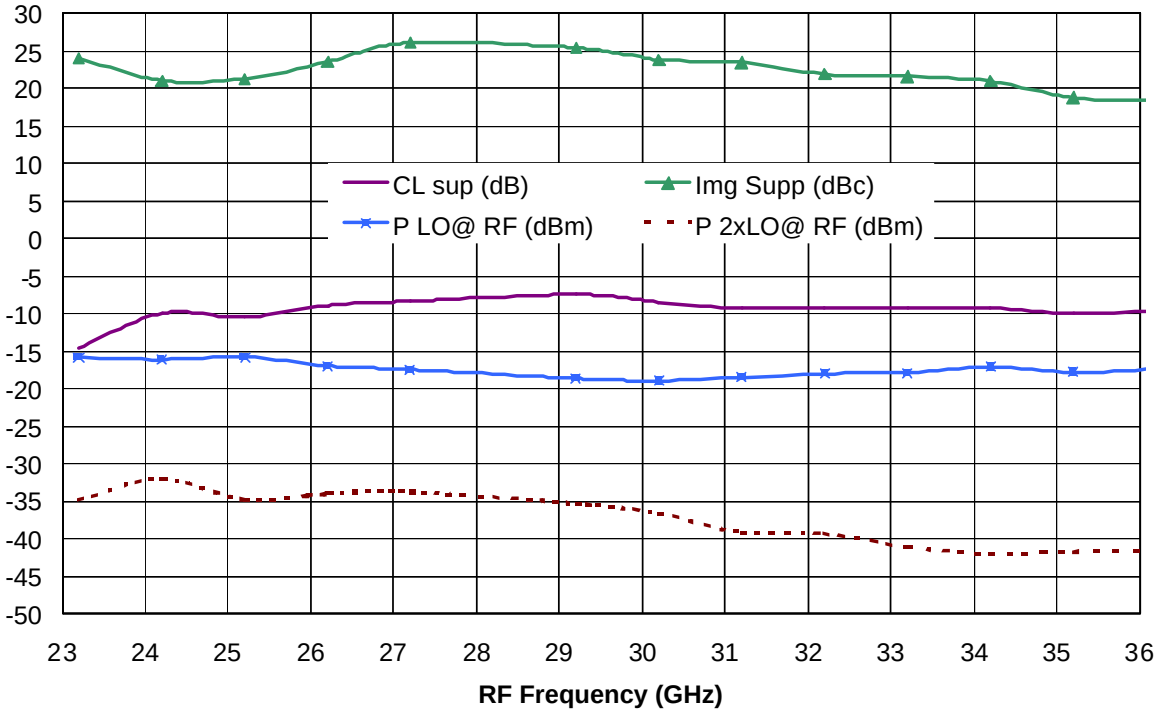
Typical On-wafer Measurements

Bias Conditions :
Vd= 4 V, Id= 55mA

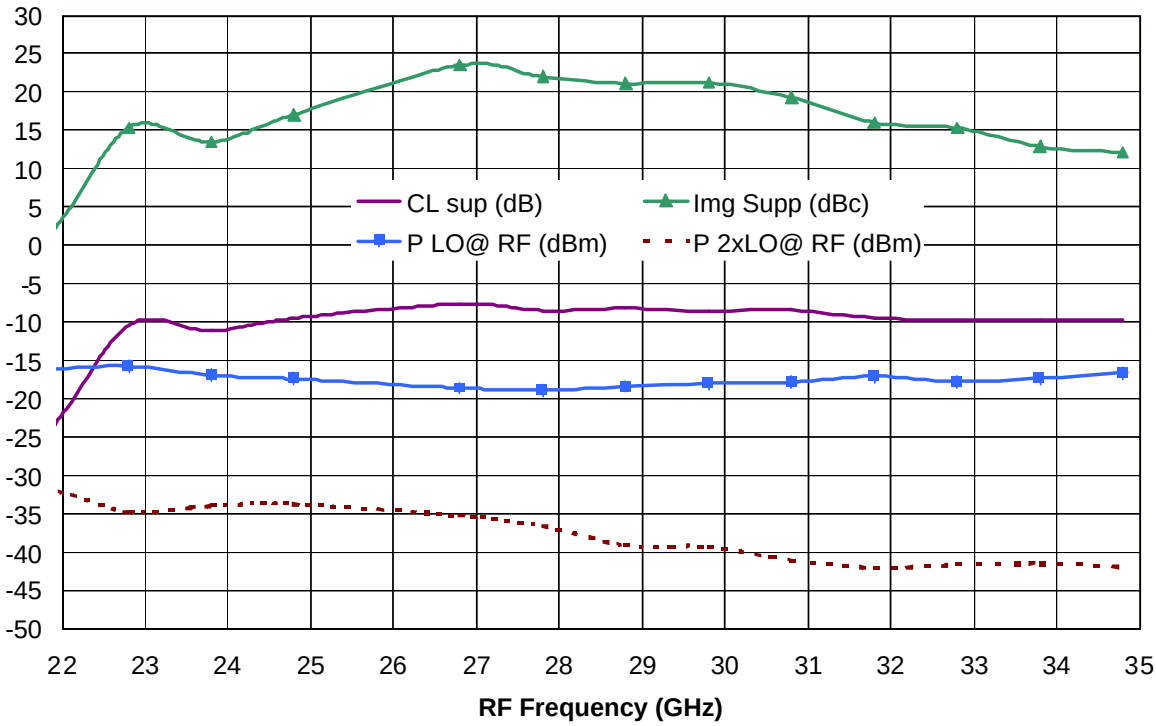
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Conversion gain, Image suppression & LO rejection with a 90° IQ combiner

UP Conversion- Supradyne mode- IF =1.2GHz



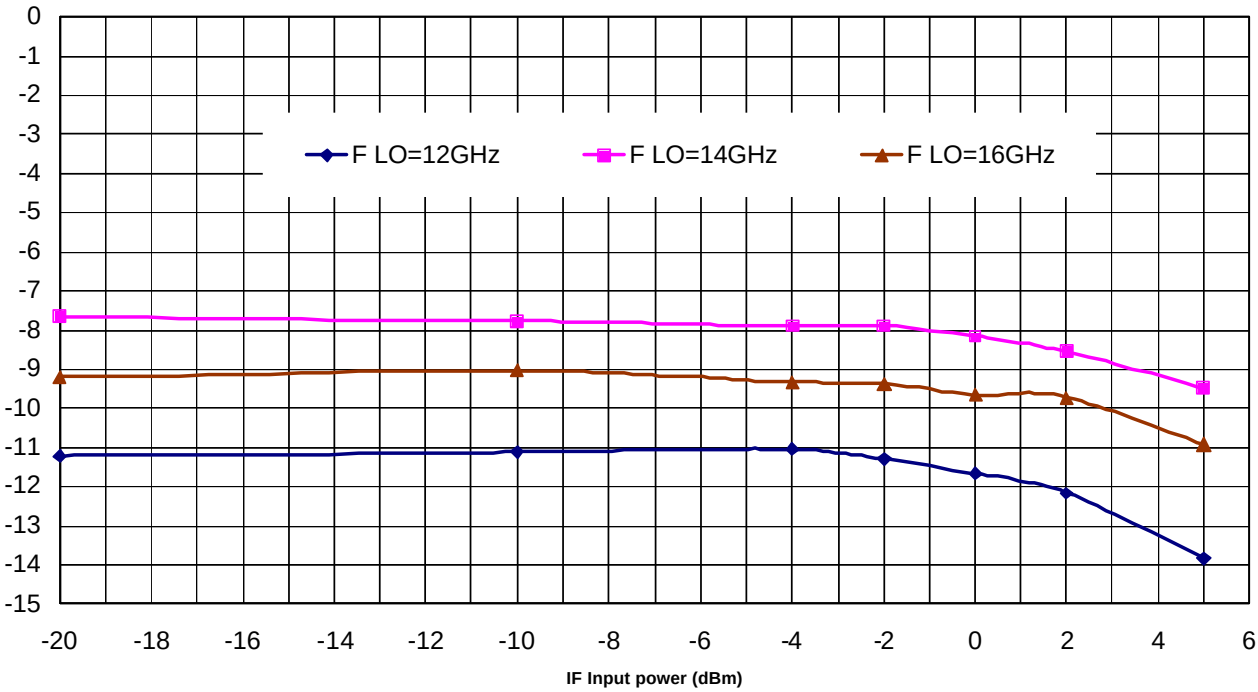
UP Conversion- Infradyne mode- IF =1.2GHz



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UP Conversion- Supradyne mode- IF =1.2GHz
Gain compression versus IF input power



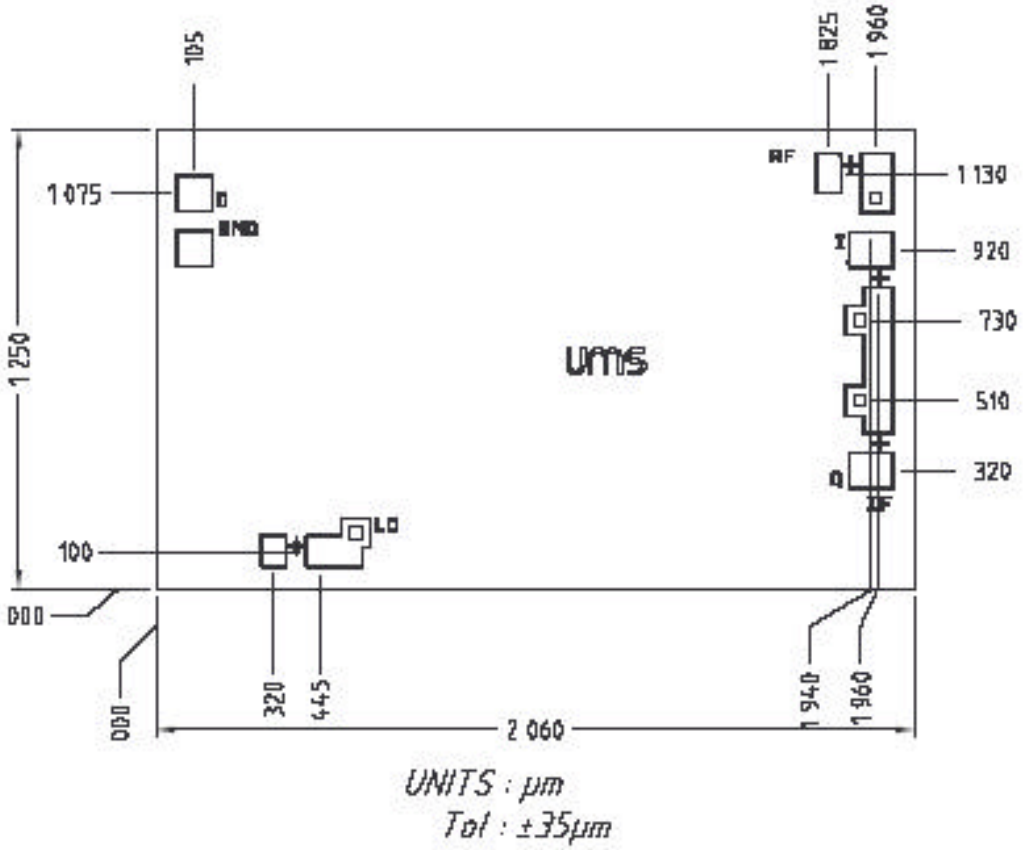
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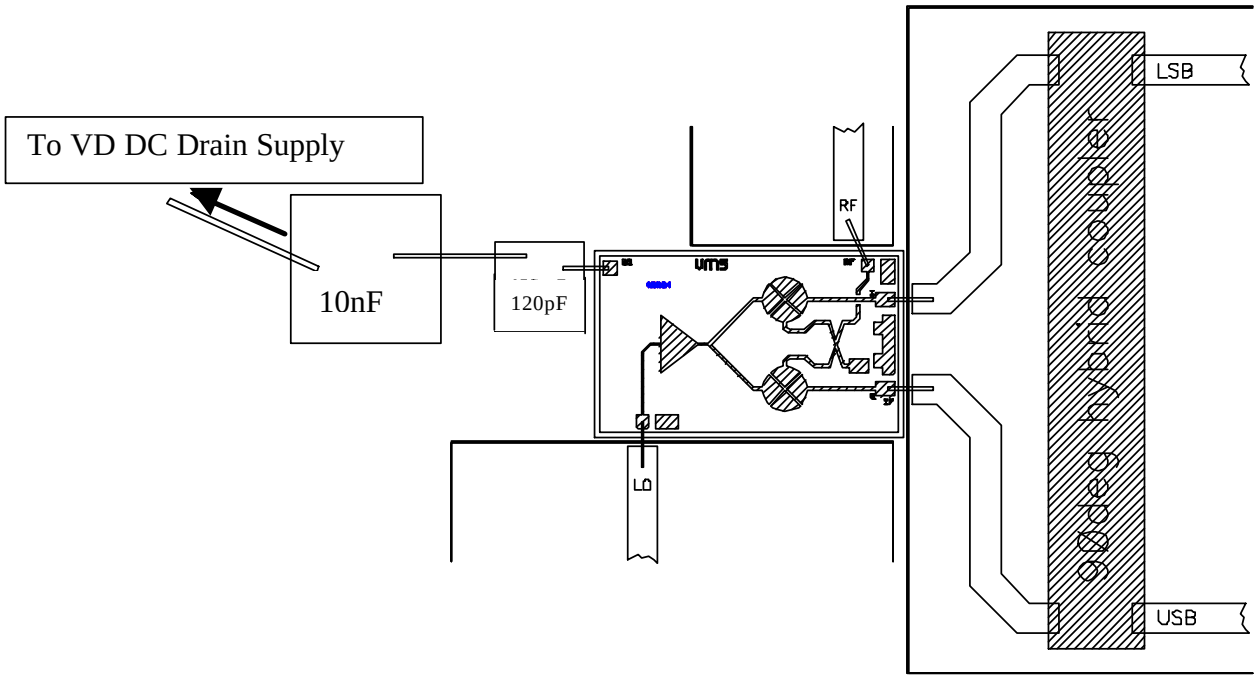
Chip Assembly and Mechanical Data

Preliminary

Bonding pad positions



(Chip thickness: 100µm)



Note : Supply feed should be capacitively bypassed. 25µm diameter gold wire is recommended

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Ordering Information

Chip form : CHR2294-99F/00

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