

# CMOS 8-bit Single-chip Microcomputer

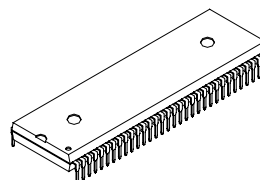
### Description

The CXP852P32A is highly integrated microcomputers composed of 8-bit CPU, PROM, RAM, and I/O ports. This IC features many other high-performance circuits in a single-chip CMOS design, including an A/D converter, serial interface, timer/counter, time base timer, vector interrupt, on-screen display function, I<sup>2</sup>C bus interface, PWM generator, remote control receiver, HSYNC counter, power supply frequency counter, and watchdog timer.

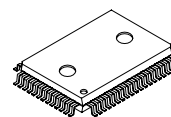
Also this IC provides power-on reset and sleep functions. The designers have ensured low power consumption for these powerful microcomputers.

The CXP852P32A is the on-chip PROM version of the CXP85232A with on-chip mask ROM, providing the function of being able to write directly into the program. Furthermore, because of the OSD character ROM can also be written directly into, it is suitable for evaluation use during system development and for small quantity production.

64 pin SDIP (Plastic)



64 pin OFP (Plastic)



## Structure

Silicon gate CMOS IC

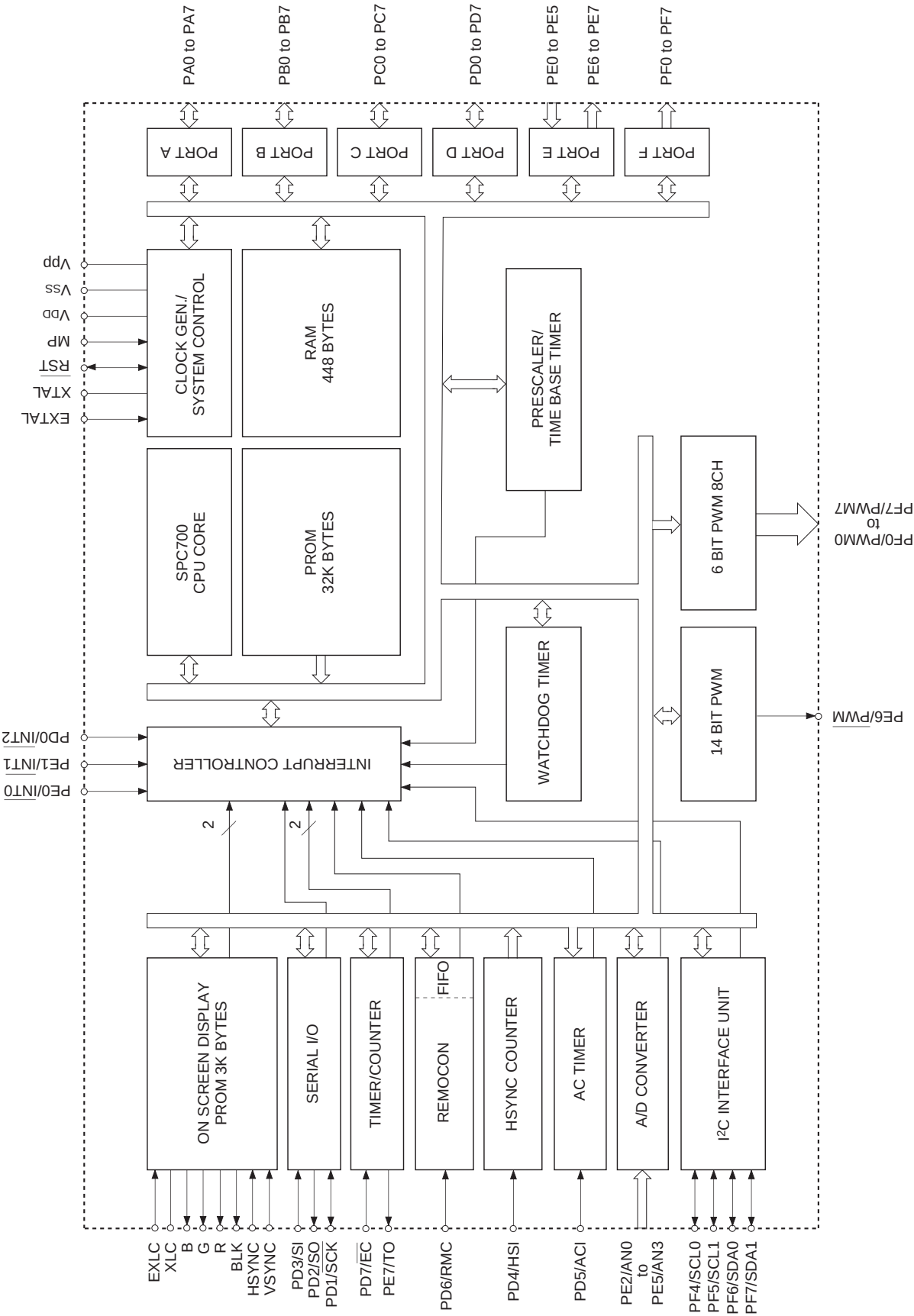
## Features

- A wide instruction set (213 instructions) to cover various types of data
  - 16-bit arithmetic/multiplication and division/boolean bit operation instructions
- Minimum instruction cycle                  During operation 1μs at 4MHz
- Incorporated PROM capacity                32K bytes (For program)  
                                                             3K bytes (for OSD)
- Incorporated RAM capacity                 448 bytes
- Peripheral functions
  - On-screen display function                12 × 16 dots, 128 types  
                                                             4 lines of 21 characters (5 or more lines possible) , double scanning mode  
                                                             supported, jitter elimination circuit
  - I<sup>2</sup>C bus interface
  - PWM output                                    14 bits, 1 channel  
                                                             6 bits, 8 channels
  - Remote control reception circuit        8-bit pulse measuring counter, 6-stage FIFO
  - A/D converter                                4 bits, 4 channels, successive approximation method  
                                                             (Conversion time of 40μs at 4MHz)
  - HSYNC counter
  - Power supply frequency counter
  - Watchdog timer
  - Serial I/O                                      8-bit clock synchronization
  - Timer                                            8-bit timer, 8-bit timer/counter, 19-bit time base timer
- Interruption                                    14 factors, 14 vectors, multi-interrupt possible
- Standby mode                                  Sleep

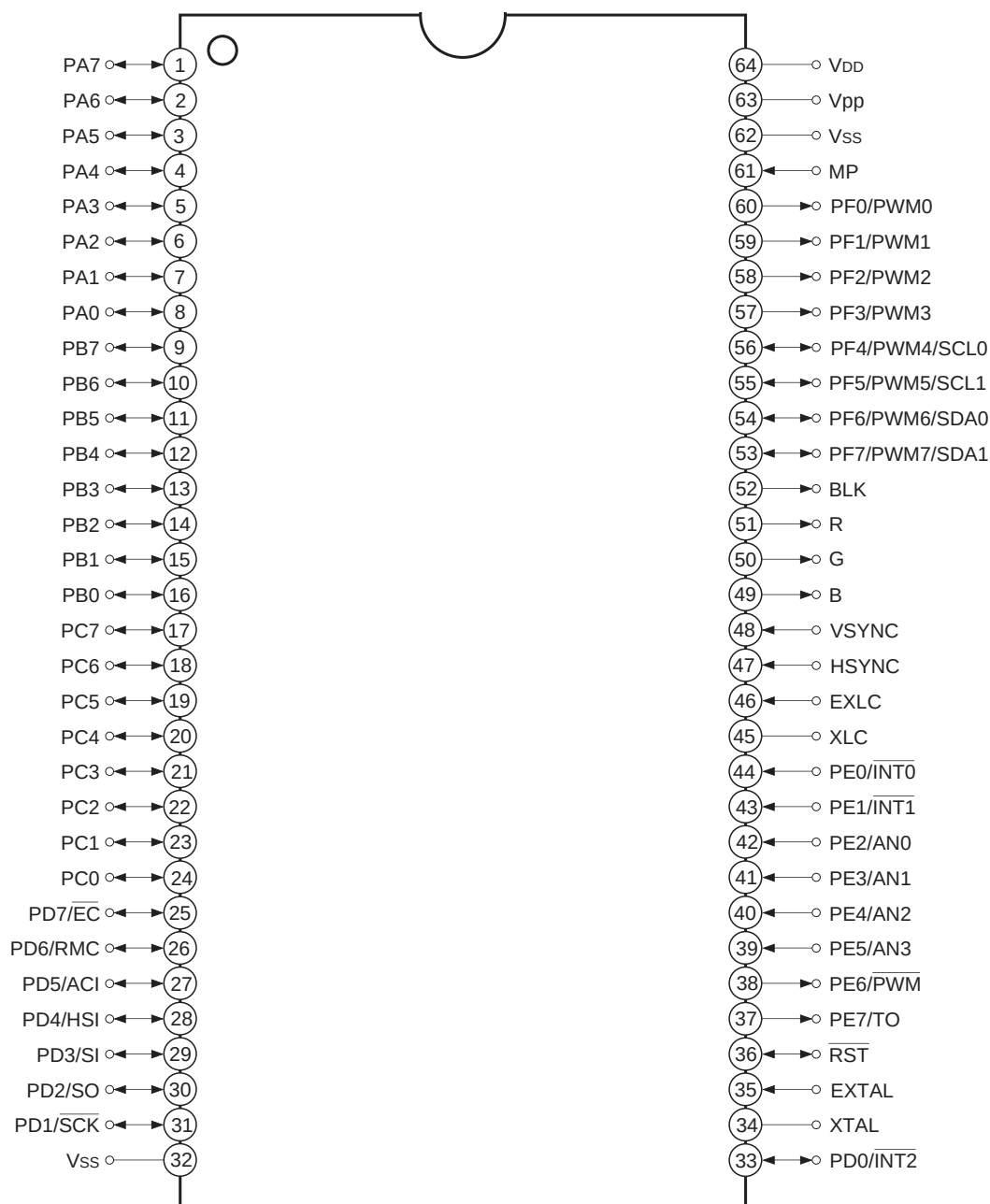
Purchase of Sony's I<sup>2</sup>C components conveys a license under the Philips I<sup>2</sup>C Patent Rights to use these components in an I<sup>2</sup>C system, provided that the system conforms to the I<sup>2</sup>C Standard Specifications as defined by Philips.

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Block Diagram

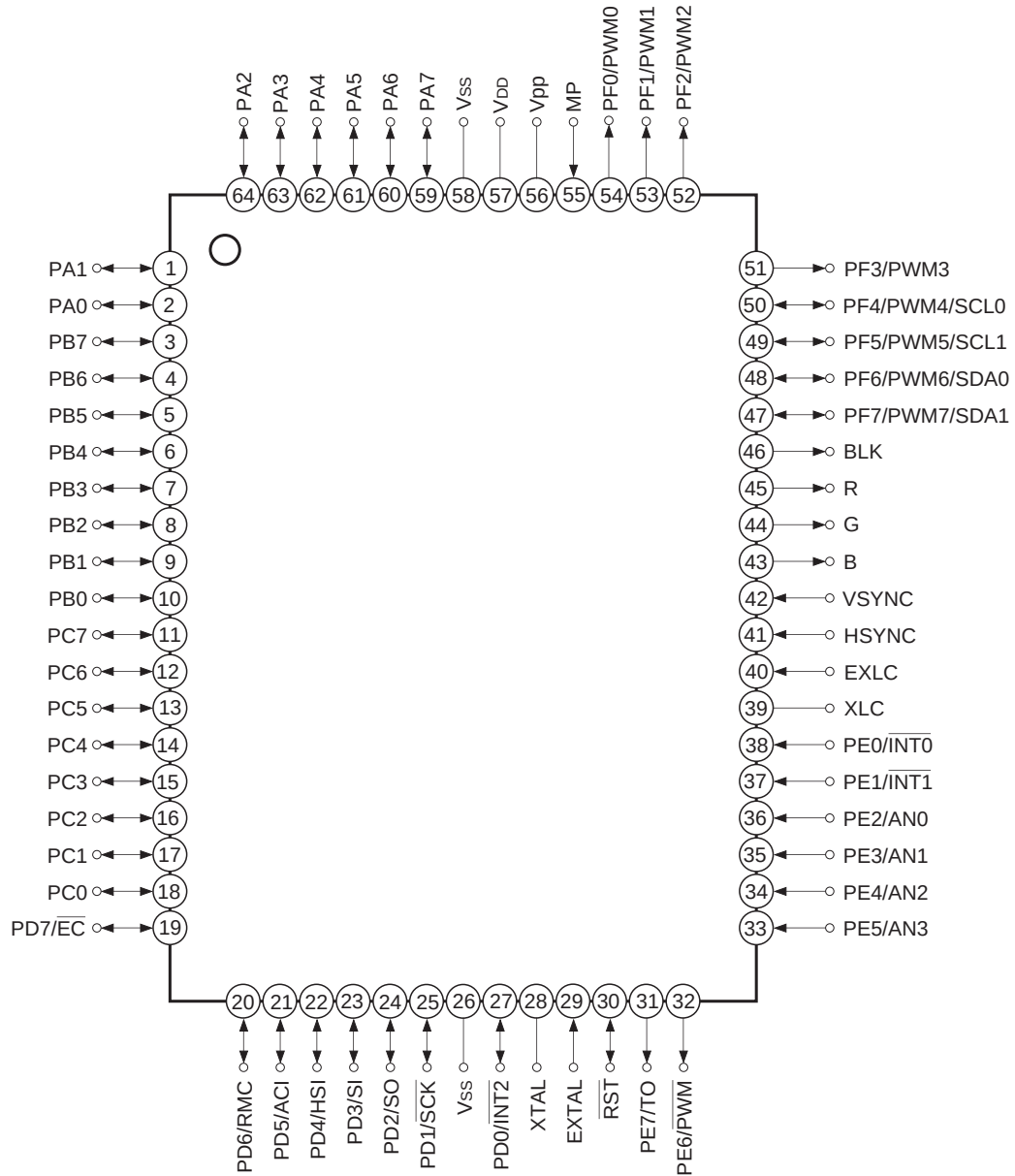


## Pin Assignment 1 (Top View) 64 pin SDIP Package



- Note)**
1. Vpp (Pin 63) is always connected to V<sub>DD</sub>.
  2. Vss (Pins 32 and 62) are both connected to GND.
  3. MP (Pin 61) is always connected to GND.

Pin Assignment 2 (Top View) 64 pin QFP Package



- Note)**
1. Vpp (Pin 56) is always connected to VDD.
  2. Vss (Pins 26 and 58) are both connected GND.
  3. MP (Pin 55) is always connected to GND.

## Pin Description

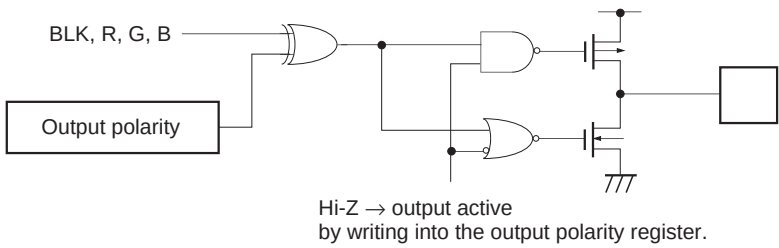
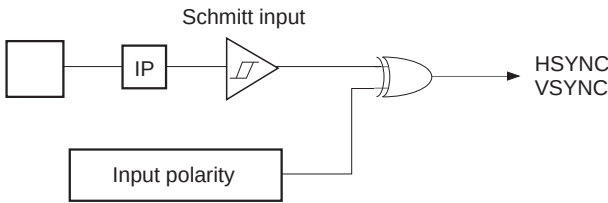
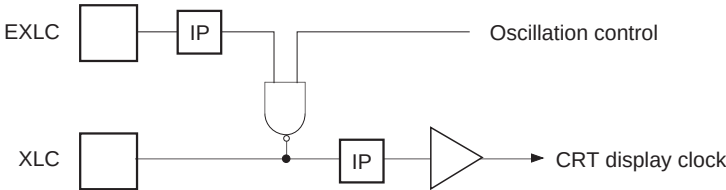
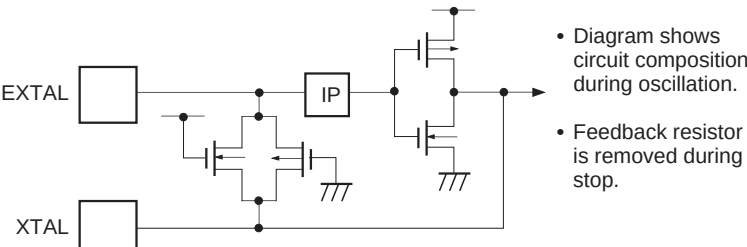
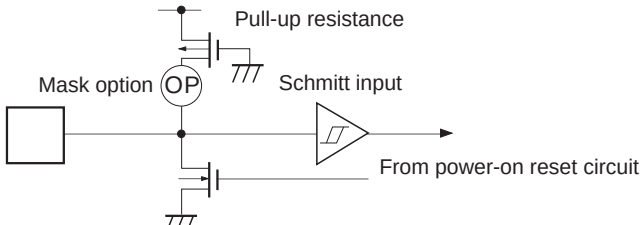
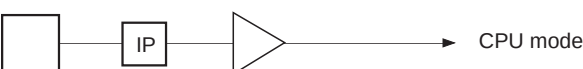
| Symbol                                                                             | I/O                   | Description                                                                                                                                                                                               |                                                                              |
|------------------------------------------------------------------------------------|-----------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------------------------------------------------------------|
| PA0 to PA7                                                                         | I/O                   | (Port A)<br>8-bit I/O port. I/O can be set in a unit of single bits.<br>(8 pins)                                                                                                                          |                                                                              |
| PB0 to PB7                                                                         | I/O                   | (Port B)<br>8-bit I/O port. I/O can be set in a unit of single bits.<br>(8 pins)                                                                                                                          |                                                                              |
| PC0 to PC7                                                                         | I/O                   | (Port C)<br>8-bit I/O port. I/O can be set in a unit of single bits.<br>(8 pins)                                                                                                                          |                                                                              |
| PD0/ $\overline{\text{INT2}}$                                                      | I/O/Input             | (Port D)<br>8-bit I/O port. I/O can be set in a unit of single bits.<br>Capable of driving 12mA sink current.<br>(8 pins)                                                                                 | External interruption request input.<br>Active at falling edge.              |
| PD1/ $\overline{\text{SCK}}$                                                       | I/O/I/O               |                                                                                                                                                                                                           | Serial clock I/O.                                                            |
| PD2/ $\overline{\text{SO}}$                                                        | I/O/Output            |                                                                                                                                                                                                           | Serial data output.                                                          |
| PD3/ $\overline{\text{SI}}$                                                        | I/O/Input             |                                                                                                                                                                                                           | Serial data input.                                                           |
| PD4/ $\overline{\text{HSI}}$                                                       | I/O/Input             |                                                                                                                                                                                                           | HSYNC counter input.                                                         |
| PD5/ $\overline{\text{ACI}}$                                                       | I/O/Input             |                                                                                                                                                                                                           | Input for power supply frequency counter.                                    |
| PD6/ $\overline{\text{RMC}}$                                                       | I/O/Input             |                                                                                                                                                                                                           | Input for remote control reception circuit.                                  |
| PD7/ $\overline{\text{EC}}$                                                        | I/O/Input             |                                                                                                                                                                                                           | External event input for timer/counter.                                      |
| PE0/ $\overline{\text{INT0}}$<br>PE1/ $\overline{\text{INT1}}$                     | Input/Input           | (Port E)<br>8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs.<br>(8 pins)                                                                                                            | External interruption request inputs.<br>Active at falling edge.<br>(2 pins) |
| PE2/ $\overline{\text{AN0}}$<br>to<br>PE5/ $\overline{\text{AN3}}$                 | Input/Input           |                                                                                                                                                                                                           | Analog inputs for A/D converter.<br>(4 pins)                                 |
| PE6/ $\overline{\text{PWM}}$                                                       | Output/Output         |                                                                                                                                                                                                           | 14-bit PWM output.<br>(CMOS output)                                          |
| PE7/ $\overline{\text{TO}}$                                                        | Output/Output         |                                                                                                                                                                                                           | Rectangular waveform output for Timer 1.<br>(Duty output 50%)                |
| PF0/ $\overline{\text{PWM0}}$<br>to<br>PF3/ $\overline{\text{PWM3}}$               | Output/Output         | (Port F)<br>8-bit output port, operating as N-ch open drain output for high current (12mA).<br>Lower 4 bits are for medium voltage drive outputs (12V), upper 4bits are for 5V drive outputs.<br>(8 pins) | 6-bit PWM outputs.<br>(8 pins)                                               |
| PF4/ $\overline{\text{PWM4}}$ /<br>SCL0<br>PF5/ $\overline{\text{PWM5}}$ /<br>SCL1 | Output/Output/<br>I/O |                                                                                                                                                                                                           | Transfer clock I/Os for I <sup>2</sup> C bus interface.                      |
| PF6/ $\overline{\text{PWM6}}$ /<br>SDA0<br>PF7/ $\overline{\text{PWM7}}$ /<br>SDA1 | Output/Output/<br>I/O |                                                                                                                                                                                                           | Transfer data I/Os for I <sup>2</sup> C data bus.                            |
| R, G, B, BLK                                                                       | Output                | 4-bit outputs for CRT display.                                                                                                                                                                            |                                                                              |
| HSYNC                                                                              | Input                 | Horizontal synchronizing signal input for CRT display.                                                                                                                                                    |                                                                              |
| VSYNC                                                                              | Input                 | Vertical synchronizing signal input for CRT display.                                                                                                                                                      |                                                                              |

| Symbol                  | I/O    | Description                                                                                                                                                                       |
|-------------------------|--------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| EXLC                    | Input  | Clock oscillation I/Os for CRT display.<br>Oscillation frequency is set using the external L and C.                                                                               |
| XLC                     | Output |                                                                                                                                                                                   |
| EXTAL                   | Input  | Crystai connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL and leave XTAL open.                                                       |
| XTAL                    | Output |                                                                                                                                                                                   |
| $\overline{\text{RST}}$ | I/O    | Low-level active, system reset. $\overline{\text{RST}}$ is an I/O, from which Low level is output when the built-in power-on reset function is activated at the rise of power on. |
| MP                      | Input  | Microprocessor mode input. For this device, this pin must be grounded.                                                                                                            |
| V <sub>DD</sub>         |        | Positive power supply.                                                                                                                                                            |
| V <sub>pp</sub>         |        | Positive power supply pin for on-chip PROM writing.<br>Connect to V <sub>DD</sub> for normal operation.                                                                           |
| V <sub>ss</sub>         |        | GND. Both V <sub>ss</sub> mvst be grounded.                                                                                                                                       |

Input/Output Circuit Formats for Pins

| Pin                                                                                                                   | Circuit format             |                                                                                                                                                                                                                                                           | When reset |
|-----------------------------------------------------------------------------------------------------------------------|----------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------|
| PA0 to PA7<br>PB0 to PB7<br>PC0 to PC7<br><br>24 pins                                                                 | Port A<br>Port B<br>Port C | <p>Data for Ports A, B, and C</p> <p>Direction for Ports A, B, and C</p> <p>Data bus</p> <p>RD (Ports A, B, and C)</p> <p>IP Input protection circuit</p>                                                                                                 | Hi-Z       |
| PD0/ $\overline{\text{INT2}}$<br>PD3/SI<br>PD4/HSI<br>PD5/ACI<br>PD6/RMC<br>PD7/ $\overline{\text{EC}}$<br><br>6 pins | Port D                     | <p>Port D data</p> <p>Port D direction</p> <p>Data bus</p> <p>RD (Port D)</p> <p><math>\overline{\text{INT2}}</math>, SI, HSI, ACI, RMC, <math>\overline{\text{EC}}</math></p> <p>Schmitt input</p> <p>High current 12mA</p> <p>IP</p>                    | Hi-Z       |
| PD1/ $\overline{\text{SCK}}$<br>PD2/SO<br><br>2 pins                                                                  | Port D                     | <p><math>\overline{\text{SCK}}</math> or SO</p> <p>Output enable</p> <p>Port D data</p> <p>Port D direction</p> <p>Data bus</p> <p>RD (Port D)</p> <p><math>\overline{\text{SCK}}</math> only</p> <p>Schmitt input</p> <p>High current 12mA</p> <p>IP</p> | Hi-Z       |

| Pin                                                                                                                                                                                    | Circuit format    | When reset |
|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|-------------------|------------|
| PE0/ $\overline{\text{INT0}}$<br>PE1/ $\overline{\text{INT1}}$<br><br>2 pins                                                                                                           | <div>Port E</div> | Hi-Z       |
| PE2/AN0<br>to<br>PE5/AN3<br><br>4 pins                                                                                                                                                 | <div>Port E</div> | Hi-Z       |
| PE6/ $\overline{\text{PWM}}$<br>PE7/ $\overline{\text{TO}}$<br><br>2 pins                                                                                                              | <div>Port E</div> | High level |
| PF0/ $\overline{\text{PWM0}}$<br>to<br>PF3/ $\overline{\text{PWM3}}$<br><br>4 pins                                                                                                     | <div>Port F</div> | Hi-Z       |
| PF4/ $\overline{\text{PWM4}}$ /<br>SCL0<br>PF5/ $\overline{\text{PWM5}}$ /<br>SCL1<br>PF6/ $\overline{\text{PWM6}}$ /<br>SDA0<br>PF7/ $\overline{\text{PWM7}}$ /<br>SDA1<br><br>4 pins | <div>Port F</div> | Hi-Z       |

| Pin                                  | Circuit format                                                                                                                                                                                                                                      | When reset             |
|--------------------------------------|-----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|------------------------|
| BLK<br>R<br>G<br>B<br><br>4 pins     |  <p>Hi-Z → output active by writing into the output polarity register.</p>                                                                                        | Hi-Z                   |
| HSYNC<br>VSYNC<br><br>2 pins         |                                                                                                                                                                   | Hi-Z                   |
| EXLC<br>XLC<br><br>2 pins            |  <p>Oscillation control</p> <p>CRT display clock</p>                                                                                                             | Oscillation terminated |
| EXTAL<br>XTAL<br><br>2 pins          |  <ul style="list-style-type: none"> <li>• Diagram shows circuit composition during oscillation.</li> <li>• Feedback resistor is removed during stop.</li> </ul> | Oscillation            |
| $\overline{\text{RST}}$<br><br>1 pin |  <p>Pull-up resistance</p> <p>Mask option OP</p> <p>Schmitt input</p> <p>From power-on reset circuit</p>                                                        | Low level              |
| MP<br><br>1 pin                      |  <p>CPU mode</p>                                                                                                                                                | Hi-Z                   |

## Absolute Maximum Ratings

(Vss = 0V reference)

| Item                                | Symbol            | Rating                     | Unit | Remarks                            |
|-------------------------------------|-------------------|----------------------------|------|------------------------------------|
| Supply voltage                      | V <sub>DD</sub>   | −0.3 to +7.0               | V    |                                    |
|                                     | V <sub>pp</sub>   | −0.3 to +13.0              | V    | Incorporated PROM                  |
| Input voltage                       | V <sub>IN</sub>   | −0.3 to +7.0* <sup>1</sup> | V    |                                    |
| Output voltage                      | V <sub>OUT</sub>  | −0.3 to +7.0* <sup>1</sup> | V    |                                    |
| Medium voltage drive output voltage | V <sub>OUTP</sub> | −0.3 to +15.0              | V    | Pins PF0 to PF3                    |
| High level output current           | I <sub>OH</sub>   | −5                         | mA   |                                    |
| High level total output current     | ΣI <sub>OH</sub>  | −50                        | mA   | Total for all output pins          |
| Low level output current            | I <sub>OL</sub>   | 15                         | mA   | Excludes high current outputs      |
|                                     | I <sub>OLC</sub>  | 20                         | mA   | High current outputs* <sup>2</sup> |
| Low level total output current      | ΣI <sub>OL</sub>  | 130                        | mA   | Total for all output pins          |
| Operating temperature               | T <sub>opr</sub>  | −10 to +75                 | °C   |                                    |
| Storage temperature                 | T <sub>stg</sub>  | −55 to +150                | °C   |                                    |
| Allowable power dissipation         | P <sub>D</sub>    | 1000                       | mW   | SDIP                               |
|                                     |                   | 600                        | mW   | QFP                                |

\*<sup>1</sup> V<sub>IN</sub> and V<sub>OUT</sub> must not exceed V<sub>DD</sub> + 0.3V.

\*<sup>2</sup> The high current operation transistor are the N-ch transistors of the PD and PF0 to PF3 ports.

**Note)** Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions.

Exceeding these conditions may adversely affect the reliability of the LSI.

## Recommended Operating Conditions

(V<sub>SS</sub> = 0V reference)

| Item                     | Symbol            | Min.                              | Max.                  | Unit | Remarks                                                 |
|--------------------------|-------------------|-----------------------------------|-----------------------|------|---------------------------------------------------------|
| Supply voltage           | V <sub>DD</sub>   | 4.5                               | 5.5                   | V    | Guaranteed operation range                              |
|                          |                   | 3.5                               | 5.5                   | V    | Low-speed mode guaranteed operation range* <sup>1</sup> |
|                          |                   | 2.5                               | 5.5                   | V    | Guaranteed data hold range during stop                  |
|                          | V <sub>pp</sub>   | V <sub>pp</sub> = V <sub>DD</sub> |                       | V    | * <sup>5</sup>                                          |
| High level input voltage | V <sub>IH</sub>   | 0.7V <sub>DD</sub>                | V <sub>DD</sub>       | V    | Includes I <sup>2</sup> C Schmitt input* <sup>2</sup>   |
|                          | V <sub>IHS</sub>  | 0.8V <sub>DD</sub>                | V <sub>DD</sub>       | V    | CMOS Schmitt input* <sup>3</sup>                        |
|                          | V <sub>IHEX</sub> | V <sub>DD</sub> - 0.4             | V <sub>DD</sub> + 0.3 | V    | EXTAL* <sup>4</sup>                                     |
| Low level input voltage  | V <sub>IL</sub>   | 0                                 | 0.3V <sub>DD</sub>    | V    | Includes I <sup>2</sup> C Schmitt input* <sup>2</sup>   |
|                          | V <sub>ILS</sub>  | 0                                 | 0.2V <sub>DD</sub>    | V    | CMOS Schmitt input* <sup>3</sup>                        |
|                          | V <sub>ILEX</sub> | -0.3                              | 0.4                   | V    | EXTAL* <sup>4</sup>                                     |
| Operating temperature    | Topr              | -10                               | +75                   | °C   |                                                         |

\*<sup>1</sup> Specifies only for 1/16 frequency demultiplication mode and sleep mode.

\*<sup>2</sup> Value for each pin of normal input ports (PA, PB, PC, PE2 to PE5), PF4 to PF7, and MP.

\*<sup>3</sup> Value of the following pins: PD0/ $\overline{\text{INT2}}$ , PD1/ $\overline{\text{SCK}}$ , PD2, PD3/SI, PD4/HSI, PD5/ACI, PD6/RMC, PD7/ $\overline{\text{EC}}$ , PE0/ $\overline{\text{INT0}}$ , PE1/ $\overline{\text{INT1}}$ , HSYNC, VSYNC,  $\overline{\text{RST}}$ .

\*<sup>4</sup> Specifies only during external clock input.

\*<sup>5</sup> V<sub>pp</sub> and V<sub>DD</sub> should be set to the same voltage.

## Electrical Characteristics

## DC Characteristics

(Ta = -10 to +75°C, Vss = 0V reference)

| Item                                                                        | Symbol            | Pins                                                | Conditions                                                                                                                                      | Min. | Typ. | Max. | Unit |
|-----------------------------------------------------------------------------|-------------------|-----------------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------|------|------|------|------|
| High level output current                                                   | V <sub>OH</sub>   | PA to PD, PE6, PE7, R, G, B, BLK                    | V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -0.5mA                                                                                                | 4.0  |      |      | V    |
|                                                                             |                   |                                                     | V <sub>DD</sub> = 4.5V, I <sub>OH</sub> = -1.2mA                                                                                                | 3.5  |      |      | V    |
| Low level output current                                                    | V <sub>OL</sub>   | PA to PD, PE6, PE7, R, G, B, BLK, PF0 to PF3, RST   | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 1.8mA                                                                                                 |      |      | 0.4  | V    |
|                                                                             |                   |                                                     | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.6mA                                                                                                 |      |      | 0.6  | V    |
|                                                                             |                   | PD, PF0 to PF3                                      | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 12.0mA                                                                                                |      |      | 1.5  | V    |
|                                                                             |                   | PF4 to PF7 (SCL0, SCL1, SDA0, SDA1)                 | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 3.0mA                                                                                                 |      |      | 0.4  | V    |
|                                                                             |                   |                                                     | V <sub>DD</sub> = 4.5V, I <sub>OL</sub> = 4.0mA                                                                                                 |      |      | 0.6  | V    |
| Input current                                                               | I <sub>IHE</sub>  | EXTAL                                               | V <sub>DD</sub> = 5.5V, V <sub>IH</sub> = 5.5V                                                                                                  | 0.5  |      | 40   | μA   |
|                                                                             | I <sub>IHL</sub>  |                                                     | V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V                                                                                                  | -0.5 |      | -40  | μA   |
|                                                                             | I <sub>ILR</sub>  | RST                                                 | V <sub>DD</sub> = 5.5V, V <sub>IL</sub> = 0.4V                                                                                                  | -1.5 |      | -400 | μA   |
| I/O leakage current                                                         | I <sub>Iz</sub>   | PA to PE, HSYNC, VSYNC, R, G, B, BLK, MP            | V <sub>DD</sub> = 5.5V<br>V <sub>I</sub> = 0, 5.5V                                                                                              |      |      | ±10  | μA   |
| Open drain output leakage current (N-ch Tr in off state)                    | I <sub>LOH</sub>  | PF0 to PF3                                          | V <sub>DD</sub> = 5.5V, V <sub>OH</sub> = 12.0V                                                                                                 |      |      | 50   | μA   |
|                                                                             |                   | PF4 to PF7                                          | V <sub>DD</sub> = 5.5V, V <sub>OH</sub> = 5.5V                                                                                                  |      |      | 10   | μA   |
| Impedance connected to I <sup>2</sup> C bus switch (output Tr in off state) | R <sub>BS</sub>   | SCL0: SCL1<br>SDA0: SDA1                            | V <sub>DD</sub> = 4.5V<br>V <sub>SCL0</sub> = V <sub>SCL1</sub> = 2.25V<br>V <sub>SDA0</sub> = V <sub>SDA1</sub> = 2.25V                        |      |      | 120  | Ω    |
| Power supply current                                                        | I <sub>DD</sub>   | V <sub>DD</sub> *1                                  | Operation mode*1<br>(1/2 frequency demultiplier clock)<br>4MHz crystal oscillation (C <sub>1</sub> = C <sub>2</sub> = 22pF)<br>All outputs open |      | 10   | 25   | mA   |
|                                                                             | I <sub>DDSL</sub> |                                                     | Sleep mode                                                                                                                                      |      | 0.7  | 3    | mA   |
|                                                                             | I <sub>DDST</sub> |                                                     | Stop mode*4                                                                                                                                     | —    | —    | —    | μA   |
| Input capacity                                                              | C <sub>IN</sub>   | Pins other than V <sub>DD</sub> and V <sub>SS</sub> | Clock 1MHz<br>0V for no-measured pins                                                                                                           |      | 10   | 20   | pF   |

\*1 Rating applies only if OSD oscillator is halted.

\*2 This device does not enter in the stop mode.

## AC Characteristics

## (1) Clock timing

(Ta = -10 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

| Item                                           | Symbol                               | Pins                   | Conditions                             | Min.                    | Max. | Unit |
|------------------------------------------------|--------------------------------------|------------------------|----------------------------------------|-------------------------|------|------|
| System clock frequency                         | f <sub>c</sub>                       | XTAL<br>EXTAL          | Fig. 1, Fig. 2                         | 3.5                     | 4.5  | MHz  |
| System clock input pulse width                 | t <sub>XL</sub> ,<br>t <sub>XH</sub> | EXTAL                  | Fig. 1, Fig. 2<br>External clock drive | 100                     |      | ns   |
| System clock input rise time, fall time        | t <sub>CR</sub> ,<br>t <sub>CF</sub> | EXTAL                  | Fig. 1, Fig. 2<br>External clock drive |                         | 200  | ns   |
| Event counter input clock pulse width          | t <sub>EH</sub> ,<br>t <sub>EL</sub> | $\overline{\text{EC}}$ | Fig. 3                                 | t <sub>sys</sub> + 50*1 |      | ns   |
| Event counter input clock rise time, fall time | t <sub>ER</sub> ,<br>t <sub>EF</sub> | $\overline{\text{EC}}$ | Fig. 3                                 |                         | 20   | ms   |

\*1 t<sub>sys</sub> indicates the three values below according to the upper two bits (CPU clock selection) of the clock control register (address: 00FEH).

t<sub>sys</sub> [ns] = 2000/f<sub>c</sub> (upper two bits = "00"), 4000/f<sub>c</sub> (upper two bits = "01"), 16000/f<sub>c</sub> (upper two bits = "11")

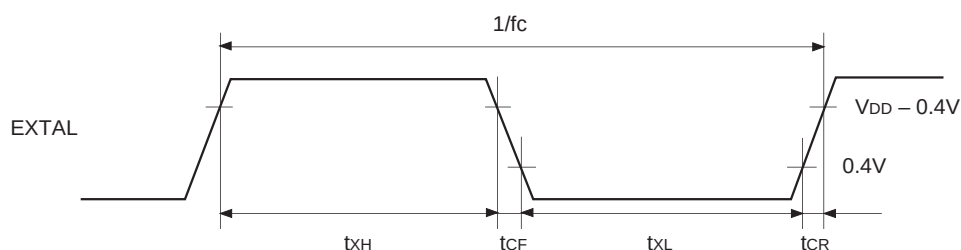


Fig. 1. Clock timing

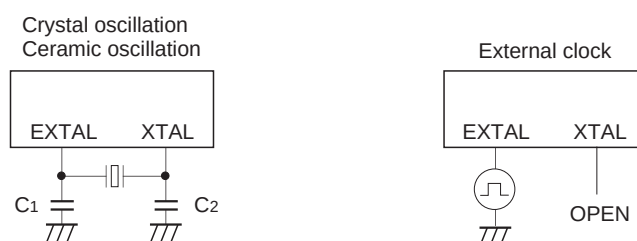


Fig. 2. Clock applied condition

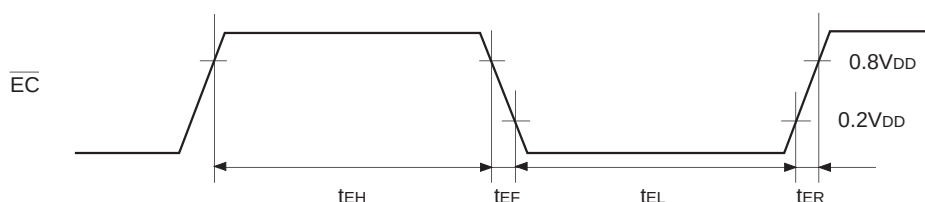
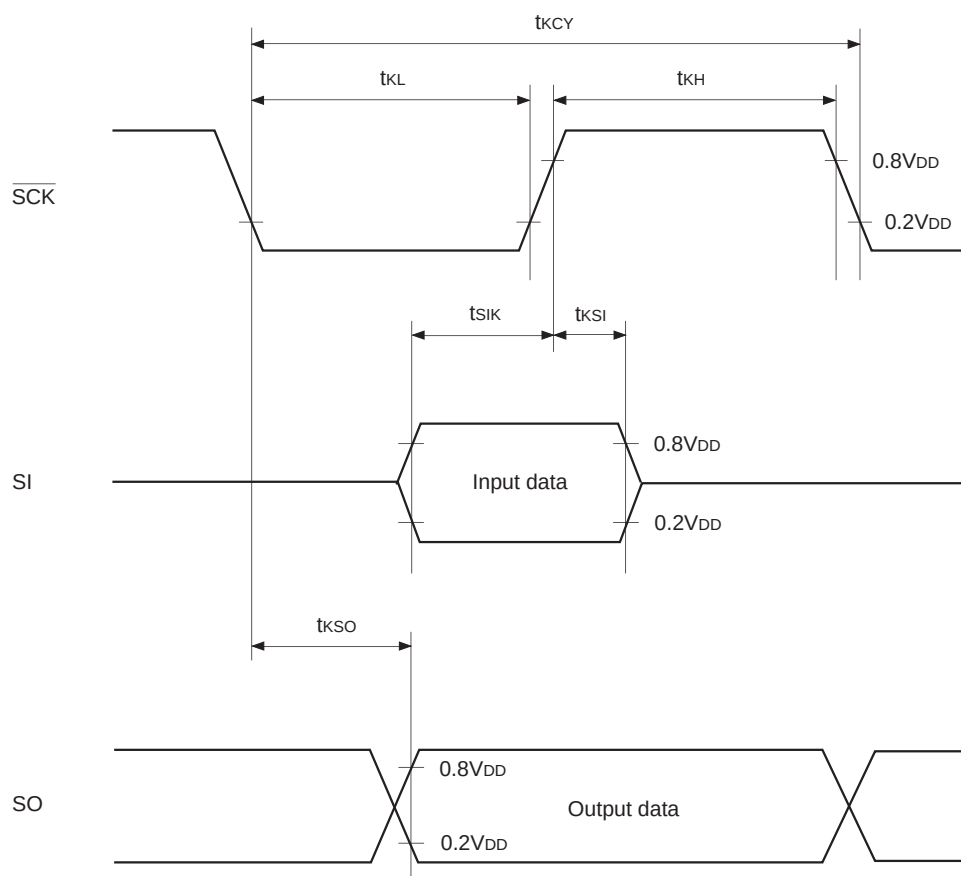


Fig. 3. Event count clock timing

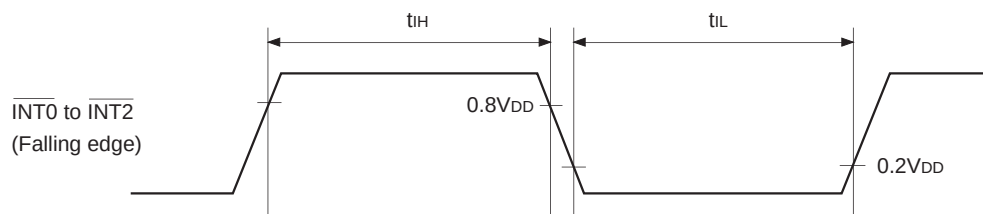
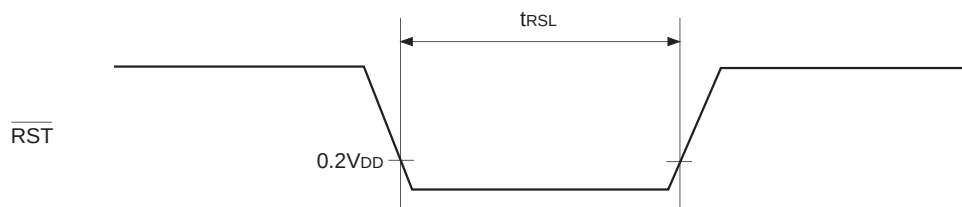
**(2) Serial transfer**(Ta = -10 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

| Item                                                                | Symbol                             | Pins                    | Conditions                          | Min.         | Max. | Unit |
|---------------------------------------------------------------------|------------------------------------|-------------------------|-------------------------------------|--------------|------|------|
| $\overline{\text{SCK}}$ cycle time                                  | $t_{\text{KCY}}$                   | $\overline{\text{SCK}}$ | Input mode                          | 1000         |      | ns   |
|                                                                     |                                    |                         | Output mode                         | 8000/fc      |      | ns   |
| $\overline{\text{SCK}}$ High and Low level widths                   | $t_{\text{KH}}$<br>$t_{\text{KL}}$ | $\overline{\text{SCK}}$ | $\overline{\text{SCK}}$ input mode  | 400          |      | ns   |
|                                                                     |                                    |                         | $\overline{\text{SCK}}$ output mode | 4000/fc - 50 |      | ns   |
| SI input setup time (for $\overline{\text{SCK}} \uparrow$ )         | $t_{\text{SIK}}$                   | SI                      | $\overline{\text{SCK}}$ input mode  | 100          |      | ns   |
|                                                                     |                                    |                         | $\overline{\text{SCK}}$ output mode | 200          |      | ns   |
| SI input hold time (for $\overline{\text{SCK}} \uparrow$ )          | $t_{\text{KSI}}$                   | SI                      | $\overline{\text{SCK}}$ input mode  | 200          |      | ns   |
|                                                                     |                                    |                         | $\overline{\text{SCK}}$ output mode | 100          |      | ns   |
| $\overline{\text{SCK}} \downarrow \rightarrow \text{SO}$ delay time | $t_{\text{KSO}}$                   | SO                      | $\overline{\text{SCK}}$ input mode  |              | 200  | ns   |
|                                                                     |                                    |                         | $\overline{\text{SCK}}$ output mode |              | 100  | ns   |

**Note)** The load condition for the  $\overline{\text{SCK}}$  output mode, SO output delay time is 50pF + 1TTL.**Fig. 4. Serial transfer timing**

**(3) Interruption, reset input**(Ta = -10 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

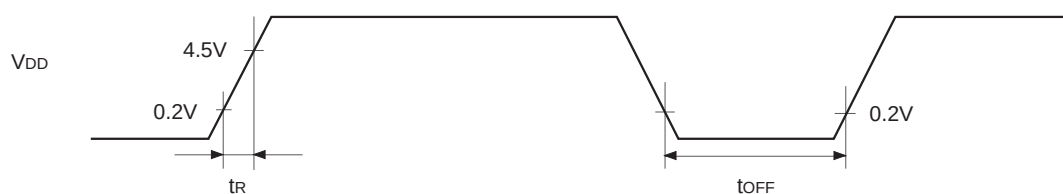
| Item                                               | Symbol                             | Pins         | Conditions | Min. | Max. | Unit |
|----------------------------------------------------|------------------------------------|--------------|------------|------|------|------|
| External interruption<br>High and Low level widths | t <sub>IH</sub><br>t <sub>IL</sub> | INT0 to INT2 |            | 1    |      | μs   |
| Reset input Low level width                        | t <sub>RSL</sub>                   | RST          |            | 8/fc |      | μs   |

**Fig. 5. Interruption input timing****Fig. 6. RST input timing****(4) Power-on reset**

Power-on reset

(Ta = -10 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

| Item                      | Symbol           | Pins            | Conditions                | Min. | Max. | Unit |
|---------------------------|------------------|-----------------|---------------------------|------|------|------|
| Power supply rise time    | t <sub>R</sub>   | V <sub>DD</sub> | Power-on reset            | 0.05 | 50   | ms   |
| Power supply cut-off time | t <sub>OFF</sub> |                 | Repetitive power-on reset | 1    |      | ms   |

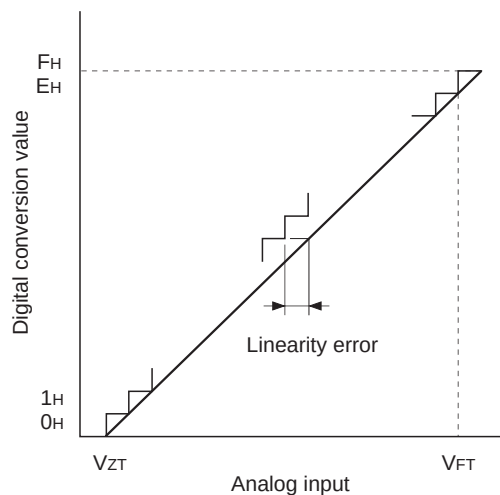


The power supply should be raised smoothly.

**Fig. 7. Power-on reset**

**(5) A/D converter characteristics**(Ta = -10 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

| Item                          | Symbol             | Pin        | Condition                                                   | Min.   | Typ. | Max.            | Unit |
|-------------------------------|--------------------|------------|-------------------------------------------------------------|--------|------|-----------------|------|
| Resolution                    |                    |            |                                                             |        |      | 4               | Bits |
| Linearity error               |                    |            | Ta = 25°C<br>V <sub>DD</sub> = 5.0V<br>V <sub>SS</sub> = 0V |        |      | ±1              | LSB  |
| Zero transition voltage       | V <sub>ZT</sub> *1 |            |                                                             | -10    | 160  | 320             | mV   |
| Full-scale transition voltage | V <sub>FT</sub> *2 |            |                                                             | 4370   | 4530 | 4690            | mV   |
| Conversion time               | t <sub>CONV</sub>  |            |                                                             | 160/fc |      |                 | μs   |
| Sampling time                 | t <sub>SAMP</sub>  |            |                                                             | 12/fc  |      |                 | μs   |
| Analog input voltage          | V <sub>IAN</sub>   | AN0 to AN3 |                                                             | 0      |      | V <sub>DD</sub> | V    |



\*1 V<sub>ZT</sub>: Value at which the digital conversion value changes from 0<sub>H</sub> to 1<sub>H</sub> and vice versa.

\*2 V<sub>FT</sub>: Value at which the digital conversion value changes from E<sub>H</sub> to F<sub>H</sub> and vice versa.

**Fig. 8. Definition of A/D converter terms**

**Note)** The 4-bit conversion specifies values based on the upper 5 bits of the A/D data register (ADD: Address 00F5H), compensated into 4-bit data. A program example is shown below:

(A/D converter program example)

```

MOV    A, ADD    ; ACC ← conversion data
LSR    A         ; Shift to the right (4 times)
LSR    A         ;
LSR    A         ;
LSR    A         ;
ADC    A, #00H   ; Addition with carry (data increment if AD3 = 1)
CMP    A, #10H   ;
BNE    ADC_SKIP  ;
MOV    A, #0FH   ;

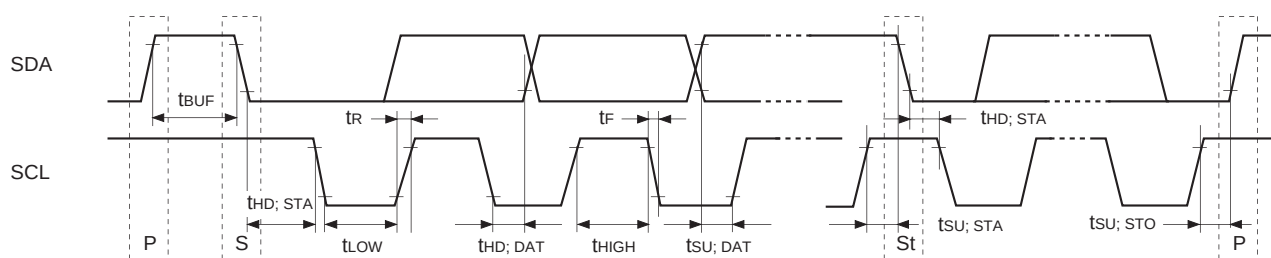
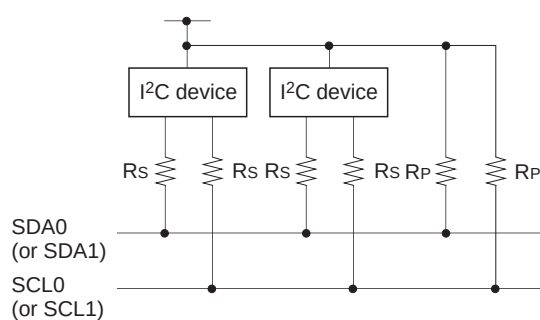
```

ADC\_SKIP:

**(6) I<sup>2</sup>C bus timing**(Ta = -10 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

| Item                                  | Symbol               | Pins     | Conditions | Min. | Max. | Unit |
|---------------------------------------|----------------------|----------|------------|------|------|------|
| SCL clock frequency                   | f <sub>SCL</sub>     | SCL      |            | 0    | 100  | kHz  |
| Bus free time prior to transfer start | t <sub>BUF</sub>     | SDA, SCL |            | 4.7  |      | μs   |
| Transfer start hold time              | t <sub>HD; STA</sub> | SDA, SCL |            | 4.0  |      | μs   |
| Clock Low level width                 | t <sub>LOW</sub>     | SCL      |            | 4.7  |      | μs   |
| Clock High level width                | t <sub>HIGH</sub>    | SCL      |            | 4.0  |      | μs   |
| Setup time during repetitive transfer | t <sub>SU; STA</sub> | SDA, SCL |            | 4.7  |      | μs   |
| Data hold time                        | t <sub>HD; DAT</sub> | SDA, SCL |            | 0*1  |      | μs   |
| Data setup time                       | t <sub>SU; DAT</sub> | SDA, SCL |            | 250  |      | ns   |
| SDA, SCL rise time                    | t <sub>R</sub>       | SDA, SCL |            |      | 1    | μs   |
| SDA, SCL fall time                    | t <sub>F</sub>       | SDA, SCL |            |      | 300  | ns   |
| Transfer end setup time               | t <sub>SU; STO</sub> | SDA, SCL |            | 4.7  |      | μs   |

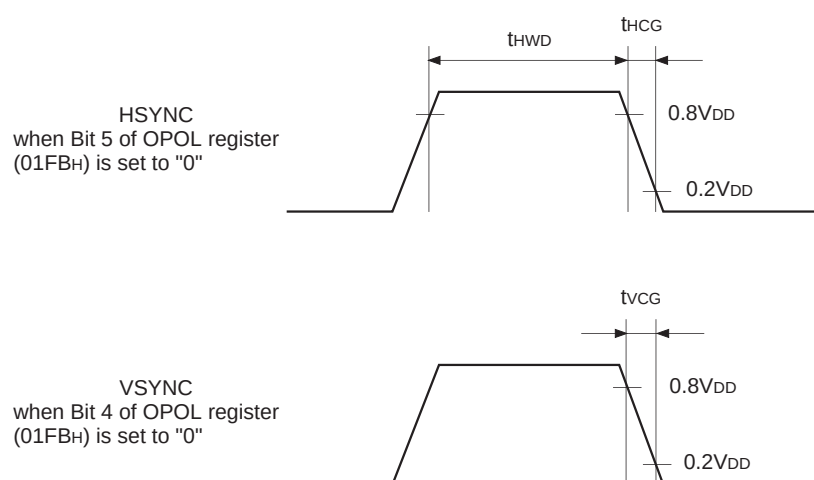
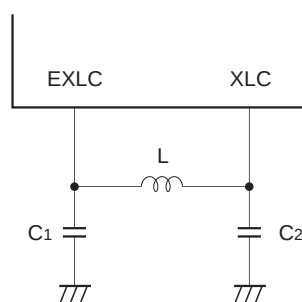
\*1 The data hold time does not take into consideration SCL rise time (300ns max.). Ensure that the data hold time exceeds 300ns.

**Fig. 9. I<sup>2</sup>C bus transfer timing****Fig. 10. Recommended circuit example for I<sup>2</sup>C device**

- Pull-up resistors must be connected to SDA0 (or SDA1) and SCL0 (or SCL1).
- Serial resistance (Rs = 300Ω and under) of SDA0 (or SDA1) and SCL0 (or SCL1) reduces spike noise caused by CRT flashover.

**(7) OSD (On-Screen Display) timing**(Ta = -10 to +75°C, V<sub>DD</sub> = 4.5 to 5.5V, V<sub>SS</sub> = 0V reference)

| Item                                 | Symbol           | Pins        | Condition | Min. | Max. | Unit |
|--------------------------------------|------------------|-------------|-----------|------|------|------|
| OSD clock frequency                  | f <sub>OSC</sub> | EXLC<br>XLC | Fig. 12   | 4    | 13   | MHz  |
| HSYNC pulse width                    | t <sub>HWD</sub> | HSYNC       | Fig. 11   | 1.2  |      | μs   |
| HSYNC after-edge rise time/fall time | t <sub>HCG</sub> | HSYNC       | Fig. 11   |      | 200  | ns   |
| VSYNC after-edge rise time/fall time | t <sub>VCG</sub> | VSYNC       | Fig. 11   |      | 1.0  | μs   |

**Fig. 11. OSC timing****Fig. 12. LC oscillation circuit example**

## Supplement



Fig. 13. Recommended Oscillation circuit

| Manufacturer             | Model        | fc (MHz) | C <sub>1</sub> (pF) | C <sub>2</sub> (pF) | Rd (Ω) | Circuit example |
|--------------------------|--------------|----------|---------------------|---------------------|--------|-----------------|
| MURATA MFG CO., LTD.     | CSA4.00MG    | 4.00     | 30                  | 30                  | 0      | (i)             |
|                          | CSA4.19MG    | 4.19     |                     |                     |        |                 |
|                          | CST4.00MGW*  | 4.00     |                     |                     |        | (ii)            |
|                          | CST4.19MGW*  | 4.19     |                     |                     |        |                 |
| RIVER ELETEC CORPORATION | HC-49/U03    | 4.00     | 10                  | 10                  | 0      | (i)             |
|                          |              | 4.19     |                     |                     |        |                 |
| KINSEKI LTD.             | HC-49/U (-S) | 4.00     | 18                  | 18                  | 0      |                 |
|                          |              | 4.19     |                     |                     |        |                 |

\* Indicates types with on-chip grounding capacitance (C<sub>1</sub> and C<sub>2</sub>).

## Product List

| Option item                | Mask                                                                                        | CXP852P32AS-1- □□□                  | CXP852P32AQ-1- □□□                  |
|----------------------------|---------------------------------------------------------------------------------------------|-------------------------------------|-------------------------------------|
| Package                    | 64-pin plastic SDIP/QFP                                                                     | 64-pin plastic SDIP                 | 64-pin plastic QFP                  |
| PROM capacitance           | 12K/16K bytes (CXP85112B/85116B)<br>20K/24K/28K/32K bytes (CXP85220A/85224A /85228A/85232A) | PROM 32K bytes                      | PROM 32K bytes                      |
| Reset pin pull-up resistor | Existent/Non-existent                                                                       | Existent                            | Existent                            |
| Power-on reset circuit     | Existent/Non-existent                                                                       | Existent                            | Existent                            |
| Font data                  | User specified                                                                              | User specified (PROM)* <sup>1</sup> | User specified (PROM)* <sup>1</sup> |

\*<sup>1</sup> The font data for the one-time PROM version is operated in the same way as the program writing.

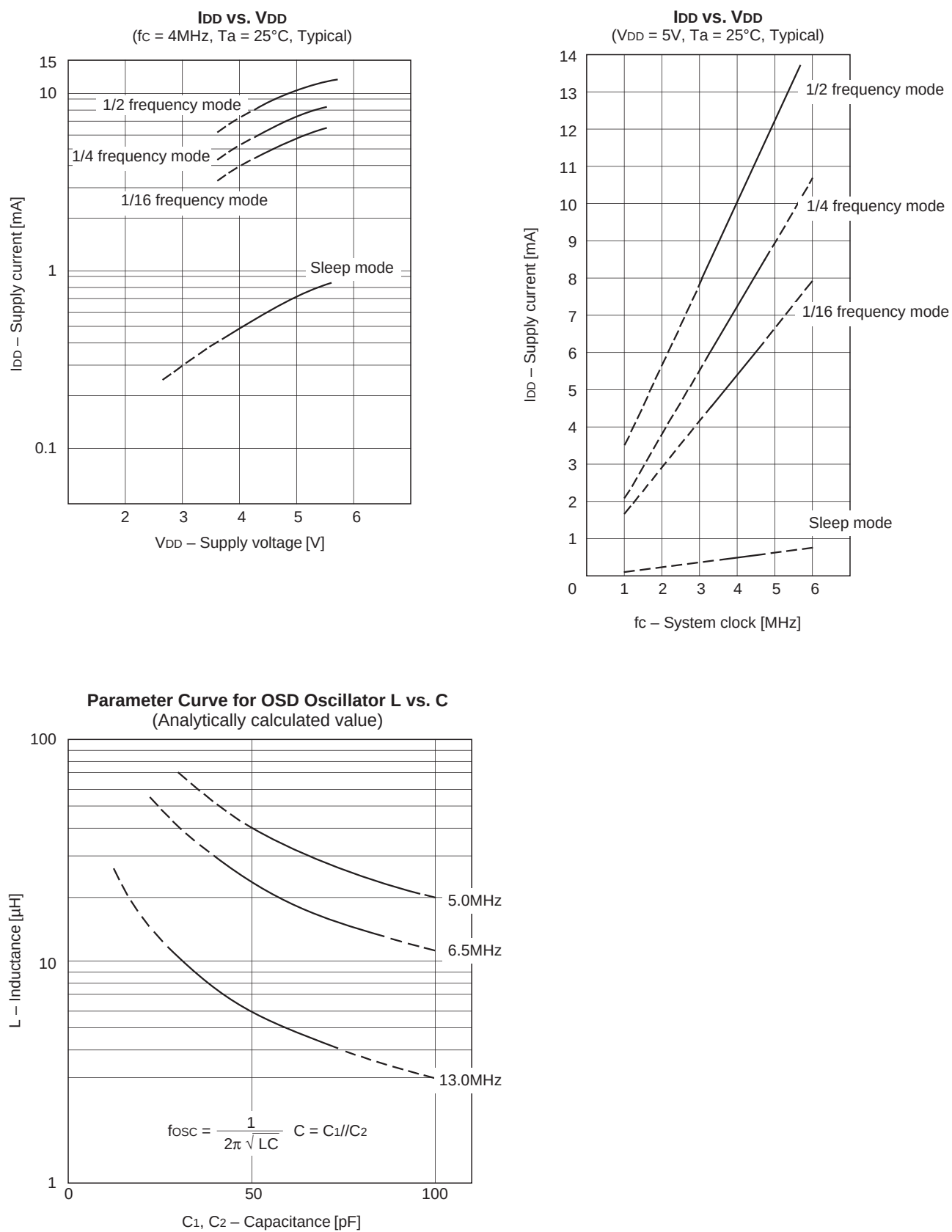
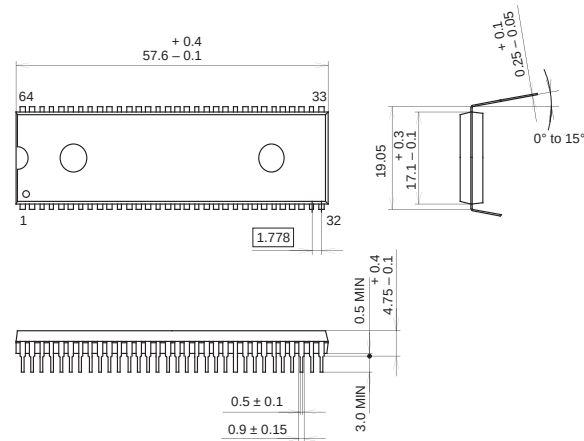


Fig. 14. Characteristics curves

Package Outline      Unit: mm

64PIN SDIP (PLASTIC)

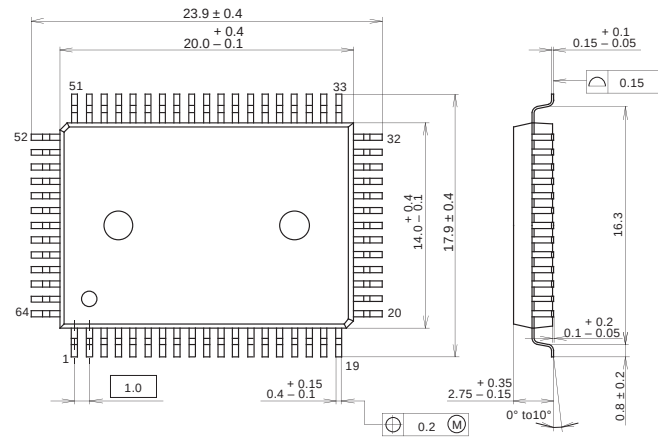


PACKAGE STRUCTURE

|            |                |
|------------|----------------|
| SONY CODE  | SDIP-64P-01    |
| EIAJ CODE  | SDIP064-P-0750 |
| JEDEC CODE |                |

|                  |                |
|------------------|----------------|
| PACKAGE MATERIAL | EPOXY RESIN    |
| LEAD TREATMENT   | SOLDER PLATING |
| LEAD MATERIAL    | 42 ALLOY       |
| PACKAGE MASS     | 8.6g           |

64PIN QFP(PLASTIC)



PACKAGE STRUCTURE

|            |               |
|------------|---------------|
| SONY CODE  | QFP-64P-L01   |
| EIAJ CODE  | QFP064-P-1420 |
| JEDEC CODE |               |

|                  |                          |
|------------------|--------------------------|
| PACKAGE MATERIAL | EPOXY RESIN              |
| LEAD TREATMENT   | SOLDER/PALLADIUM PLATING |
| LEAD MATERIAL    | 42/COPPER ALLOY          |
| PACKAGE MASS     | 1.5g                     |