19-2011; Rev 3; 4/05

EVALUATION KIT AVAILABLE

WCDMA Cellular Phone 600mA Buck Regulators

General Description

The MAX1820/MAX1821 low-dropout, pulse-width-modulated (PWM) DC-DC buck regulators are optimized to provide power to the power amplifier (PA) in WCDMA cell phones; however, they may be applied in many other applications where high efficiency is a priority. The supply voltage range is from 2.6V to 5.5V, and the guaranteed output current is 600mA; 1MHz PWM switching allows for small external components, while skip mode reduces quiescent current to 180µA with light loads.

The MAX1820 is dynamically controlled to provide varying output voltages from 0.4V to 3.4V. The circuit is designed such that the output voltage settles in <30µs for a full-scale change in voltage and current. The MAX1821 is set with external resistors to provide any fixed output voltage in the 1.25V to 5.5V range.

The MAX1820/MAX1821 include a low on-resistance internal MOSFET switch and synchronous rectifier to maximize efficiency and minimize external component count; 100% duty-cycle operation allows for low dropout of only 150mV at 600mA load, including the external inductor resistance. The devices are offered in 10-pin µMAX® and tiny 3 × 4 chip-scale (UCSP™) packages.

Applications

WCDMA Cell Phone Power Amplifiers
PDA, Palmtop, and Notebook Computers
Microprocessor Core Supplies
Digital Cameras
PCMCIA and Network Cards
Hand-Held Instruments

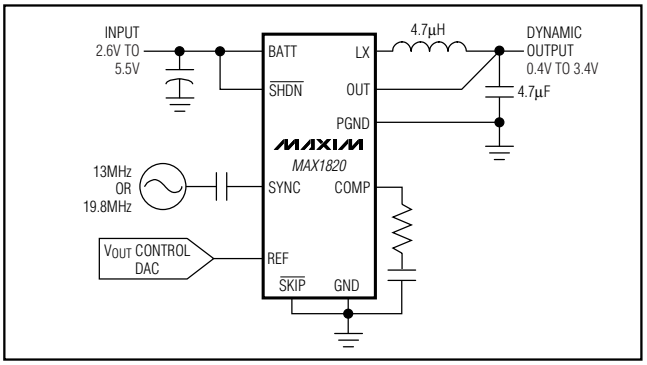
Typical Operating Circuits continued at end of data sheet.
Ordering Information continued at end of data sheet.
Pin Configurations appear at end of data sheet.

UCSP is a trademark of Maxim Integrated Products, Inc.
µMAX is a registered trademark of Maxim Integrated Products, Inc.

Features

- ♦ **Dynamically Adjustable Output from 0.4V to 3.4V (MAX1820)**
- ♦ **Programmable Output from 1.25V to 5.5V (MAX1821)**
- ♦ **SYNC to 13MHz External Clock (MAX1820X)**
- ♦ **SYNC to 19.8MHz External Clock (MAX1820Y)**
- ♦ **NO SYNC, Internal 1MHz Oscillator (MAX1820Z)**
- ♦ **Low Quiescent Current**
  180µA (typ) in Skip Mode
  0.1µA (typ) in Shutdown Mode
- ♦ **No External Schottky Diode Required**
- ♦ **600mA Guaranteed Output Current**
- ♦ **0% to 100% Duty-Cycle Operation**
- ♦ **150mV Dropout at 600mA Load (Including R_{DC} of External Inductor)**
- ♦ **µMAX or UCSP Packaging**

Typical Operating Circuits



Ordering Information

PART	SYNC FREQ (MHz)	OUTPUT VOLTAGE	TEMP RANGE	PIN-PACKAGE	UCSP MARK
MAX1820ZEBC*	No Sync	Dynamic	-40°C to +85°C	3 × 4 UCSP	AAB
MAX1820YEBC*	19.8	Dynamic	-40°C to +85°C	3 × 4 UCSP	AAL
MAX1820XEBC*	13	Dynamic	-40°C to +85°C	3 × 4 UCSP	AAM
MAX1820ZEUB	No Sync	Dynamic	-40°C to +85°C	10 µMAX	—
MAX1820YEUB	19.8	Dynamic	-40°C to +85°C	10 µMAX	—
MAX1820XEUB	13	Dynamic	-40°C to +85°C	10 µMAX	—

**UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. See the UCSP Reliability Notice in the UCSP Reliability section of this data sheet for more information.*

For pricing, delivery, and ordering information, please contact Maxim/Dallas Direct! at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

WCDMA Cellular Phone 600mA Buck Regulators

ABSOLUTE MAXIMUM RATINGS

BATT, OUT (FB), $\overline{SHDN}$, SYNC, $\overline{SKIP}$, REF to GND .....-0.3V to +6.0V
PGND to GND .....-0.3V to +0.3V
LX, COMP to GND.....-0.3V to (V_{BATT} + 0.3V)
Output Short-Circuit Duration .....Infinite
Continuous Power Dissipation (T_A = +70°C)
3 × 4 UCSP (derate 10.4mW/°C above +70°C).....832mW
10-Pin µMAX (derate 5.6mW/°C above +70°C).....444mW
Operating Temperature Range .....-40°C to +85°C
Junction Temperature.....+150°C
Storage Temperature Ranges
3 × 4 UCSP .....-40°C to +150°C
10-Pin µMAX.....-65°C to +150°C
Solder Profile (UCSP) .....(Note 1)
Lead Temperature (soldering, 10s) .....+300°C

Note 1: For UCSP solder profile information, visit www.maxim-ic.com/1st_pages/UCSP.htm.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{BATT} = 3.6V, $\overline{SHDN}$ = BATT, $\overline{SKIP}$ = SYNC = GND, V_{REF} = 1.25V (MAX1820 only), **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input BATT Voltage	V_{IN}		2.6		5.5	V
Undervoltage Lockout Threshold	V_{UVLO}	V_{BATT} rising, 1% hysteresis	2.20	2.35	2.55	V
Quiescent Current	I_Q	$\overline{SKIP}$ = GND (MAX1820Z/MAX1821)		180	300	µA
		$\overline{SKIP}$ = BATT, no switching		450	2000	
		$\overline{SKIP}$ = GND (MAX1820Y, MAX1820X, and MAX1821X)		240	360	
		$\overline{SKIP}$ = BATT, 1MHz switching		3300		
Quiescent Current in Dropout		$\overline{SKIP}$ = GND		530	1000	µA
		$\overline{SKIP}$ = BATT, no switching		550	1000	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND		0.1	6	µA
ERROR AMPLIFIER						
OUT Voltage Accuracy (MAX1820)	V_{OUT}	V_{REF} = 1.932 ±0.005V, load = 0 to 600mA, $\overline{SKIP}$ = BATT or GND	3.33	3.4	3.47	V
		V_{REF} = 0.227 ±0.005V, load = 0 to 30mA, $\overline{SKIP}$ = BATT, $V_{BATT} \le$ 4.2V	0.35	0.40	0.45	
OUT Input Resistance (MAX1820)	R_{OUT}		250	400		kΩ
REF Input Current (MAX1820)	I_{REF}			0.1	1	µA
FB Voltage Accuracy (MAX1821)	V_{FB}	FB = COMP	1.225	1.25	1.275	V
FB Input Current (MAX1821)	I_{FB}	V_{FB} = 1.4V		0.01	50	nA
Transconductance	g_m		30	50	85	µS
COMP Clamp Low Voltage			0.2	0.45	1.0	V
COMP Clamp High Voltage			2.04	2.15	2.28	V

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = 3.6V, $\overline{SHDN}$ = BATT, $\overline{SKIP}$ = SYNC = GND, V_{REF} = 1.25V (MAX1820 only), **T_A = 0°C to +85°C**, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
CONTROLLER						
P-Channel On-Resistance	P_{RDS}	I_{LX} = 180mA, V_{BATT} = 3.6V		0.15	0.3	Ω
		I_{LX} = 180mA, V_{BATT} = 2.6V		0.2		
N-Channel On-Resistance	N_{RDS}	I_{LX} = 180mA, V_{BATT} = 3.6V		0.2	0.35	Ω
		I_{LX} = 180mA, V_{BATT} = 2.6V		0.3		
Current-Sense Transresistance	R_{CS}		0.25	0.50	0.75	V/A
P-Channel Current-Limit Threshold		Duty factor = 100%	0.75	1.2	1.55	A
P-Channel Pulse-Skipping Current Threshold		$\overline{SKIP}$ = GND	0.04	0.13	0.24	A
N-Channel Current-Limit Threshold		$\overline{SKIP}$ = BATT	-1.6	-0.85	-0.45	A
		$\overline{SKIP}$ = GND	0.02	0.08	0.14	
LX Leakage Current	I_{LX}	V_{BATT} = 5.5V, LX = GND or BATT	-1	0.1	1	µA
Maximum Duty Cycle	$duty_{MAX}$		100			%
Minimum Duty Cycle	$duty_{MIN}$	$\overline{SKIP}$ = GND			0	%
		$\overline{SKIP}$ = BATT, V_{BATT} = 4.2V_{P-P}			10	
SYNC AND OSCILLATOR						
SYNC Divide Ratio (MAX1820X)		SYNC = sine wave, SYNC input = 200mV_{P-P}	13		13	Hz/Hz
		SYNC = sine wave, SYNC input = 800mV_{P-P}	13		13	
SYNC Capture Range (MAX1820X)		SYNC = sine wave, AC-coupled, SYNC input = 500mV_{P-P}	10	13	16	MHz
SYNC Leakage Current Frequency	I_{SYNC}	V_{SYNC} = 1V (MAX1820Z, MAX1821)	-1		+1	µA
		V_{SYNC} = 1V (MAX1820X, MAX1820Y, and MAX1821X)	-5		+5	
SYNC Divide Ratio (MAX1820Y)		SYNC = sine wave, SYNC input = 200mV_{P-P}	18		18	Hz/Hz
		SYNC = sine wave, SYNC input = 800mV_{P-P}	18		18	
SYNC Capture Range (MAX1820Y)		SYNC = sine wave, AC-coupled, SYNC input = 500mV_{P-P}	15	19.8	21	MHz
Internal Oscillator Frequency (MAX1820Z, MAX1821)	f_{OSC}	SYNC = GND	0.8	1	1.2	MHz
LOGIC INPUTS ($\overline{SKIP}$, $\overline{SHDN}$)						
Logic Input High	V_{IH}		1.6			V
Logic Input Low	V_{IL}				0.4	V
Logic Input Current			-1	0.1	1	µA

WCDMA Cellular Phone 600mA Buck Regulators

ELECTRICAL CHARACTERISTICS

(V_{BATT} = 3.6V, $\overline{SHDN}$ = BATT, $\overline{SKIP}$ = SYNC = GND, V_{REF} = 1.25V (MAX1820 only), **T_A = -40°C to +85°C**, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Input BATT Voltage	V_{IN}		2.6	5.5	V
Undervoltage Lockout Threshold	V_{UVLO}	V_{BATT} rising, 1% hysteresis	2.15	2.55	V
Quiescent Current	I_Q	$\overline{SKIP}$ = GND (MAX1820Z, MAX1821)		300	µA
		$\overline{SKIP}$ = GND (MAX1820X, MAX1820Y, and MAX1821X)		360	
		$\overline{SKIP}$ = BATT, no switching		2000	
Quiescent Current in Dropout		$\overline{SKIP}$ = GND		1000	µA
		$\overline{SKIP}$ = BATT, no switching		1000	
Shutdown Supply Current	$I_{\overline{SHDN}}$	$\overline{SHDN}$ = GND		6	µA
ERROR AMPLIFIER					
OUT Voltage Accuracy (MAX1820)	V_{OUT}	V_{REF} = 1.932 ±0.005V, load = 0 to 600mA, $\overline{SKIP}$ = BATT or GND	3.33	3.47	V
		V_{REF} = 0.227 ±0.005V, load = 0 to 30mA, $\overline{SKIP}$ = BATT, $V_{BATT} \le 4.2V$	0.35	0.45	
OUT Input Resistance (MAX1820)	R_{OUT}		250		kΩ
REF Input Current (MAX1820)	I_{REF}			1	µA
FB Voltage Accuracy (MAX1821)	V_{FB}	FB = COMP	1.225	1.275	V
FB Input Current (MAX1821)	I_{FB}	V_{FB} = 1.4V		50	nA
Transconductance	g_m		30	85	µS
COMP Clamp Low Voltage			0.2	1.0	V
COMP Clamp High Voltage			2.04	2.28	V
CONTROLLER					
P-Channel On-Resistance	P_{RDS}	I_{LX} = 180mA, V_{BATT} = 3.6V		0.3	Ω
N-Channel On-Resistance	N_{RDS}	I_{LX} = 180mA, V_{BATT} = 3.6V		0.35	Ω
Current-Sense Transresistance	R_{CS}		0.25	0.75	V/A
P-Channel Current-Limit Threshold		Duty factor = 100%	0.75	1.55	A
P-Channel Pulse-Skipping Current Threshold		$\overline{SKIP}$ = GND	0.04	0.24	A
N-Channel Current-Limit Threshold		$\overline{SKIP}$ = BATT	-1.6	-0.45	A
		$\overline{SKIP}$ = GND	0.01	0.14	

ELECTRICAL CHARACTERISTICS (continued)

(V_{BATT} = 3.6V, $\overline{SHDN}$ = BATT, $\overline{SKIP}$ = SYNC = GND, V_{REF} = 1.25V (MAX1820 only), **T_A = -40°C to +85°C**, unless otherwise noted.) (Notes 2, 3)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
LX Leakage Current	I_{LX}	V_{BATT} = 5.5V, LX = GND or BATT	-1	1	µA
Maximum Duty Cycle	$duty_{MAX}$		100		%
Minimum Duty Cycle	$duty_{MIN}$	$\overline{SKIP}$ = GND		0	%
		$\overline{SKIP}$ = BATT, V_{BATT} = 4.2V		10	
SYNC AND OSCILLATOR					
SYNC Divide Ratio (MAX1820X)		SYNC = sine wave, SYNC input = 200mV_{P-P}	13	13	Hz/Hz
		SYNC = sine wave, SYNC input = 800mV_{P-P}	13	13	
SYNC Capture Range (MAX1820X)		SYNC = sine wave, AC-coupled, SYNC input = 500mV_{P-P}	10	16	MHz
SYNC Divide Ratio (MAX1820Y)		SYNC = sine wave, SYNC input = 200mV_{P-P}	18	18	Hz/Hz
		SYNC = sine wave, SYNC input = 800mV_{P-P}	18	18	
SYNC Capture Range (MAX1820Y)		SYNC = sine wave, AC-coupled, SYNC input = 500mV_{P-P}	15	21	MHz
SYNC Leakage Current	I_{SYNC}	V_{SYNC} = IV (MAX1820Z, MAX1821)	-1	+1	µA
		V_{SYNC} = IV (MAX1820X, MAX1820Y, and MAX1821X)	-5	+5	
Internal Oscillator Frequency (MAX1820Z, MAX1821)	f_{OSC}	SYNC = GND	0.8	1.2	MHz
LOGIC INPUTS ($\overline{SKIP}$, $\overline{SHDN}$)					
Logic Input High	V_{IH}		1.6		V
Logic Input Low	V_{IL}			0.4	V
Logic Input Current				1	µA

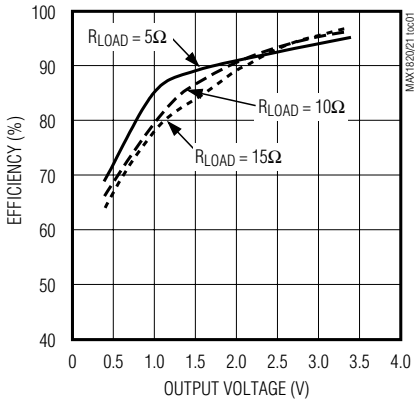
Note 2: Limits are 100% production tested at T_A = +25°C for UCSP parts. Limits over the entire operating temperature range are guaranteed by design and characterization but are not production tested.

Note 3: Specifications to -40°C are guaranteed by design and not subject to production test.

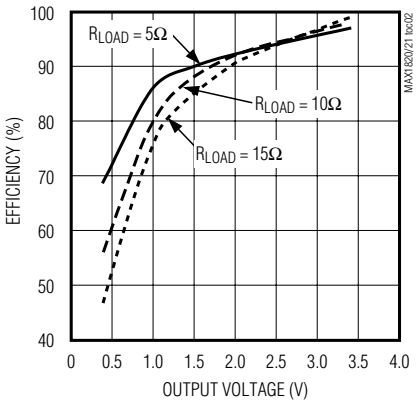
Typical Operating Characteristics

(T_A = +25°C, unless otherwise noted.)

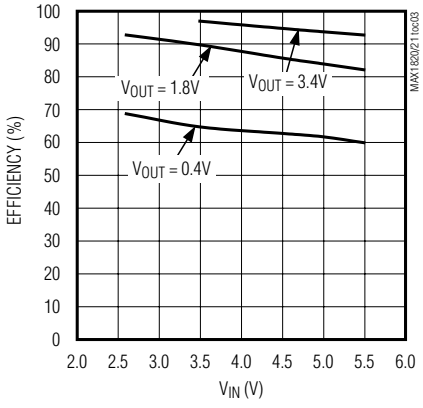
EFFICIENCY vs. OUTPUT VOLTAGE (NORMAL MODE, V_{IN} = 3.6V)



EFFICIENCY vs. OUTPUT VOLTAGE (PWM MODE, V_{IN} = 3.6V)



EFFICIENCY vs. INPUT VOLTAGE NORMAL MODE, R_{LOAD} = 10Ω

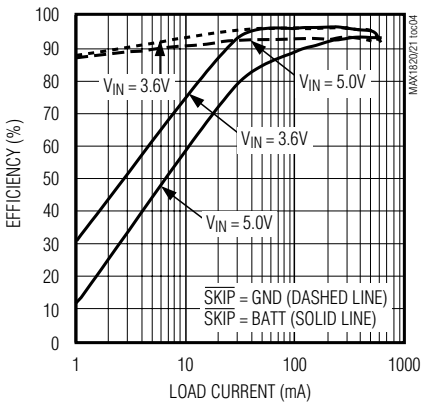


WCDMA Cellular Phone 600mA Buck Regulators

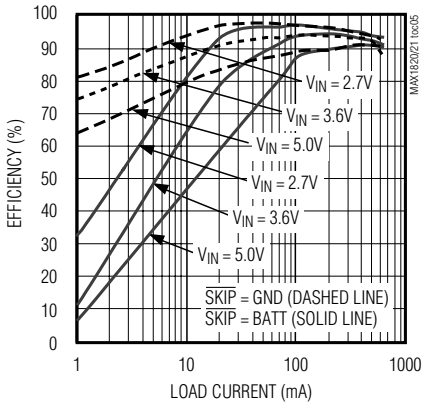
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

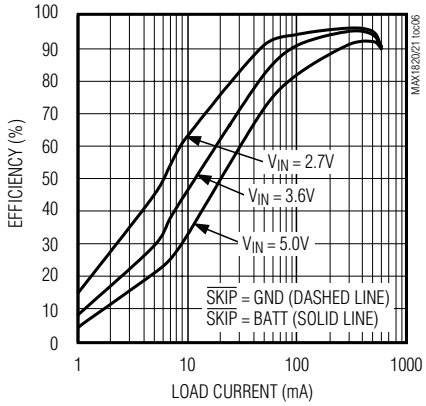
MAX1821 EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 3.3V)



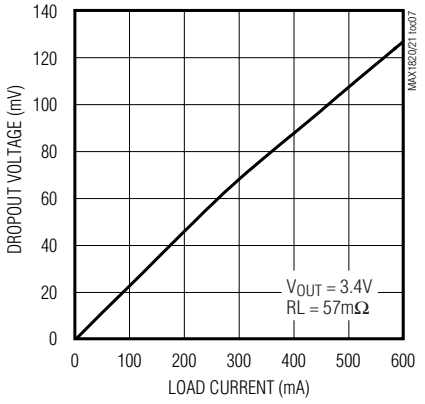
MAX1821 EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 2.5V)



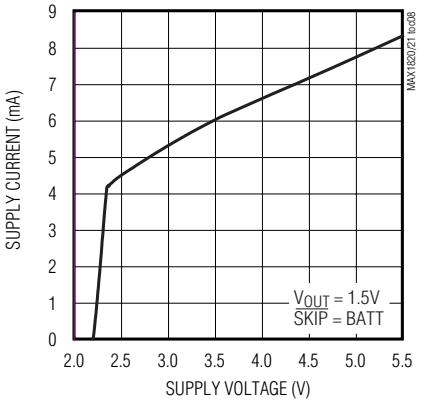
MAX1821 EFFICIENCY vs. LOAD CURRENT (V_{OUT} = 1.5V)



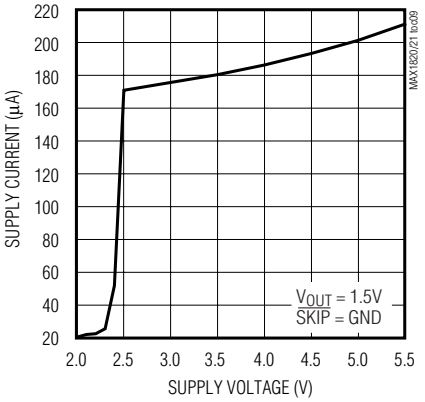
DROPOUT VOLTAGE vs. LOAD CURRENT



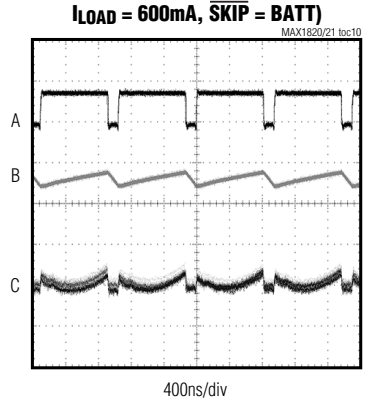
SUPPLY CURRENT vs. SUPPLY VOLTAGE



SUPPLY CURRENT vs. SUPPLY VOLTAGE

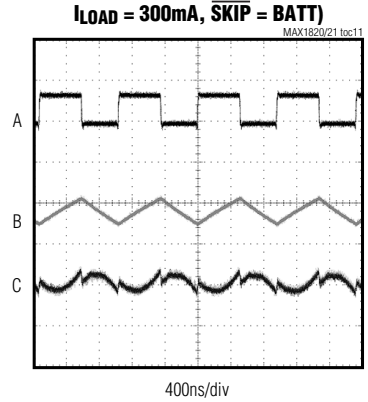


HEAVY-LOAD SWITCHING WAVEFORMS (V_{IN} = 3.8V, V_{OUT} = 3.4V, I_{LOAD} = 600mA, $\overline{SKIP}$ = BATT)



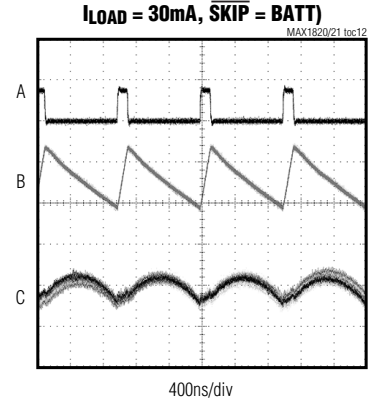
A: V_{LX}, 5V/div
B: INDUCTOR CURRENT, 500mA/div
C: V_{OUT} (AC-COUPLED), 5mV/div

MEDIUM-LOAD SWITCHING WAVEFORMS (V_{IN} = 3.8V, V_{OUT} = 1.8V, I_{LOAD} = 300mA, $\overline{SKIP}$ = BATT)



A: V_{LX}, 5V/div
B: INDUCTOR CURRENT, 500mA/div
C: V_{OUT} (AC-COUPLED), 5mV/div

LIGHT-LOAD PWM SWITCHING WAVEFORMS (V_{IN} = 3.8V, V_{OUT} = 0.45V, I_{LOAD} = 30mA, $\overline{SKIP}$ = BATT)

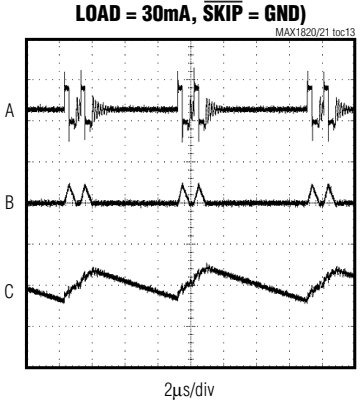


A: V_{LX}, 5V/div
B: INDUCTOR CURRENT, 100mA/div
C: V_{OUT} (AC-COUPLED), 5mV/div

Typical Operating Characteristics (continued)

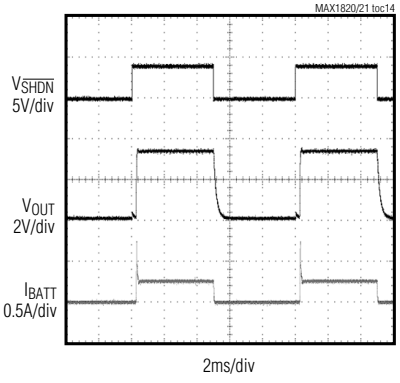
(T_A = +25°C, unless otherwise noted.)

LIGHT-LOAD SKIP-SWITCHING WAVEFORMS (V_{IN} = 4.2V, V_{OUT} = 1.5V, LOAD = 30mA, $\overline{SKIP}$ = GND)

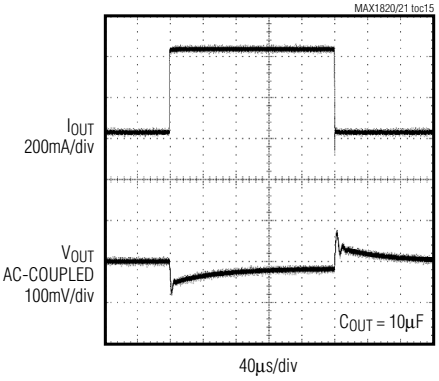


A: V_{LX}, 5V/div
B: INDUCTOR CURRENT, 500mA/div
C: V_{OUT} (AC-COUPLED), 20mV/div

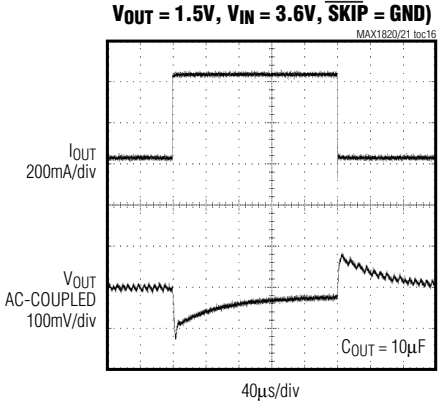
EXITING AND ENTERING SHUTDOWN (V_{IN} = 3.6V, V_{OUT} = 3.4V, R_{LOAD} = 15Ω)



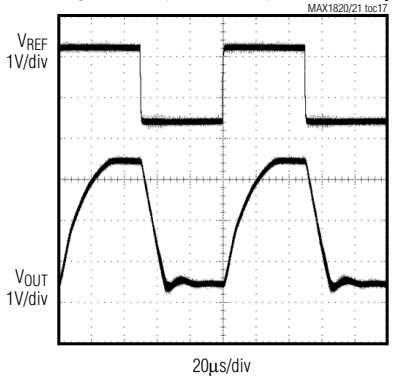
LOAD TRANSIENT (I_{LOAD} = 20mA TO 420mA, V_{OUT} = 1.5V, V_{IN} = 3.6V, $\overline{SKIP}$ = BATT)



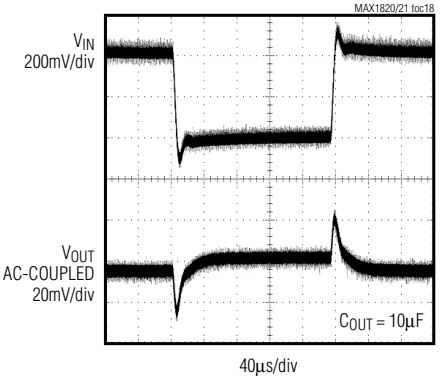
LOAD TRANSIENT (I_{LOAD} = 20mA TO 420mA, V_{OUT} = 1.5V, V_{IN} = 3.6V, $\overline{SKIP}$ = GND)



MAX1820 REF TRANSIENT (V_{REF} = 0.23V TO 1.932V, R_{LOAD} = 10Ω, V_{IN} = 3.6V, $\overline{SKIP}$ = BATT)



LINE TRANSIENT (V_{IN} = 3.6V TO 4.0V, V_{OUT} = 1.5V, I_{LOAD} = 300mA)

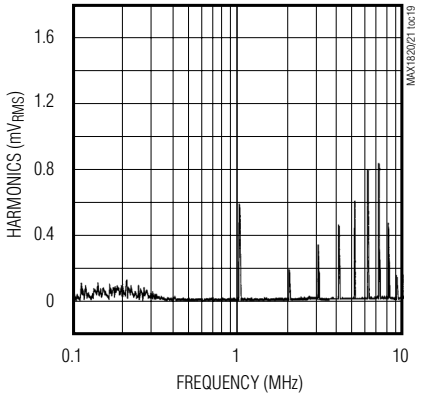


WCDMA Cellular Phone 600mA Buck Regulators

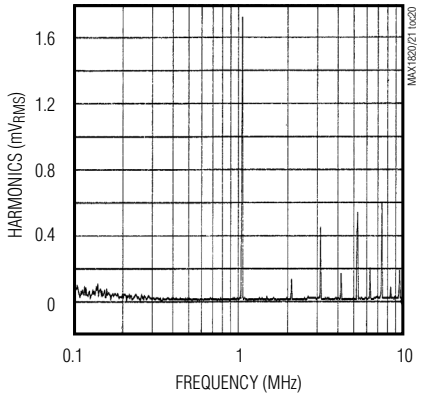
Typical Operating Characteristics (continued)

(T_A = +25°C, unless otherwise noted.)

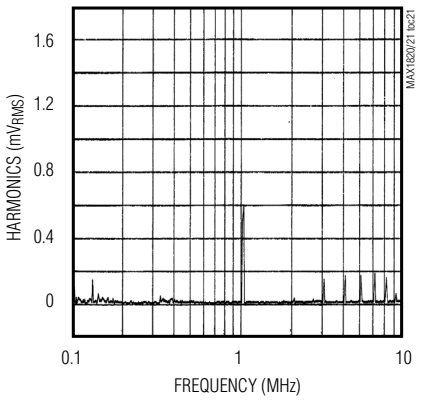
OUTPUT SWITCHING HARMONICS vs. FREQUENCY (V_{IN} = 3.8V, V_{OUT} = 3.4V, I_{LOAD} = 600mA)



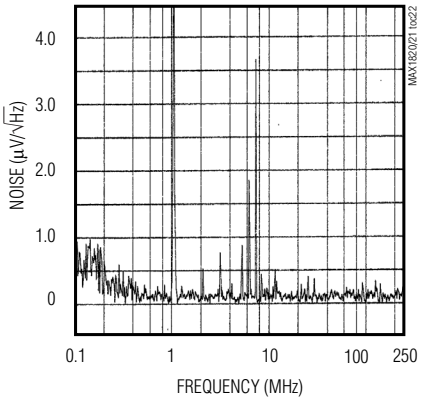
OUTPUT SWITCHING HARMONICS vs. FREQUENCY (V_{IN} = 3.8V, V_{OUT} = 1.8V, I_{LOAD} = 300mA)



OUTPUT SWITCHING HARMONICS vs. FREQUENCY (V_{IN} = 4.2V, V_{OUT} = 0.4V, I_{LOAD} = 30mA)



OUTPUT NOISE (V_{IN} = 3.6V, V_{OUT} = 1.8V, I_{OUT} = 300mA)



Pin Description

PIN				NAME	FUNCTION
MAX1820 UCSP	MAX1820 µMAX	MAX1821 UCSP	MAX1821 µMAX		
A1	1	A1	1	$\overline{SKIP}$	PWM/Skip-Mode Input. Drive with logic 0 to use PWM at medium and heavy loads and pulse skipping at light loads. Drive with logic 1 to force PWM at all loads.
A2	2	A2	2	COMP	Compensation. Typically, connect an 82kΩ (for MAX1821) or 43kΩ (for MAX1820) series resistor and 330pF capacitor from this pin to GND to stabilize the regulator.
A3	3	—	—	OUT	Output Voltage Sense Input. Connect OUT directly to the output.

Pin Description (continued)

PIN				NAME	FUNCTION
MAX1820 UCSP	MAX1820 µMAX	MAX1821 UCSP	MAX1821 µMAX		
—	—	A3	3	FB	Output Feedback Sense Input. To set the output voltage, connect FB to the center of an external resistive divider between the output and GND. FB voltage regulates to 1.25V.
A4	4	—	—	REF	External Reference Input. Connect REF to the output of a D/A converter for dynamic adjustment of the output voltage. REF-to-OUT gain is 1.76.
—	—	A4	4	REF	Internal Reference Bypass. Connect a 0.047µF capacitor from REF to GND.
B4	5	B4	5	GND	Ground
C4	6	C4	6	PGND	Power Ground
C3	7	C3	7	LX	Inductor Connection. LX connects to the drains of the internal power MOSFETs. LX is high impedance in shutdown mode.
C2	8	C2	8	BATT	Supply Voltage Input. Connect BATT to a 2.6V to 5.5V source. Bypass BATT to PGND with a low-ESR 10µF capacitor.
C1	9	C1	9	$\overline{SHDN}$	Active-Low, Shutdown Control Input
B1	10	B1	10	SYNC	Clock Synchronization Input. Drive SYNC with a 13MHz (MAX1820X, MAX1821X) or 19.8MHz (MAX1820Y) AC-coupled sine-wave input to synchronize power switching at 1MHz. MAX1820Z and MAX1821 do not have SYNC capability. Connect SYNC to GND to use the internally generated, free-running 1MHz clock. MAX1820Z and MAX1821 SYNC pin must be connected to GND.

Detailed Description

The MAX1820/MAX1821 PWM step-down DC-DC converters are optimized for low-voltage, battery-powered applications where high efficiency and small size are priorities. The MAX1821 is a general-purpose device that uses external feedback resistors to set the output voltage from 1.25V to V_{BATT}, and the MAX1820 is specifically intended to power a linear PA in WCDMA handsets. An analog control signal dynamically adjusts the MAX1820's output voltage from 0.4V to 3.4V with a settling time <30µs.

The MAX1820/MAX1821 operate at a high 1MHz switching frequency that reduces external component size. Each device includes an internal synchronous rectifier that provides for high efficiency and eliminates the need for an external Schottky diode. The normal operating mode uses constant-frequency PWM switching at medium and heavy loads, and automatically pulse skips at light loads to reduce supply current and extend battery life. An additional forced PWM mode (with optional external synchronization) switches at a constant frequency, regardless of load, to provide a well-controlled spectrum in noise-sensitive applications. Battery life is maximized by low-dropout operation at 100% duty-cycle and a 0.1µA (typ) logic-controlled shutdown mode.

PWM Control

The MAX1820/MAX1821 use a slope-compensated, current-mode PWM controller capable of achieving 100% duty cycle. The current-mode control design is capable of minimum duty cycles of less than 10%, ensuring a constant switching frequency with outputs as low as 0.4V when powered from a single lithium-ion (Li+) cell. Current-mode feedback provides stable switching and cycle-by-cycle current limiting for superior load and line response and protection of the internal MOSFET and synchronous rectifier. The output voltage is regulated by switching at a constant frequency and then modulating the power transferred to the load dur-

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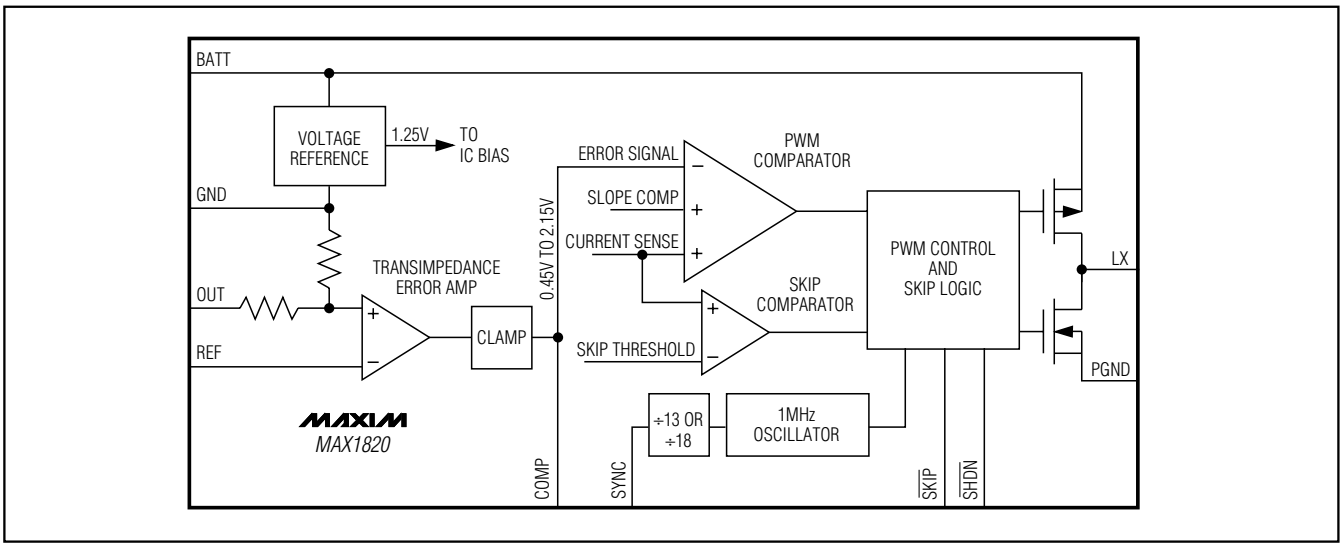


Figure 1. MAX1820 Simplified Functional Diagram (No SYNC for MAX1820Z)

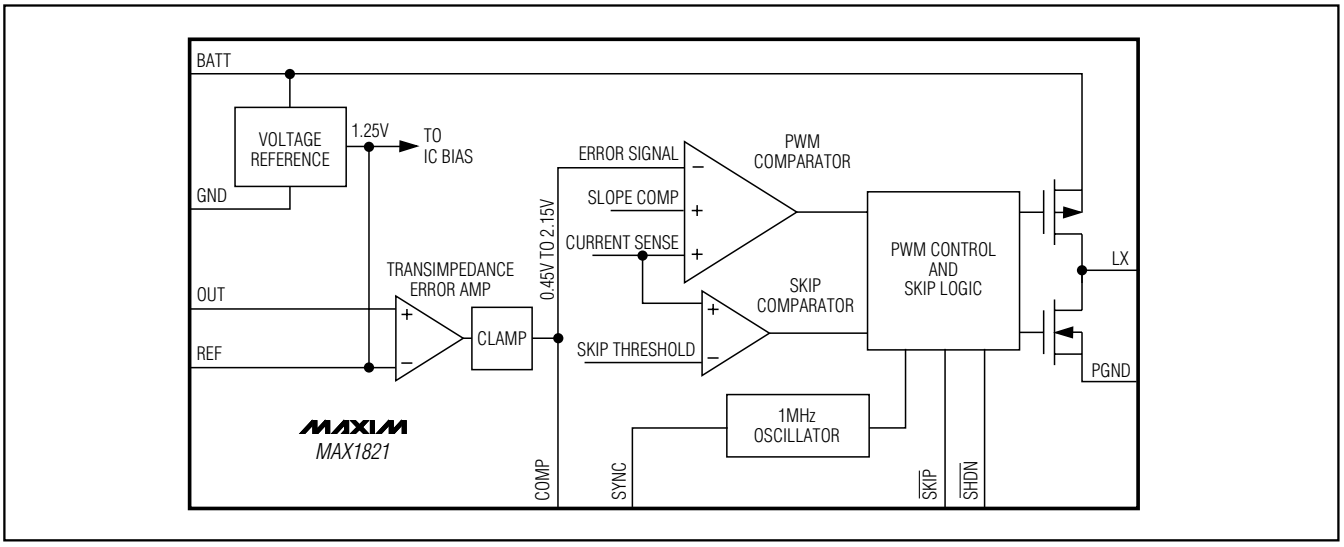


Figure 2. MAX1821 Simplified Functional Diagram (No SYNC for MAX1821)

ing each cycle, using the PWM comparator. The power transferred to the load is adjusted by changes in the inductor peak current limit during the first half of each cycle, based on the output error voltage.

A new cycle begins at each falling edge of the internal oscillator. The controller turns on the P-channel MOSFET to increase the inductor current, and the slope compensation block initiates a new reference current ramp that is summed with the internal P-channel MOSFET current (Figures 1 and 2).

The second half of the cycle begins when the reference ramp is greater than the error voltage. The P-channel MOSFET is turned off, the synchronous rectifier is turned on, and inductor current continues to flow to the output capacitor. The output capacitor stores charge when the current is high and releases it when the inductor current is low, smoothing the voltage across

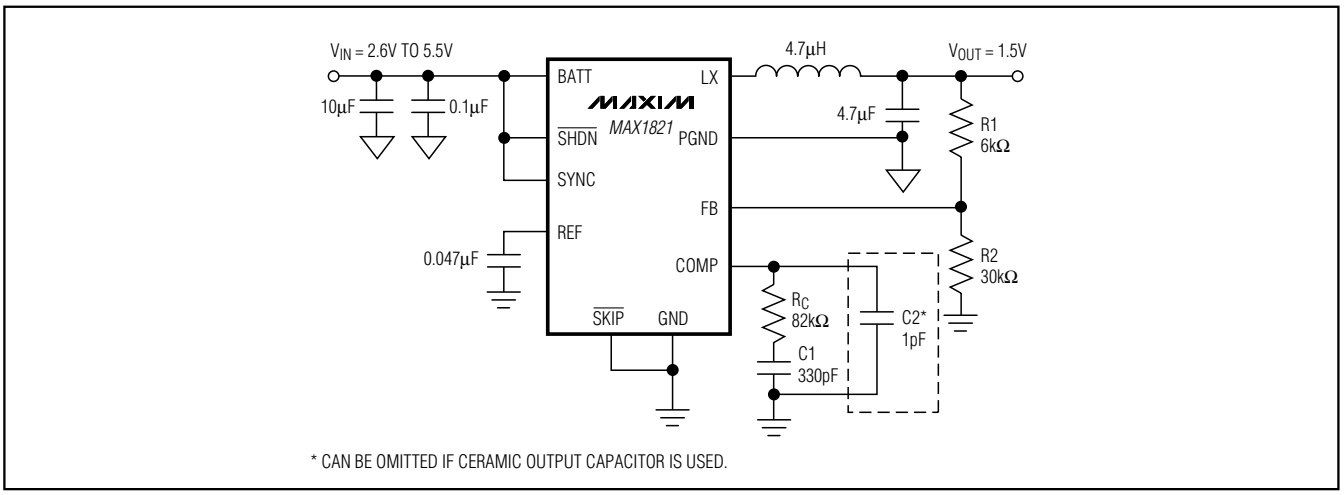


Figure 3. Standard Operating Circuit

the load. The duty cycle of a buck step-down converter is ideally a ratio of the output voltage to input voltage in steady-state condition.

The MAX1820/MAX1821 have internal switch current limits of 1.2A (typ). If I_{LX} exceeds this maximum, the high-side FET turns off and the synchronous rectifier turns on. This lowers the duty cycle and causes the output voltage to droop as long as the load current remains excessive. There is also a synchronous rectifier current limit of -0.85A when the device is operating in forced PWM mode (see the *Forced PWM Operation* section). If the negative current limit is exceeded, the synchronus rectifier is turned off, and the inductor current continues to flow through its body diode until the beginning of the next cycle or the inductor current drops to zero. This means there is a limit on how much current the device is allowed to shuttle in response to output power reduction.

Normal Mode Operation

Connecting $\overline{SKIP}$ to GND enables MAX1820/MAX1821 normal operation (Figure 3). This allows automatic PWM control at medium and heavy loads and skip mode at light loads to improve efficiency and reduce quiescent current to 180µA. Operating in normal mode also allows the MAX1820/MAX1821 to pulse skip when the peak inductor current drops below 130mA, corresponding to a load current of approximately 65mA.

During skip operation, the MAX1820/MAX1821 switch only as needed to service the load, reducing the switching frequency and associated losses in the internal switch, the synchronous rectifier, and the external inductor.

There are three steady-state operating conditions for the MAX1820/MAX1821 in normal mode. The device performs in continuous conduction for heavy loads in a manner identical to forced PWM mode. The inductor current becomes discontinuous at medium loads, requiring the synchronous rectifier to be turned off before the end of a cycle as the inductor current reaches zero. The device enters into skip mode when the converter output voltage exceeds its regulation limit before the inductor current reaches its skip threshold level.

During skip mode, a switching cycle initiates when the output voltage has dropped out of regulation. The P-channel MOSFET switch turns on and conducts current to the output-filter capacitor and load until the inductor current reaches the skip peak current limit. Then the main switch turns off, and the magnetic field in the inductor collapses, while current flows through the synchronous rectifier to the output filter capacitor and the load. The synchronous rectifier is turned off when the inductor current reaches zero. The MAX1820/ MAX1821 wait until the skip comparator senses a low output voltage again.

Forced PWM Operation

Connect $\overline{SKIP}$ to BATT for forced PWM operation. Forced PWM operation is desirable in sensitive RF and data-acquisition applications to ensure that switching harmonics do not interfere with sensitive IF and data-sampling frequencies. A minimum load is not required during forced PWM operation since the synchronous rectifier passes reverse-inductor current as needed to allow constant-frequency operation with no load.

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Forced PWM operation uses higher supply current with no load (3.3mA typ) compared to skip mode.

100% Duty-Cycle Operation

The on-time can exceed one internal oscillator cycle, which permits operation up to 100% duty cycle. As the input voltage drops, the duty cycle increases until the P-channel MOSFET is held on continuously. Dropout voltage in 100% duty cycle is the output current multiplied by the on-resistance of the internal switch and inductor, approximately 150mV (I_{OUT} = 600mA). Near dropout, the on-time may exceed one PWM clock cycle; therefore, small-amplitude subharmonic ripple may occur.

COMP Clamp

The MAX1820/MAX1821 compensation network has a 0.45V to 2.15V error regulation range. The clamp prevents COMP from rising too high or falling too low to optimize transient response.

Dropout

Dropout occurs when the input voltage is less than the desired output voltage plus the IR drops in the circuit components. The duty cycle is 100% during this condition, and the main switch remains on, continuously delivering current to the output up to the current limit. IR drops in the circuit are primarily caused by the on-resistance of the main switch and the resistance in the inductor.

During dropout, the high-side P-channel MOSFET turns on, and the controller enters a low-current consumption mode. Every 6µs (6 cycles), the MAX1820/MAX1821 check to see if the device is still in dropout. The device remains in this mode until the MAX1820/MAX1821 are no longer in dropout.

Undervoltage Lockout (UVLO)

The MAX1820/MAX1821 do not operate with battery voltages below the UVLO threshold of 2.35V (typ). The BATT input remains high impedance until the supply voltage exceeds the UVLO threshold. This guarantees the integrity of the output voltage regulation and prevents excessive current during startup and as the battery supply voltage drops during usage.

Synchronous Rectification

An N-channel synchronous rectifier eliminates the need for an external Schottky diode and improves efficiency. The synchronous rectifier turns on during the second half of each cycle (off-time). During this time, the voltage across the inductor is reversed, and the inductor current falls. In normal mode, the synchronous rectifier is turned off when either the output falls out of regulation (and another on-time begins) or when the inductor current approaches zero. In forced PWM mode, the synchronous rectifier remains active until the beginning of a new cycle.

SYNC Input and Frequency Control

The MAX1820Z and MAX1821 internal oscillator is set to a fixed 1MHz switching frequency. The MAX1820Z and MAX1821 do not have synchronizing capability and the SYNC pin must be connected to GND. The MAX1820Y, MAX1820X, and MAX1821X are capable of synchronizing to external signals. For external synchronization, drive the SYNC pin with a 13MHz (MAX1820X and MAX1821X) or 19.8MHz (MAX1820Y) AC-coupled sine wave. SYNC has a perfect 13:1 (MAX1820X and MAX1821X) or 18:1 (MAX1820Y) clock divider for 1MHz (MAX1820X and MAX1821X) or 1.1MHz (MAX1820Y) switching from common system clocks. The input frequency range for SYNC is 10MHz to 16MHz (MAX1820X, MAX1821X) or 15MHz to 21MHz (MAX1820Y). Connect SYNC to GND to use the internal free-running oscillator at 1MHz.

Shutdown Mode

Drive $\overline{SHDN}$ to GND to place the MAX1820/MAX1821 in shutdown mode. In shutdown, the reference, control circuitry, internal switching MOSFET, and the synchronous rectifier turn off, reducing the supply current to 0.1µA, and the output goes high impedance. Connect $\overline{SHDN}$ to BATT for normal operation.

Current-Sense Comparators

The MAX1820/MAX1821 use several internal current-sense comparators. In PWM operation, the PWM comparator terminates the cycle-by-cycle on-time (Figures 1 and 2) and provides improved load and line response. This allows tighter specification of the inductor-saturation current limit to reduce inductor cost. A second current-sense comparator used across the P-channel switch controls entry into skip mode. A third current-sense comparator monitors current through the internal N-channel MOSFET to prevent excessive reverse currents and determine when to turn off the synchronous rectifier. A fourth comparator used at the P-channel MOSFET detects overcurrent. This protects the system, external components, and internal MOSFETs under overload conditions.

Applications Information

Setting the Output Voltage (MAX1820)

The MAX1820 is optimized for highest system efficiency when applying power to a linear PA in WCDMA handsets. When transmitting at less than full power, the supply voltage to the PA is reduced (from 3.4V to as low as 0.4V) to greatly reduce battery current. Figure 4 shows the typical WCDMA PA load profile. The use of a DC-DC converter such as the MAX1820 dramatically reduces battery drain in these applications.

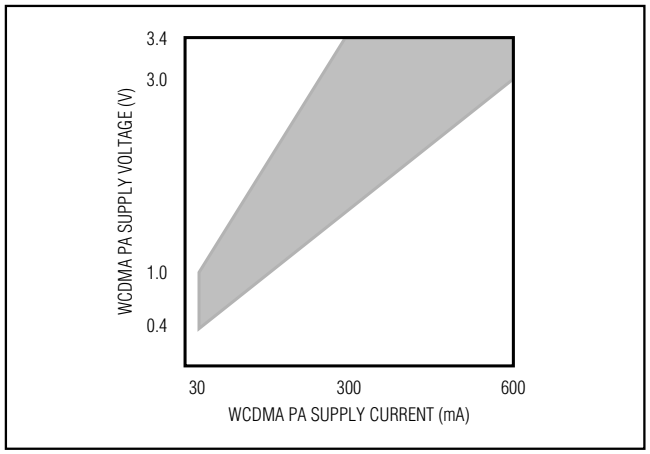


Figure 4. Typical WCDMA PA Load Profile

The MAX1820's output voltage is dynamically adjustable from 0.4V to V_{BATT} by the use of the REF input. The gain from V_{REF} to V_{OUT} is internally set to 1.76. V_{OUT} can be adjusted during operation by driving REF with an external DAC. The MAX1820 output responds to full-scale change in voltage and current in <30µs.

Setting the Output Voltage (MAX1821)

The MAX1821 is intended for general-purpose step-down applications where high efficiency is a priority. Select an output voltage between 1.25V and V_{BATT} by connecting FB to a resistive divider between the output and GND (Figure 3). Select feedback resistor R2 in the 5kΩ to 30kΩ range. R1 is then given by:

$$R1 = R2\left(\frac{V_{OUT}}{V_{FB}} - 1\right)$$

where V_{FB} = 1.25V.

Compensation and Stability

The MAX1820/MAX1821 are externally compensated by placing a resistor and a capacitor (R_C and C1) in series, from COMP to GND (Figure 3). The capacitor integrates the current from the transimpedance amplifier, averaging output capacitor ripple. This sets the device speed for transient responses and allows the use of small ceramic output capacitors because the phase-shifted capacitor ripple does not disturb the current regulation loop. The resistor sets the proportional gain of the output error voltage by a factor $g_m \times R_C$. Increasing this resistor also increases the sensitivity of the control loop to the output capacitor ripple.

This resistor and capacitor set a compensation zero that defines the system's transient response. The load pole is a dynamic pole, shifting the pole frequency with changes in load. As the load decreases, the pole frequency shifts to the left. System stability requires that the compensation zero must be placed properly to ensure adequate phase margin (at least 30° at unity gain). The following is a design procedure for the compensation network:

1) Select an appropriate converter bandwidth (f_C) to stabilize the system while maximizing transient response. This bandwidth should not exceed 1/5 of the switching frequency. Use 100kHz as a reasonable starting point.
2) Calculate the compensation capacitor, C1, based on this bandwidth:

$$C1 = \left(\frac{V_{O(MAX)}}{I_{O(MAX)}}\right)\left(\frac{1}{R_{CS}}\right)\left(g_m \times \frac{R2}{R1+R2}\right)\left(\frac{1}{2\times\pi\times f_C}\right)$$

Resistors R1 and R2 are internal to the MAX1820; use R1 = 151kΩ and R2 = 199kΩ as nominal values for calculations. These resistors are external to the MAX1821 (see the *Setting the Output Voltage* section). Using V_{OMAX} = 3.4V, I_{OMAX} = 0.6A, g_m = 50µs, R_{CS} = 0.75Ω, C1 is evaluated as:

$$C1 = \left(\frac{3.4V}{0.6A}\right)\left(\frac{1}{0.75\Omega}\right)\left(50\mu s \times \frac{199k\Omega}{151k\Omega+199k\Omega}\right) \times \left(\frac{1}{2\times 3.14\times 100kHz}\right) = 341pF$$

Selecting the nearest standard value of 330pF corresponds to a 103kHz bandwidth, which is still acceptable per the above criteria.

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Table 1. Suggested Inductors

MANUFACTURER	PART NUMBER	INDUCTANCE (µH)	ESR (mΩ)	SATURATION CURRENT (A)	DIMENSIONS (mm)
Coilcraft	DO1606	4.7	120	1.2	5.3 × 5.3 × 2.0
Coilcraft	LPT1606-472	4.7	240 (max)	1.2	6.5 × 5.3 × 2.0
Sumida	CDRH4D18-4R7	4.7	125	0.84	5 × 5 × 2
Sumida	CR43	4.7	108.7	1.15	4.5 × 4.0 × 3.5
Sumida	CDRH5D18-4R1	4.1	57	1.95	5.5 × 5.5 × 2.0

3) Calculate the equivalent load impedance, R_L, by:

$$R_L \approx \frac{V_{OUT(MAX)}}{I_{OUT(MAX)}}$$

4) Calculate the compensation resistance (R_C) value to cancel out the dominant pole created by the output load and the output capacitance:

$$\frac{1}{2\times\pi\times R_L\times C_{OUT}} = \frac{1}{2\times\pi\times R_C\times C1}$$

Solving for R_C gives:

$$R_C = \frac{R_L\times C_{OUT}}{C1} = \left(\frac{3.4V}{0.6A}\right)\left(\frac{4.7\mu F}{330pF}\right) = 80.8k\Omega$$

5) Calculate the high-frequency compensation pole to cancel the zero created by the output capacitor's equivalent series resistance (ESR):

$$\frac{1}{2\times\pi\times R_{ESR}\times C_{OUT}} = \frac{1}{2\times\pi\times R3\times C2}$$

Solving for C2 gives:

$$C2 = \frac{R_{ESR}\times C_{OUT}}{R3} = \frac{4.7\mu F\times 0.01\Omega}{80.8k\Omega} = 0.55pF$$

In this case, C2 can be omitted due to the use of ceramic capacitors. Larger output capacitors and higher ESR may require the use of capacitor C2.

Inductor Selection

A 4µH to 6µH inductor with a saturation current of at least 800mA is recommended for most applications. For best efficiency, the inductor's DC resistance should be <200mΩ, and saturation current should be >1A. See Table 1 for recommended inductors and manufacturers.

For most designs, a reasonable inductor value (L_{IDEAL}) can be derived from the following equation:

$$L_{IDEAL} = \frac{V_{OUT}(V_{BATT} - V_{OUT})}{V_{BATT}\times LIR\times I_{OUT(MAX)}\times f_{OSC}}$$

where LIR is the inductor current ripple as a percentage. LIR should be kept between 20% and 40% of the maximum load current for best performance and stability.

The maximum inductor current is:

$$I_{L(MAX)} = \left(1+\frac{LIR}{2}\right)I_{OUT(MAX)}$$

The inductor current becomes discontinuous if I_{OUT} decreases to LIR/2 from the output current value used to determine L_{IDEAL}.

Input Capacitor Selection

The input capacitor reduces the current peaks drawn from the battery or input power source and reduces switching noise in the IC. The impedance of the input capacitor at the switching frequency should be less than that of the input source so high-frequency switching currents do not pass through the input source.

The input capacitor must meet the ripple-current requirement (I_{RMS}) imposed by the switching currents. Nontantalum chemistries (ceramic, POSCAP, or OS-CON) are preferred due to their resistance to power-up surge currents:

$$I_{RMS} = I_{LOAD}\left(\frac{\sqrt{V_{OUT}(V_{BATT} - V_{OUT})}}{V_{BATT}}\right)$$

For optimal circuit reliability, choose a capacitor that has less than 10°C temperature rise at the peak ripple current.

Output Capacitor Selection

The output capacitor is required to keep the output voltage ripple small and to ensure regulation control loop stability. The output capacitor must have low impedance at the switching frequency. Ceramic capacitors are recommended. The output ripple is approximately:

$$V_{RIPPLE} \approx LIR \times I_{OUT(MAX)} \times \left[ESR + \frac{1}{(2 \times f_{OSC} \times C_{OUT})} \right]$$

See the *Compensation Design* section for a discussion of the influence of output capacitance and ESR on regulation control-loop stability.

The capacitor voltage rating must exceed the maximum applied capacitor voltage. Consult the manufacturer's specifications for proper capacitor derating. Avoid Y5V and Z5U dielectric types due to their huge voltage and temperature coefficients of capacitance and ESR.

PC Board Layout and Routing

High switching frequencies and large peak currents make PC board layout a very important part of design. Good design minimizes excessive EMI on the feedback paths and voltage gradients in the ground plane, both of which can result in instability or regulation errors. Connect the inductor, input filter capacitor, and output filter capacitor as close together as possible, and keep their traces short, direct, and wide. Connect their ground pins at a single common node in a star-ground configuration. The external voltage-feedback network should be very close to the FB pin, within 0.2in (5mm). Keep noisy traces (from the LX pin, for example) away from the voltage-feedback network; also, keep them separate, using grounded copper. Connect GND and PGND at a single point, as close as possible to the MAX1820/MAX1821. The MAX1820/MAX1821 evaluation kit manual illustrates an example PC board layout and routing scheme.

UCSP Package Consideration

For general UCSP package information and PC layout considerations, refer to the Maxim Application Note (Wafer-Level Ultra-Chip-Board-Scale Package).

Table 2. Capacitor Selection

CAPACITOR	CAPACITOR VALUE (µF)	ESR (mΩ)	CAPACITOR TYPE
C_{BATT}	4.7 to 10	<150	Ceramic
C_{OUT} (MAX1820)	2.2 to 4.7	<50	Ceramic
C_{OUT} (MAX1821)	4.7 to 10	<150	Ceramic

Table 3. Component Manufacturers

MANUFACTURER	USA PHONE NUMBER	WEBSITE
Coilcraft	847-639-6400	www.coilcraft.com
Kemet	408-986-0424	www.kemet.com
Panasonic	847-468-5624	www.panasonic.com
Sumida	847-956-0666	www.sumida.com
Taiyo Yuden	408-573-4150	www.t-yuden.com

UCSP Reliability

The chip-scale package (UCSP) represents a unique packaging form factor that may not perform equally to a packaged product through traditional mechanical reliability tests. UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and usage environment. The user should closely review these areas when considering use of a UCSP package. Performance through Operating Life Test and Moisture Resistance remains uncompromised as it is primarily determined by the wafer-fabrication process.

Mechanical stress performance is a greater consideration for a UCSP package. UCSPs are attached through direct solder contact to the user's PC board, foregoing the inherent stress relief of a packaged-product lead frame. Solder joint contact integrity must be considered. Information on Maxim's qualification plan, test data, and recommendations are detailed in the UCSP application note, which can be found on Maxim's website, www.maxim-ic.com.

Chip Information

TRANSISTOR COUNT: 2722

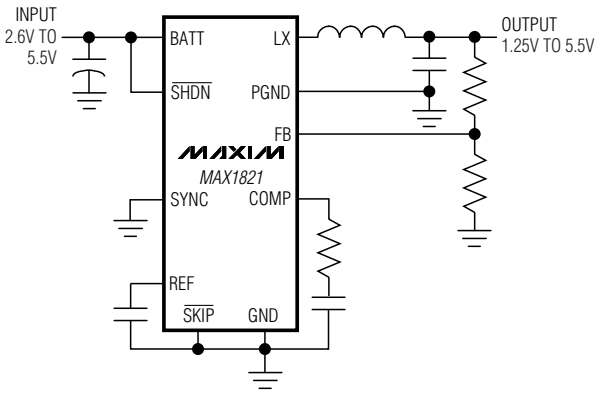
WCDMA Cellular Phone 600mA Buck Regulators

Ordering Information (continued)

PART	SYNC FREQ (MHz)	OUTPUT VOLTAGE	TEMP RANGE	PIN-PACKAGE	UCSP MARK
MAX1821EBC*	No Sync	Programmable	-40°C to +85°C	3 × 4 UCSP	AAC
MAX1821EUB	No Sync	Programmable	-40°C to +85°C	10 µMAX	—
MAX1821XEBC*	13	Programmable	-40°C to +85°C	3 × 4 UCSP	AAV
MAX1821XEUB	13	Programmable	-40°C to +85°C	10 µMAX	—

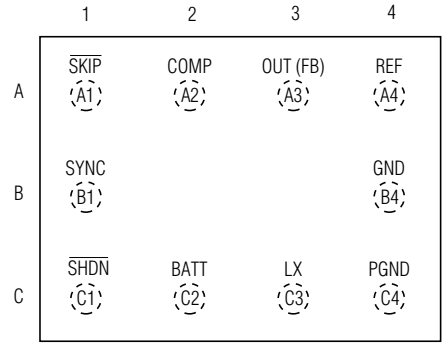
**UCSP reliability is integrally linked to the user's assembly methods, circuit board material, and environment. Refer to the UCSP Reliability Notice in the UCSP Reliability section for more information.*

Typical Operating Circuits (continued)



Pin Configurations

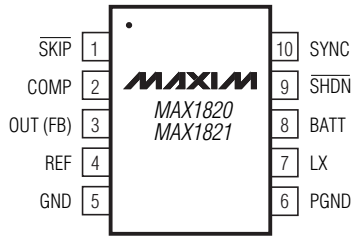
TOP VIEW AFTER ASSEMBLED ON PC BOARD (BUMPS AT THE BOTTOM)



UCSP

( ) ARE FOR MAX1821 ONLY.

TOP VIEW



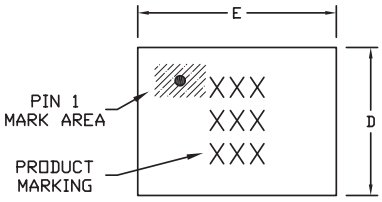
µMAX

( ) ARE FOR MAX1821 ONLY.

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

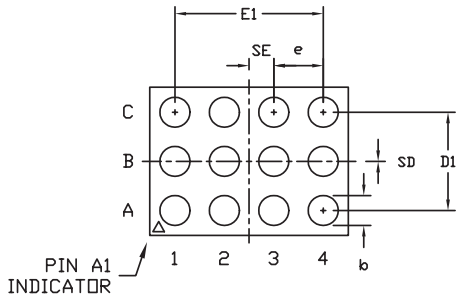
12L, UCSP 4x3.EPS



TOP VIEW

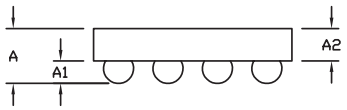
COMMON DIMENSIONS	
A	0.62+0.05-0.08
A1	0.29±0.02
A2	0.33 REF.
b	ø0.35±0.03
D1	1.00 BASIC
E1	1.50 BASIC
e	0.50 BASIC
SD	0.00 BASIC
SE	0.25 BASIC

PKG. CODE	VARIABLE DIMENSIONS		DEPOPULATED SOLDER BALLS
	D	E	
B12-1	1.54±0.05	2.02±0.05	NONE
B12-2	1.54±0.05	2.02±0.05	B3
B12-3	1.54±0.05	2.12±0.05	NONE
B12-4	1.54±0.05	2.02±0.05	B2, B3
B12-5	1.64±0.05	2.12±0.05	B2
B12-6	1.64±0.05	2.12±0.05	B3
B12-7	1.54±0.05	2.02±0.05	B1, B3
B12-8	1.54±0.05	2.02±0.05	B2
B12-9	1.54±0.05	2.12±0.05	B2, B3
B12-10	1.54±0.05	2.02±0.05	B1, B2, B3, B4
B12-11	1.54±0.05	2.02±0.05	A2, C3



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. PRODUCT MARKING: NUMBER OF CHARACTERS AND LINES VARY PER PRODUCT.



SIDE VIEW

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 4x3 UCSP

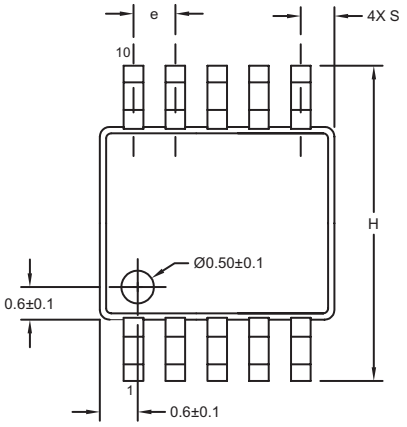
APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0104	F	1/1

WCDMA Cellular Phone 600mA Buck Regulators

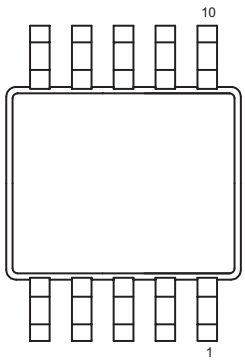
Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

10LUMAX.EPS

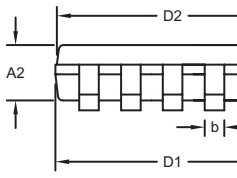


TOP VIEW

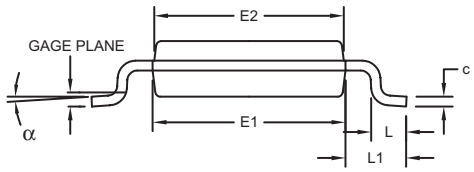


BOTTOM VIEW

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	-	0.043	-	1.10
A1	0.002	0.006	0.05	0.15
A2	0.030	0.037	0.75	0.95
D1	0.116	0.120	2.95	3.05
D2	0.114	0.118	2.89	3.00
E1	0.116	0.120	2.95	3.05
E2	0.114	0.118	2.89	3.00
H	0.187	0.199	4.75	5.05
L	0.0157	0.0275	0.40	0.70
L1	0.037 REF		0.940 REF	
b	0.007	0.0106	0.177	0.270
e	0.0197 BSC		0.500 BSC	
c	0.0035	0.0078	0.090	0.200
S	0.0196 REF		0.498 REF	
α	0°	6°	0°	6°



FRONT VIEW



SIDE VIEW

NOTES:
1. D&E DO NOT INCLUDE MOLD FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm (.006").
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC MO-187C-BA.

DALLAS SEMICONDUCTOR MAXIM

PROPRIETARY INFORMATION

TITLE: PACKAGE OUTLINE, 10L uMAX/uSOP

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0061	I	1/1

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