



# 512MB – 64Mx72 DDR2 SDRAM REGISTERED DIMM, w/PLL

## FEATURES

- Registered 240-pin, dual in-line memory module
- Fast data transfer rates: PC2-6400\*, PC2-5300\*, PC2-4200 and PC2-3200
- Utilizes 800\*, 667\*, 533 and 400 MT/s DDR2 SDRAM components
- $V_{CC} = V_{CCQ} = 1.8V \pm 0.1V$
- $V_{CCSPD} = 1.7V$  to 3.6V
- JEDEC standard 1.8V I/O (SSTL\_18-compatible)
- Differential data strobe (DQS, DQS#) option
- Four-bit prefetch architecture
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Write Latency = Read Latency  $1^{t_{CK}}$
- Programmable CAS# latency (CL): 3, 4, 5\* and 6\*
- Adjustable data-output drive strength
- On-die termination (ODT)
- 7.8µs average periodic refresh interval
- Posted CAS# latency: 0, 1, 2, 3 and 4
- Serial Presence Detect (SPD) with EEPROM
- Auto & Self Refresh (8k/64ms refresh)
- Gold edge contacts
- RoHS compliant
- Package option
  - 240 Pin DIMM
  - PCB – 30.00mm (1.181") TYP

## DESCRIPTION

The WV3HG64M72EER is a 64Mx72 Double Data Rate DDR2 SDRAM high density module. This memory module consists of nine 64Mx8 bit with 4 banks DDR2 Synchronous DRAMs in FBGA packages, mounted on a 240-pin DIMM FR4 substrate.

\* This product is under development, is not qualified or characterized and is subject to change or cancellation without notice.

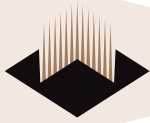
NOTE: Consult factory for availability of:

- Vendor source control options
- Industrial temperature option

## OPERATING FREQUENCIES

	PC2-3200	PC2-4200	PC2-5300*	PC2-6400*
Clock Speed	200MHz	266MHz	333MHz	400MHz
CL-t <sub>RC</sub> -t <sub>RP</sub>	3-3-3	4-4-4	5-5-5	6-6-6

\* Consult factory for availability



### PIN CONFIGURATION

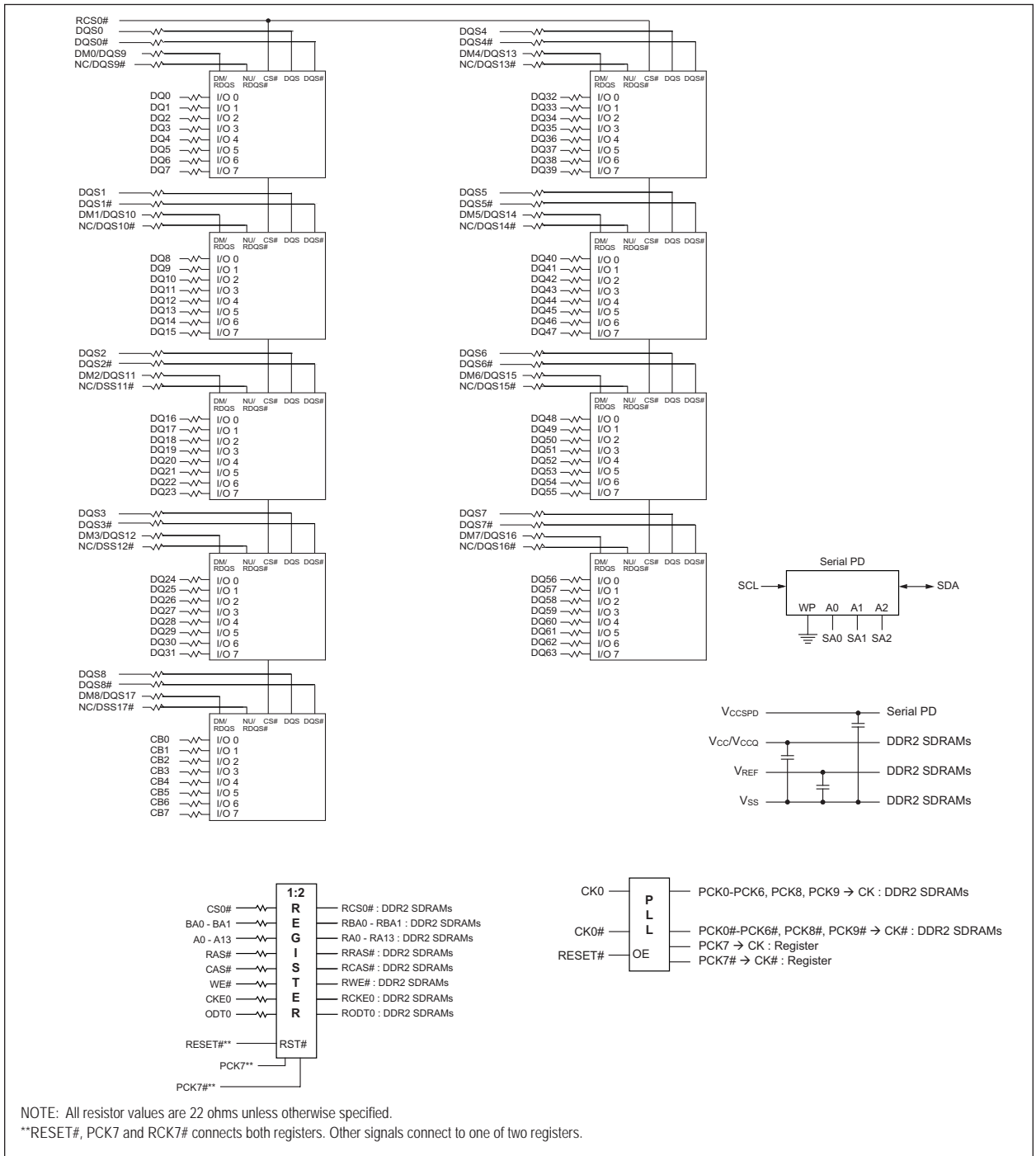
Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol	Pin No.	Symbol
1	V <sub>REF</sub>	61	A4	121	V <sub>SS</sub>	181	V <sub>CC</sub>
2	V <sub>SS</sub>	62	V <sub>CC</sub>	122	DO4	182	A3
3	DQ0	63	A2	123	DO5	183	A1
4	DQ1	64	V <sub>CC</sub>	124	V <sub>SS</sub>	184	V <sub>CC</sub>
5	V <sub>SS</sub>	65	V <sub>SS</sub>	125	DM0/DQS9	185	CK0
6	DQS0#	66	V <sub>SS</sub>	126	NC/DQS9#	186	CK0#
7	DQS0	67	V <sub>CC</sub>	127	V <sub>SS</sub>	187	V <sub>CC</sub>
8	V <sub>SS</sub>	68	NC	128	DO6	188	A0
9	DQ2	69	V <sub>CC</sub>	129	DO7	189	V <sub>CC</sub>
10	DQ3	70	A10/AP	130	V <sub>SS</sub>	190	BA1
11	V <sub>SS</sub>	71	BA0	131	DQ12	191	V <sub>CC</sub>
12	DO8	72	V <sub>CC</sub>	132	DQ13	192	RAS#
13	DO9	73	WE#	133	V <sub>SS</sub>	193	CS0#
14	V <sub>SS</sub>	74	CAS#	134	DM1/DQS10	194	V <sub>CC</sub>
15	DQS1#	75	V <sub>CC</sub>	135	NC/DQS10#	195	ODT0
16	DQS1	76	NC	136	V <sub>SS</sub>	196	A13
17	V <sub>SS</sub>	77	NC	137	NC	197	V <sub>CC</sub>
18	RESET#	78	V <sub>CC</sub>	138	NC	198	V <sub>SS</sub>
19	NC	79	V <sub>SS</sub>	139	V <sub>SS</sub>	199	DQ36
20	V <sub>SS</sub>	80	DO32	140	DO14	200	DO37
21	DQ10	81	DO33	141	DO15	201	V <sub>SS</sub>
22	DQ11	82	V <sub>SS</sub>	142	V <sub>SS</sub>	202	DM4/DQS13
23	V <sub>SS</sub>	83	DQS4#	143	DO20	203	NC/DQS13#
24	DO16	84	DQS4	144	DO21	204	V <sub>SS</sub>
25	DO17	85	V <sub>SS</sub>	145	V <sub>SS</sub>	205	DO38
26	V <sub>SS</sub>	86	DQ34	146	DM2/DQS11	206	DQ39
27	DQS2#	87	DO35	147	NC/DQS11#	207	V <sub>SS</sub>
28	DQS2	88	V <sub>SS</sub>	148	V <sub>SS</sub>	208	DO44
29	V <sub>SS</sub>	89	DO40	149	DO22	209	DO45
30	DQ18	90	DO41	150	DO23	210	V <sub>SS</sub>
31	DO19	91	V <sub>SS</sub>	151	V <sub>SS</sub>	211	DM5/DQS14
32	V <sub>SS</sub>	92	DQS5#	152	DO28	212	NC/DQS14#
33	DO24	93	DQS5	153	DO29	213	V <sub>SS</sub>
34	DO25	94	V <sub>SS</sub>	154	V <sub>SS</sub>	214	DO46
35	V <sub>SS</sub>	95	DO42	155	DM3/DQS12	215	DO47
36	DQS3#	96	DO43	156	NC/DQS12#	216	V <sub>SS</sub>
37	DQS3	97	V <sub>SS</sub>	157	V <sub>SS</sub>	217	DO52
38	V <sub>SS</sub>	98	DO48	158	DO30	218	DO53
39	DO26	99	DO49	159	DO31	219	V <sub>SS</sub>
40	DO27	100	V <sub>SS</sub>	160	V <sub>SS</sub>	220	NC
41	V <sub>SS</sub>	101	SA2	161	CB4	221	NC
42	CB0	102	NC	162	CB5	222	V <sub>SS</sub>
43	CB1	103	V <sub>SS</sub>	163	V <sub>SS</sub>	223	DM6/DQS15
44	V <sub>SS</sub>	104	DQS6#	164	DM8/DQS17	224	NC/DQS15#
45	DQS8#	105	DQS6	165	NC/DQS17#	225	V <sub>SS</sub>
46	DQS8	106	V <sub>SS</sub>	166	V <sub>SS</sub>	226	DO54
47	V <sub>SS</sub>	107	DO50	167	CB6	227	DO55
48	CB2	108	DO51	168	CB7	228	V <sub>SS</sub>
49	CB3	109	V <sub>SS</sub>	169	V <sub>SS</sub>	229	DO60
50	V <sub>SS</sub>	110	DO56	170	V <sub>CC</sub>	230	DO61
51	V <sub>CC</sub>	111	DO57	171	NC	231	V <sub>SS</sub>
52	CKE0	112	V <sub>SS</sub>	172	V <sub>CC</sub>	232	DM7/DQS16
53	V <sub>CC</sub>	113	DQS7#	173	NC	233	NC/DQS16#
54	NC	114	DQS7	174	NC	234	V <sub>SS</sub>
55	NC	115	V <sub>SS</sub>	175	V <sub>CC</sub>	235	DO62
56	V <sub>CC</sub>	116	DO58	176	A12	236	DO63
57	A11	117	DO59	177	A9	237	V <sub>SS</sub>
58	A7	118	V <sub>SS</sub>	178	V <sub>CC</sub>	238	V <sub>CC</sub> SPD
59	V <sub>CC</sub>	119	SDA	179	A8	239	SA0
60	A5	120	SCL	180	A6	240	SA1

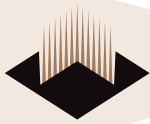
### PIN NAMES

Pin Name	Function
A0-A13	Address Inputs
BA0,BA1	SDRAM Bank Addresses
DQ0-DQ63	Data Input/Output
CB0-CB7	Check Bits
DQS0-DQS17	Data strobes
DQS0#-DQS17#	Data strobes complement
DM0 - DM8	Data Masks
ODT0	On-die termination control
CK0,CK0#	Clock Inputs
CKE0	Clock Enable
CS0#	Chip Select
RAS#	Row Address Strobe
CAS#	Column Address Strobe
WE#	Write Enable
RESET#	Register Reset Input/PLL OE
V <sub>CC</sub>	Core and I/O Power (1.8V)
V <sub>SS</sub>	Ground
SA0-SA2	SPD address
SDA	SPD Data Input/Output
SCL	Serial Presence Detect (SPD) Clock Input
V <sub>REF</sub>	Input/Output Reference Voltage
V <sub>CC</sub> SPD	SPD Power
NC	Spare pins, No connect



FUNCTIONAL BLOCK DIAGRAM





### DC OPERATING CONDITIONS

All voltages referenced to V<sub>SS</sub>

Parameter	Symbol	Min	Typical	Max	Unit	Notes
Supply Voltage	V <sub>CC</sub>	1.7	1.8	1.9	V	3
I/O Reference Voltage	V <sub>REF</sub>	0.49 x V <sub>CC</sub>	0.50 x V <sub>CC</sub>	0.51 x V <sub>CC</sub>	V	1
I/O Termination Voltage	V <sub>TT</sub>	V <sub>REF</sub> -0.04	V <sub>REF</sub>	V <sub>REF</sub> +0.04	V	2
SPD Supply Voltage	V <sub>CCSPD</sub>	1.7	-	3.6	V	

Notes:

- V<sub>REF</sub> is expected to equal V<sub>CC/2</sub> of the transmitting device and to track variations in the DC level of the same. Peak-to-peak noise on V<sub>REF</sub> may not exceed +/-1 percent of the DC value. Peak-to-peak AC noise on V<sub>REF</sub> may not exceed +/-2 percent of V<sub>REF</sub>. This measurement is to be taken at the nearest V<sub>REF</sub> bypass capacitor.
- V<sub>TT</sub> is not applied directly to the device. V<sub>TT</sub> is a system supply for signal termination resistors, is expected to be set equal to V<sub>REF</sub> and must track variations in the DC level of V<sub>REF</sub>.
- V<sub>CC0</sub> of all IC's are tied to V<sub>CC</sub>.

### ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Units	
V <sub>CC</sub>	Voltage on V <sub>CC</sub> pin relative to V <sub>SS</sub>	-0.5	2.3	V	
V <sub>IN</sub> , V <sub>OUT</sub>	Voltage on any pin relative to V <sub>SS</sub>	-0.5	2.3	V	
T <sub>STG</sub>	Storage Temperature	-55	100	°C	
I <sub>L</sub>	Input leakage current: Any input 0V < V <sub>IN</sub> < V <sub>CC</sub> ; V <sub>REF</sub> input 0V < V <sub>IN</sub> < 0.95V; Other pins not under test = 0V	Command/Address, RAS#, CAS#, WE#, CS#, CKE	-5	5	μA
		CK, CK#	-10	10	
		DM	-5	5	
I <sub>oz</sub>	Output leakage current; 0V < V <sub>OUT</sub> < V <sub>CC</sub> ; DQs and ODT are disable	-5	5	μA	
I <sub>VREF</sub>	V <sub>REF</sub> leakage current; V <sub>REF</sub> = Valid V <sub>REF</sub> level	-18	18	μA	

### CAPACITANCE

T<sub>A</sub> = 25°C, f = 100MHz

Parameter	Symbol	Min	Max	Units
Input Capacitance: (A0-A13, BA0-BA1, RAS#, CAS#, WE#)	CIN <sub>1</sub>	11	12	pF
Input Capacitance: (CKE0), (ODT0)	CIN <sub>2</sub>	11	12	pF
Input Capacitance: (CS0#)	CIN <sub>3</sub>	11	12	pF
Input Capacitance: (CK0, CK0#)	CIN <sub>4</sub>	10	11	pF
Input Capacitance: (DM0-DM8), (DQS0-DQS17)	CIN <sub>5</sub>	6.5	8	pF
Input/Output Capacitance: (DQ0 - DQ63), (CB0 -CB7)	COU <sub>T1</sub>	6.5	8	pF



**OPERATING TEMPERATURE CONDITION**

Parameter	Symbol	Rating	Units	Notes
Operating Case Temperature (Commercial)	TOPER	0 to +85°C	°C	1, 2

- NOTE:
1. Operation temperature is the case surface temperature on the center/top side of the DRAM. For the measurement conditions, please refer to JEDEC JESD51.2
  2. At 0 to +85°C, operation temperature range, all DRAM specification will be supported.

**INPUT DC LOGIC LEVEL**

All voltages referenced to V<sub>SS</sub>

Parameter	Symbol	Min	Max	Unit
Input High (Logic 1) Voltage	V <sub>IH</sub> (DC)	V <sub>REF</sub> + 0.125	V <sub>CC</sub> + 0.300	V
Input Low (Logic 0) Voltage	V <sub>IL</sub> (DC)	- 0.300	V <sub>REF</sub> - 0.125	V

**INPUT AC LOGIC LEVEL**

All voltages referenced to V<sub>SS</sub>

Parameter	Symbol	Min	Max	Unit
AC Input High (Logic 1) Voltage DDR2-400 & DDR2-533	V <sub>IH</sub> (AC)	V <sub>REF</sub> + 0.250	-	V
AC Input High (Logic 1) Voltage DDR2-667	V <sub>IH</sub> (AC)	V <sub>REF</sub> + 0.200	-	V
AC Input High (Logic 0) Voltage DDR2-400 & DDR2-533	V <sub>IL</sub> (AC)	-	V <sub>REF</sub> - 0.250	V
AC Input High (Logic 0) Voltage DDR2-667	V <sub>IL</sub> (AC)	-	V <sub>REF</sub> - 0.200	V



### DDR2 I<sub>CC</sub> SPECIFICATIONS AND CONDITIONS

Includes DDR2 SDRAM components only

Symbol	Proposed Conditions	806	665	534	403	Units	
I <sub>CC0*</sub>	Operating one bank active-precharge current; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmin</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	1,120	1,120	mA	
I <sub>CC1*</sub>	Operating one bank active-read-precharge current; I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(I <sub>CC</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmin</sub> (I <sub>CC</sub> ), t <sub>RCD</sub> = t <sub>RCD</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I <sub>CC4W</sub>	TBD	TBD	1,255	1,255	mA	
I <sub>CC2P*</sub>	Precharge power-down current; All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); CE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	TBD	472	472	mA	
I <sub>CC2O**</sub>	Precharge quiet standby current; All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	TBD	TBD	670	670	mA	
I <sub>CC2N**</sub>	Precharge standby current; All banks idle; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	715	715	mA	
I <sub>CC3P**</sub>	Active power-down current; All banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); CE is LOW; Other control and address bus inputs are STABLE; Data bus inputs are FLOATING	Fast PDN Exit MRS(12) = 0	TBD	TBD	670	670	mA
		Slow PDN Exit MRS(12) = 1	TBD	TBD	508	508	mA
I <sub>CC3N**</sub>	Active standby current; All banks open; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmax</sub> (I <sub>CC</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	850	850	mA	
I <sub>CC4W*</sub>	Operating burst write current; All banks open, Continuous burst writes; BL = 4, CL = CL(I <sub>CC</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmax</sub> (I <sub>CC</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	1,480	1,390	mA	
I <sub>CC4R*</sub>	Operating burst read current; All banks open, Continuous burst reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(I <sub>CC</sub> ), AL = 0; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RAS</sub> = t <sub>RASmax</sub> (I <sub>CC</sub> ), t <sub>RP</sub> = t <sub>RP</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are SWITCHING; Data pattern is same as I <sub>CC4W</sub>	TBD	TBD	1,525	1,390	mA	
I <sub>CC5B**</sub>	Burst auto refresh current; t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ); Refresh command at every t <sub>REFC</sub> (I <sub>CC</sub> ) interval; CE is HIGH, CS# is HIGH between valid commands; Other control and address bus inputs are SWITCHING; Data bus inputs are SWITCHING	TBD	TBD	1,160	1,660	mA	
I <sub>CC6**</sub>	Self refresh current; CK and CK\ at 0V; CE 0.2V; Other control and address bus inputs are FLOATING; Data bus inputs are FLOATING	Normal	TBD	TBD	72	72	mA
I <sub>CC7*</sub>	Operating bank interleave read current; All bank interleaving reads, I <sub>OUT</sub> = 0mA; BL = 4, CL = CL(I <sub>CC</sub> ), AL = t <sub>RCD</sub> (I <sub>CC</sub> ) - 1 * t <sub>CK</sub> (I <sub>CC</sub> ); t <sub>CK</sub> = t <sub>CK</sub> (I <sub>CC</sub> ), t <sub>RC</sub> = t <sub>RC</sub> (I <sub>CC</sub> ), t <sub>RRD</sub> = t <sub>RRD</sub> (I <sub>CC</sub> ), t <sub>RCD</sub> = 1 * t <sub>CK</sub> (I <sub>CC</sub> ); CE is HIGH, CS# is HIGH between valid commands; Address bus inputs are STABLE during DESELECTS; Data bus inputs are SWITCHING.	TBD	TBD	2,380	2,380	mA	

Note: I<sub>CC</sub> specification is based on SAMSUNG components. Other DRAM Manufacturers specification may be different.

\*: Value calculated as one module rank in this operating condition, and all other module ranks in I<sub>CC2P</sub> (CE LOW) mode.

\*\* : Value calculated reflects all module ranks in this operating condition.



AC TIMING PARAMETERS & SPECIFICATIONS

AC CHARACTERISTICS			806		665		534		403			
PARAMETER			SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Clock	Clock cycle time	CL = 6	t <sub>CK</sub> (6)	TBD	TBD							ps
		CL = 5	t <sub>CK</sub> (5)	TBD	TBD	3,000	8,000					ps
		CL = 4	t <sub>CK</sub> (4)	TBD	TBD	3,750	8,000	3,750	8,000	5,000	8,000	ps
		CL = 3	t <sub>CK</sub> (3)	TBD	TBD	5,000	8,000	5,000	8,000	5,000	8,000	ps
	CK high-level width		t <sub>CH</sub>	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>
	CK low-level width		t <sub>CL</sub>	TBD	TBD	0.45	0.55	0.45	0.55	0.45	0.55	t <sub>CK</sub>
	Half clock period		t <sub>HP</sub>	TBD	TBD	MIN(t <sub>CH</sub> , t <sub>CL</sub> )		MIN(t <sub>CH</sub> , t <sub>CL</sub> )		MIN(t <sub>CH</sub> , t <sub>CL</sub> )		ps
Clock jitter		t <sub>JIT</sub>	TBD	TBD	-125	125	-125	125	-125	125	ps	
Data	DQ output access time from CK/CK#		t <sub>AC</sub>	TBD	TBD	-450	+450	-500	+500	-600	+600	ps
	Data-out high-impedance window from CK/CK#		t <sub>HZ</sub>	TBD	TBD		t <sub>AC</sub> (MAX)		t <sub>AC</sub> (MAX)		t <sub>AC</sub> (MAX)	ps
	Data-out low-impedance window from CK/CK#		t <sub>LZ</sub>	TBD	TBD	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)	t <sub>AC</sub> (MIN)	t <sub>AC</sub> (MAX)	ps
	DQ and DM input setup time relative to DQS		t <sub>DS</sub>	TBD	TBD	100		100		150		
	DQ and DM input hold time relative to DQS		t <sub>DH</sub>	TBD	TBD	225		225		275		
	DQ and DM input pulse width (for each input)		t <sub>DLPW</sub>	TBD	TBD	0.35		0.35		0.35		t <sub>CK</sub>
	Data hold skew factor		t <sub>QHS</sub>	TBD	TBD		340		400		450	ps
	DQ...DQS hold, DQS to first DQ to go nonvalid, per access		t <sub>QH</sub>	TBD	TBD	t <sub>HP</sub> - t <sub>QHS</sub>		t <sub>HP</sub> - t <sub>QHS</sub>		t <sub>HP</sub> - t <sub>QHS</sub>		ps
	Data valid output window (DVW)		t <sub>DVW</sub>	TBD	TBD	t <sub>QH</sub> - t <sub>DQSQ</sub>		t <sub>QH</sub> - t <sub>DQSQ</sub>		t <sub>QH</sub> - t <sub>DQSQ</sub>		ns
	Data Strobe	DQS input high pulse width		t <sub>DQSH</sub>	TBD	TBD	0.35		0.35		0.35	
DQS input low pulse width		t <sub>DQSL</sub>	TBD	TBD	0.35		0.35		0.35		t <sub>CK</sub>	
DQS output access time from CK/CK#		t <sub>DQSCK</sub>	TBD	TBD	-400	+400	-450	+450	-500	+500	ps	
DQS falling edge to CK rising ... setup time		t <sub>DSS</sub>	TBD	TBD	0.2		0.2		0.2		t <sub>CK</sub>	
DQS falling edge from CK rising ... hold time		t <sub>DSH</sub>	TBD	TBD	0.2		0.2		0.2		t <sub>CK</sub>	
DQS...DQ skew, DQS to last DQ valid, per group, per access		t <sub>DQSQ</sub>	TBD	TBD		240		300		350	ps	
DQS read preamble		t <sub>RPRE</sub>	TBD	TBD	0.9	1.1	0.9	1.1	0.9	1.1	t <sub>CK</sub>	
DQS read postamble		t <sub>RPST</sub>	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	
DQS write preamble setup time		t <sub>WPRES</sub>	TBD	TBD	0		0		0		ps	
DQS write preamble		t <sub>WPRE</sub>	TBD	TBD	0.35		0.35		0.35		t <sub>CK</sub>	
DQS write postamble		t <sub>WPST</sub>	TBD	TBD	0.4	0.6	0.4	0.6	0.4	0.6	t <sub>CK</sub>	
Write command to first DQS latching transition		t <sub>DQSS</sub>	TBD	TBD	WL- 0.25	WL+ 0.25	WL- 0.25	WL+ 0.25	WL- 0.25	WL+ 0.25	t <sub>CK</sub>	
Address and control input pulse width for each input		t <sub>IPW</sub>	TBD	TBD	0.6		0.6		0.6		t <sub>CK</sub>	
Address and control input setup time		t <sub>IS</sub>	TBD	TBD	200		250		250		ps	
Address and control input hold time		t <sub>IH</sub>	TBD	TBD	275		375		475		ps	
Address and control input hold time		t <sub>ICD</sub>	TBD	TBD	2		2		2		t <sub>CK</sub>	

\* AC specification is based on SAMSUNG components. Other DRAM manufactures specification may be different.

Continued on next page



AC TIMING PARAMETERS (cont'd)

AC CHARACTERISTICS			806		665		534		403		
PARAMETER		SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Command and Address	ACTIVE to ACTIVE (same bank) command	t <sub>RC</sub>	TBD	TBD	55		55		55		ns
	ACTIVE bank a to ACTIVE bank b command	t <sub>RRD</sub>	TBD	TBD	7.5		7.5		7.5		ns
	ACTIVE to READ or WRITE delay	t <sub>RCD</sub>	TBD	TBD	15		15		15		ns
	Four Bank Activate period	t <sub>FAW</sub>	TBD	TBD	37.5	37.5	37.5	37.5	37.5	37.5	ns
	ACTIVE to PRECHARGE command	t <sub>RAS</sub>	TBD	TBD	40	70,000	40	70,000	40	70,000	ns
	Internal READ to precharge command delay	t <sub>RTP</sub>	TBD	TBD	7.5		7.5		7.5		ns
	Write recovery time	t <sub>WR</sub>	TBD	TBD	15		15		15		ns
	Auto precharge write recovery + precharge time	t <sub>DAL</sub>	TBD	TBD	t <sub>WR</sub> +t <sub>RP</sub>		t <sub>WR</sub> +t <sub>RP</sub>		t <sub>WR</sub> +t <sub>RP</sub>		ns
	Internal WRITE to READ command delay	t <sub>WTR</sub>	TBD	TBD	7.5		7.5		7.5		ns
	PRECHARGE command period	t <sub>RP</sub>	TBD	TBD	15		15		15		ns
	PRECHARGE ALL command period	t <sub>RPA</sub>	TBD	TBD	t <sub>RP</sub> +t <sub>CK</sub>		t <sub>RP</sub> +t <sub>CK</sub>		t <sub>RP</sub> +t <sub>CK</sub>		ns
	LOAD MODE command cycle time	t <sub>MRD</sub>	TBD	TBD	2		2		2		tck
CKE low to CK,CK# uncertainty	t <sub>DELAY</sub>	TBD	TBD	t <sub>IS</sub> +t <sub>CK</sub> t <sub>IH</sub>		t <sub>IS</sub> +t <sub>CK</sub> t <sub>IH</sub>		t <sub>IS</sub> +t <sub>CK</sub> t <sub>IH</sub>		ns	
Self Refresh	REFRESH to Active of Refresh to Refresh command interfal	t <sub>RFC</sub>	TBD	TBD	127.5	70,000	127.5	70,000	127.5	70,000	ns
	Average periodic refresh interval	t <sub>REFI</sub>	TBD	TBD		7.8		7.8		7.8	μs
	Exit self refresh to non-READ command	t <sub>XSNR</sub>	TBD	TBD	t <sub>RFC(MIN)</sub> +10		t <sub>RFC(MIN)</sub> +10		t <sub>RFC(MIN)</sub> +10		ns
	Exit self refresh to READ command	t <sub>XSRD</sub>	TBD	TBD	200		200		200		tck
	Exit self refresh timing reference	t <sub>ISXR</sub>	TBD	TBD	t <sub>IS</sub>		t <sub>IS</sub>		t <sub>IS</sub>		ps
ODT	ODT turn-on delay	t <sub>AOND</sub>	TBD	TBD	2	2	2	2	2	2	tck
	ODT turn-on	t <sub>AON</sub>	TBD	TBD	t <sub>AC(MIN)</sub>	t <sub>AC(MAX)</sub> +1000	t <sub>AC(MIN)</sub>	t <sub>AC(MAX)</sub> +1000	t <sub>AC(MIN)</sub>	t <sub>AC(MAX)</sub> +1000	ps
	ODT turn-off delay	t <sub>AOFD</sub>	TBD	TBD	2.5	2.5	2.5	2.5	2.5	2.5	tck
	ODT turn-off	t <sub>AOF</sub>	TBD	TBD	t <sub>AC(MIN)</sub>	t <sub>AC(MAX)</sub> +600	t <sub>AC(MIN)</sub>	t <sub>AC(MAX)</sub> +600	t <sub>AC(MIN)</sub>	t <sub>AC(MAX)</sub> +600	ps
	ODT turn-on (power-down mode)	t <sub>AONPD</sub>	TBD	TBD	t <sub>AC(MIN)</sub> +2000	2 x t <sub>CK</sub> + t <sub>AC(MAX)</sub> +1000	t <sub>AC(MIN)</sub> +2000	2 x t <sub>CK</sub> + t <sub>AC(MAX)</sub> +1000	t <sub>AC(MIN)</sub> +2000	2 x t <sub>CK</sub> + t <sub>AC(MAX)</sub> +1000	ps
	ODT turn-off (power-down mode)	t <sub>AOFFD</sub>	TBD	TBD	t <sub>AC(MIN)</sub> +2000	2.5 x t <sub>CK</sub> + t <sub>AC(MAX)</sub> +1000	t <sub>AC(MIN)</sub> +2000	2.5 x t <sub>CK</sub> + t <sub>AC(MAX)</sub> +1000	t <sub>AC(MIN)</sub> +2000	2.5 x t <sub>CK</sub> + t <sub>AC(MAX)</sub> +1000	ps
	ODT to power-down entry latency	t <sub>ANPD</sub>	TBD	TBD	3		3		3		tck
	ODT power-down exit latency	t <sub>AXPD</sub>	TBD	TBD	8		8		8		tck
Power-Down	Exit active power-down to READ command, MR[bit12=0]	t <sub>XARD</sub>	TBD	TBD	2		2		2		tck
	Exit active power-down to READ command, MR[bit12=1]	t <sub>XARDS</sub>	TBD	TBD	7-AL		6-AL		6-AL		tck
	A Exit precharge power-down to any non-READ command.	t <sub>XP</sub>	TBD	TBD	2		2		2		tck
	CKE minimum high/low time	t <sub>CKE</sub>	TBD	TBD	3		3		3		tck

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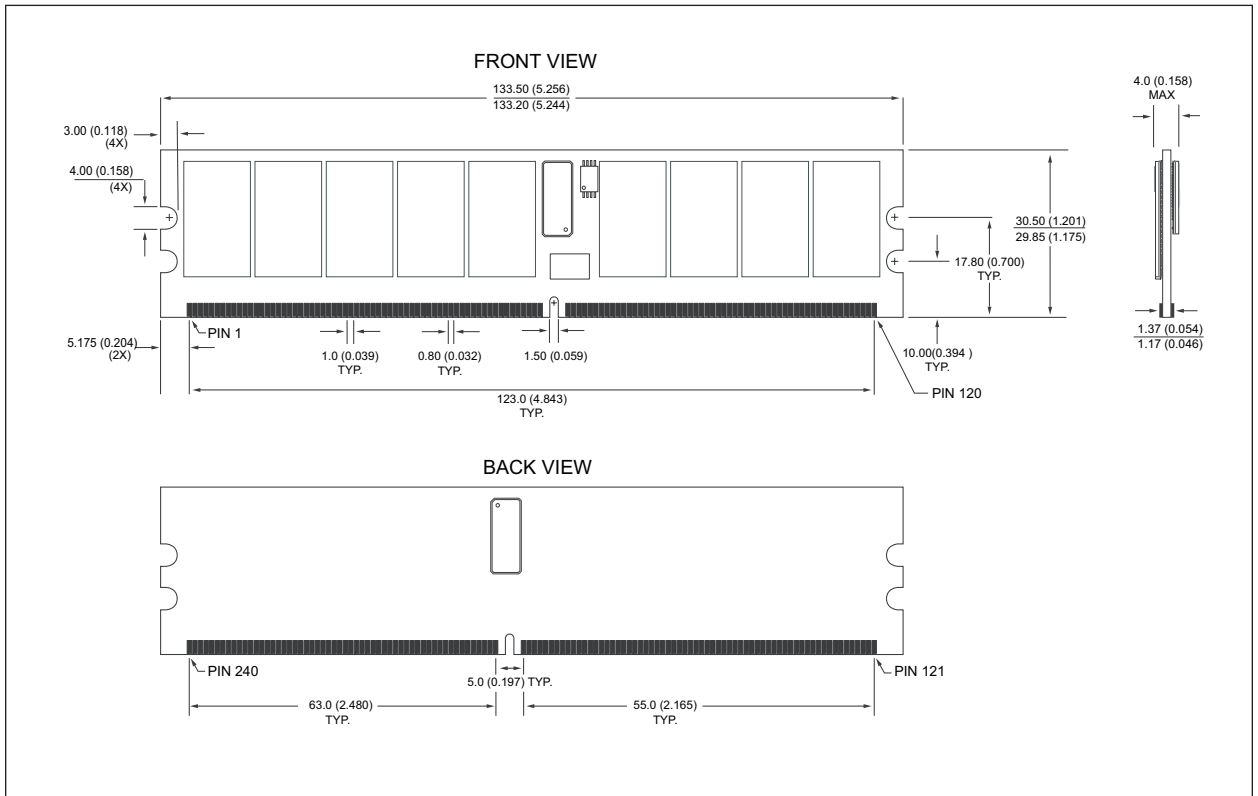
ORDERING INFORMATION FOR D6

Part Number	Speed	CAS Latency	t <sub>RCD</sub>	t <sub>RP</sub>	Height*
WV3HG64M72EER806D6	400MHz/800Mb/s	6	6	6	30.00mm (1.181") TYP
WV3HG64M72EER665D6	333MHz/667Mb/s	5	5	5	30.00mm (1.181") TYP
WV3HG64M72EER534D6	266MHz/533Mb/s	4	4	4	30.00mm (1.181") TYP
WV3HG64M72EER403D6	200MHz/400Mb/s	3	3	3	30.00mm (1.181") TYP

NOTES:

- RoHS products. (\*G\* = RoHS Compliant)
- Vendor specific part numbers are used to provide memory component source control. The place holder for this is shown as a lower case "x" in the part numbers above and is to be replaced with respective vendors code. Consult factory for qualified sourcing options. (M = Micron, S = Samsung & consult factory for others)
- Consult factory for availability of industrial temperature (-40°C to 85°C) option

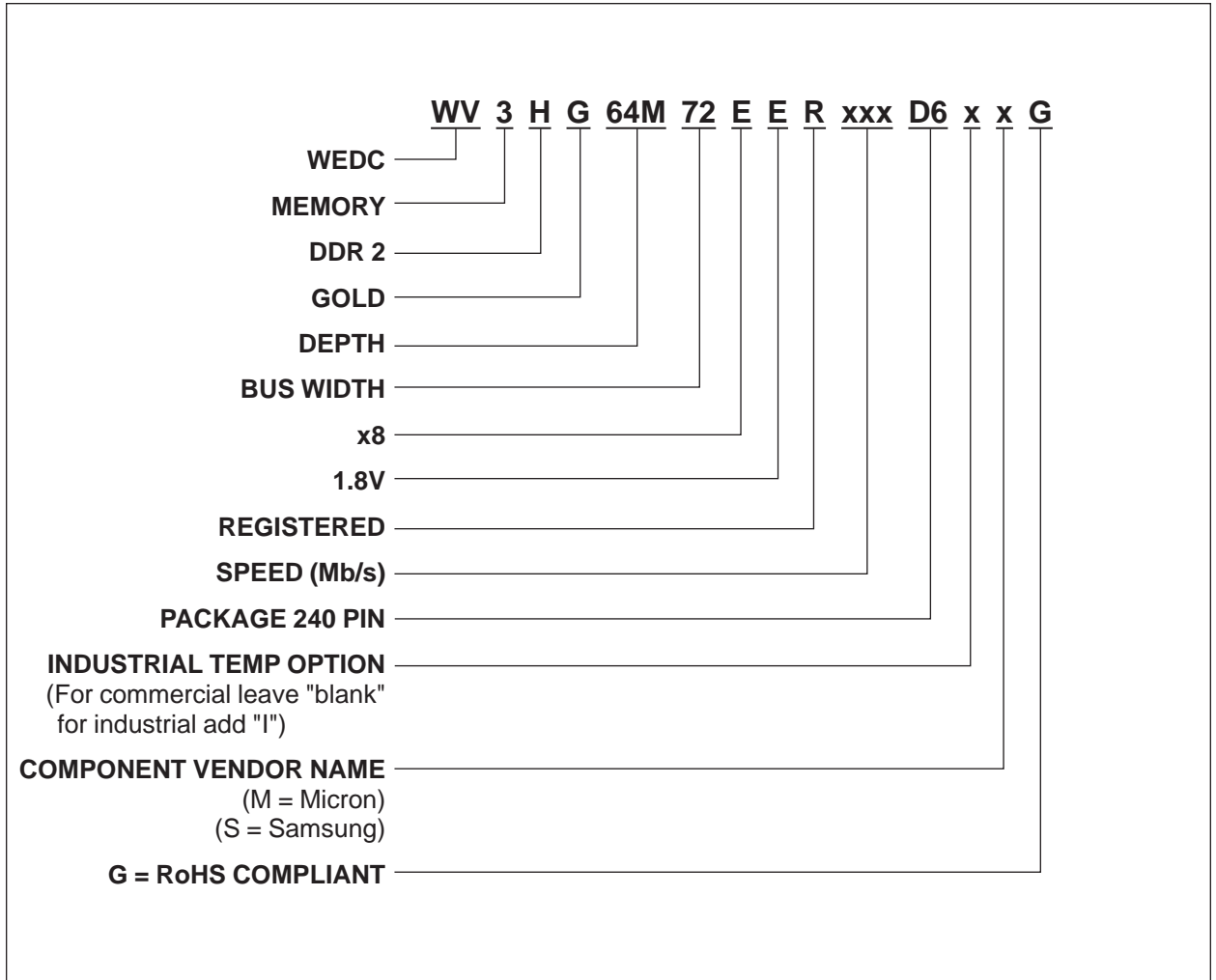
PACKAGE DIMENSIONS FOR D6

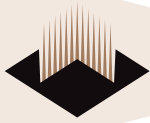


\* ALL DIMENSIONS ARE IN MILLIMETERS AND (INCHES)



PART NUMBERING GUIDE





### Document Title

512MB – 64Mx72 DDR2 SDRAM REGISTERED, w/PLL

### DRAM DIE OPTIONS:

- SAMSUNG: C-Die, will move to E-Die Q2'06
- MICRON: U37: B-Die

### Revision History

Rev #	History	Release Date	Status
Rev 0	Created	August 2006	Concept
Rev 1	1.0 Moved to Advanced	August 14 2006	Advanced