ISL6292

Li-ion/Li Polymer Battery Charger

FN9105
Rev.9.00
December 17, 2007

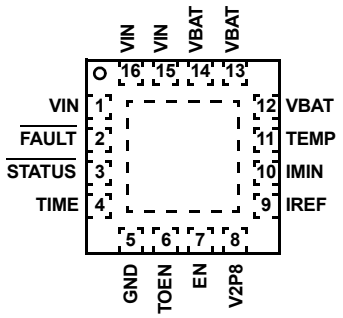
The ISL6292 is an integrated single-cell Li-ion or Li-polymer battery charger capable of operating with an input voltage as low as 2.4V. This charger is designed to work with various types of AC adapters or a USB port.

The ISL6292 operates as a linear charger when the AC adapter is a voltage source. The battery is charged in a CC/CV (constant current/constant voltage) profile. The charge current is programmable with an external resistor up to 2A. The ISL6292 can also work with a current-limited adapter to minimize the thermal dissipation, in which case, the ISL6292 combines the benefits of both a linear charger and a pulse charger.

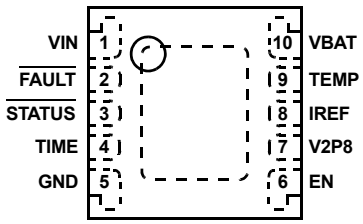
The ISL6292 features charge current thermal foldback to guarantee safe operation when the printed circuit board is space limited for thermal dissipation. Additional features include preconditioning of an over-discharged battery, an NTC thermistor interface for charging the battery in a safe temperature range, automatic recharge, and thermally enhanced QFN or DFN packages.

Pinouts

ISL6292
(16 LD QFN)
TOP VIEW



ISL6292
(10 LD DFN)
TOP VIEW



Features

- Complete Charger for Single-Cell Li-ion Batteries
- **Very Low Thermal Dissipation**
- Integrated Pass Element and Current Sensor
- No External Blocking Diode Required
- 1% Voltage Accuracy
- Programmable Current Limit up to 2A
- Programmable End-of-Charge Current
- **Charge Current Thermal Foldback**
- NTC Thermistor Interface for Battery Temperature Monitor
- **Accepts Multiple Types of Adapters or USB BUS Power**
- **Guaranteed to Operate at 2.65V After Start-Up**
- Ambient Temperature Range: -20°C to +70°C
- Thermally-Enhanced QFN Packages
- Handheld Devices, including Medical Handhelds
- PDAs, Cell Phones and Smart Phones
- Portable Instruments, MP3 Players
- Self-Charging Battery Packs
- Stand-Alone Chargers
- USB Bus-Powered Chargers
- Pb-Free Available (RoHS Compliant)

Related Literature

- Technical Brief TB363 “Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)”
- Technical Brief TB379 “Thermal Characterization of Packaged Semiconductor Devices”
- Technical Brief TB389 “PCB Land Pattern Design and Surface Mount Guidelines for QFN Packages”

Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	PACKAGE	PKG. DWG. #
ISL6292-1CR3*	92-1	-20 to +70	10 Ld 3x3 DFN	L10.3x3
ISL6292-1CR3Z* (Note)	921Z	-20 to +70	10 Ld 3x3 DFN (Pb-free)	L10.3x3
ISL6292-2CR3*	92-2	-20 to +70	10 Ld 3x3 DFN	L10.3x3
ISL6292-2CR3Z* (Note)	922Z	-20 to +70	10 Ld 3x3 DFN (Pb-free)	L10.3x3
ISL6292-1CR4*	629 2-1CR4	-20 to +70	16 Ld 4x4 QFN	L16.4x4
ISL6292-1CR4Z* (Note)	629 21CR4Z	-20 to +70	16 Ld 4x4 QFN (Pb-free)	L16.4x4
ISL6292-2CR4*	629 2-2CR4	-20 to +70	16 Ld 4x4 QFN	L16.4x4
ISL6292-2CR4Z* (Note)	629 22CR4Z	-20 to +70	16 Ld 4x4 QFN (Pb-free)	L16.4x4
ISL6292-1CR5*	629 2-1CR5	-20 to +70	16 Ld 5x5 QFN	L16.5x5B
ISL6292-1CR5Z* (Note)	6292-1CR5Z	-20 to +70	16 Ld 5x5 QFN (Pb-free)	L16.5x5B
ISL6292-2CR5*	629 2-2CR5	-20 to +70	16 Ld 5x5 QFN	L16.5x5B
ISL6292-2CR5Z* (Note)	6292-2CR5Z	-20 to +70	16 Ld 5x5 QFN (Pb-free)	L16.5x5B
ISL6292EVAL1Z	Evaluation Board for the 3x3 DFN Package Part			
ISL6292EVAL2	Evaluation Board for the 4x4 QFN Package Part			

*Add “-T” suffix for tape and reel. Please refer to TB347 for details on reel specifications.

NOTE: These Intersil Pb-free plastic packaged products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate PLUS ANNEAL - e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Absolute Maximum Ratings

Supply Voltage (VIN) . . . . . -0.3V to 7V
Output Pin Voltage (BAT) . . . . . -0.3V to 5.5V
Signal Input Voltage (TOEN, TIME, IREF, IMIN) . . . . . -0.3V to 3.2V
Output Pin Voltage (STATUS, FAULT) . . . . . -0.3V to 7V
Charge Current (For 4x4 or 5x5 QFN Packages) 2.1A
Charge Current (For 3x3 DFN Package) 1.6A

Recommended Operating Conditions

Ambient Temperature Range . . . . . -20°C to +70°C
Supply Voltage, VIN . . . . . 4.3V to 6.5V

Thermal Information

Thermal Resistance (Junction to Ambient)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
5x5 QFN Package (Notes 1, 2)	34	4
4x4 QFN Package (Notes 1, 2)	41	4
3x3 DFN Package (Notes 1, 2)	46	4

Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
Pb-free reflow profile . . . . . .see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
2. θ_{JC}, “case temperature” location is at the center of the exposed metal pad on the package underside. See Tech Brief TB379.

Electrical Specifications

Typical values are tested at V_{IN} = 5V and +25°C Ambient Temperature, maximum and minimum values are guaranteed over 0°C to +70°C Ambient Temperature with a supply voltage in the range of 4.3V to 6.5V, unless otherwise noted.

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
POWER-ON RESET						
Rising VIN Threshold			3.0	3.4	4.0	V
Falling VIN Threshold			2.11	2.4	2.65	V
STANDBY CURRENT						
VBAT Pin Sink Current	$I_{STANDBY}$	VIN floating or EN = LOW	-	-	3.0	µA
VIN Pin Supply Current	I_{VIN}	VBAT floating and EN pulled low	-	30	-	µA
VIN Pin Supply Current	I_{VIN}	VBAT floating and EN floating	-	1	-	mA
VOLTAGE REGULATION						
Output Voltage	V_{CH}	ISL6292-1	4.059	4.10	4.141	V
Output Voltage	V_{CH}	ISL6292-2	4.158	4.20	4.242	V
Dropout Voltage		VBAT = 3.7V, 0.5A, 4x4 or 5x5 package	-	140	-	mV
Dropout Voltage		VBAT = 3.7V, 0.5A, 3x3 package	-	175	-	mV
CHARGE CURRENT						
Constant Charge Current	I_{CHARGE}	R_{IREF} = 80kΩ, V_{BAT} = 3.7V	0.9	1.0	1.1	A
Trickle Charge Current	$I_{TRICKLE}$	R_{IREF} = 80kΩ, V_{BAT} = 2.0V	-	110	-	mA
Constant Charge Current	I_{CHARGE}	IREF Pin Voltage > 1.2V, V_{BAT} = 3.7V	400	450	520	mA
Trickle Charge Current	$I_{TRICKLE}$	IREF Pin Voltage > 1.2V, V_{BAT} = 2.0V	-	45	-	mA
Constant Charge Current	I_{CHARGE}	IREF Pin Voltage < 0.4V, V_{BAT} = 3.7V	-	-	100	mA
Trickle Charge Current	$I_{TRICKLE}$	IREF Pin Voltage < 0.4V, V_{BAT} = 2.0V	-	10	-	mA
End-of-Charge Threshold		R_{IMIN} = 80kΩ	85	110	135	mA
RECHARGE THRESHOLD						
Recharge Voltage Threshold	V_{RECHRG}	ISL6292-2	-	4.0	-	V
Recharge Voltage Threshold	V_{RECHRG}	ISL6292-1	-	3.90	-	V

Electrical Specifications

Typical values are tested at V_{IN} = 5V and +25°C Ambient Temperature, maximum and minimum values are guaranteed over 0°C to +70°C Ambient Temperature with a supply voltage in the range of 4.3V to 6.5V, unless otherwise noted. **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
TRICKLE CHARGE THRESHOLD						
Trickle Charge Threshold Voltage	V_{MIN}		2.7	2.8	3.0	V
TEMPERATURE MONITORING						
Low Battery Temperature Threshold	V_{TMIN}	V2P8 = 3.0V	1.45	1.51	1.57	V
High Battery Temperature Threshold	V_{TMAX}	V2P8 = 3.0V	0.36	0.38	0.40	V
Battery Removal Threshold	V_{RMV}	V2P8 = 3.0V	-	2.25	-	V
Charge Current Foldback Threshold	T_{FOLD}		85	100	115	°C
Current Foldback Gain	G_{FOLD}		-	100	-	mA/°C
OSCILLATOR						
Oscillation Period	t_{OSC}	C_{TIME} = 15nF	2.4	3.0	3.6	ms
LOGIC INPUT AND OUTPUT						
TOEN Input High			2.0	-	-	V
TOEN and EN Input Low			-	-	0.8	V
IREF and IMIN Input High			1.2	-	-	V
IREF and IMIN Input Low			-	-	0.4	V
STATUS/FAULT Sink Current		Pin Voltage = 0.8V	5	-	-	mA

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = +25°C, R_{IREF} = R_{IMIN} = 80kΩ, V_{BAT} = 3.7V, Unless Otherwise Noted.

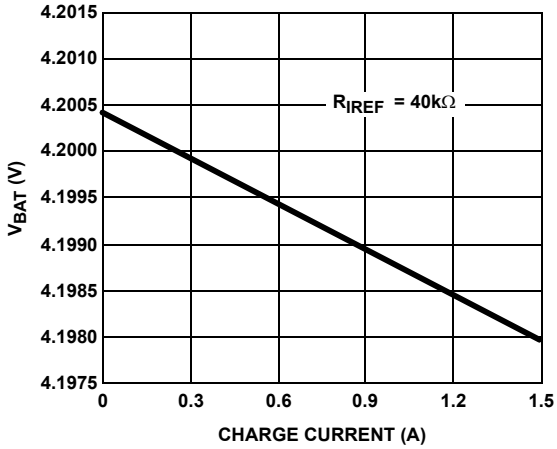


FIGURE 1. CHARGER OUTPUT VOLTAGE vs CHARGE CURRENT

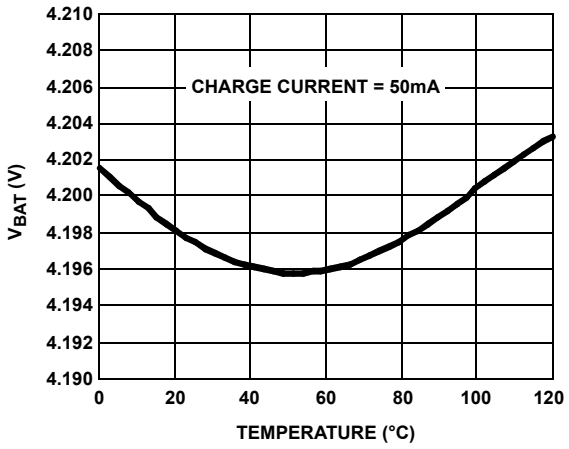


FIGURE 2. CHARGER OUTPUT VOLTAGE vs TEMPERATURE

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = +25°C, R_{IREF} = R_{IMIN} = 80kΩ, V_{BAT} = 3.7V, Unless Otherwise Noted. **(Continued)**

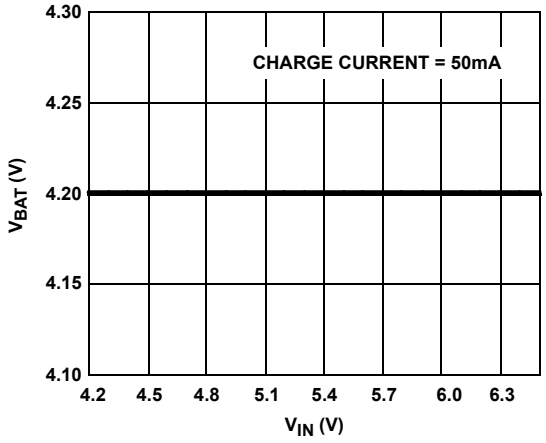


FIGURE 3. CHARGER OUTPUT VOLTAGE vs INPUT VOLTAGE CHARGE CURRENT = 50mA

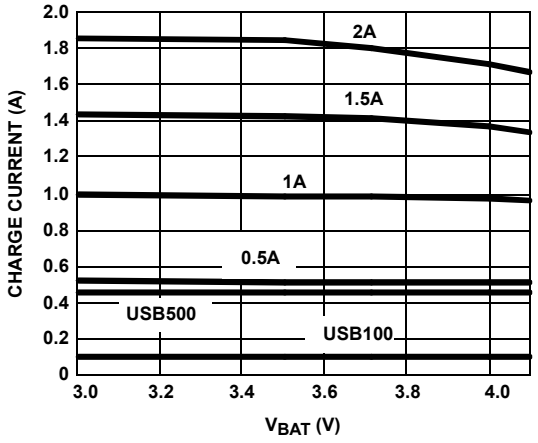


FIGURE 4. CHARGE CURRENT vs OUTPUT VOLTAGE

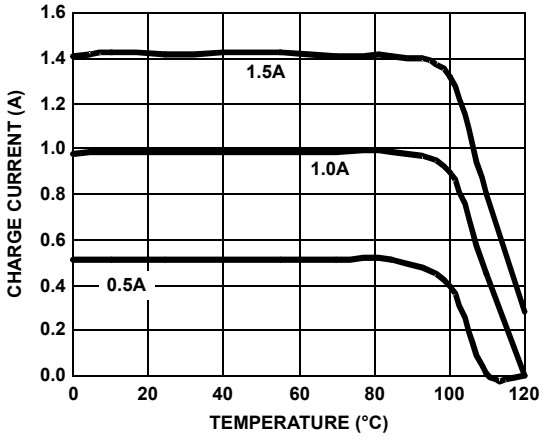


FIGURE 5. CHARGE CURRENT vs AMBIENT TEMPERATURE

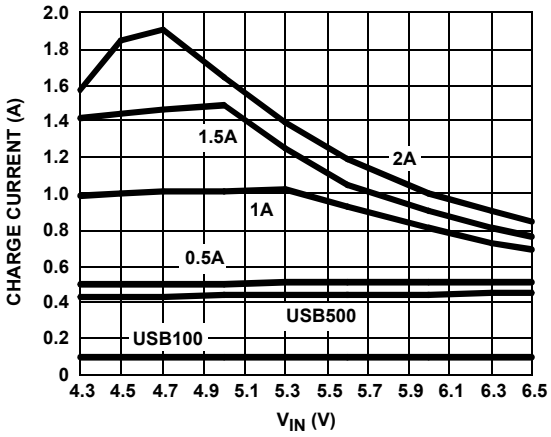


FIGURE 6. CHARGE CURRENT vs INPUT VOLTAGE

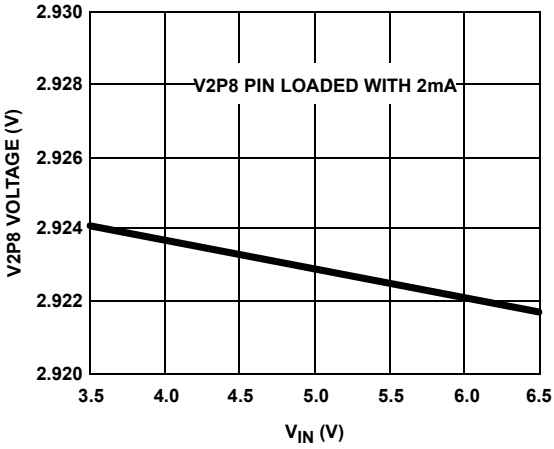


FIGURE 7. V2P8 OUTPUT vs INPUT VOLTAGE

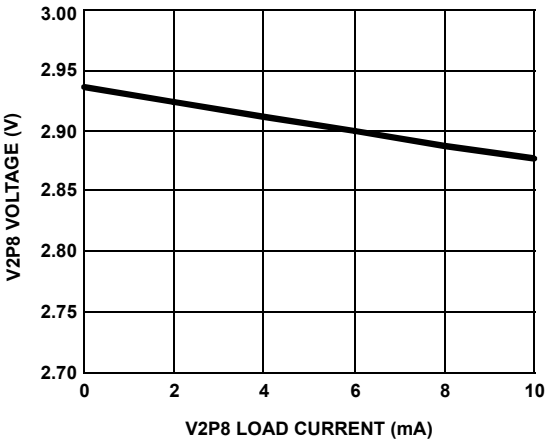


FIGURE 8. V2P8 OUTPUT vs ITS LOAD CURRENT

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = +25°C, R_{IREF} = R_{IMIN} = 80kΩ, V_{BAT} = 3.7V, Unless Otherwise Noted. **(Continued)**

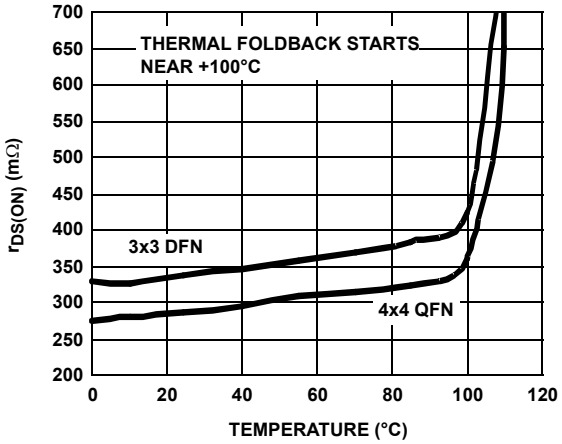


FIGURE 9. $r_{DS(ON)}$ vs TEMPERATURE AT 3.7V OUTPUT

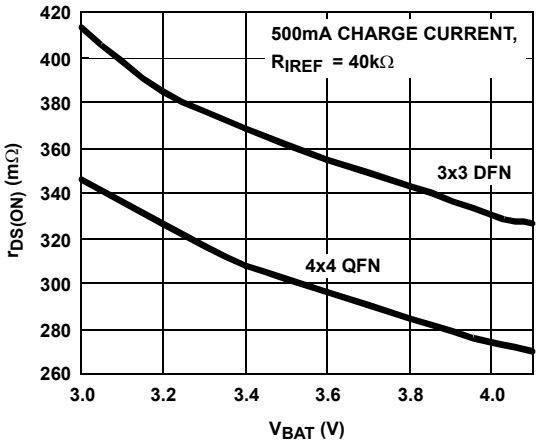


FIGURE 10. $r_{DS(ON)}$ vs OUTPUT VOLTAGE USING CURRENT LIMITED ADAPTERS

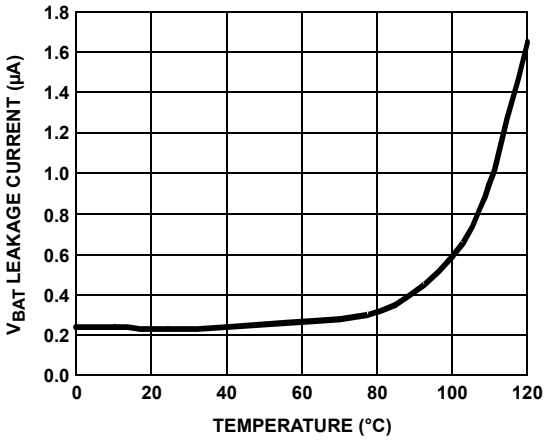


FIGURE 11. REVERSE CURRENT vs TEMPERATURE

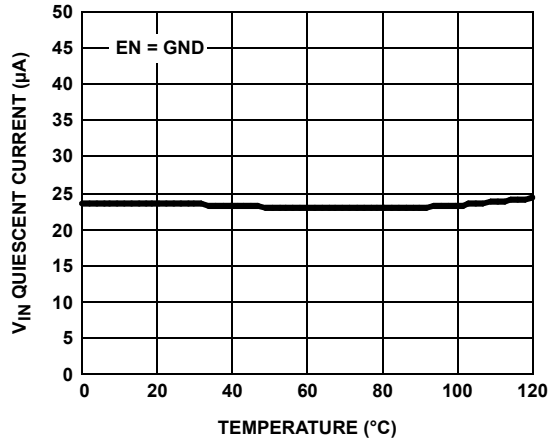


FIGURE 12. INPUT QUIESCENT CURRENT vs TEMPERATURE

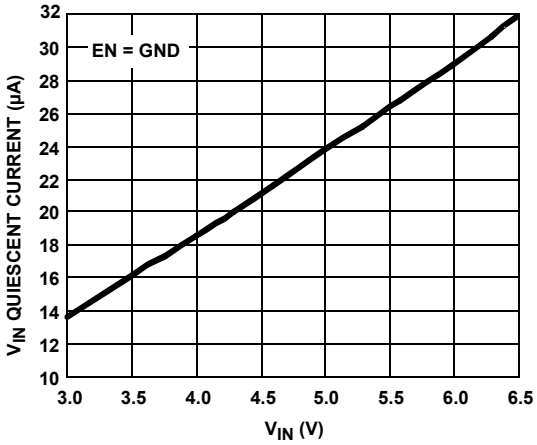


FIGURE 13. INPUT QUIESCENT CURRENT vs INPUT VOLTAGE WHEN SHUTDOWN

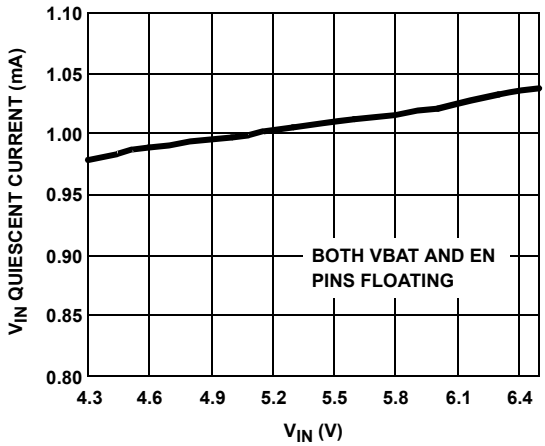


FIGURE 14. INPUT QUIESCENT CURRENT vs INPUT VOLTAGE WHEN NOT SHUTDOWN

Typical Operating Performance

The test conditions for the Typical Operating Performance are: V_{IN} = 5V, T_A = +25°C, R_{IREF} = R_{IMIN} = 80kΩ, V_{BAT} = 3.7V, Unless Otherwise Noted. **(Continued)**

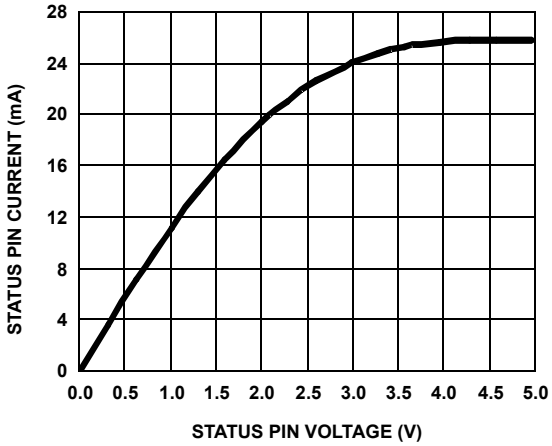


FIGURE 15. STATUS/FAULT PIN VOLTAGE vs CURRENT WHEN THE OPEN-DRAIN MOSFET TURNS ON

Pin Descriptions

VIN (Pin 1, 15, 16 for 4x4, 5x5; Pin 1 for 3x3)

VIN is the input power source. Connect to a wall adapter.

$\overline{FAULT}$ (Pin 2)

FAULT is an open-drain output indicating fault status. This pin is pulled to LOW under any fault conditions.

$\overline{STATUS}$ (Pin 3)

STATUS is an open-drain output indicating charging and inhibit states. The $\overline{STATUS}$ pin is pulled LOW when the charger is charging a battery.

Time (Pin 4)

The TIME pin determines the oscillation period by connecting a timing capacitor between this pin and GND. The oscillator also provides a time reference for the charger.

GND (Pin 5)

GND is the connection to system ground.

TOEN (Pin 6 for 4x4, 5x5; N/A for 3x3)

TOEN is the TIMEOUT enable input pin. Pulling this pin to LOW disables the TIMEOUT charge-time limit for the fast charge modes. Leaving this pin HIGH or floating enables the TIMEOUT limit.

EN (Pin 7 for 4x4, 5x5; Pin 6 for 3x3)

EN is the enable logic input. Connect the EN pin to LOW to disable the charger or leave it floating to enable the charger.

V2P8 (Pin 8 for 4x4, 5x5; Pin 7 for 3x3)

This is a 2.8V reference voltage output. This pin outputs a 2.8V voltage source when the input voltage is above POR threshold and outputs zero otherwise. The V2P8 pin can be used as an indication for adapter presence.

IREF (Pin 9 for 4x4, 5x5; Pin 8 for 3x3)

This is the programming input for the constant charging current.

IMIN (Pin 10 for 4x4, 5x5; N/A for 3x3)

IMIN is the programmable input for the end-of-charge current.

TEMP (Pin 11 for 4x4, 5x5; Pin 9 for 3x3)

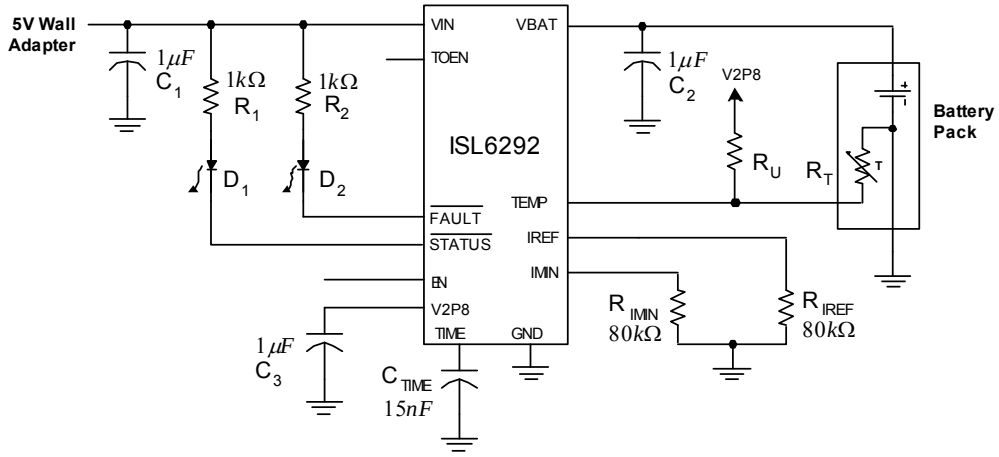
TEMP is the input for an external NTC thermistor. The TEMP pin is also used for battery removal detection.

VBAT (Pin 12, 13, 14 for 4x4, 5x5; Pin 10 for 3x3)

VBAT is the connection to the battery. Typically a 10µF Tantalum capacitor is needed for stability when there is no battery attached. When a battery is attached, only a 0.1µF ceramic capacitor is required.

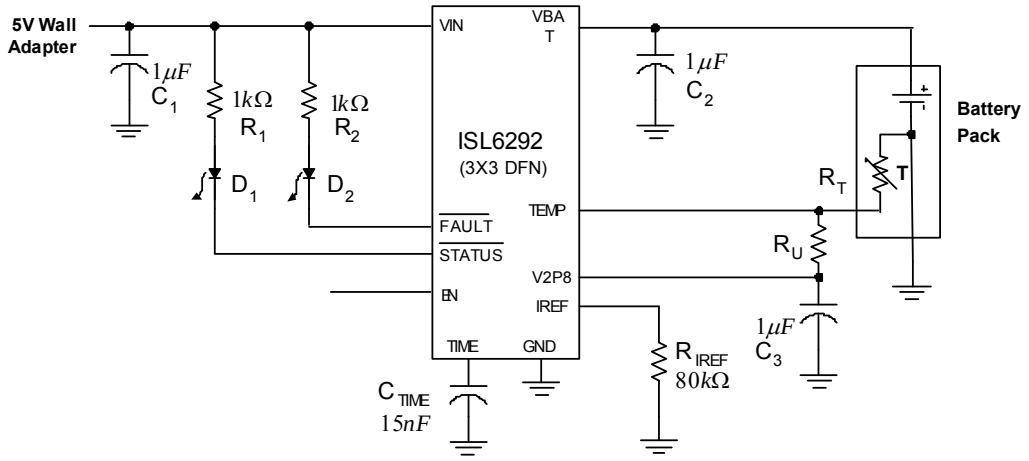
Typical Applications

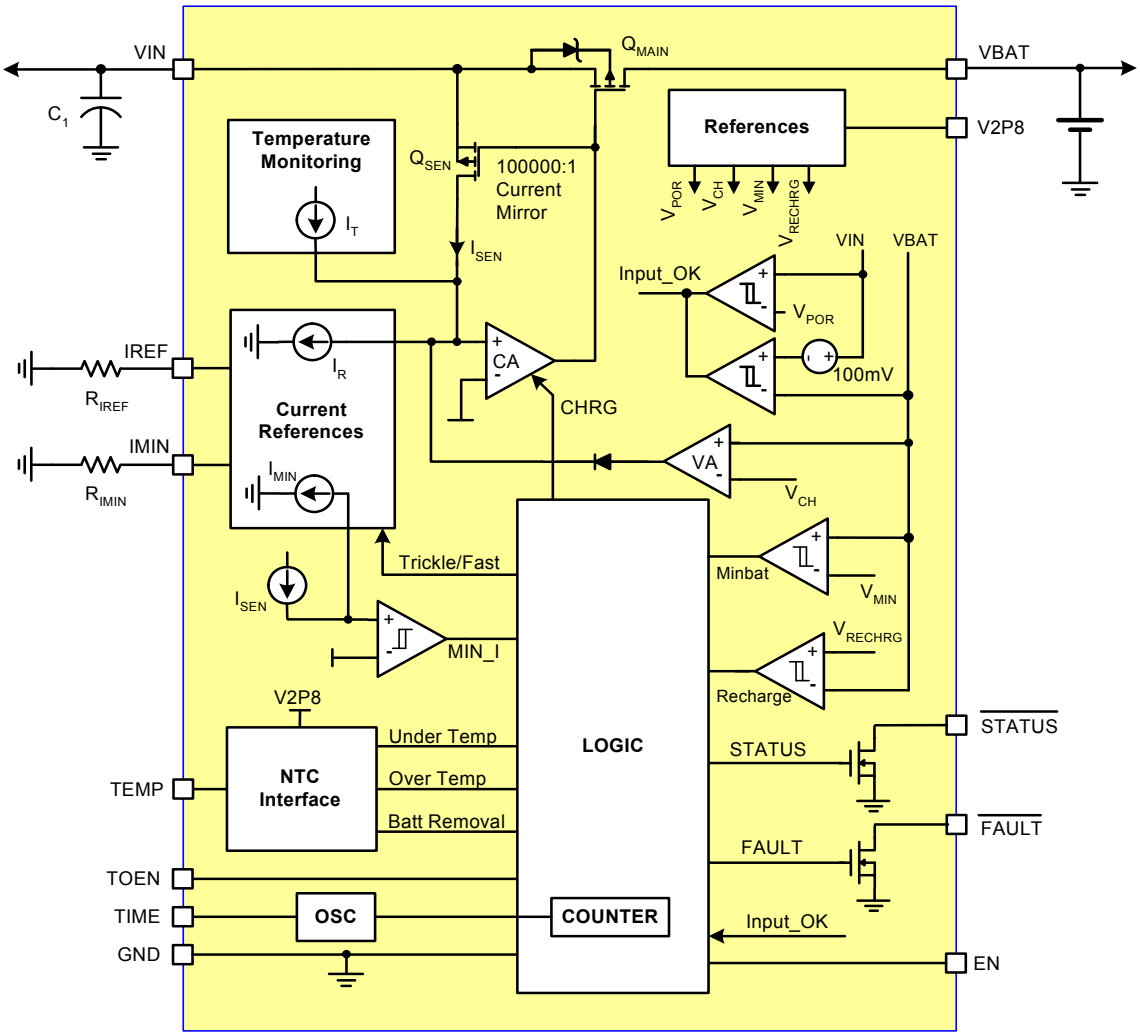
Typical Application Circuit For 4x4 or 5x5 QFN Package Options



Typical Applications (Continued)

Typical Application Circuit For 3x3 DFN Package Option





NOTE: For the 3x3 DFN package, the TOEN pin is left floating and the IMIN pin is connected to the V2P8 pin internally.

FIGURE 16. BLOCK PROGRAM

Theory of Operation

The ISL6292 is an integrated charger for single-cell Li-ion or Li-polymer batteries. The ISL6292 functions as a traditional linear charger when powered with a voltage-source adapter. When powered with a current-limited adapter, the charger minimizes the thermal dissipation commonly seen in traditional linear chargers.

As a linear charger, the ISL6292 charges a battery in the popular constant current (CC) and constant voltage (CV) profile. The constant charge current I_{REF} is programmable up to 2A (1.5A for the 3x3 DFN package) with an external resistor or a logic input. The charge voltage V_{CH} has 1% accuracy over the entire recommended operating condition range. The charger always preconditions the battery with 10% of the programmed current at the beginning of a charge cycle, until the battery voltage is verified to be above the minimum fast charge voltage, V_{MIN}. This low-current preconditioning charge mode is named trickle mode. The verification takes 15 cycles of an internal oscillator whose period is programmable with the timing capacitor. A thermal-foldback feature removes the thermal concern typically seen in linear chargers. The charger reduces the charge current automatically as the IC internal temperature rises above +100°C to prevent further temperature rise. The thermal-foldback feature guarantees safe operation when the printed circuit board (PCB) is space limited for thermal dissipation.

A TEMP pin monitors the battery temperature to ensure a safe charging temperature range. The temperature range is programmable with an external negative temperature coefficient (NTC) thermistor. The TEMP pin is also used to detect the removal of the battery.

The charger offers a safety timer for setting the fast charge time (TIMEOUT) limit to prevent charging a dead battery for an extensively long time. The TIMEOUT limit can be disabled as needed by the TOEN pin. The trickle mode is limited to 1/8 of TIMEOUT and **cannot** be disabled by the TOEN pin.

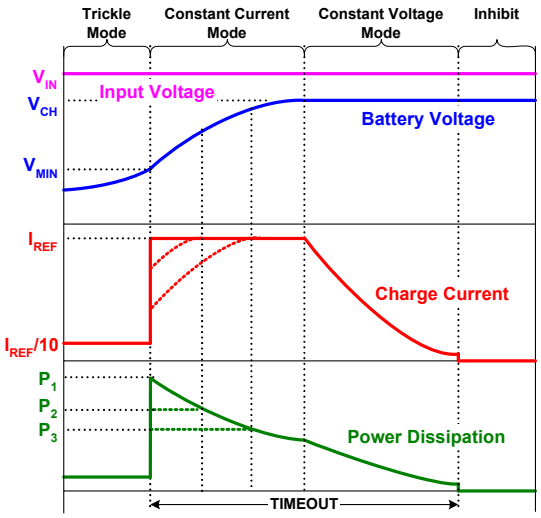


FIGURE 17. TYPICAL CHARGE CURVES USING A CONSTANT-VOLTAGE ADAPTER

The charger automatically re-charges the battery when the battery voltage drops below a recharge threshold. When the wall adapter is not present, the ISL6292 draws less than 1µA current from the battery.

Three indication pins are available from the charger to indicate the charge status. The V2P8 outputs a 2.8VDC voltage when the input voltage is above the power-on reset (POR) level and can be used as the power-present indication. This pin is capable of sourcing a 2mA current, so it can also be used to bias external circuits. The STATUS pin is an open-drain logic output that turns LOW at the beginning of a charge cycle until the end-of-charge (EOC) condition is qualified. The EOC condition is: the battery voltage rises above the recharge threshold and the charge current falls below a user-programmable EOC current threshold. Once the EOC condition is qualified, the STATUS output rises to HIGH and is latched. The latch is released at the beginning of a charge or re-charge cycle. The open-drain FAULT pin turns low when any fault conditions occur. The fault conditions include the external battery temperature fault, a charge time fault, or the battery removal.

Figure 17 shows the typical charge curves in a traditional linear charger powered with a constant-voltage adapter. From top to bottom, the curves represent the constant input voltage, the battery voltage, the charge current and the power dissipation in the charger. The power dissipation P_{CH} is given by Equation 1:

$$P_{CH} = (V_{IN}-V_{BAT}) \cdot I_{CHARGE} \quad \text{(EQ. 1)}$$

where I_{CHARGE} is the charge current. The maximum power dissipation occurs during the beginning of the CC mode. The maximum power the IC is capable of dissipating is dependent on the thermal impedance of the printed-circuit board (PCB). Figure 17 shows (with dotted lines) two cases that the charge currents are limited by the maximum power dissipation capability due to the thermal foldback.

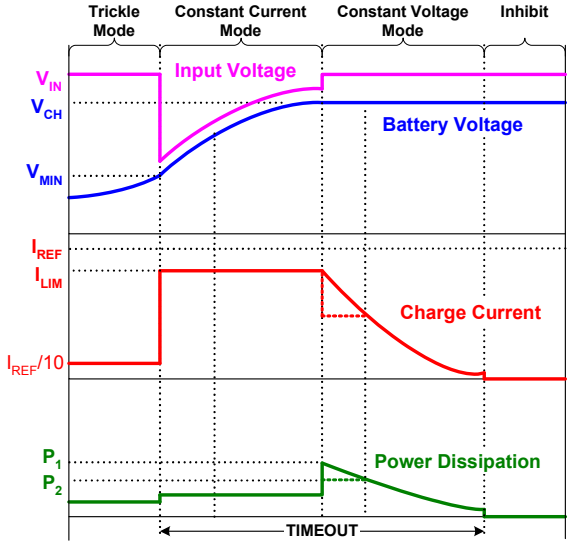


FIGURE 18. TYPICAL CHARGE CURVES USING A CURRENT-LIMITED ADAPTER

When using a current-limited adapter, the thermal situation in the ISL6292 is totally different. Figure 18 shows the typical charge curves when a current-limited adapter is employed. The operation requires the I_{REF} to be programmed higher than the limited current I_{LIM} of the adapter, as shown in Figure 18. The key difference of the charger operating under such conditions occurs during the CC mode.

The Block Diagram (Figure 16) aids in understanding the operation. The current loop consists of the current amplifier CA and the sense MOSFET Q_{SEN}. The current reference I_R is programmed by the IREF pin. The current amplifier CA regulates the gate of the sense MOSFET Q_{SEN} so that the sensed current I_{SEN} matches the reference current I_R. The main MOSFET Q_{MAIN} and the sense MOSFET Q_{SEN} form a current mirror with a ratio of 100,000:1, that is, the output charge current is 100,000 times I_R. In the CC mode, the current loop tries to increase the charge current by enhancing the sense MOSFET Q_{SEN}, so that the sensed current matches the reference current. On the other hand, the adapter current is limited, the actual output current will never meet what is required by the current reference. As a result, the current error amplifier CA keeps enhancing the Q_{SEN} as well as the main MOSFET Q_{MAIN}, until they are fully turned on. Therefore, the main MOSFET becomes a power switch instead of a linear regulation device. The power dissipation in the CC mode becomes Equation 2:

$$P_{CH} = r_{DS(ON)} \cdot I_{CHARGE}^2 \quad \text{(EQ. 2)}$$

where $r_{DS(ON)}$ is the resistance when the main MOSFET is fully turned on. This power is typically much less than the peak power in the traditional linear mode.

The worst power dissipation when using a current-limited adapter typically occurs at the beginning of the CV mode, as shown in Figure 18. Equation 1 applies during the CV mode. When using a very small PCB whose thermal impedance is relatively large, it is possible that the internal temperature can still reach the thermal foldback threshold. In that case, the IC is thermally protected by lowering the charge current, as shown with the dotted lines in the charge current and power curves. Appropriate design of the adapter can further reduce the peak power dissipation of the ISL6292. See“Applications Information” on page 11 for more information.

Figure 19 illustrates the typical signal waveforms for the linear charger from the power-up to a recharge cycle. More detailed Applications Information is given in the following.

Applications Information

Power on Reset (POR)

The ISL6292 resets itself as the input voltage rises above the POR rising threshold. The V2P8 pin outputs a 2.8V voltage, the internal oscillator starts to oscillate, the internal timer is reset, and the charger begins to charge the battery.

The two indication pins, STATUS and FAULT, indicate a LOW and a HIGH logic signal respectively. Figure 19 illustrates the start-up of the charger between t_0 to t_2.

The ISL6292 has a typical rising POR threshold of 3.4V and a falling POR threshold of 2.4V. The 2.4V falling threshold guarantees charger operation with a current-limited adapter to minimize the thermal dissipation.

Charge Cycle

A charge cycle consists of three charge modes: trickle mode, constant current (CC) mode, and constant voltage (CV) mode. The charge cycle always starts with the trickle mode until the battery voltage stays above V_{MIN} (2.8V typical) for 15 consecutive cycles of the internal oscillator. If the battery voltage drops below V_{MIN} during the 15 cycles, the 15-cycle counter is reset and the charger stays in the trickle mode. The charger moves to the CC mode after verifying the battery voltage. As the battery-pack terminal voltage rises to the final charge voltage V_{CH}, the CV mode begins. The terminal voltage is regulated at the constant V_{CH} in the CV mode and the charge current is expected to decline. After the charge current drops below I_{MIN} (programmable for the 4x4 and 5x5 package and programmed to 1/10 of I_{REF} for the 3x3 package; see “End-of-Charge (EOC) Current” on page 13 for more detail), the ISL6292 indicates the end-of-charge (EOC) with the STATUS pin. The charging actually does not terminate until the internal timer completes its length of TIMEOUT in order to bring the battery to its full capacity. Signals in a charge cycle are illustrated in Figure 19 between points t_2 to t_5.

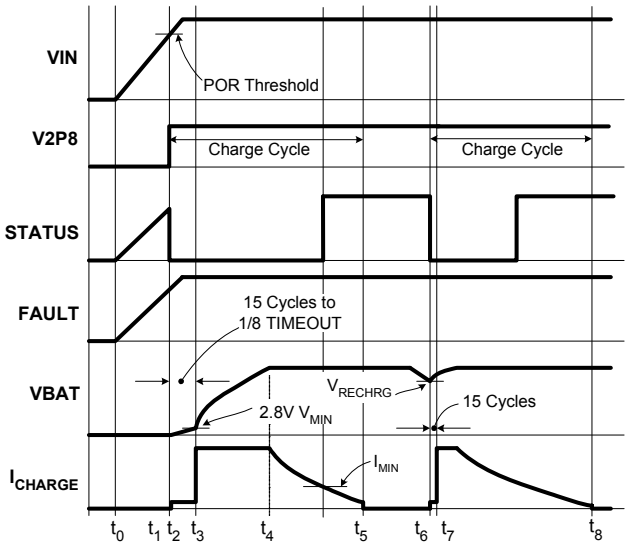


FIGURE 19. OPERATION WAVEFORMS

The following events initiate a new charge cycle:

- POR,
- a new battery being inserted (detected by TEMP pin),
- the battery voltage drops below a recharge threshold after completing a charge cycle,
- recovery from an battery over-temperature fault,
- or, the EN pin is toggled from GND to floating.

Further description of these events are given later in this data sheet.

Recharge

After a charge cycle completes, charging is prohibited until the battery voltage drops to a recharge threshold, V_{RECHRG} (see "Electrical Specifications" on page 3). Then a new charge cycle starts at point t_6 and ends at point t_8, as shown in Figure 19. The safety timer is reset at t_6.

Internal Oscillator

The internal oscillator establishes a timing reference. The oscillation period is programmable with an external timing capacitor, C_{TIME}, as shown in Typical Applications. The oscillator charges the timing capacitor to 1.5V and then discharges it to 0.5V in one period, both with 10µA current. The period t_{OSC} is:

$$t_{OSC} = 0.2 \cdot 10^6 \cdot C_{TIME} \quad \text{(seconds)} \qquad \text{(EQ. 3)}$$

A 1nF capacitor results in a 0.2ms oscillation period. The accuracy of the period is mainly dependent on the accuracy of the capacitance and the internal current source.

Total Charge Time

The total charge time for the CC mode and CV mode is limited to a length of TIMEOUT. A 22-stage binary counter increments each oscillation period of the internal oscillator to set the TIMEOUT. The TIMEOUT can be calculated as:

$$TIMEOUT = 2^{22} \cdot t_{OSC} = 14 \cdot \frac{C_{TIME}}{1nF} \quad \text{(minutes)} \qquad \text{(EQ. 4)}$$

A 1nF capacitor leads to 14 minutes of TIMEOUT. For example, a 15nF capacitor sets the TIMEOUT to be 3.5 hours. The charger has to reach the end-of-charge condition before the TIMEOUT, otherwise, a TIMEOUT fault is issued. The TIMEOUT fault latches up the charger. There are two ways to release such a latch-up: either to recycle the input power, or toggle the EN pin to disable the charger and then enable it again.

The trickle mode charge has a time limit of 1/8 TIMEOUT. If the battery voltage does not reach V_{MIN} within this limit, a TIMEOUT fault is issued and the charger latches up. The charger stays in trickle mode for at least 15 cycles of the internal oscillator and, at most, 1/8 of TIMEOUT, as shown in Figure 19.

Disabling TIMEOUT Limit

The TIMEOUT limit for the fast charge modes can be disabled by pulling the TOEN pin to LOW or shorting it to GND. When this happens, the charger becomes a current-limited LDO (low-dropout) supply with its voltage regulated at the final charge voltage V_{CH} and the current limit determined by the IREF pin. If the LDO load current drops below the end-of-charge current (refer to "End-of-Charge (EOC) Current" on page 13), the STATUS pin will indicate.

The trickle charge time limit, however, is not disabled even when the TOEN pin is pulled to LOW. The charger operates in the trickle mode at the beginning of a charge cycle even if the TIMEOUT is disabled. Leaving the TOEN pin floating is recommended to enable the TIMEOUT. Driving the TOEN pin above 3.0V is not recommended.

Charge Current Programming

The charge current is programmed by the IREF pin. There are three ways to program the charge current:

1. Driving the IREF pin above 1.3V
2. Driving the IREF pin below 0.4V,
3. or using the R_{IREF} as shown in "Typical Applications" on page 8.

The voltage of IREF is regulated to a 0.8V reference voltage when not driven by any external source. The charging current during the constant current mode is 100,000 times that of the current in the R_{IREF} resistor. Hence, depending on how IREF pin is used, the charge current is:

$$I_{REF} = \begin{cases} 500mA & V_{IREF} > 1.3V \\ \frac{0.8V}{R_{IREF}} \times 10^5 (A) & R_{IREF} \\ 100mA & V_{IREF} < 0.4V \end{cases} \qquad \text{(EQ. 5)}$$

The 500mA current is a guaranteed maximum value for the high-power USB port, with the typical value of 450mA. The 100mA current is also a guaranteed maximum value for the low-power USB port. This design accommodates the USB power specification.

The internal reference voltage at the IREF pin is capable of sourcing less than 100µA current. When pulling down the IREF pin with a logic circuit, the logic circuit needs to be able to sink at least 100µA current.

When the adapter is current limited, it is recommended that the reference current be programmed to at least 30% higher than the adapter current limit (which equals the charge current). In addition, the charge current should be at least 350mA so that the voltage difference between the VIN and the VBAT pins is higher than 100mV. The 100mV is the offset voltage of the input-output voltage comparator shown in the block diagram on page 9.

End-of-Charge (EOC) Current

The end-of-charge current I_{MIN} sets the level at which the charger starts to indicate the end of the charge with the STATUS pin, as shown in Figure 19. The charger actually does not terminate charging until the end of the TIMEOUT, as described in "Total Charge Time" on page 12. The I_{MIN} is set in two ways, by connecting a resistor between the IMIN pin and ground, or by connecting the IMIN pin to the V2P8 pin. When programming with the resistor, the I_{MIN} is set in Equation 6.

$$I_{MIN} = 10000 \cdot \frac{V_{REF}}{R_{IMIN}} = \frac{0.8V}{R_{IMIN}} \times 10^4 (A) \quad \text{(EQ. 6)}$$

where R_{IMIN} is the resistor connected between the IMIN pin and the ground. When connected to the V2P8 pin, the I_{MIN} is set to 1/10 of I_{REF}, except when the IREF pin is shorted to GND. Under this exception, I_{MIN} is 5mA. For the ISL6292 in the 3x3 DFN package, the IMIN pin is bonded internally to V2P8.

Charge Current Thermal Foldback

Over-heating is always a concern in a linear charger. The maximum power dissipation usually occurs at the beginning of a charge cycle when the battery voltage is at its minimum but the charge current is at its maximum. The charge current thermal foldback function in the ISL6292 frees users from the over-heating concern.

Figure 20 shows the current signals at the summing node of the current error amplifier CA in the Block Diagram shown on page 9. I_R is the reference and I_T is the current from the Temperature Monitoring block. The I_T has no impact on the charge current until the internal temperature reaches approximately +100°C; then I_T rises at a rate of 1µA/°C. When I_T rises, the current control loop forces the sensed current I_{SEN} to reduce at the same rate. As a mirrored current, the charge current is 100,000 times that of the sensed current and reduces at a rate of 100mA/°C. For a charger with the constant charge current set at 1A, the charge current is reduced to zero when the internal temperature rises to +110°C. The actual charge current settles between +100°C to +110°C.

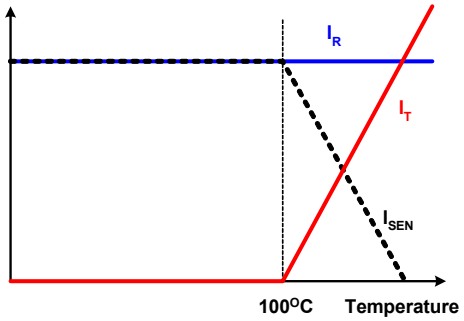


FIGURE 20. CURRENT SIGNALS AT THE AMPLIFIER CA INPUT

Usually the charge current should not drop below I_{MIN} because of the thermal foldback. For some extreme cases (if that does happen) the charger does not indicate end-of-charge unless the battery voltage is already above the recharge threshold.

2.8V Bias Voltage

The ISL6292 provides a 2.8V voltage for biasing the internal control and logic circuit. This voltage is also available for external circuits such as the NTC thermistor circuit. The maximum allowed external load is 2mA.

NTC Thermistor

The ISL6292 uses two comparators (CP2 and CP3) to form a window comparator, as shown in Figure 22. When the TEMP pin voltage is "out of the window," determined by the V_{TMIN} and V_{TMAX}, the ISL6292 stops charging and indicates a fault condition. When the temperature returns to the set range, the charger re-starts a charge cycle. The two MOSFETs, Q1 and Q2, produce hysteresis for both upper and lower thresholds. The temperature window is shown in Figure 21.

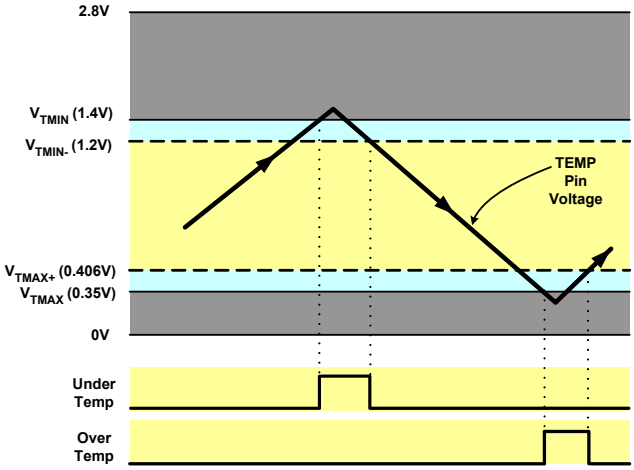


FIGURE 21. CRITICAL VOLTAGE LEVELS FOR TEMP PIN

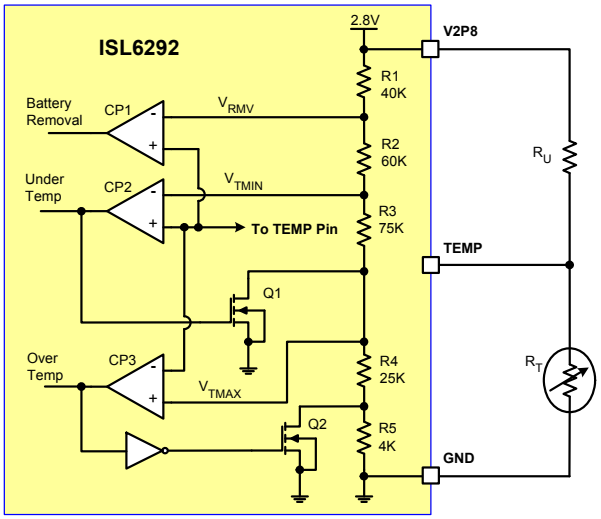


FIGURE 22. THE INTERNAL AND EXTERNAL CIRCUIT FOR THE NTC INTERFACE

As the TEMP pin voltage rises from low and exceeds the 1.4V threshold, the under temperature signal rises and does not clear until the TEMP pin voltage falls below the 1.2V falling threshold. Similarly, the over-temperature signal is given when the TEMP pin voltage falls below the 0.35V threshold and does

not clear until the voltage rises above 0.406V. The actual accuracy of the 2.8V is **not important** because all the thresholds and the TEMP pin voltage are ratios determined by the resistor dividers, as shown in Figure 22.

The NTC thermistor is required to have a resistance ratio of 7:1 at the low and the high temperature limits, that is:

$$\frac{R_{COLD}}{R_{HOT}} = 7 \quad \text{(EQ. 7)}$$

This is because at the low temperature limit, the TEMP pin voltage is 1.4V, which is 1/2 of the 2.8V bias. Thus:

$$R_{COLD} = R_U \quad \text{(EQ. 8)}$$

where R_U is the pull-up resistor as shown in Figure 22. On the other hand, at the high temperature limit the TEMP pin voltage is 0.35V, 1/8 of the 2.8V bias. Therefore:

$$R_{HOT} = \frac{R_U}{7} \quad \text{(EQ. 9)}$$

Various NTC thermistors are available for this application. Table 1 shows the resistance ratio and the negative temperature coefficient of the curve-1 NTC thermistor from Vishay (http://www.vishay.com) at various temperatures. The resistance at +3°C is approximately seven times the resistance at +47°C, which is shown in Equation 10:

$$\frac{R_{3°C}}{R_{47°C}} = 7 \quad \text{(EQ. 10)}$$

Therefore, if +3°C is the low temperature limit, then the high temperature limit is approximately +47°C. The pull-up resistor R_U can choose the same value as the resistance at +3°C.

TABLE 1. RESISTANCE RATIO OF VISHAY'S CURVE-1 NTC

TEMPERATURE (°C)	$R_T/R_{25°C}$	NTC (%/°C)
0	3.266	5.1
3	2.806	5.1
5	2.540	5.0
25	1.000	4.4
45	0.4368	4.0
47	0.4041	3.9
50	0.3602	3.9

The temperature hysteresis can be estimated. At the low temperature, the hysteresis is approximately estimated in Equation 11:

$$T_{hysLOW} \approx \frac{1.4V - 1.2V}{1.4V \cdot 0.051} \approx 3 \quad (°C) \quad \text{(EQ. 11)}$$

where 0.051 is the NTC at +3°C. Similarly, the high temperature hysteresis is estimated in Equation 12:

$$T_{hysHIGH} \approx \frac{0.406V - 0.35V}{0.35V \cdot 0.039} \approx 4 \quad (°C) \quad \text{(EQ. 12)}$$

where the 0.039 is the NTC at +47°C.

For applications that do not need to monitor the battery temperature, the NTC thermistor can be replaced with a regular resistor of a half value of the pull-up resistor R_U. Another option is to connect the TEMP pin to the IREF pin that has a 0.8V output. With such connection, the IREF pin can no longer be programmed with logic inputs.

Battery Removal Detection

The ISL6292 assumes that the thermistor is co-packed with the battery and is removed together with the battery. When the charger senses a TEMP pin voltage that is 2.1V or higher, it assumes that the battery is removed. The battery removal detection circuit is also shown in Figure 22. When a battery is removed, a FAULT signal is indicated and charging is halted. When a battery is inserted again, a new charge cycle starts.

Indications

The ISL6292 has three indications: the input presence, the charge status, and the fault indication. The input presence is indicated by the V2P8 pin while the other two indications are presented by the STATUS pin and FAULT pin respectively. Figure 23 shows the V2P8 pin voltage vs the input voltage. Table 2 summarizes the other two pins.

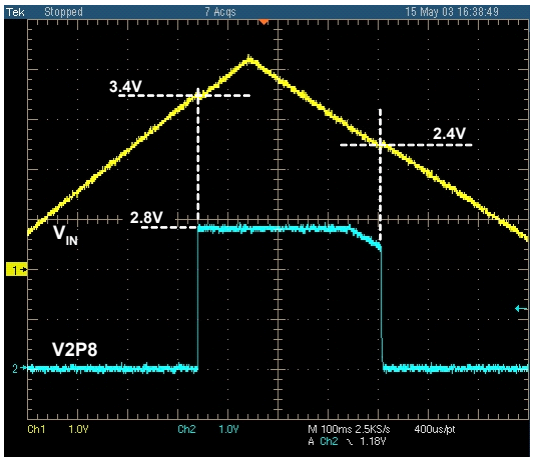


FIGURE 23. THE V2P8 PIN OUTPUT vs THE INPUT VOLTAGE AT THE VIN PIN. VERTICAL: 1V/DIV, HORIZONTAL: 100ms/DIV

Shutdown

The ISL6292 can be shutdown by pulling the EN pin to ground. When shut down, the charger draws typically less than 30µA current from the input power and the 2.8V output at the V2P8 pin is also turned off. The EN pin needs to be driven with an open-drain or open-collector logic output, so that the EN pin is floating when the charger is enabled.

TABLE 2. STATUS INDICATIONS

FAULT	STATUS	INDICATION
High	High	Charge completed with no fault (Inhibit) or Standby

*Both outputs are pulled up with external resistors.

TABLE 2. STATUS INDICATIONS

FAULT	STATUS	INDICATION
High	Low	Charging in one of the three modes
Low	High	Fault

*Both outputs are pulled up with external resistors.

Input and Output Capacitor Selection

Typically any type of capacitors can be used for the input and the output. Use of a 0.47µF or higher value ceramic capacitor for the input is recommended. When the battery is attached to the charger, the output capacitor can be any ceramic type with the value higher than 0.1µF. However, if there is a chance the charger will be used as an LDO linear regulator, a 10µF tantalum capacitor is recommended.

Current-Limited Adapter

Figure 24 shows the ideal current-voltage characteristics of a current-limited adapter. V_{NL} is the no-load adapter output voltage and V_{FL} is the full load voltage at the current limit I_{LIM}. Before its output current reaches the limit I_{LIM}, the adapter presents the characteristics of a voltage source. The slope r_O represents the output resistance of the voltage supply. For a well regulated supply, the output resistance can be very small, but some adapters naturally have a certain amount of output resistance.

The adapter is equivalent to a current source when running in the constant-current region. Being a current source, its output voltage is dependent on the load, which, in this case, is the charger and the battery. As the battery is being charged, the adapter output rises from a lower voltage in the current-voltage characteristics curve, such as point A, to higher voltage until reaching the breaking point B, as shown in Figure 24.

The adapter is equivalent to a voltage source with output resistance when running in the constant-voltage region; because of this characteristic. As the charge current drops, the adapter output moves from point B to point C, shown in Figure 24.

The battery pack can be approximated as an ideal cell with a lumped-sum resistance in series, also shown in Figure 24. The ISL6292 charger sits between the adapter and the battery.

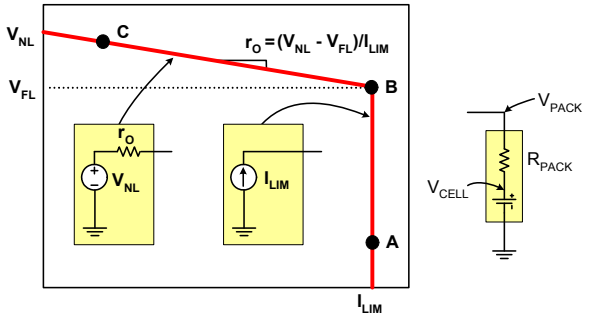


FIGURE 24. THE IDEAL I-V CHARACTERISTICS OF A CURRENT LIMITED ADAPTER

Working with Current-Limited Adapter

As described earlier, the ISL6292 minimizes the thermal dissipation when running off a current-limited AC adapter, as shown in Figure 18. The thermal dissipation can be further reduced when the adapter is properly designed. The following demonstrates that the thermal dissipation can be minimized if the adapter output reaches the full-load output voltage (point B in Figure 24) before the battery pack voltage reaches the final charge voltage (4.1V or 4.2V). The assumptions for the following discussion are: the adapter current limit = 750mA, the battery pack equivalent resistance = 200mΩ, and the charger ON-resistance is 350mΩ.

When charging in the constant-current region, the pass element in the charger is fully turned on. The charger is equivalent to the ON-resistance of the internal P-Channel MOSFET. The entire charging system is equivalent to the circuit shown in Figure 25A. The charge current is the constant current limit I_{LIM}, and the adapter output voltage can be easily found out as calculated in Equation 13:

$$V_{Adapter} = I_{LIM} \cdot r_{DS(ON)} + V_{PACK} \quad \text{(EQ. 13)}$$

where V_{PACK} is the battery pack voltage. The power dissipation in the charger is given in Equation 2, where $I_{CHARGE} = I_{LIM}$.

A critical condition of the adapter design is that the adapter output reaches point B in Figure 24 at the same time as the battery pack voltage reaches the final charge voltage (4.1V or 4.2V), that is:

$$V_{Critical} = I_{LIM} \cdot r_{DS(ON)} + V_{CH} \quad \text{(EQ. 14)}$$

For example, if the final charge voltage is 4.2V, the $r_{DS(ON)}$ is 350mΩ, and the current limit I_{LIM} is 750mA, the critical adapter full-load voltage is 4.4625V.

When the above condition is true, the charger enters the constant-voltage mode simultaneously as the adapter exits the current-limit mode. The equivalent charging system is shown in Figure 25C. Since the charge current drops at a higher rate in the constant-voltage mode than the increase rate of the adapter voltage, the power dissipation decreases as the charge current decreases. Therefore, the worst case thermal dissipation occurs in the constant-current charge mode. Figure 25A shows the I-V curves of the adapter output, the battery pack voltage and the cell voltage during the charge. The 5.9V no-load voltage is just an example value higher than the full-load voltage. The cell voltage 4.05V uses the assumption that the pack resistance is 200mΩ. Figure 26A illustrates the adapter voltage, battery pack voltage, the charge current and the power dissipation in the charger respectively in the time domain.

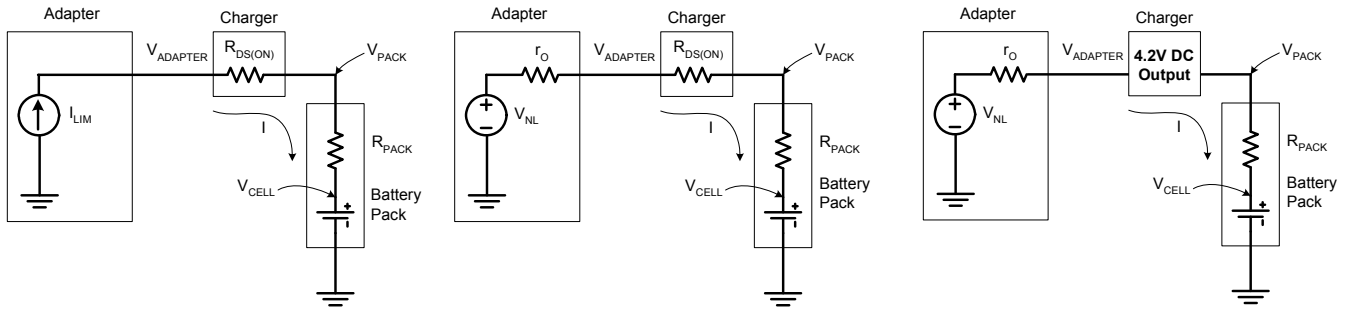


FIGURE 25A. THE EQUIVALENT CIRCUIT IN THE CONSTANT CURRENT REGION

FIGURE 25B. THE EQUIVALENT CIRCUIT IN THE RESISTANCE-LIMIT REGION

FIGURE 25C. THE EQUIVALENT CIRCUIT WHEN THE PACK VOLTAGE REACHES THE FINAL CHARGE VOLTAGE

FIGURE 25. THE EQUIVALENT CIRCUIT OF THE CHARGING SYSTEM WORKING WITH CURRENT LIMITED ADAPTERS

If the battery pack voltage reaches 4.2V (or 4.1V) before the adapter reaches point B in Figure 24, a voltage step is expected at the adapter output when the pack voltage reaches the final charge voltage. As a result, the charger power dissipation is also expected to have a step rise. This case is shown in Figure 18 as well as Figure 27C. Under this condition, the worst case thermal dissipation in the charger happens when the charger enters the constant voltage mode.

If the adapter voltage reaches the full-load voltage before the pack voltage reaches 4.2V (or 4.1V), the charger will experience the resistance-limit situation. In this situation, the ON-resistance of the charger is in series with the adapter output resistance. The equivalent circuit for the resistance-limit region is shown in Figure 25B. Eventually, the battery pack voltage will reach 4.2V (or 4.1V) because the adapter no-load voltage is higher than 4.2V (or 4.1V), then Figure 25C becomes the equivalent circuit until charging ends. In this case, the worst-case thermal dissipation also occurs in the constant-current charge mode. Figure 26B shows the I-V curves of the adapter output, the battery pack voltage and the cell voltage for the case V_{FL} = 4V. In the case, the full-load voltage is lower than the final charge voltage (4.2V), but the charger is still able to fully charge the battery as long as the no-load voltage is above 4.2V. Figure 26B illustrates the adapter voltage, battery pack voltage, the charge current and the power dissipation in the charger respectively in the time domain.

Based on the previous discussion, the worst-case power dissipation occurs during the constant-current charge mode if the adapter full-load voltage is lower than the critical voltage given in Equation 14. Even if that is not true, the power dissipation is still much less than the power dissipation in the traditional linear charger. Figures 28 and 29 are scope-captured waveforms to demonstrate the operation with a current-limited adapter.

The waveforms in Figure 28 are the adapter output voltage (1V/div), the battery voltage (1V/div), and the charge current (200mA/div) respectively. The time scale is 1ks/div. The adapter current is limited to 600mA and the charge current is programmed to 1A. Note that the voltage difference is only approximately 200mV and the adapter voltage tracks the battery voltage in the CC mode. Figure 28 also shows the resistance-limit mode before entering the CV mode.

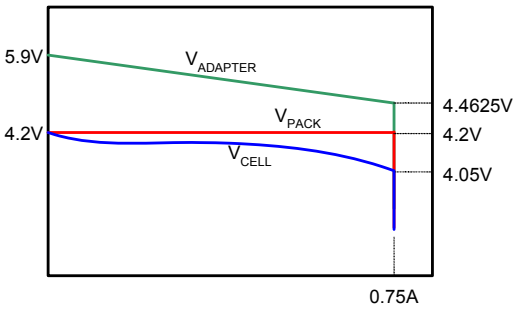


FIGURE 26A.

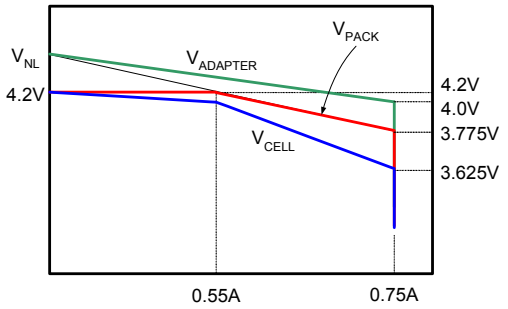


FIGURE 26B.

FIGURE 26. THE I-V CHARACTERISTICS OF THE CHARGER WITH DIFFERENT CURRENT LIMITED ADAPTERS

Figure 29 shows the actual captured waveforms depicted in Figure 27C. The constant charge current is 750mA. A step in the adapter voltage during the transition from CC mode to CV mode is demonstrated.

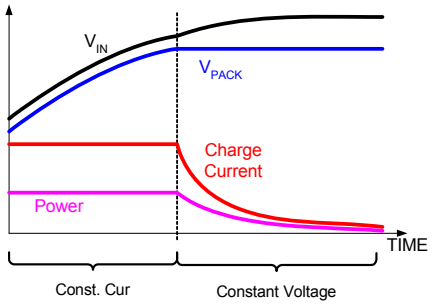


FIGURE 27A.

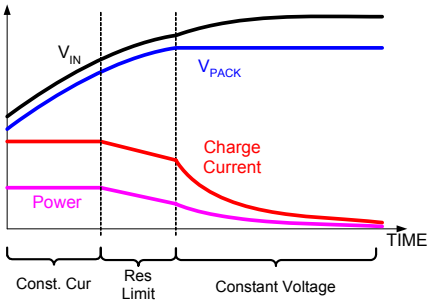


FIGURE 27B.

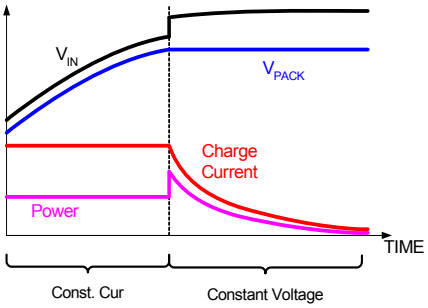


FIGURE 27C.

FIGURE 27. THE OPERATING CURVES WITH THREE DIFFERENT CURRENT LIMITED ADAPTERS

IREF Programming Using Current-Limited Adapter

The ISL6292 has 10% tolerance for the charge current. Typically the current-limited adapter also has 10% tolerance. In order to guarantee proper operation, it is recommended that the nominal charge current be programmed **at least 30% higher** than the nominal current limit of the adapter.

Board Layout Recommendations

The ISL6292 internal thermal foldback function limits the charge current when the internal temperature reaches approximately +100°C. In order to maximize the current capability, it is very important that the exposed pad under the package is properly soldered to the board and is connected to other layers through thermal vias. More thermal vias and more copper attached to the exposed pad usually result in better thermal performance. On the other hand, the number of vias is limited by the size of the pad. The exposed pads for the 5x5 and 4x4 QFN packages are able to have 9 and 5 vias respectively. The 3x3 DFN package allows 8 vias be placed in two rows. Since the pins on the 3x3 DFN package are on only two sides, as much top layer copper as possible should be connected to the exposed pad to minimize the thermal impedance. Refer to the ISL6292 evaluation boards for layout examples.

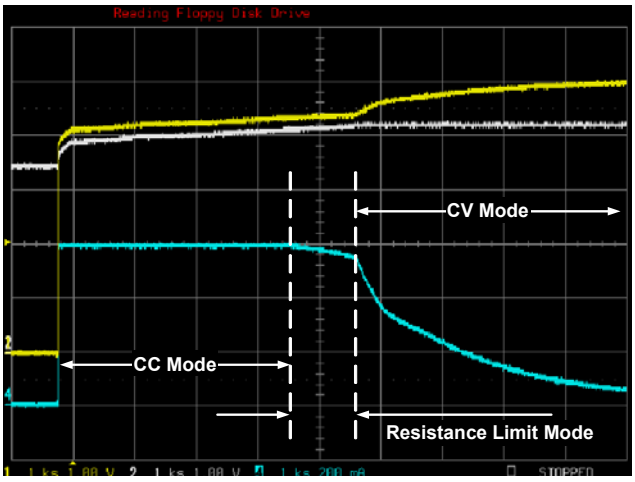


FIGURE 28. SCOPE CAPTURED WAVEFORMS SHOWING THE THREE MODES

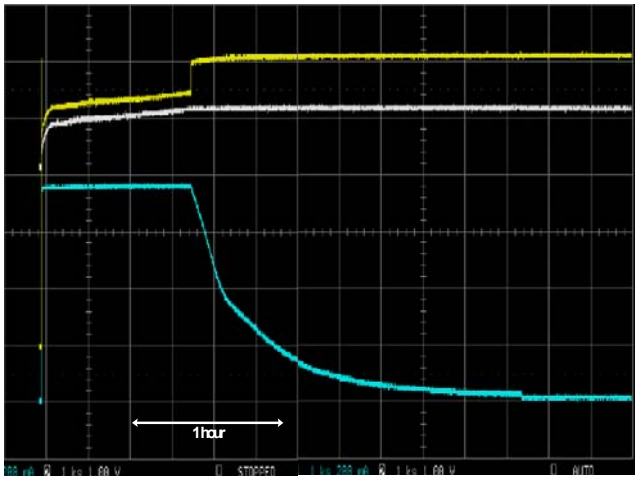
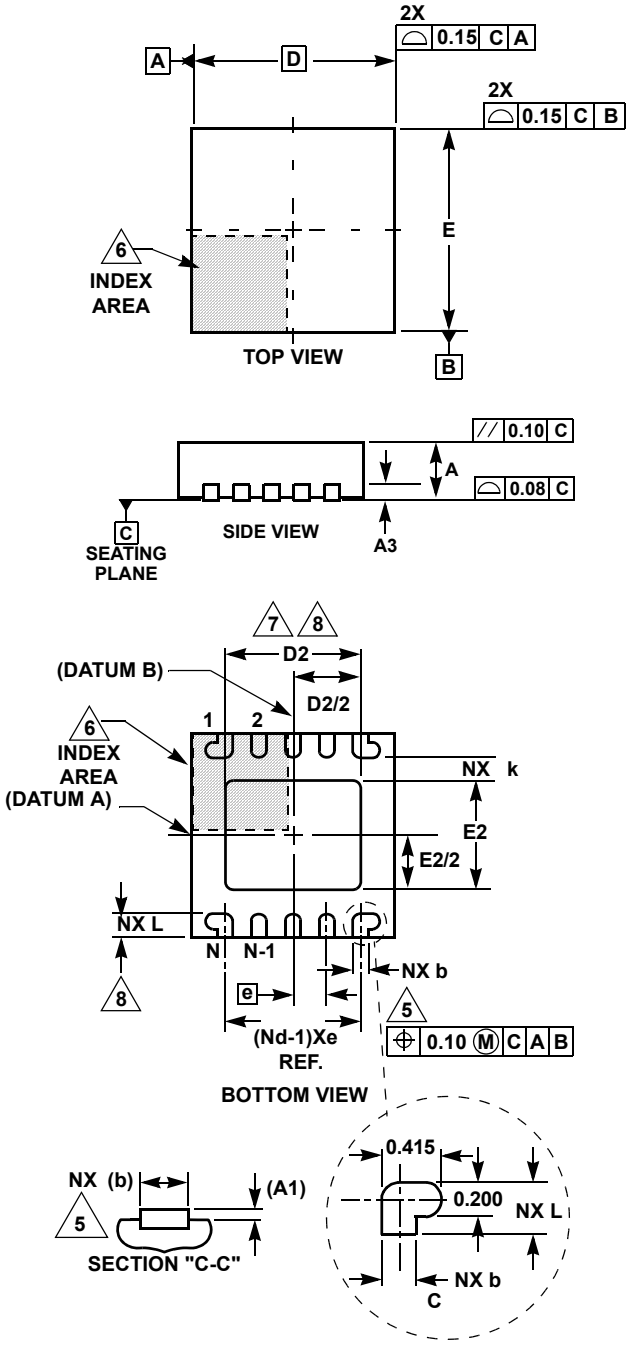


FIGURE 29. SCOPE CAPTURED WAVEFORMS SHOWING THE CASE THAT THE FULL-LOAD ADAPTER VOLTAGE IS HIGHER THAN THE CRITICAL VOLTAGE

Dual Flat No-Lead Plastic Package (DFN)



L10.3x3

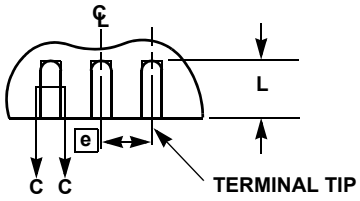
10 LEAD DUAL FLAT NO-LEAD PLASTIC PACKAGE

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A3		0.20 REF		-
b	0.18	0.23	0.28	5,8
D		3.00 BSC		-
D2	1.95	2.00	2.05	7,8
E		3.00 BSC		-
E2	1.55	1.60	1.65	7,8
e		0.50 BSC		-
k	0.25	-	-	-
L	0.30	0.35	0.40	8
N		10		2
Nd		5		3

Rev. 3 6/04

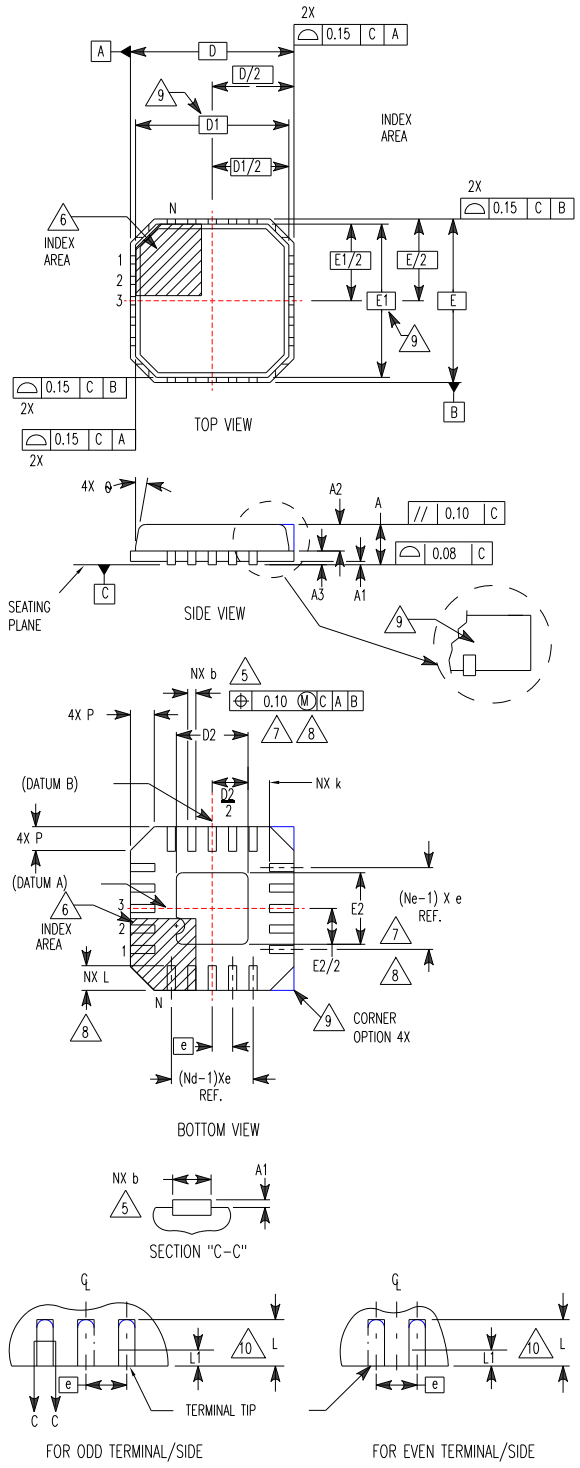
NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd refers to the number of terminals on D.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.



FOR ODD TERMINAL/SIDE

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.4x4

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220-VGGC ISSUE C)

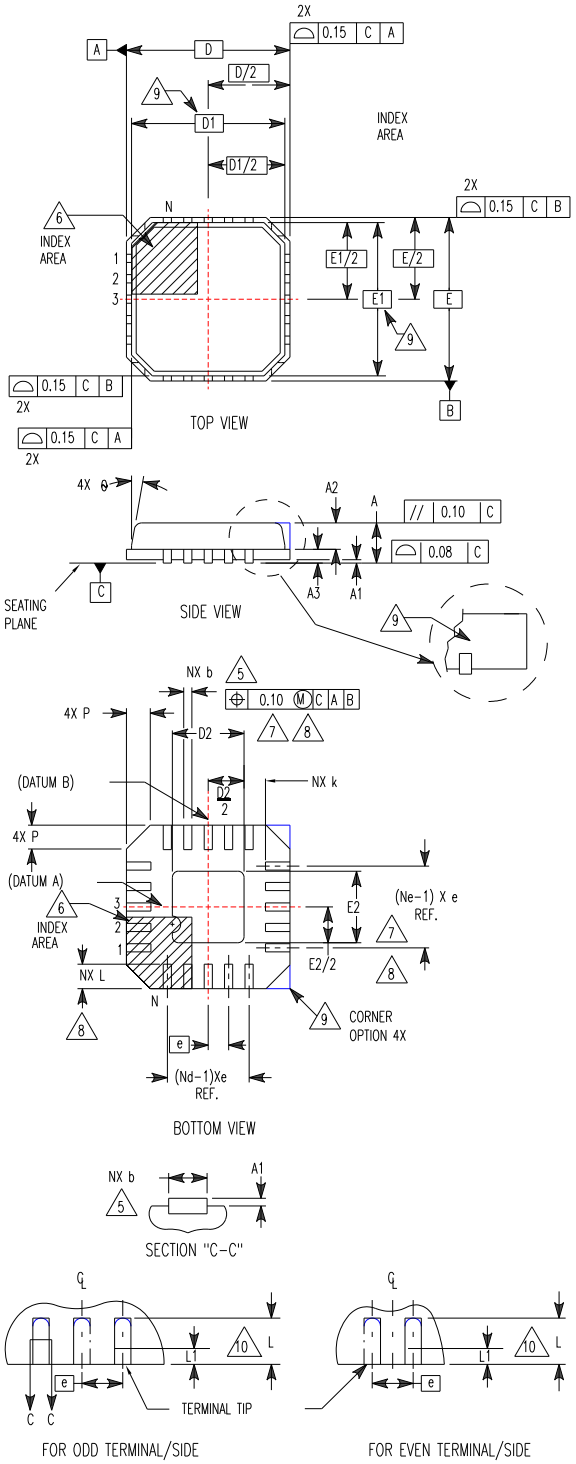
SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.23	0.28	0.35	5, 8
D		4.00 BSC		-
D1		3.75 BSC		9
D2	1.95	2.10	2.25	7, 8
E		4.00 BSC		-
E1		3.75 BSC		9
E2	1.95	2.10	2.25	7, 8
e		0.65 BSC		-
k	0.25	-	-	-
L	0.50	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 5 5/04

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.

Quad Flat No-Lead Plastic Package (QFN)
Micro Lead Frame Plastic Package (MLFP)



L16.5x5B

16 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE (COMPLIANT TO JEDEC MO-220VHHB ISSUE C)

SYMBOL	MILLIMETERS			NOTES
	MIN	NOMINAL	MAX	
A	0.80	0.90	1.00	-
A1	-	-	0.05	-
A2	-	-	1.00	9
A3		0.20 REF		9
b	0.28	0.33	0.40	5, 8
D		5.00 BSC		-
D1		4.75 BSC		9
D2	2.95	3.10	3.25	7, 8
E		5.00 BSC		-
E1		4.75 BSC		9
E2	2.95	3.10	3.25	7, 8
e		0.80 BSC		-
k	0.25	-	-	-
L	0.35	0.60	0.75	8
L1	-	-	0.15	10
N		16		2
Nd		4		3
Ne		4		3
P	-	-	0.60	9
θ	-	-	12	9

Rev. 1 10/02

NOTES:

1. Dimensioning and tolerancing conform to ASME Y14.5-1994.
2. N is the number of terminals.
3. Nd and Ne refer to the number of terminals on each D and E.
4. All dimensions are in millimeters. Angles are in degrees.
5. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.
7. Dimensions D2 and E2 are for the exposed pads which provide improved electrical and thermal performance.
8. Nominal dimensions are provided to assist with PCB Land Pattern Design efforts, see Intersil Technical Brief TB389.
9. Features and dimensions A2, A3, D1, E1, P & θ are present when Anvil singulation method is used and not present for saw singulation.
10. Depending on the method of lead termination at the edge of the package, a maximum 0.15mm pull back (L1) maybe present. L minus L1 to be equal to or greater than 0.3mm.