700V N-Channel MOSFET

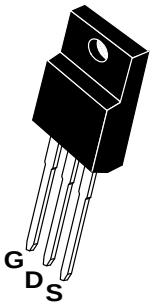
General Description：

FIR4N70FG the silicon N-channel Enhanced VDMOSFETs, is obtained by the self-aligned planar Technology which reduce the conduction loss, improve switching performance and enhance the avalanche energy. The transistor can be used in various power switching circuit for system miniaturization and higher efficiency. The package form is TO-220F, which accords with the RoHS standard.

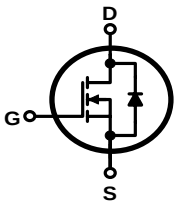
Features

- **Fast Switching**
- **Low ON Resistance(Rdson≤3.0)**
- **Low Gate Charge (Typical Data:12.7nC)**
- **Low Reverse transfer capacitances(Typical:2**
- **100% Single Pulse avalanche energy Test**

PIN Connection TO-220F



Schematic diagram



Marking Diagram



Y	= Year
A	= Assembly Location
WW	= Work Week
FIR4N70F	= Specific Device Code

Applications：

Power switch circuit of adaptor and charger.

Absolute（Tc= 25℃ unless otherwise specified）：

Symbol	Parameter	Rating	Units
V_{DSS}	Drain-to-Source Voltage	700	V
I_D	Continuous Drain Current	4	A
	Continuous Drain Current T_C = 100 °C	2.5	A
I_{DM} [a1]	Pulsed Drain Current	28	A
V_{GS}	Gate-to-Source Voltage	±30	V
E_{AS} [a2]	Single Pulse Avalanche Energy	196	mJ
dv/dt [a3]	Peak Diode Recovery dv/dt	5.0	V/ns
P_D	Power Dissipation	30	W
	Derating Factor above 25°C	0.6	W/℃
T_J， T_{stg}	Operating Junction and Storage Temperature Range	150，–55 to 150	℃
T_L	Maximum Temperature for Soldering	300	℃

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Electrical Characteristics（Tc= 25℃ unless otherwise s ecified）：

OFF Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
V_{DSS}	Drain to Source Breakdown Voltage	V_{GS}=0V, I_D=250μA	700	--	--	V
$\Delta BV_{DSS}/\Delta T_J$	Bvdss Temperature Coefficient	ID=250uA,Reference25℃	--	0.7	--	V/
I_{DSS}	Drain to Source Leakage Current	V_{DS} =700V, V_{GS}= 0V, T_a = 25℃	--	--	1	μA
		V_{DS} =560V, V_{GS}= 0V, T_a = 125℃	--	--	100	μA
$I_{GSS(F)}$	Gate to Source Forward Leakage	V_{GS} =+30V	--	--	100	nA
$I_{GSS(R)}$	Gate to Source Reverse Leakage	V_{GS} =-30V	--	--	-100	nA

ON Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$R_{DS(ON)}$	Drain-to-Source On-Resistance	V_{GS}=10V,I_D=2A	--	2.55	3.0	Ω
$V_{GS(TH)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	2.0	--	4.0	V
Pulse width tp≤300μs, δ ≤2%						

Dynamic Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
g_{fs}	Forward Transconductance	V_{DS}=15V, I_D =2A	--	3.7	--	S
C_{iss}	Input Capacitance	V_{GS} = 0V V_{DS} = 25V f = 1.0MHz	--	606	--	pF
C_{oss}	Output Capacitance		--	48	--	
C_{rss}	Reverse Transfer Capacitance		--	2.7	--	

Resistive Switching Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
$t_{d(ON)}$	Turn-on Delay Time	I_D =4A V_{DD} = 350V R_G =10	--	14	--	ns
tr	Rise Time		--	15	--	
$t_{d(OFF)}$	Turn-Off Delay Time		--	30	--	
t_f	Fall Time		--	9	--	
Q_g	Total Gate Charge	I_D =4A V_{DD} =560V V_{GS} = 10V	--	12.7	--	nC
Q_{gs}	Gate to Source Charge		--	3.0	--	
Q_{gd}	Gate to Drain (“Miller”)Charge		--	5.1	--	

Source-Drain Diode Characteristics						
Symbol	Parameter	Test Conditions	Rating			Units
			Min.	Typ.	Max.	
I_S	Continuous Source Current (Body Diode)		--	--	4	A
I_{SM}	Maximum Pulsed Current (Body Diode)		--	--	16	A
V_{SD}	Diode Forward Voltage	I_S=4A,V_{GS}=0V	--	--	1.5	V
trr	Reverse Recovery Time	I_S=4A,T_j = 25℃ dI$_F$/dt=100A/us, V_{GS}=0V	--	325.3	--	ns
Qrr	Reverse Recovery Charge		--	1470	--	nC
I_{RRM}	Reverse Recovery Current		--	9.0	--	A
Pulse width tp≤300μs, δ ≤2%						

Symbol	Parameter	Max.	Units
$R_{\theta JC}$	Junction-to-Case	4.16	℃/W
$R_{\theta JA}$	Junction-to-Ambient	120	℃/W

[a1]: Repetitive rating; pulse width limited by maximum junction temperature
[a2]: L=10mH, I_D=6.3A, Start T_J=25℃
[a3]: I_{SD} =4A,di/dt ≤100A/us,V_{DD}≤$BV_{DS,}$ Start T_J=25℃

Characteristics Curve:

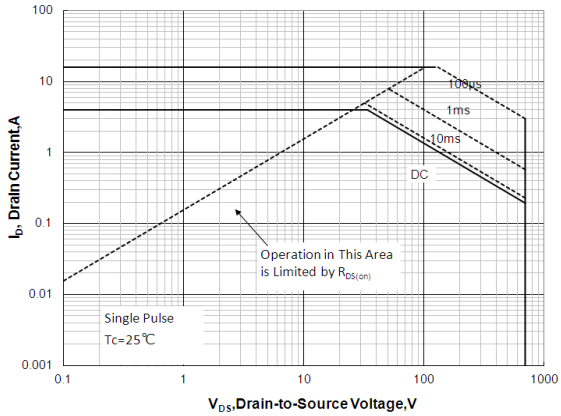


Figure 1 Maximum Forward Bias Safe Operating Area

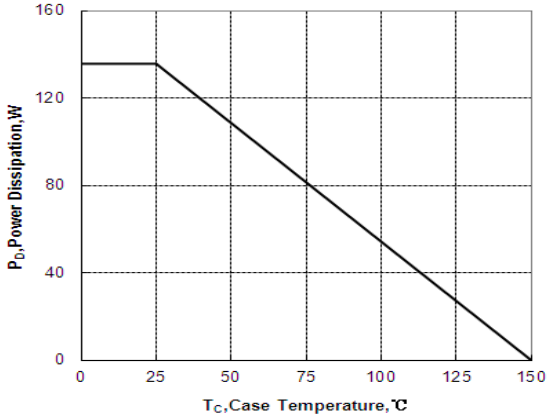


Figure 2 Maximum Power dissipation vs Case Temperature

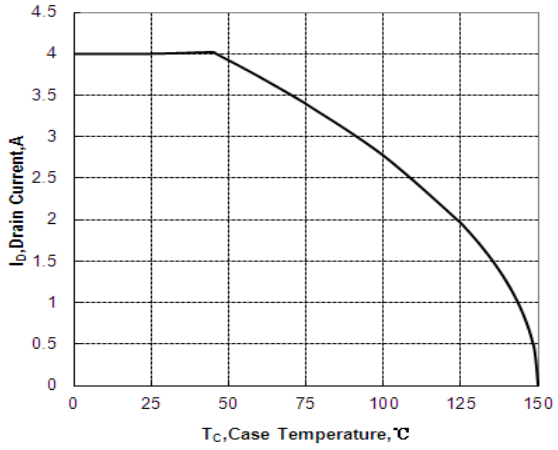


Figure 3 Maximum Continuous Drain Current vs Case Temperature

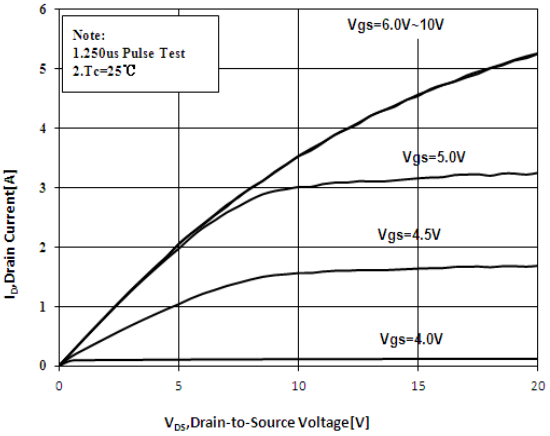


Figure 4 Typical Output Characteristics

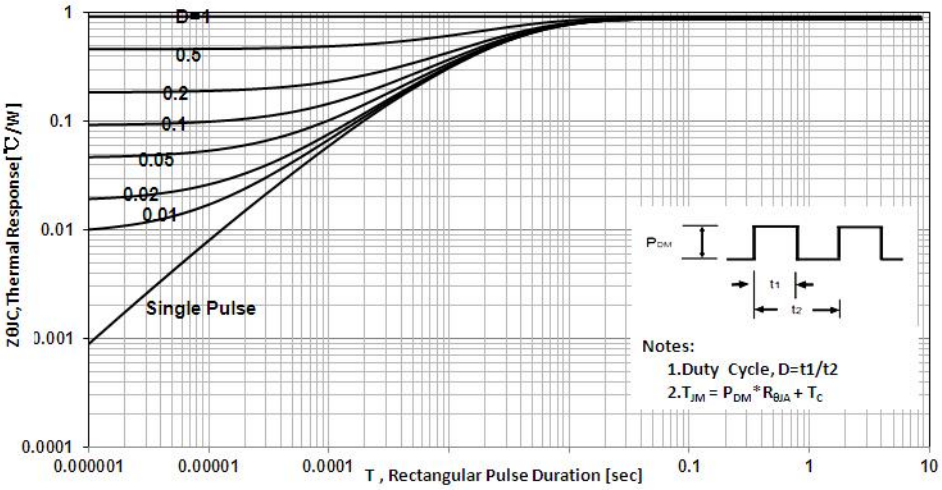


Figure 5 Maximum Effective Thermal Impedance , Junction to Case

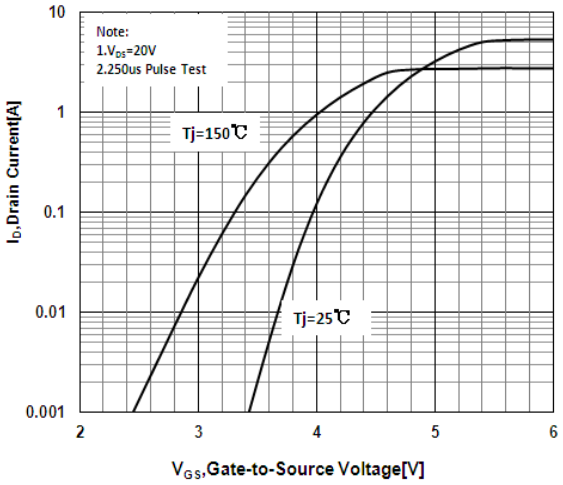


Figure 6 Typical Transfer Characteristics

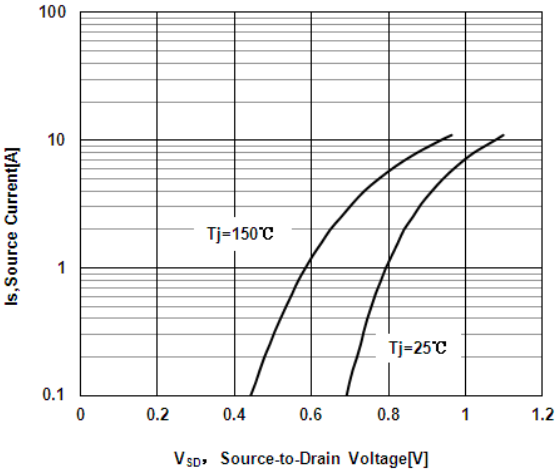


Figure 7 Typical Body Diode Transfer Characteristics

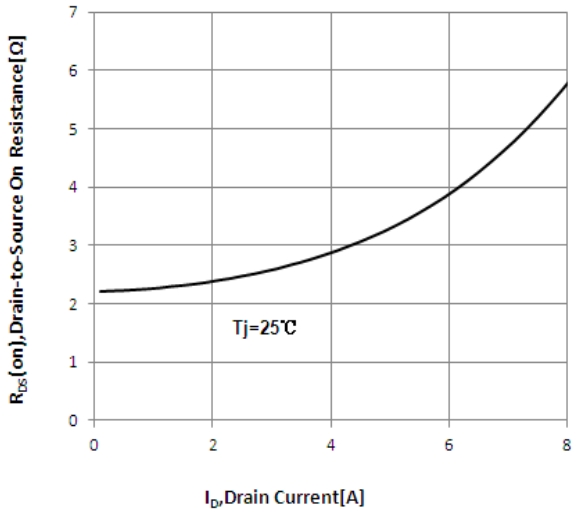


Figure 8 Typical Drain to Source ON Resistance vs Drain Current

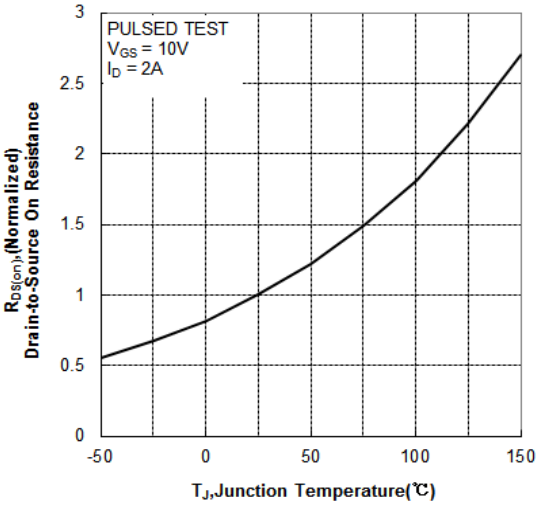


Figure 9 Typical Drian to Source on Resistance vs Junction Temperature

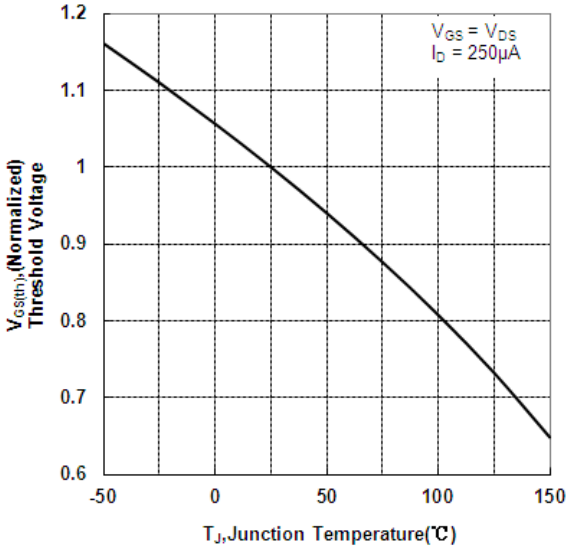


Figure 10 Typical Theshold Voltage vs Junction Temperature

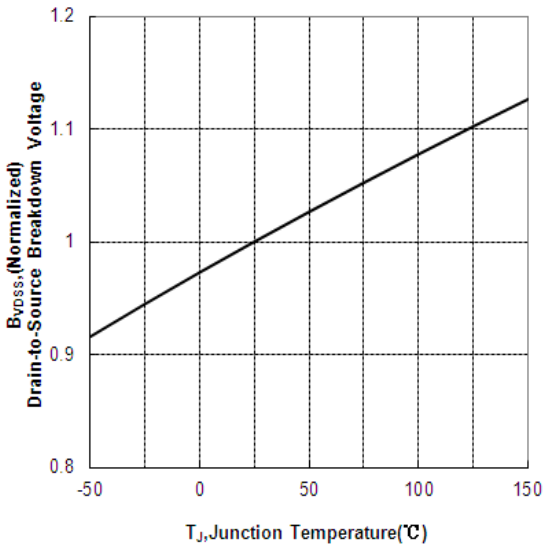


Figure 11 Typical Breakdown Voltage vs Junction Temperature

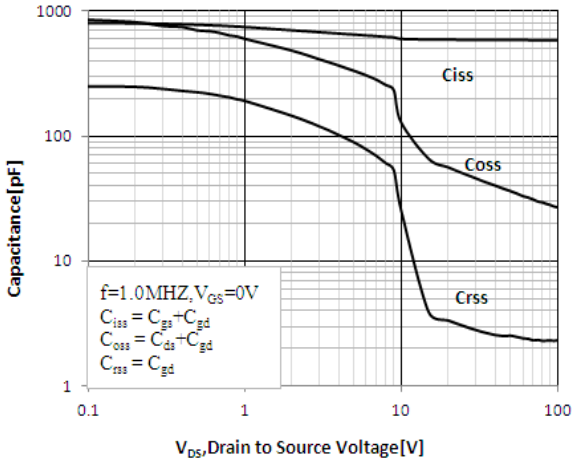


Figure 12 Typical Capacitance vs Drain to Source Voltage

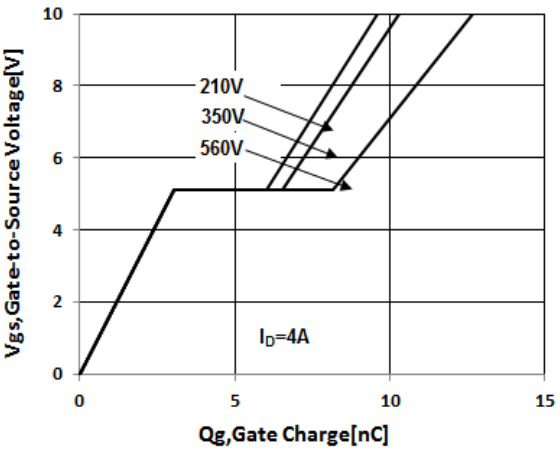


Figure 13 Typical Gate Charge vs Gate to Source Voltage

Test Circuit and Waveform

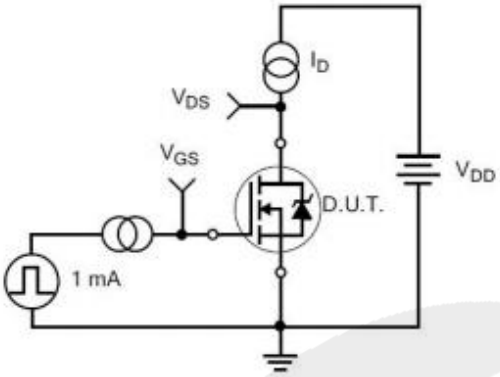


Figure 14. Gate Charge Test Circuit

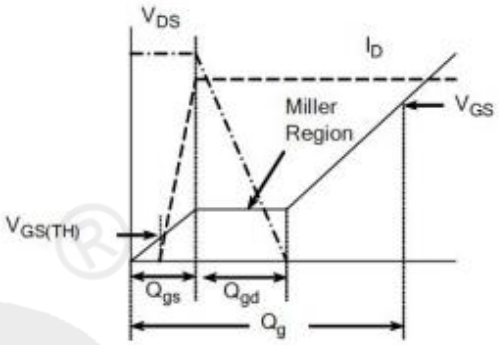


Figure 15. Gate Charge Waveforms

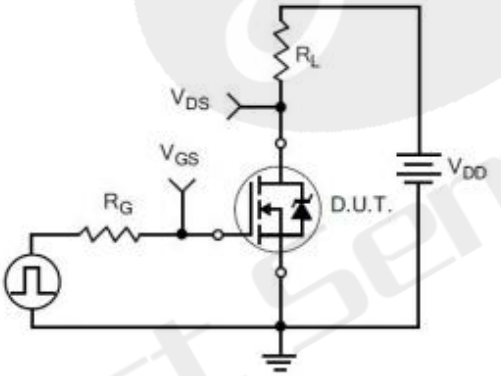


Figure 16. Resistive Switching Test Circuit

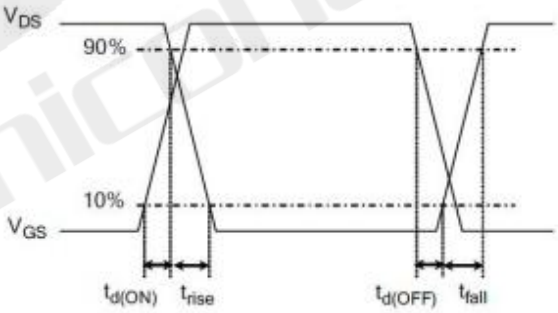


Figure 17. Resistive Switching Waveforms

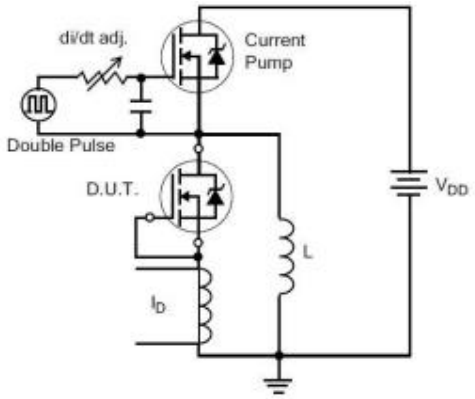


Figure 18. Diode Reverse Recovery Test Circuit

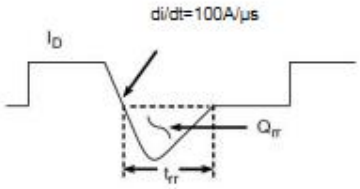


Figure 19. Diode Reverse Recovery Waveform

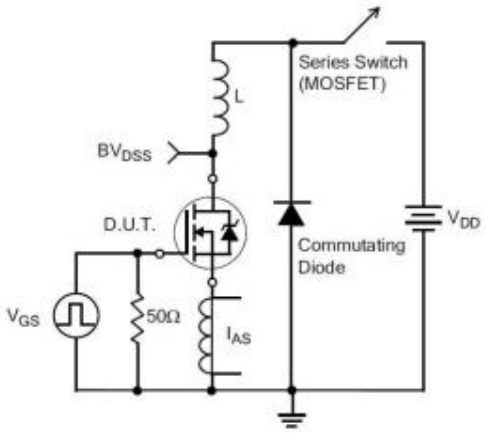


Figure 20. Unclamped Inductive Switching Test Circuit

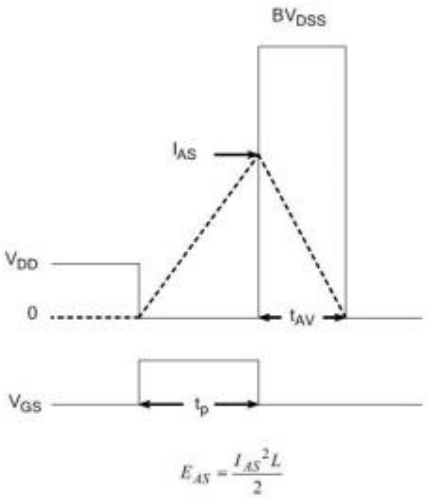
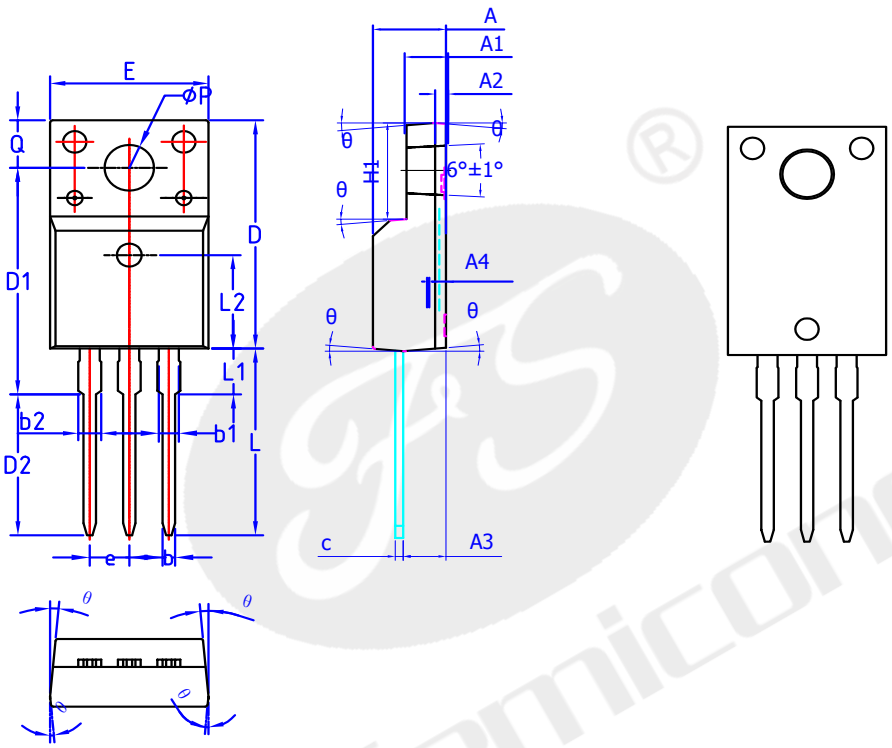


Figure 21. Unclamped Inductive Switching Waveform

Package Dimension

TO-220F

Unit: mm



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	4.50	4.70	4.90
A1	2.34	2.54	2.74
A2		0.70 REF	
A3	2.56	2.76	2.96
b	0.70	0.80	0.90
b1	1.17	1.2	1.25
b2	1.17	1.2	1.25
c	0.45	0.50	0.60
D	15.67	15.87	16.07
D1	15.55	15.75	15.95
D2	10.0	10.2	10.4
E	9.96	10.16	10.36
e		2.54BSC	
H1	6.48	6.68	6.88
L	12.68	12.98	13.28
L1	-	-	3.50
L2		6.50REF	
ØP	3.08	3.18	3.28
Q	3.20	3.30	3.40
θ1	1°	3°	5°
A4	0.53	0.56	0.59

Declaration

- FIRST reserves the right to change the specifications, the same specifications of products due to different packaging line mold, the size of the appearance will be slightly different, shipped in kind, without notice! Customers should obtain the latest version information before ordering, and verify whether the relevant information is complete and up-to-date.
- Any semiconductor product under certain conditions has the possibility of failure or failure,The buyer has the responsibility to comply with safety standards and take safety measures when using FIRST products for system design and manufacturing,To avoid To avoid potential failure risks, which may cause personal injury or property damage!
- Product promotion endless, our company will wholeheartedly provide customers with better products!

ATTACHMENT

Revision History

Date	REV	Description	Page
2018.01.01	1.0	Initial release	