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July 2004 FN3605.6

Dual, 425MHz, Low Power, Video Operational Amplifier

The HFA1205 is a dual, high speed, low power current feedback amplifier built with Intersil's proprietary complementary bipolar UHF-1 process.

These amplifiers deliver 425MHz bandwidth and 1350V/μs slew rate, on only 60mW of quiescent power. They are specifically designed to meet the performance, power, and cost requirements of high volume video applications. The excellent gain flatness and differential gain/phase performance make these amplifiers well suited for component or composite video applications. Video performance is maintained even when driving a back terminated cable (R_L = 150Ω), and degrades only slightly when driving two back terminated cables (R_L = 75Ω). RGB applications will benefit from the high slew rates, and high full power bandwidth.

The HFA1205 is a pin compatible, low power, high performance upgrade for the popular Intersil HA5023. For a dual amplifier with output disable capability, please see the HFA1245 data sheet.

Part # Information

PART NUMBER (BRAND)	TEMP. RANGE (^oC)	PACKAGE	PKG. NO.
HFA1205IP	-40 to 85	8 Ld PDIP	E8.3
HFA1205IB (H1205I)	-40 to 85	8 Ld SOIC	M8.15
HA5023EVAL	High Speed Op Amp DIP Evaluation Board		

Features

- Low Supply Current . . . . . 5.8mA/Op Amp
- High Input Impedance 2MΩ
- Wide -3dB Bandwidth (A_V = +2) 425MHz
- Very Fast Slew Rate 1350V/μs
- Gain Flatness (to 50MHz) . . . . . ±0.04dB
- Differential Gain 0.03%
- Differential Phase . . . . . 0.03 Degrees
- Pin Compatible Upgrade to HA5023

Applications

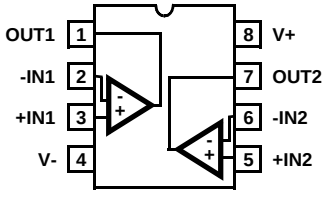
- Flash A/D Drivers
- High Resolution Monitors
- Video Switching and Routing
- Professional Video Processing
- Video Digitizing Boards/Systems
- Multimedia Systems
- RGB Preamps
- Medical Imaging
- Hand Held and Miniaturized RF Equipment
- Battery Powered Communications
- High Speed Oscilloscopes and Analyzers

Related Literature

- Technical Brief TB363 "Guidelines for Handling and Processing Moisture Sensitive Surface Mount Devices (SMDs)"

Pinout

HFA1205
(PDIP, SOIC)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Absolute Maximum Ratings

Voltage Between V+ and V- 11V
DC Input Voltage . . . . . V_{SUPPLY}
Differential Input Voltage 8V
Output Current (Note 2) . . . . . Short Circuit Protected
30mA Continuous
60mA $\leq$ 50% Duty Cycle
ESD Rating
Human Body Model (Per MIL-STD-883 Method 3015.7) . . . 600V

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
PDIP Package	105
SOIC Package	160

Maximum Junction Temperature (Plastic Package) . . . . . 150^{o}C
Maximum Storage Temperature Range . . . . . -65^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{o}C
(SOIC - Lead Tips Only)

Operating Conditions

Temperature Range . . . . . -40^{o}C to 85^{o}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTES:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
2. Output is short circuit protected to ground. Brief short circuits to ground will not degrade reliability, however continuous (100% duty cycle) output current must not exceed 30mA for maximum reliability.

Electrical Specifications

V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_L = 100Ω, Unless Otherwise Specified

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (^{o}C)	MIN	TYP	MAX	UNITS
INPUT CHARACTERISTICS							
Input Offset Voltage		A	25	-	2	5	mV
		A	Full	-	3	8	mV
Average Input Offset Voltage Drift		B	Full	-	1	10	µV/^{o}C
Input Offset Voltage Common-Mode Rejection Ratio	ΔV_{CM} = ±1.8V	A	25	45	48	-	dB
	ΔV_{CM} = ±1.8V	A	85	43	46	-	dB
	ΔV_{CM} = ±1.2V	A	-40	43	46	-	dB
Input Offset Voltage Power Supply Rejection Ratio	ΔV_{PS} = ±1.8V	A	25	48	52	-	dB
	ΔV_{PS} = ±1.8V	A	85	46	50	-	dB
	ΔV_{PS} = ±1.2V	A	-40	46	50	-	dB
Non-Inverting Input Bias Current		A	25	-	6	15	µA
		A	Full	-	10	25	µA
Non-Inverting Input Bias Current Drift		B	Full	-	5	60	nA/^{o}C
Non-Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	25	-	0.5	1	µA/V
	ΔV_{PS} = ±1.8V	A	85	-	0.8	3	µA/V
	ΔV_{PS} = ±1.2V	A	-40	-	0.8	3	µA/V
Non-Inverting Input Resistance	ΔV_{CM} = ±1.8V	A	25	0.8	2	-	MΩ
	ΔV_{CM} = ±1.8V	A	85	0.5	1.3	-	MΩ
	ΔV_{CM} = ±1.2V	A	-40	0.5	1.3	-	MΩ
Inverting Input Bias Current		A	25	-	2	8.5	µA
		A	Full	-	5	15	µA
Inverting Input Bias Current Drift		B	Full	-	60	200	nA/^{o}C
Inverting Input Bias Current Common-Mode Sensitivity	ΔV_{CM} = ±1.8V	A	25	-	3	6	µA/V
	ΔV_{CM} = ±1.8V	A	85	-	4	8	µA/V
	ΔV_{CM} = ±1.2V	A	-40	-	4	8	µA/V

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Inverting Input Bias Current Power Supply Sensitivity	ΔV_{PS} = ±1.8V	A	25	-	2	5	µA/V
	ΔV_{PS} = ±1.8V	A	85	-	4	8	µA/V
	ΔV_{PS} = ±1.2V	A	-40	-	4	8	µA/V
Inverting Input Resistance		C	25	-	55	-	Ω
Input Capacitance		C	25	-	1.5	-	pF
Input Voltage Common Mode Range (Implied by V_{IO} CMRR, $+R_{IN}$, and $-I_{BIAS}$ CMS tests)		A	25, 85	±1.8	±2.4	-	V
		A	-40	±1.2	±1.7	-	V
Input Noise Voltage Density (Note 6)	f = 100kHz	B	25	-	3.5	-	nV/√Hz
Non-Inverting Input Noise Current Density (Note 6)	f = 100kHz	B	25	-	2.5	-	pA/√Hz
Inverting Input Noise Current Density (Note 6)	f = 100kHz	B	25	-	25	-	pA/√Hz
TRANSFER CHARACTERISTICS							
Open Loop Transimpedance Gain (Note 6)		C	25	-	400	-	kΩ
AC CHARACTERISTICS A_V = +2, R_F = 464Ω, Unless Otherwise Specified							
-3dB Bandwidth (V_{OUT} = 0.2V_{P-P}, Note 6)	A_V = +1, $+R_S$ = 432Ω	B	25	-	300	-	MHz
	A_V = +2	B	25	-	425	-	MHz
	A_V = -1, R_F = 332Ω	B	25	-	350	-	MHz
Full Power Bandwidth (V_{OUT} = 5V_{P-P} at A_V = +2/-1, 4V_{P-P} at A_V = +1, Note 6)	A_V = +1, R_S = 432Ω	B	25	-	135	-	MHz
	A_V = +2	B	25	-	130	-	MHz
	A_V = -1, R_F = 332Ω	B	25	-	200	-	MHz
Gain Flatness (A_V = +2,V_{OUT} = 0.2V_{P-P}, Note 6)	To 25MHz	B	25	-	±0.04	-	dB
	To 50MHz	B	25	-	±0.04	-	dB
	To 100MHz	B	25	-	±0.07	-	dB
Minimum Stable Gain		A	Full	-	1	-	V/V
Crosstalk (A_V = +2, Note 6)	5MHz	B	25	-	-60	-	dB
	10MHz	B	25	-	-54	-	dB
OUTPUT CHARACTERISTICS							
Output Voltage Swing (Note 6)	A_V = -1, R_L = 100Ω R_F = 560Ω	A	25	±3	±3.5	-	V
		A	Full	±2.8	±3	-	V
Output Current (Note 6)	A_V = -1, R_L = 50Ω R_F = 560Ω	A	25, 85	50	60	-	mA
		A	-40	28	42	-	mA
Output Short Circuit Current	R_F = 560Ω	B	25	-	90	-	mA
Closed Loop Output Impedance (Note 6)	DC, A_V = +2, R_F = 464Ω	B	25	-	0.07	-	Ω
Second Harmonic Distortion (A_V = +2, R_F = 464Ω, V_{OUT} = 2V_{P-P})	10MHz	B	25	-	-53	-	dBc
	20MHz	B	25	-	-45	-	dBc
Third Harmonic Distortion (A_V = +2, R_F = 464Ω, V_{OUT} = 2V_{P-P})	10MHz	B	25	-	-55	-	dBc
	20MHz	B	25	-	-50	-	dBc
TRANSIENT CHARACTERISTICS A_V = +2, R_F = 464Ω, Unless Otherwise Specified							
Rise and Fall Times (V_{OUT} = 0.5V_{P-P})	Rise Time	B	25	-	1.0	-	ns
	Fall Time	B	25	-	1.4	-	ns
Overshoot (V_{OUT} = 0 to 0.5V, V_{IN} t_{RISE} = 1ns, Note 4)	+OS	B	25	-	5	-	%
	-OS	B	25	-	4	-	%
Overshoot (V_{OUT} = 0.5V_{P-P}, V_{IN} t_{RISE} = 1ns, Note 4)	+OS	B	25	-	5	-	%
	-OS	B	25	-	10	-	%

Electrical Specifications V_{SUPPLY} = ±5V, A_V = +1, R_F = 560Ω, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

PARAMETER	TEST CONDITIONS	(NOTE 3) TEST LEVEL	TEMP. (°C)	MIN	TYP	MAX	UNITS
Slew Rate (V_{OUT} = $4V_{P-P}$, A_V = +1, $+R_S$ = 432Ω)	+SR	B	25	-	1150	-	V/µs
	-SR (Note 5)	B	25	-	800	-	V/µs
Slew Rate (V_{OUT} = $5V_{P-P}$, A_V = +2)	+SR	B	25	-	1425	-	V/µs
	-SR (Note 5)	B	25	-	900	-	V/µs
Slew Rate (V_{OUT} = $5V_{P-P}$, A_V = -1, R_F = 332Ω)	+SR	B	25	-	2400	-	V/µs
	-SR (Note 5)	B	25	-	1350	-	V/µs
Settling Time (V_{OUT} = +2V to 0V step, Note 6)	To 0.1%	B	25	-	23	-	ns
	To 0.05%	B	25	-	33	-	ns
	To 0.025%	B	25	-	85	-	ns
Overdrive Recovery Time	V_{IN} = ±2V	B	25	-	10	-	ns
VIDEO CHARACTERISTICS A_V = +2, R_F = 464Ω, Unless Otherwise Specified							
Differential Gain (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.03	-	%
	R_L = 75Ω	B	25	-	0.03	-	%
Differential Phase (f = 3.58MHz)	R_L = 150Ω	B	25	-	0.03	-	Degrees
	R_L = 75Ω	B	25	-	0.05	-	Degrees
POWER SUPPLY CHARACTERISTICS							
Power Supply Range		C	25	±4.5	-	±5.5	V
Power Supply Current (Note 6)		A	25	5.6	5.8	6.1	mA/ Op Amp
		A	Full	5.4	5.9	6.3	mA/ Op Amp

NOTES:

3. Test Level: A. Production Tested.; B. Typical or Guaranteed Limit Based on Characterization.; C. Design Typical for Information Only.
4. Undershoot dominates for output signal swings below GND (e.g., $0.5V_{P-P}$), yielding a higher overshoot limit compared to the V_{OUT} = 0V to 0.5V condition. See the “Application Information “section for details.
5. Slew rates are asymmetrical if the output swings below GND (e.g., a bipolar signal). Positive unipolar output signals have symmetric positive and negative slew rates comparable to the +SR specification. See the “Application Information” text, and the pulse response graphs for details.
6. See Typical Performance Curves for more information.

Application Information

Optimum Feedback Resistor

Although a current feedback amplifier’s bandwidth dependency on closed loop gain isn’t as severe as that of a voltage feedback amplifier, there can be an appreciable decrease in bandwidth at higher gains. This decrease may be minimized by taking advantage of the current feedback amplifier’s unique relationship between bandwidth and R_F . All current feedback amplifiers require a feedback resistor, even for unity gain applications, and R_F, in conjunction with the internal compensation capacitor, sets the dominant pole of the frequency response. Thus, the amplifier’s bandwidth is inversely proportional to R_F. The HFA1205 design is optimized for a 464Ω R_F at a gain of +2. Decreasing R_F decreases stability, resulting in excessive peaking and overshoot (Note: Capacitive feedback will cause the same problems due to the feedback impedance decrease at higher frequencies). At higher gains the amplifier is more stable, so R_F can be decreased in a trade-off of stability for bandwidth.

Table 1 lists recommended RF values for various gains, and the expected bandwidth. For good channel-to-channel gain matching, it is recommended that all resistors (termination as well as gain setting) be ±1% tolerance or better. Note that a series input resistor, on +IN, is required for a gain of +1, to reduce gain peaking and increase stability.

TABLE 1. OPTIMUM FEEDBACK RESISTOR

GAIN (A_{CL})	R_F (Ω)	BANDWIDTH (MHz)
-1	332	350
+1	464 ($+R_S$ = 432Ω)	300
+2	464	425
+5	215	270
+10	180	115

Non-inverting Input Source Impedance

For best operation, the DC source impedance seen by the non-inverting input should be ≥50Ω. This is especially important in inverting gain configurations where the non-inverting input would normally be connected directly to GND.

Pulse Undershoot and Asymmetrical Slew Rates

The HFA1205 utilizes a quasi-complementary output stage to achieve high output current while minimizing quiescent supply current. In this approach, a composite device replaces the traditional PNP pulldown transistor. The composite device switches modes after crossing 0V, resulting in added distortion for signals swinging below ground, and an increased undershoot on the negative portion of the output waveform (see Figures 7, 11, 15 and 19). This undershoot isn't present for small bipolar signals, or large positive signals (see Figures 5, 6, 9, 10, 13, 14, 17 and 18). Another artifact of the composite device is asymmetrical slew rates for output signals with a negative voltage component. The slew rate degrades as the output signal crosses through 0V (see Figures 7, 11, 15, and 19), resulting in a slower overall negative slew rate. Positive only signals have symmetrical slew rates as illustrated in the large signal positive pulse response graphs (see Figures 5, 9, 13 and 17).

PC Board Layout

The frequency response of this amplifier depends greatly on the amount of care taken in designing the PC board. **The use of low inductance components such as chip resistors and chip capacitors is strongly recommended, while a solid ground plane is a must!**

Attention should be given to decoupling the power supplies. A large value (10μF) tantalum in parallel with a small value (0.1μF) chip capacitor works well in most cases.

Terminated microstrip signal lines are recommended at the input and output of the device. Capacitance directly on the output must be minimized, or isolated as discussed in the next section.

Care must also be taken to minimize the capacitance to ground at the amplifier's inverting input (-IN). The larger this capacitance, the worse the gain peaking, resulting in pulse overshoot and possible instability. Reduce this capacitance by removing the ground plane under traces connected to -IN, and keep connections to -IN as short as possible.

Driving Capacitive Loads

Capacitive loads, such as an A/D input, or an improperly terminated transmission line will degrade the amplifier's phase margin resulting in frequency response peaking and possible oscillations. In most cases, the oscillation can be avoided by placing a resistor (R_S) in series with the output prior to the capacitance.

Figure 1 details starting points for the selection of this resistor. The points on the curve indicate the R_S and C_L combinations for the optimum bandwidth, stability, and settling time, but experimental fine tuning is recommended. Picking a point above or to the right of the curve yields an overdamped response, while points below or left of the curve indicate areas of underdamped performance.

R_S and C_L form a low pass network at the output, thus limiting system bandwidth well below the amplifier bandwidth of 425MHz (for A_V = +2). By decreasing R_S as C_L increases (as illustrated in the curves), the maximum bandwidth is obtained without sacrificing stability. In spite of this, bandwidth still decreases as the load capacitance increases. For example, at A_V = +2, R_S = 50Ω, C_L = 22pF, the overall bandwidth is limited to 230MHz, and bandwidth drops to 80MHz at A_V = +2, R_S = 7Ω, C_L = 390pF.

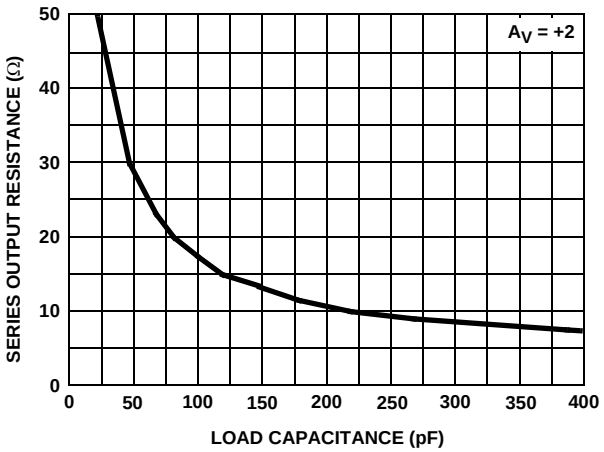


FIGURE 1. RECOMMENDED SERIES OUTPUT RESISTOR vs LOAD CAPACITANCE

Evaluation Board

The performance of the HFA1205 may be evaluated using the HA5023 Evaluation Board.

The performance of the HFA1205IB (SOIC) may be evaluated using the HA5023 Evaluation Board and a SOIC to DIP adaptor like the Aries Electronics Part Number 08-350000-10.

The schematic for amplifier 1 and the board layout are shown in Figure 2 and Figure 3. Resistors R_F, R_G and R_S may require a change to the appropriate value (see "Optimum Feedback Resistor" section) for the gain being evaluated.

To order evaluation boards (Part Number HA5023EVAL), please contact your local sales office.

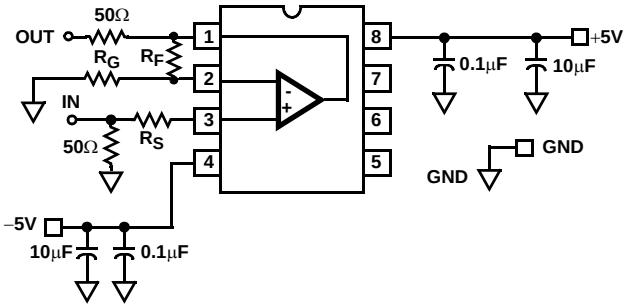


FIGURE 2. MODIFIED EVALUATION BOARD SCHEMATIC

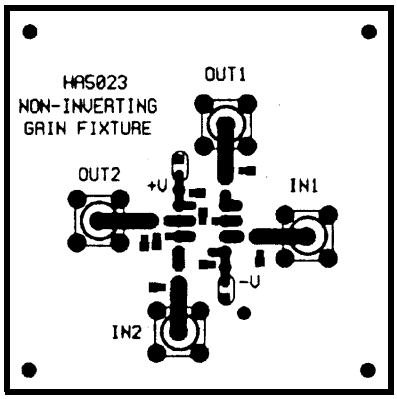


FIGURE 3A. TOP LAYOUT

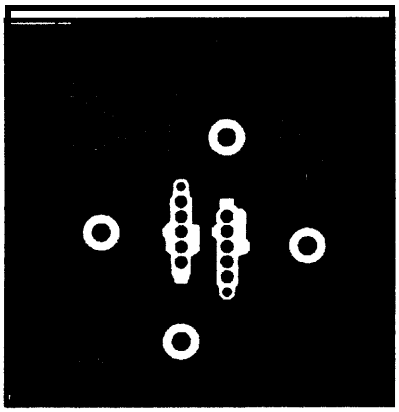


FIGURE 3B. BOTTOM LAYOUT

FIGURE 3. EVALUATION BOARD LAYOUT

Typical Performance Curves

$V_{SUPPLY} = \pm 5V$, R_F = Value From the Optimum Feedback Resistor Table, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified

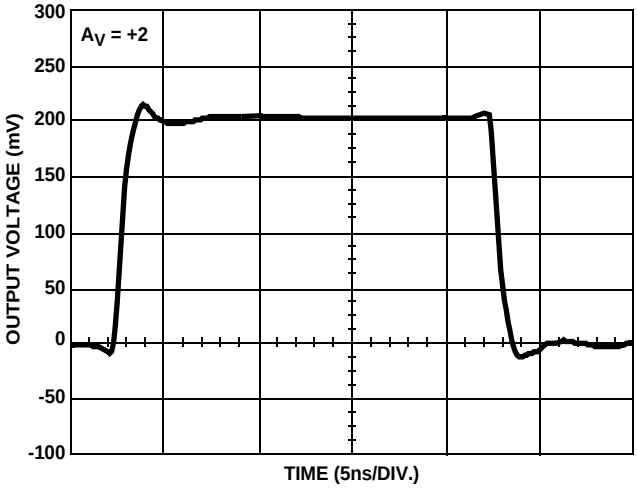


FIGURE 4. SMALL SIGNAL POSITIVE PULSE RESPONSE

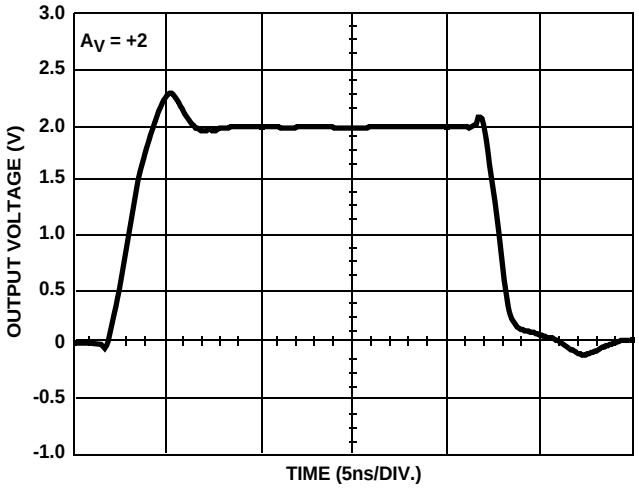


FIGURE 5. LARGE SIGNAL POSITIVE PULSE RESPONSE

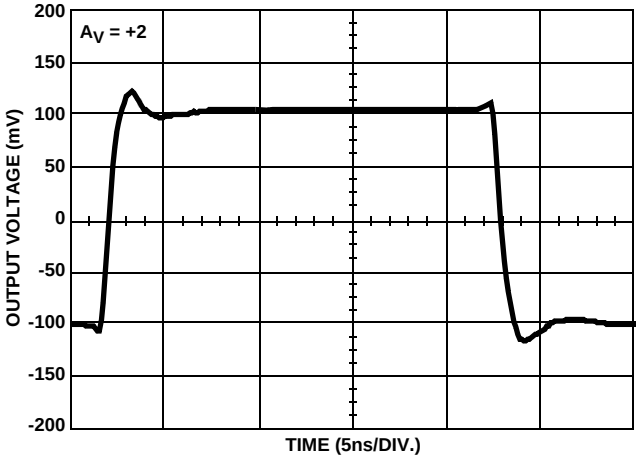


FIGURE 6. SMALL SIGNAL BIPOLAR PULSE RESPONSE

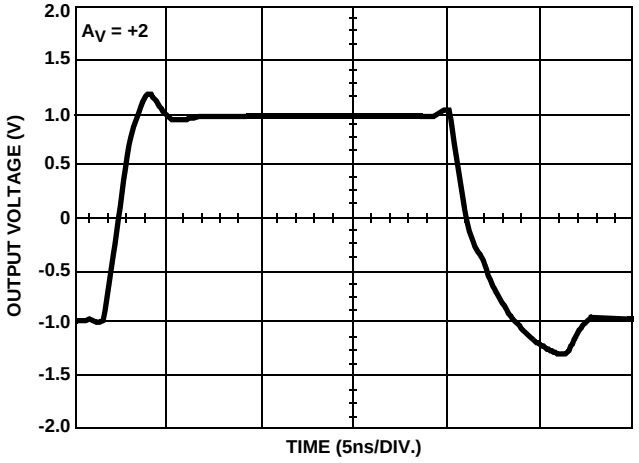


FIGURE 7. LARGE SIGNAL BIPOLAR PULSE RESPONSE

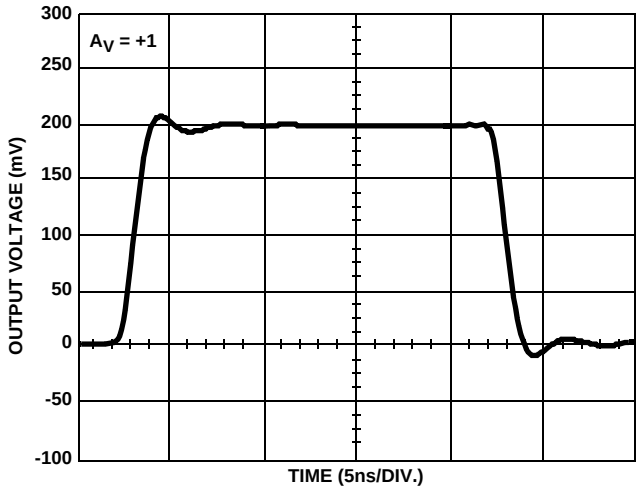


FIGURE 8. SMALL SIGNAL POSITIVE PULSE RESPONSE

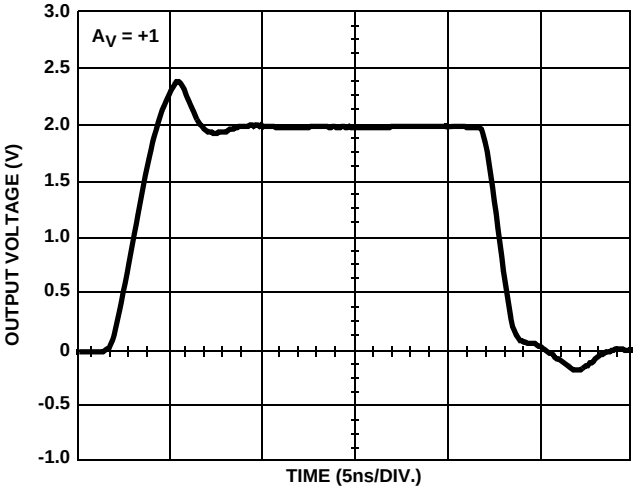


FIGURE 9. LARGE SIGNAL POSITIVE PULSE RESPONSE

Typical Performance Curves

$V_{SUPPLY} = \pm 5V$, R_F = Value From the Optimum Feedback Resistor Table, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

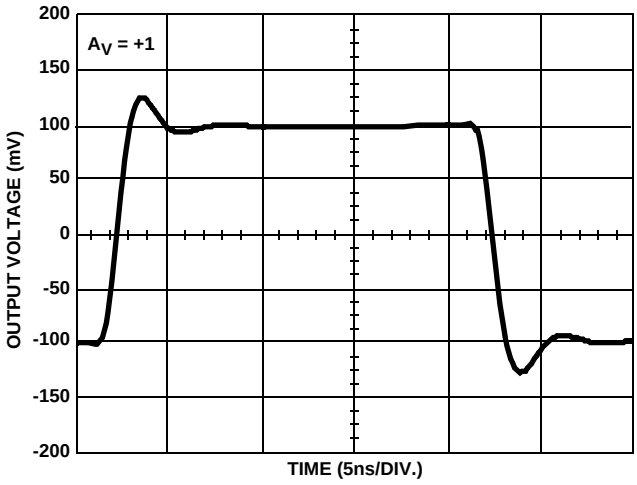


FIGURE 10. SMALL SIGNAL BIPOLAR PULSE RESPONSE

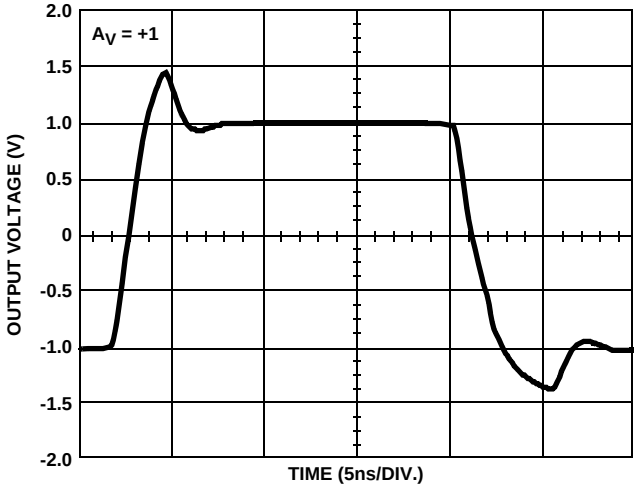


FIGURE 11. LARGE SIGNAL BIPOLAR PULSE RESPONSE

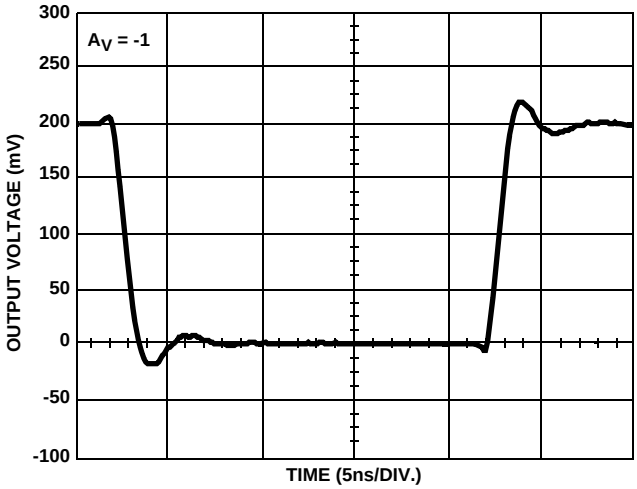


FIGURE 12. SMALL SIGNAL POSITIVE PULSE RESPONSE

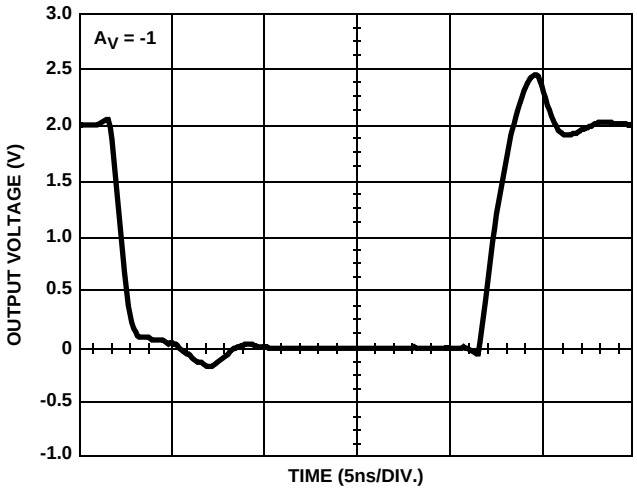


FIGURE 13. LARGE SIGNAL POSITIVE PULSE RESPONSE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, R_F = Value From the Optimum Feedback Resistor Table, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

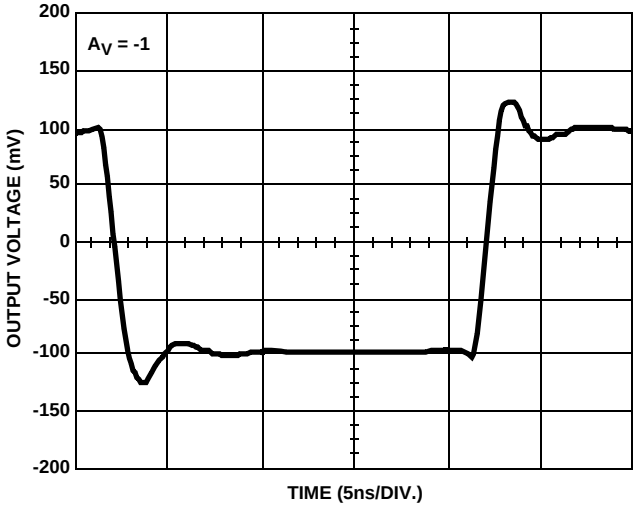


FIGURE 14. SMALL SIGNAL BIPOLAR PULSE RESPONSE

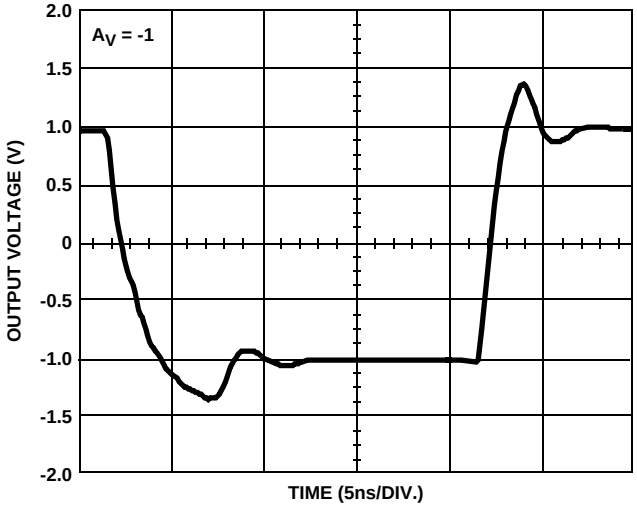


FIGURE 15. LARGE SIGNAL BIPOLAR PULSE RESPONSE

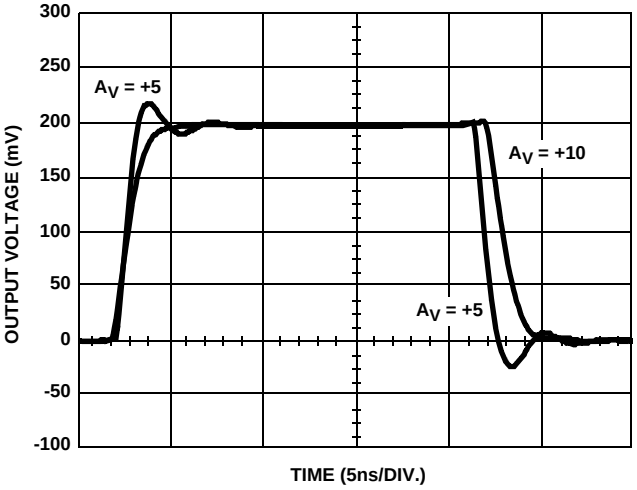


FIGURE 16. SMALL SIGNAL POSITIVE PULSE RESPONSE

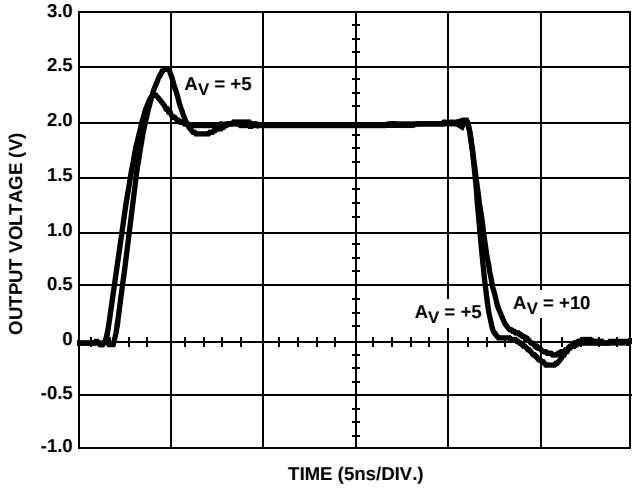


FIGURE 17. LARGE SIGNAL POSITIVE PULSE RESPONSE

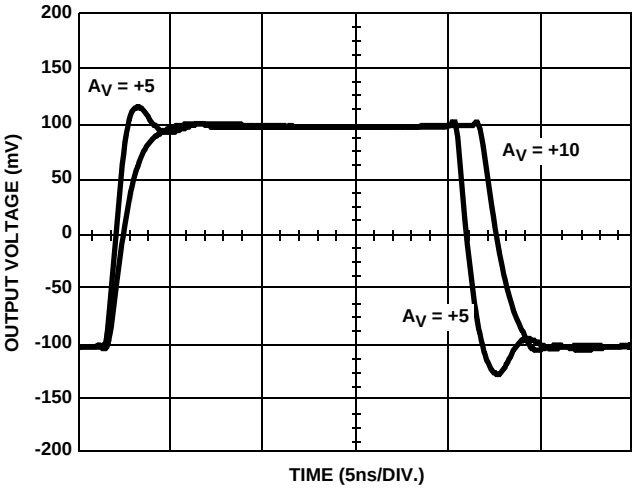


FIGURE 18. SMALL SIGNAL BIPOLAR PULSE RESPONSE

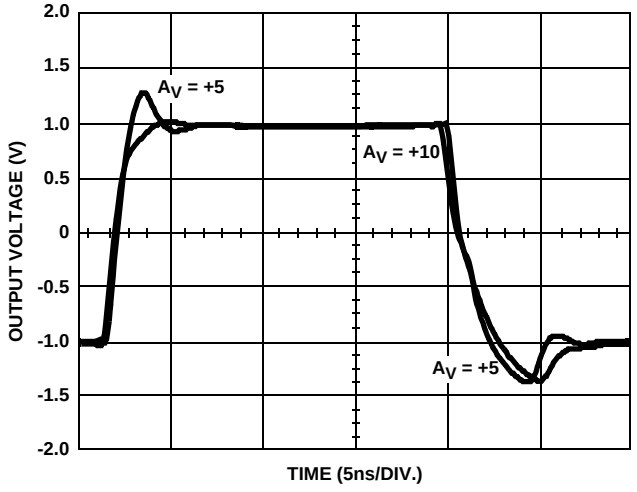


FIGURE 19. LARGE SIGNAL BIPOLAR PULSE RESPONSE

Typical Performance Curves

$V_{SUPPLY} = \pm5V$, R_F = Value From the Optimum Feedback Resistor Table, $T_A = 25^oC$, $R_L = 100\Omega$, Unless Otherwise Specified **(Continued)**

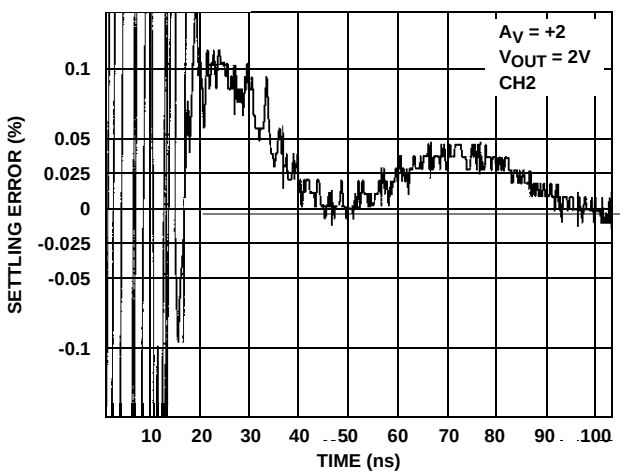


FIGURE 20. SETTLING TIME RESPONSE

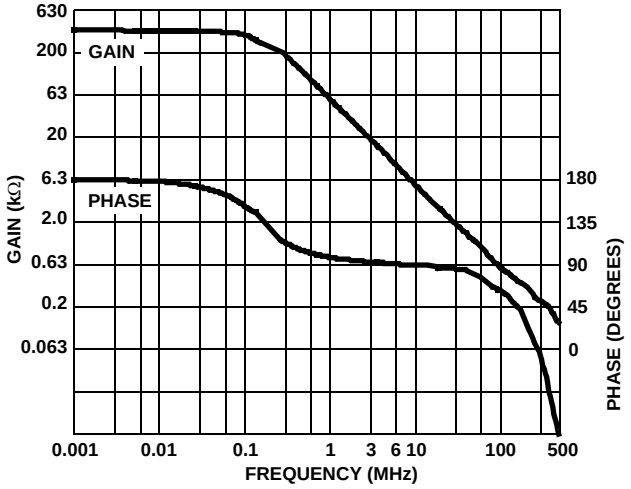


FIGURE 21. OPEN LOOP TRANSIMPEDANCE

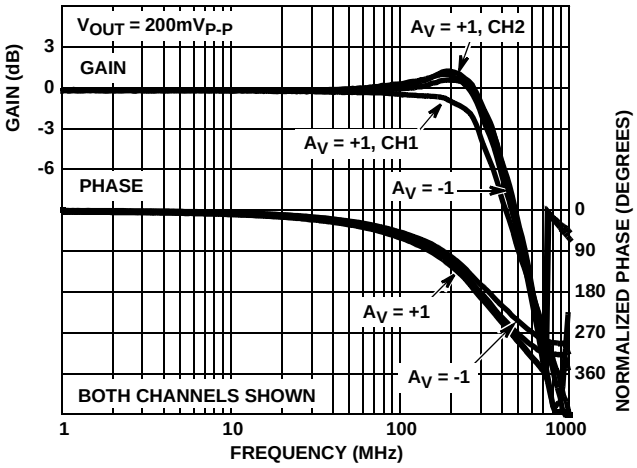


FIGURE 22. FREQUENCY RESPONSE

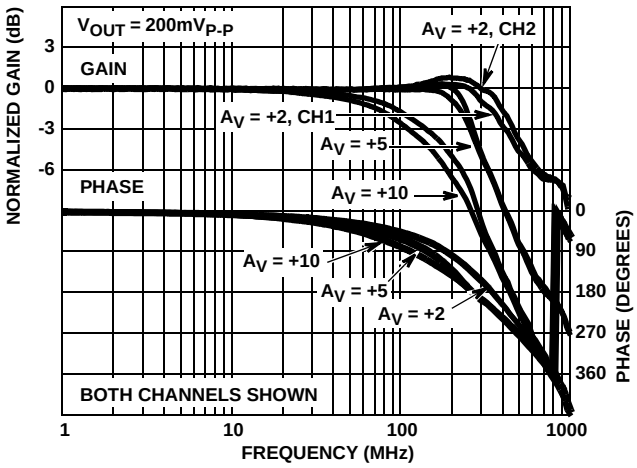


FIGURE 23. FREQUENCY RESPONSE

Typical Performance Curves

V_{SUPPLY} = ±5V, R_F = Value From the Optimum Feedback Resistor Table, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

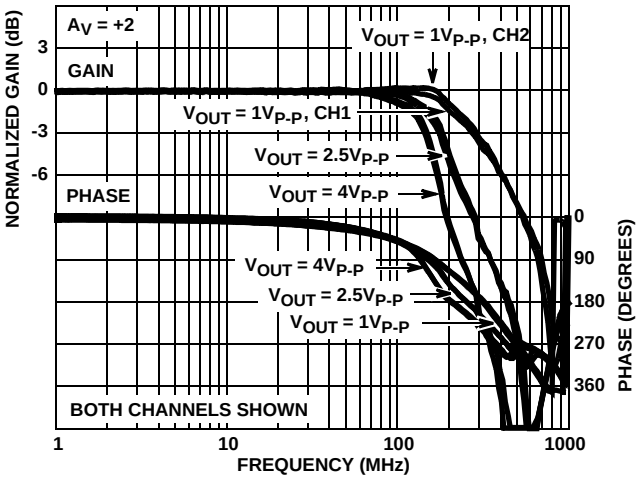


FIGURE 24. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

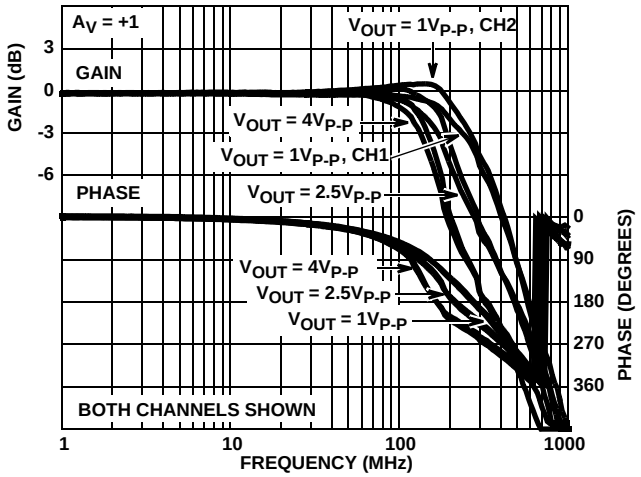


FIGURE 25. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

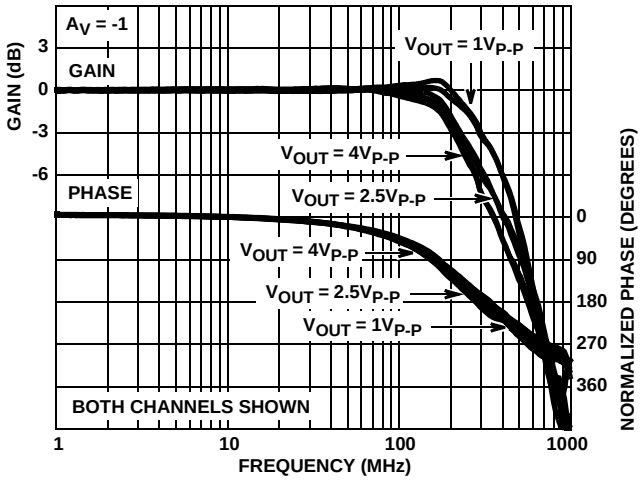


FIGURE 26. FREQUENCY RESPONSE FOR VARIOUS OUTPUT VOLTAGES

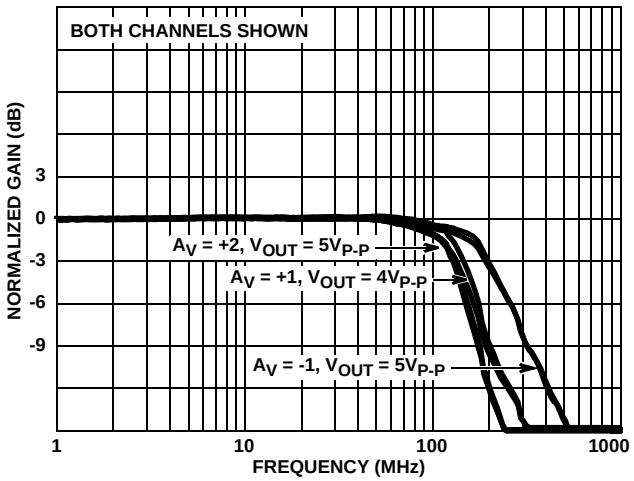


FIGURE 27. FULL POWER BANDWIDTH

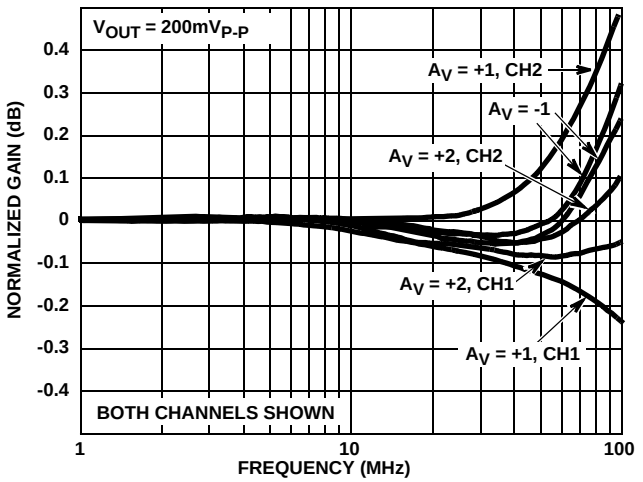


FIGURE 28. GAIN FLATNESS

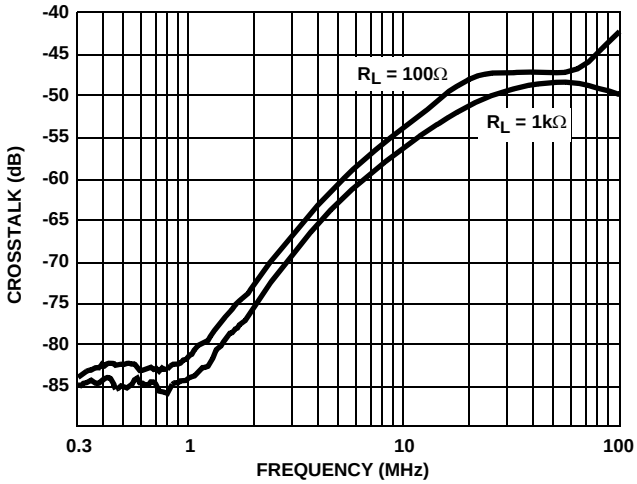


FIGURE 29. CROSSTALK

Typical Performance Curves

V_{SUPPLY} = ±5V, R_F = Value From the Optimum Feedback Resistor Table, T_A = 25°C, R_L = 100Ω, Unless Otherwise Specified **(Continued)**

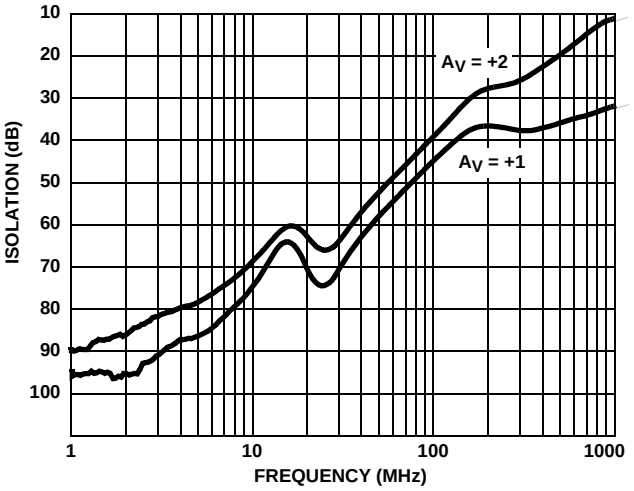


FIGURE 30. REVERSE ISOLATION (S_{12})

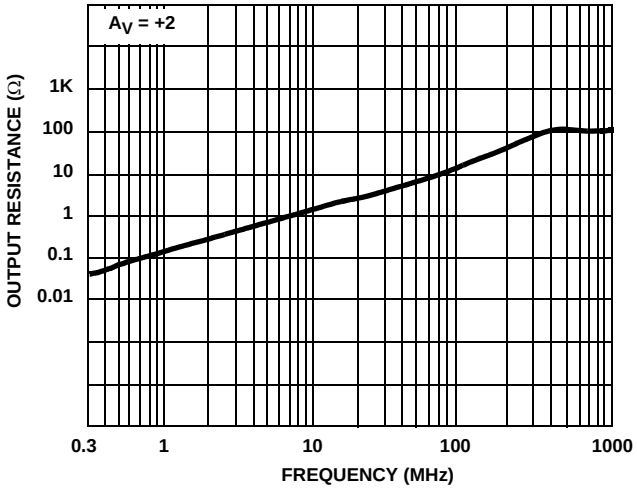


FIGURE 31. OUTPUT RESISTANCE

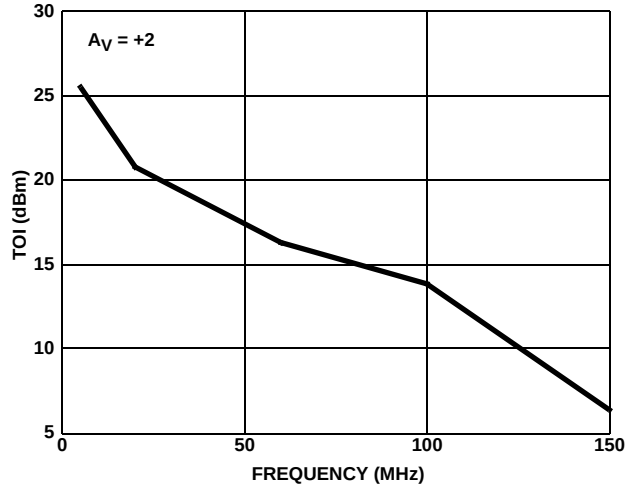


FIGURE 32. 3rd ORDER INTERCEPT vs FREQUENCY

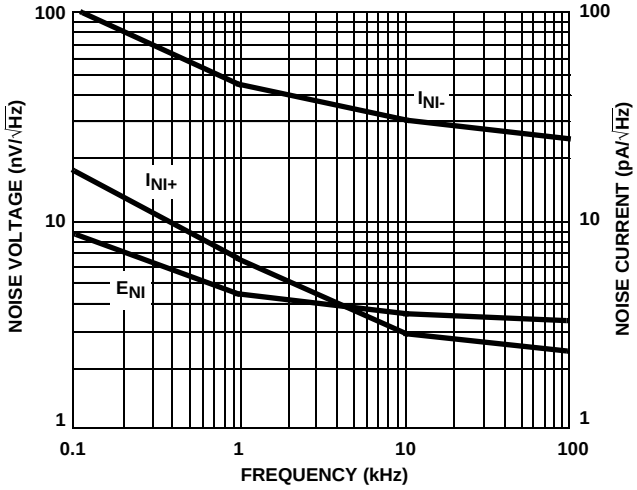


FIGURE 33. INPUT NOISE CHARACTERISTICS

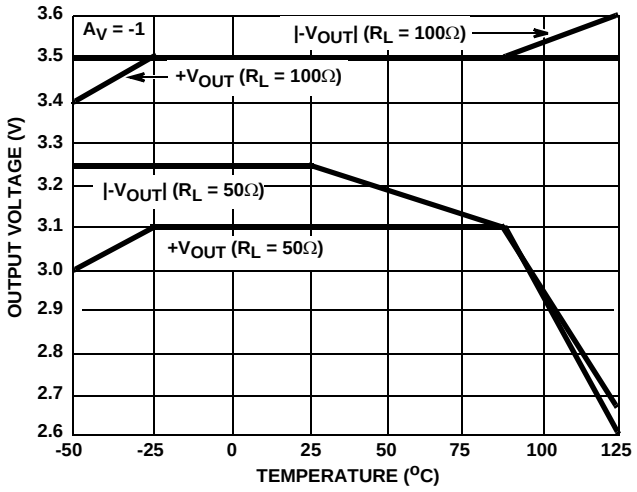


FIGURE 34. OUTPUT VOLTAGE vs TEMPERATURE

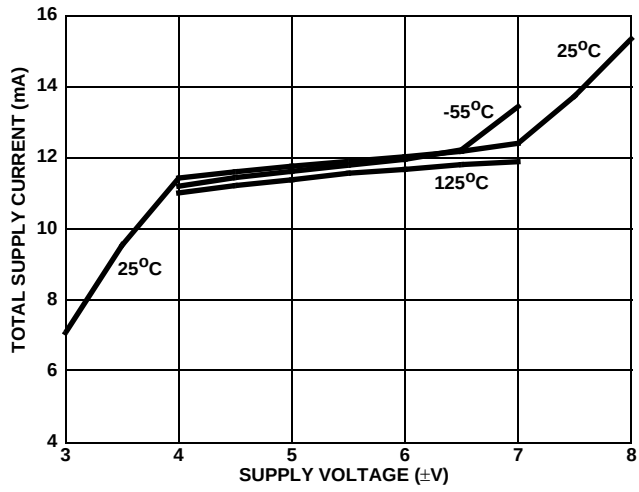


FIGURE 35. SUPPLY CURRENT vs SUPPLY VOLTAGE

Die Characteristics

DIE DIMENSIONS:

69 mils x 92 mils
1750μm x 2330μm

METALLIZATION:

Type: Metal 1: AICu (2%)/TiW
Thickness: Metal 1: 8kÅ ± 0.4kÅ
Type: Metal 2: AICu (2%)
Thickness: Metal 2: 16kÅ ± 0.8kÅ

SUBSTRATE POTENTIAL (POWERED UP):

Floating (Recommend Connection to V-)

PASSIVATION:

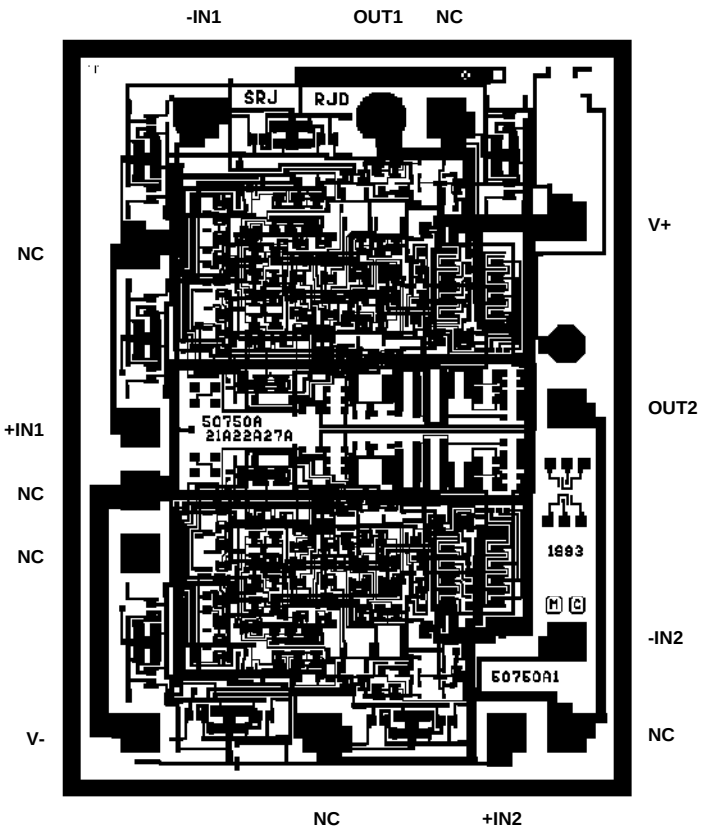
Type: Nitride
Thickness: 4kÅ ± 0.5kÅ

TRANSISTOR COUNT:

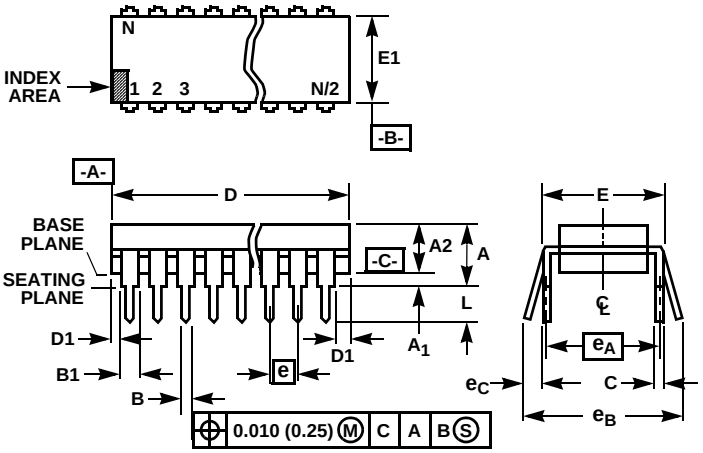
180

Metallization Mask Layout

HFA1205



Dual-In-Line Plastic Packages (PDIP)



NOTES:

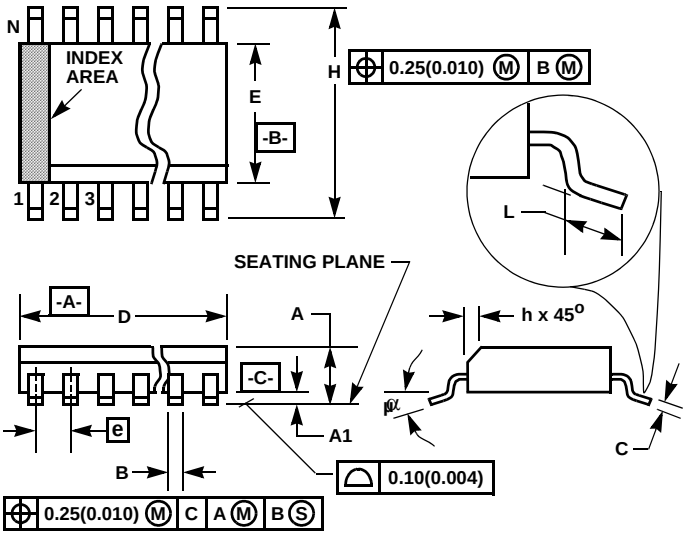
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E8.3 (JEDEC MS-001-BA ISSUE D)
8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

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Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M8.15 (JEDEC MS-012-AA ISSUE C)
8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0532	0.0688	1.35	1.75	-
A1	0.0040	0.0098	0.10	0.25	-
B	0.013	0.020	0.33	0.51	9
C	0.0075	0.0098	0.19	0.25	-
D	0.1890	0.1968	4.80	5.00	3
E	0.1497	0.1574	3.80	4.00	4
e	0.050 BSC		1.27 BSC		-
H	0.2284	0.2440	5.80	6.20	-
h	0.0099	0.0196	0.25	0.50	5
L	0.016	0.050	0.40	1.27	6
N	8		8		7
α	0^o	8^o	0^o	8^o	-

Rev. 0 12/93

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