NCP4200

Programmable Multi-Phase Synchronous Buck Converter with PMBus

The NCP4200 is an integrated power control IC with a PMBus interface. It combines a highly efficient, multi−phase, synchronous buck switching regulator controller with a PMBus interface, which enables digital programming of key system parameters to optimize system performance and provide feedback to the system.

It uses an internal 8−bit DAC to read a Voltage Identification (VID) code directly from the processor, which is used to set the output voltage between 0.375 V and 1.6 V.

This device uses a multi−mode PWM architecture to drive the logic−level outputs at a programmable switching frequency that can be optimized for VR size and efficiency. The NCP4200 can be programmed to provide 2−, 3−, or 4−phase operation, allowing for the construction of up to four complementary buck−switching stages. The NCP4200 supports $\overline{\text{PSI}}$, which is a Power Save Mode.

The NCP4200 includes a PMBus interface which can be used to program system set points such as voltage offset, load−line and phase balance and output voltage. Key system performance data, such as CPU current, CPU voltage, and power and fault conditions can also be read back over the PMBus from the NCP4200.

The NCP4200 is specified over the extended commercial temperature range of 0°C to +85°C and is available in a 40 Lead QFN package.

Features

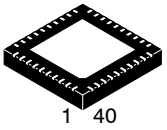
- Selectable 2−, 3−, or 4−Phase Operation at Up to 1.5 MHz per Phase
- PMBus Interface − Enables Digital Programmability of Set Points and Read−back of Monitored Values
- Logic−Level PWM Outputs for Interface to External High Power Drivers
- Fast−Enhanced PWM for Excellent Load Transient Performance
- Active Current Balancing Between All Output Phases
- Built−In Power−Good/Crowbar Blanking Supports On−The−Fly (OTF) VID Code Changes
- Digitally Programmable 0.375 V to 1.6 V Output Supports Both VR11 and VR11.1 Specifications
- Programmable Short−Circuit Protection with Programmable Latchoff Delay
- Supports $\overline{\text{PSI}}$ − Power Saving Mode During Light Loads

Applications

- Desktop PC Power Supplies for VRM Modules

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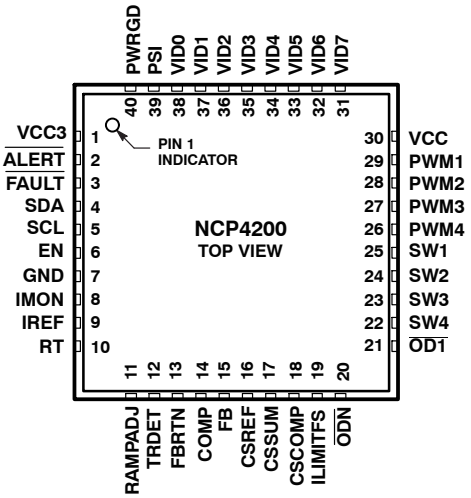
QFN40 6x6
CASE 488AR

MARKING DIAGRAM



A = Assembly Location
WL = Wafer Lot
YYWW = Date Code
G = Pb−Free Package

PIN ASSIGNMENT



ORDERING INFORMATION

Device*	Package	Shipping†
NCP4200MNR2G	QFN40	2500/Tape & Reel

*The "G' suffix indicates Pb−Free package.

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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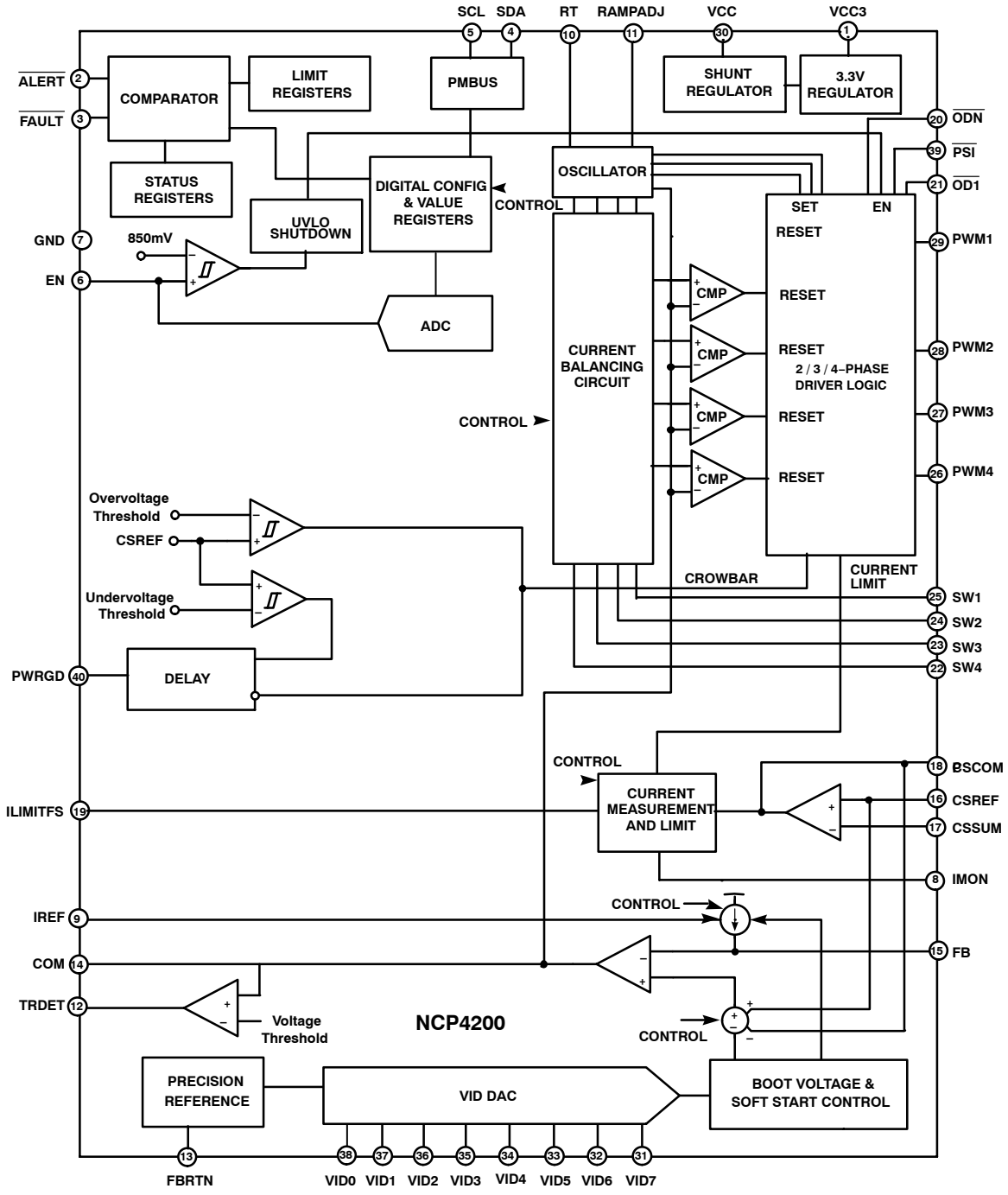


Figure 1. Simplified Block Diagram

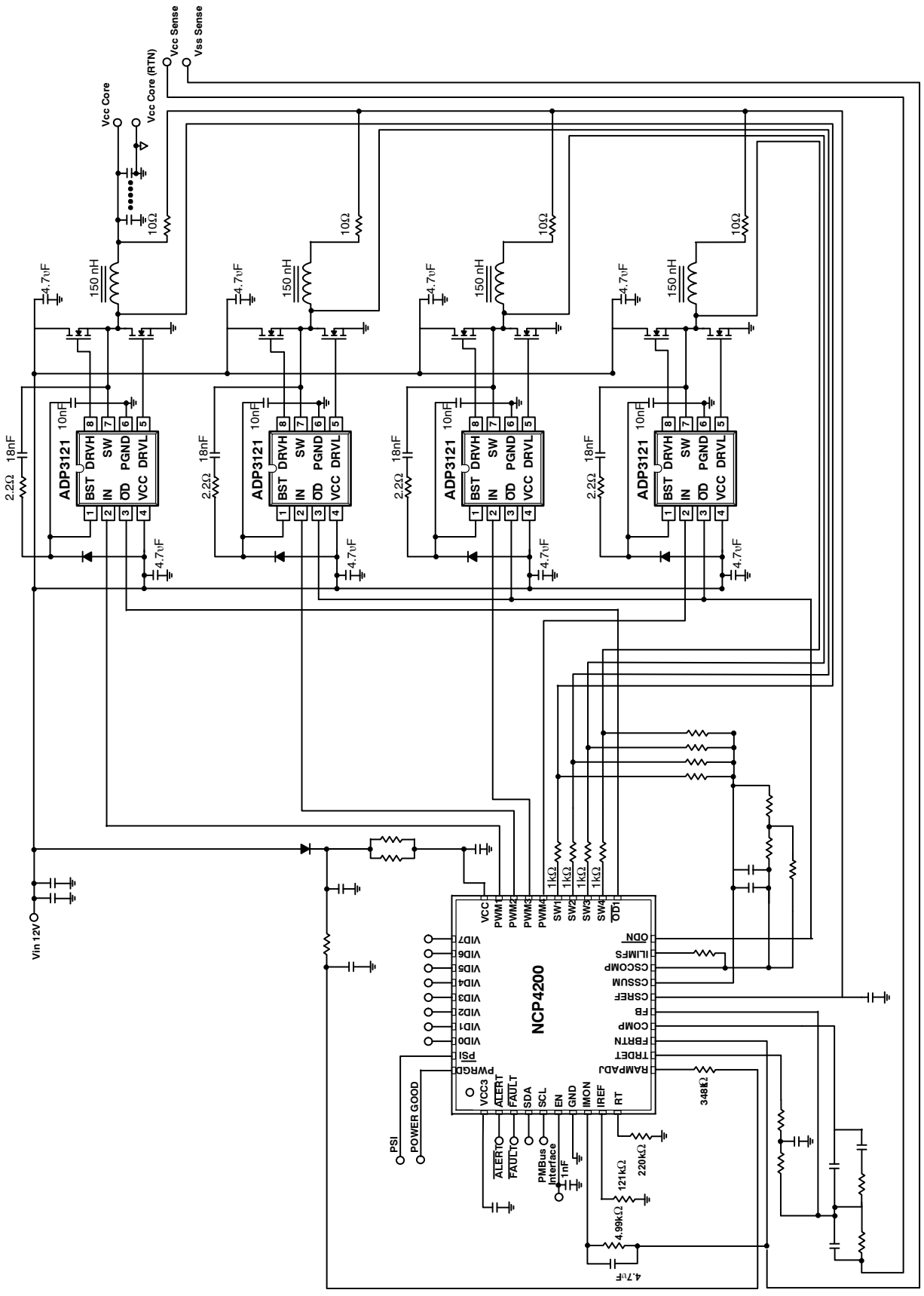


Figure 2. Application Circuit

ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Input Voltage Range (Note 1)	V_{IN}	−0.3 to 6.0	V
FBRTN	V_{FBRTN}	−0.3 to 0.3	V
PWM2 to PWM4, RAMPADJ		−0.3 to V_{IN} +0.3	V
SW1 to SW4		−5 to +25	V
SW1 to SW4 (< 200 ns)		−10 to +25	V
All Other Inputs and Outputs		−0.3 to V_{IN} + 0.3	V
Storage Temperature Range	T_{STG}	−65 to +150	°C
Operating Ambient Temperature Range		−10 to 100	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2	kV
ESD Capability, Machine Body Model (Note 2)	ESD_{MM}	100	V
Lead Temperature Soldering Re−flow (SMD Styles Only, Pb−Free Versions (Note 3)	T_{SLD}	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to Electrical Characteristics and Application Information for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
   ESD Human Body Model tested per AEC−Q100−002 (EIA/JESD22−A114)
   ESD Machine Model tested per AEC−Q100−003 (EIA/JESD22−A115)
   Latchup Current Maximum Rating: ≤150 mA per JEDEC standard: JESD78
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

THERMAL CHARACTERISTICS

Parameter	Symbol	Value	Unit
Thermal Characteristics; QFN, 6mm x 6mm (Note 1) Thermal Resistance, Junction−to−Air (Note 4)	$R_{\theta JA}$	27	°C/W

4. Values based on copper area of 645 mm^2 (or 1 in^2) of 1 oz copper thickness and FR4 PCB substrate.

OPERATING RANGES (Note 1)

Parameter	Symbol	Min	Max	Unit
Input Voltage (Note 5)	V_{IN}	1.7	24	V
Output Voltage (Adjustable Version Only)	V_{OUT}	0.375	1.8	V
Ambient Temperature	T_A	0	85	°C

5. Minimum V_{IN} = 1.7 V or (V_{OUT} + V_{DO}), whichever is higher. Maximum Limit for V_{OUT} = $V_{OUT(NOM)}$ − 10%.

PIN FUNCTION DESCRIPTIONS

Pin No	Mnemonic	Description
1	VCC3	3.3 V Power Supply Output. A capacitor from this pin to ground provided decoupling for the interval 3.3 V LDO.
2	$\overline{\text{ALERT}}$	$\overline{\text{ALERT}}$ Output. Open drain output that asserts low when the VR exceeds a programmable limit.
3	$\overline{\text{FAULT}}$	$\overline{\text{FAULT}}$ Output. Open drain output that asserts low when a fault has occurred. The fault can be due to VR or current limit, crowbar, or undervoltage. The trip points are loaded into registers.
4	SDA	Digital Input/Output. PMBus serial data bidirectional pin. Requires PMBus pullup.
5	SCL	Digital Input. PMBus serial bus clock open drain input. Requires PMBus pullup.
6	EN	Power Supply Enable Input. Pulling this pin to GND disables the PWM outputs and pulls the PWRGD output low.
7	GND	Ground. All internal biasing and the logic output signals of the device are referenced to this ground.
8	IMON	Analog Filter Output. A capacitor from this pin to ground sets the default current monitor filter frequency. The frequency can be modified using the serial interface.
9	IREF	Current Reference Input. An external resistor from this pin to ground sets the reference current for IFB, IILIMITFS and ITH(X).
10	RT	Frequency Setting Resistor Input. An external resistor connected between this pin and GND sets the oscillator frequency of the device.
11	RAMPADJ	PWM Ramp Current Input. An external resistor from the converter input voltage to this pin sets the internal PWM ramp.
12	TRDET	Transient Detect.
13	FBRTN	Feedback Return. VID DAC and error amplifier reference for remote sensing of the output voltage.
14	COMP	Error Amplifier Output and Compensation Point.
15	FB	Feedback Input. Error amplifier input for remote sensing of the output voltage. An external resistor between this pin and the output voltage sets the no load offset point.
16	CSREF	Current Sense Reference Voltage Input. The voltage on this pin is used as the reference for the current sense amplifier and the power−good and crowbar functions. This pin should be connected to the common point of the output inductors.
17	CSSUM	Current Sense Summing Node. External resistors from each switch node to this pin sum the average inductor currents together to measure the total output current.
18	CSCOMP	Current Sense Compensation Point. A resistor and capacitor from this pin to CSSUM determines the gain of the current sense amplifier and the positioning loop response time.
19	ILIMITFS	Current Sense and Limit Scaling Pin. An external resistor from this pin to CSCOMP sets the internal current sensing signal for current limit and IMON. This value can be overwritten using the PMBus interface.
20	$\overline{\text{ODN}}$	Output Disable Logic Output for phases 2−4. This pin is actively pulled low when the EN input is low or when VCC is below its UVLO threshold to signal to the Driver IC that the driver high−side and low−side outputs should go low.
21	$\overline{\text{OD1}}$	Output Disable Logic Output for phase one. This pin is actively pulled low when the EN input is low or when VCC is below its UVLO threshold to signal to the Driver IC that the driver high−side and low−side outputs should go low.
22 to 25	SW4 to SW1	Current Balance Inputs. Inputs for measuring the current level in each phase. The SW pins of unused phases should be left open.
26 to 29	PWM4 to PWM1	Logic−Level PWM Outputs. Each output is connected to the input of an external MOSFET driver such as the ADP3120A. Connecting the PWM4, and PWM3 outputs to VCC causes that phase to turn off, allowing the NCP4200 to operate as a 2−phase controller.
30	VCC	Supply Voltage for the Device.
31 to 38	VID7 to VID0	Voltage Identification DAC Inputs. These eight pins are pulled down to GND, providing a logic zero if left open. When in normal operation mode, the DAC output programs the FB regulation voltage from 0.375 V to 1.6 V.
39	$\overline{\text{PSI}}$	Power Save Interface. System signal to select single phase option.
40	PWRGD	Power−Good Output. Open−drain output that signals when the output voltage is outside of the proper operating range.

ELECTRICAL CHARACTERISTICS V_{IN} = 5.0 V, FBRTN = GND for typical values T_A = 0°C to 85°C, unless otherwise noted. (Note 1 and 3).

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
REFERENCE CURRENT						
Reference Bias Voltage	V_{IREF}		1.75	1.8	1.9	V
Reference Bias Current	I_{IREF}	R_{IREF} = 121 kΩ		16		μA
ERROR AMPLIFIER						
Output Voltage Range (Note 1)	V_{COMP}		0		4.4	V
Accuracy	V_{FB}	Relative to nominal DAC output, referenced to FBRTN (Note 2)	−7.7		+7.7	mV
	$V_{FB(BOOT)}$	In startup	1.091	1.1	1.109	V
Load Line Positioning Accuracy			−77	−80	−83	mV
Load Line Range			−350		0	mV
Load Line Attenuation			0		100	%
Differential Non−linearity			−1.0		+1.0	LSB
Input Bias Current	I_{FB}	I_{FB} = I_{IREF}	14.2	16	17.7	μA
Offset Accuracy		VR Offset Register = 111111, VID = 1.0 V VR Offset Register = 011111, VID = 1.0 V		−193.75 193.75		mV
FBRTN Current	I_{FBRTN}			70	200	μA
Output Current	I_{COMP}	FB forced to V_{OUT} − 3%		500		μA
Gain Bandwidth Product	$GBW_{(ERR)}$	COMP = FB		20		MHz
Slew Rate		COMP = FB		25		V/μs
BOOT Voltage Hold Time	t_{BOOT}	Internal Timer		2.0		ms
VID INPUTS						
Input Low Voltage	$V_{IL(VID)}$	VID(X)			0.3	V
Input High Voltage	$V_{IH(VID)}$	VID(X)	0.8			V
Input Current	$I_{IN(VID)}$			−5.0		μA
VID Transition Delay Time (Note 1)		VID code change to FB change	200			ns
No CPU Detection Turn−Off Delay Time		VID code change to PWM going low	5			μs
OSCILLATOR						
Frequency Range (Note 1)	f_{OSC}		0.25		6.0	MHz
Frequency Variation	f_{PHASE}	T_A = 25°C, R_T = 460kΩ, 4−phase T_A = 25°C, R_T = 220kΩ, 4−phase T_A = 25°C, R_T = 120kΩ, 4−phase	220	260 500 850	290	kHz
Output Voltage	V_{RT}	R_T = 500 kΩ to GND	1.93	2.03	2.13	V
RAMPADJ Output Voltage	$V_{RAMPADJ}$	RAMPADJ − FB, V_{FB} = 1.0 V, $I_{RAMPADJ}$ = −50 μA	−50		+50	mV
RAMPADJ Input Current Range	$I_{RAMPADJ}$		5.0		60	μA
CURRENT SENSE AMPLIFIER						
Offset Voltage	$V_{OS(CSA)}$	CSSUM − CSREF (Note 3)	−0.7		+0.7	mV
Input Bias Current, CSREF	$I_{BIAS(CSREF)}$	CSREF = 1.0 V	−20		+20	μA
Input Bias Current, CSSUM	$I_{BIAS(CSSUM)}$	CSREF = 1.0 V	−10		+10	nA
Gain Bandwidth Product	$GBW_{(CSA)}$	CSSUM = CSCOMP		10		MHz
Slew Rate		C_{CSCOMP} = 10 pF		10		V/μs
Input Common−Mode Range		CSSUM and CSREF	0		3.0	V
Output Voltage Range			0.05		3.0	V
Output Current	I_{CSCOMP}			500		μA
Current Limit Latchoff Delay Time		Internal Timer		8.0		ms

ELECTRICAL CHARACTERISTICS V_{IN} = 5.0 V, FBRTN = GND for typical values T_A = 0°C to 85°C, unless otherwise noted. (Note 1 and 3).

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
$\overline{PSI}$						
Input Low Voltage					0.3	V
Input High Voltage			0.8			V
Input Current				−5.0		μA
Assertion Timing		Fsw = 300 kHz		3.3		μs
De−assertion Timing		Fsw = 300 kHz		825		ns
TRDET						
Output Low Voltage	V_{OL}	I_{OUT} = −6 mA		150	300	mV
IMON						
Clamp Voltage			1.0		1.15	V
Accuracy		10 x (CSREF − CSCOMP)/R_{ILIM}	−3.0		3.0	%
Output Current					800	μA
Offset			−3.0		3.0	mV
CURRENT LIMIT COMPARATOR						
I_{LIM} Bias Current	I_{LIM}	CSREF − CSCOMP)/RILIM, (CSREF − CSCOMP) = 150 mV, RILIMC = 7.5 kΩ		20		μA
Current Limit Threshold Current	I_{CL}	4/3 x I_{IREF}		20		μA
CURRENT BALANCE AMPLIFIER						
Common−Mode Range	$V_{SW(X)CM}$		−600		+200	mV
Input Resistance	$R_{SW(X)}$	SW(X) = 0 V	14	18	21	kΩ
Input Current	$I_{SW(X)}$	SW(X) = 0 V	8	12	28	μA
Input Current Matching	$\Delta I_{SW(X)}$	SW(X) = 0 V	−6.0		+6.0	%
Phase Balance Adjustment Range Low		Phase Bal Registers = 00000		−25		%
Phase Balance Adjustment Range High		Phase Bal Registers = 11111		+25		%
DELAY TIMER						
Internal Timer		Delay Time Register = 011		2.0		ms
Timer Range Low		Delay Time Register = 000		0.5		ms
Timer Range High		Delay Time Register = 111		4.0		ms
SOFT−START						
Internal Timer		Soft−Start Slope Register = 010		0.5		V/ms
Timer Range Low		Soft−Start Slope Register = 000		0.1		V/ms
Timer Range High		Soft−Start Slope Register = 111		1.5		V/ms
ENABLE INPUT						
Input Low Voltage	$V_{IL(EN)}$				0.3	V
Input High Voltage	$V_{IH(EN)}$		0.8			V
Input Current	$I_{IN(EN)}$			−1.0		μA
Delay Time	$t_{DELAY(EN)}$	EN > 0.8V , Internal Delay		2.0		ms
$\overline{ODN}$ / $\overline{OD1}$ OUTPUTS						
Output Low Voltage	$V_{OL(\overline{OD1})}$	$I_{OD(SINK)}$ = −400 μA		160	500	mV
Output High Voltage	$V_{OH(\overline{ODN/1})}$	$I_{OD(SOURCE)}$ = 400 μA	4.0	5.0		V
$\overline{ODN}$/$\overline{OD1}$ Pulldown Resistor				60		kΩ

ELECTRICAL CHARACTERISTICS V_{IN} = 5.0 V, FBRTN = GND for typical values T_A = 0°C to 85°C, unless otherwise noted. (Note 1 and 3).

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
POWER−GOOD COMPARATOR						
Undervoltage Threshold	$V_{PWRGD(UV)}$	Relative to nominal DAC output	−600	−500	−400	mV
Undervoltage Adjustment Range Low		PWRGD_LO Register = 000		−500		mV
Undervoltage Adjustment Range High		PWRGD_LO Register = 111		−150		mV
Overvoltage Threshold	$V_{PWRGD(OV)}$	Relative to DAC output, PWRGD_Hi = 00	200	300	400	mV
Overvoltage Adjustment Range Low		PWRGD_Hi Register = 11		150		mV
Overvoltage Adjustment Range High		PWRGD_Hi Register = 00		300		mV
Output Low Voltage	$V_{OL(PWRGD)}$	$I_{PWRGD(SINK)}$ = −4 mA		150	300	mV
Power Good Delay Time						
During Soft−Start		Internal Timer		2.0		ms
VID Code Changing			100	250		μs
VID Code Static				200		ns
Crowbar Trip Point	$V_{CROWBAR}$	Relative to DAC output, PWRGD_Hi = 00	200	300	400	mV
Crowbar Adjustment Range		PWRGD_HI Register	150		300	mV
Crowbar Reset Point		Relative to FBRTN	250	300	350	mV
Crowbar Delay Time	$t_{CROWBAR}$	Overvoltage to PWM going low				
VID Code Changing			100	250		μs
VID Code Static				400		ns
PWM OUTPUTS						
Output Low Voltage	$I_{PWM(SINK)}$ = −400 μA	$V_{OL(PWM)}$		160	500	mV
Output High Voltage	$I_{PWM(SOURCE)}$ = 400 μA	$V_{OH(PWM)}$	4.0	5.0		V
PMBus INTERFACE						
Logic High Input Voltage	$V_{IH(SDA, SCL)}$		2.1			V
Logic Input Low Voltage	$V_{IL(SDA, SCL)}$				0.8	V
Hysteresis				500		mV
SDA Output Low Voltage	V_{OL}	I_{SDA} = −6mA			0.4	V
Input Current	I_{IH}; I_{IL}		−1.0		1.0	μA
Input Capacitance	$C_{SCL, SDA}$			5.0		pF
Clock Frequency	f_{SCL}				400	kHz
SCL Falling Edge to SDA Valid Time					1.0	μs
$\overline{\text{ALERT}}$ / $\overline{\text{FAULT}}$ OUTPUTS						
Output Low Voltage	V_{OL}	I_{OUT} = −6 mA			0.4	V
Output High Leakage Current	I_{OH}	V_{OH} = 5.0 V			1.0	uA
ANALOG / DIGITAL CONVERTER						
ADC Input Voltage Range			0		2	V
Total Unadjusted Error (TUE)				±1		%
Differential Non−linearity (DNL)		8 Bits		1.0		LSB
Conversion Time, Voltage Channel		Averaging Enabled (32 averages)		80		ms

ELECTRICAL CHARACTERISTICS V_{IN} = 5.0 V, FBRTN = GND for typical values T_A = 0°C to 85°C, unless otherwise noted. (Note 1 and 3).

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
SUPPLY						
VCC (Note 1)		VCC	4.70	5.25	5.75	V
DC Supply Current	I_{VCC}	V_{SYSTEM} = 13.2 V, R_{SHUNT} = 340 Ω		20	25	mA
UVLO Turn−On Current				6.5	11	mA
UVLO Threshold Voltage	V_{UVLO}	VCC rising	10			V
UVLO Turn−Off Voltage		VCC falling		4.1		V
VCC3 Output Voltage	VCC3	I_{VCC3} = 1 mA	3.0	3.3	3.6	V

1. Refer to Electrical Characteristics and Application Information for Safe Operating Area.
2. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.
3. Values based on design and/or characterization.

TYPICAL CHARACTERISTICS

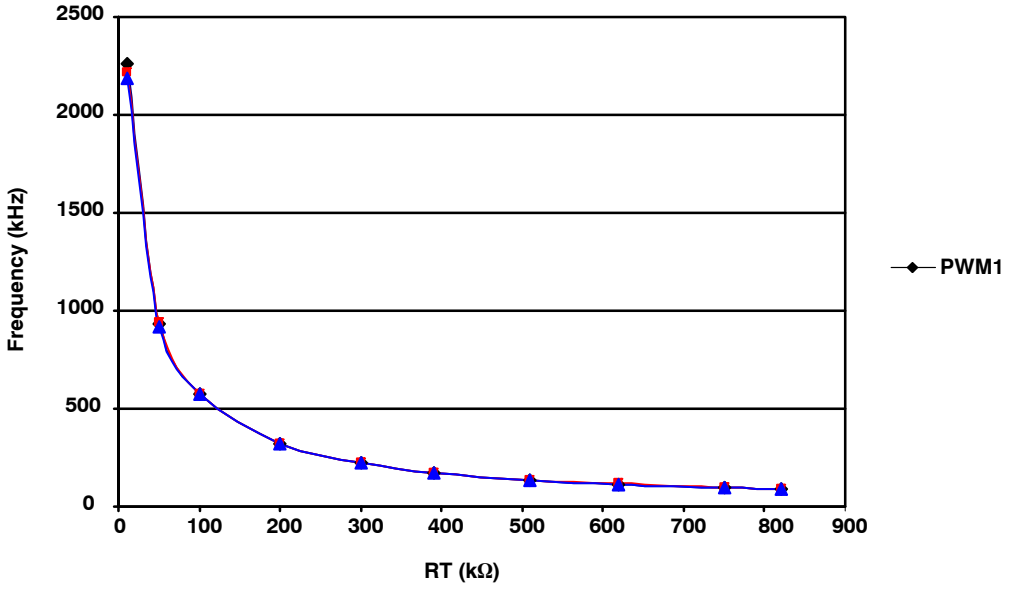


Figure 3. Master Clock Frequency vs. RT

TEST CIRCUITS

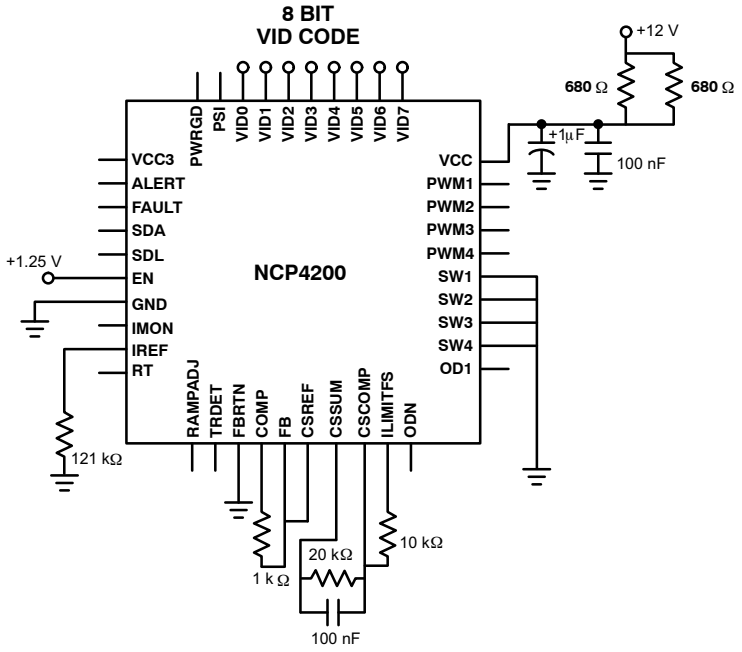


Figure 4. Closed−Loop Output Voltage Accuracy

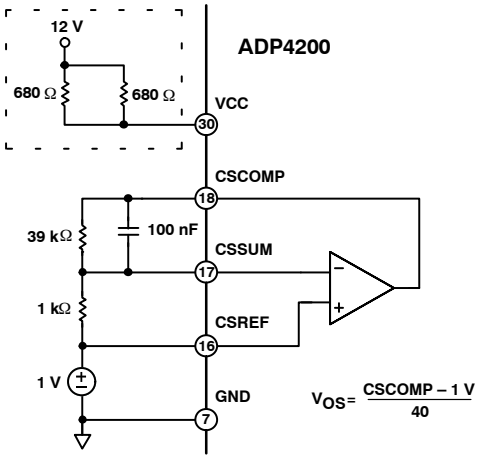


Figure 5. Current Sense Amplifier VOS

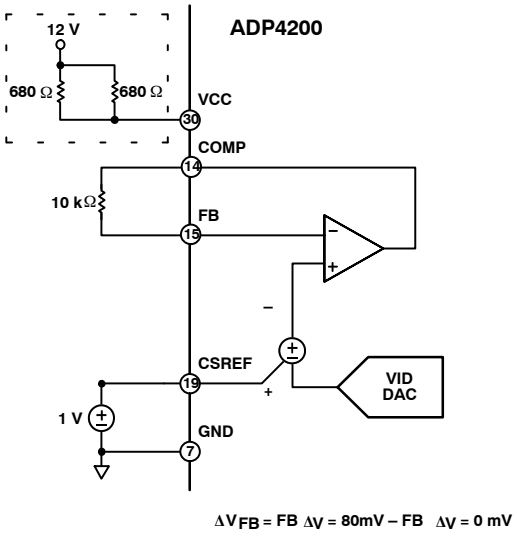


Figure 6. Positioning Voltage

Description

The NCP4200 is a 4 Phase DC−DC regulator with a PMBus Interface. A typical application circuit is shown in Figure 2.

Startup Sequence

The NCP4200 follows the startup sequence shown in Figure 7. After both the EN and UVLO conditions are met, a programmable internal timer goes through one delay cycle TD1. This delay cycle is programmed using Delay Command, default delay = 2 ms, see Table 2 for programmable values. The first six clock cycles of TD2 are blanked from the PWM outputs and used for phase detection as explained in the following section. Then the programmable internal soft−start ramp is enabled (TD2) and the output comes up to the boot voltage of 1.1 V. The boot hold time is also set by Delay Command. This second delay cycle is called TD3. During TD3 the processor VID pins settle to the required VID code. When TD3 is over, the NCP4200 reads the VID inputs and soft−starts either up or down to the final VID voltage (TD4). After TD4 has been completed and the PWRGD masking time (equal to VID OTF masking) is finished, a third cycle of the internal timer sets the PWRGD blanking (TD5).

The internal delay and soft−start times are programmable using the serial interface, the Delay Command and the Soft−Start Commands.

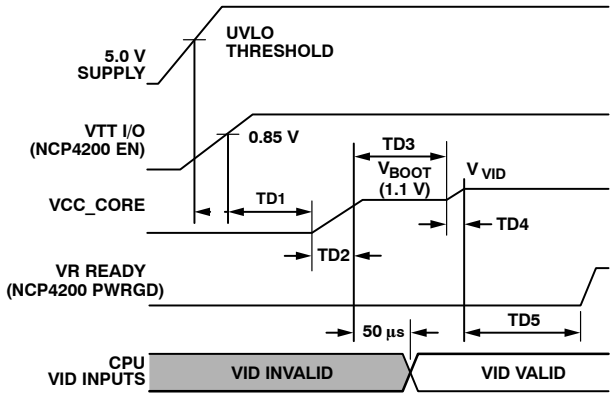


Figure 7. Startup Sequence

Internal Delay Timer

An internal timer sets the delay times for the start up sequence, TD1, TD3 and TD5. The default time is 2 msec, which can be changed using the PMBus interface. This timer is used for multiple delay timings (TD1, TD3 and TD5) during the startup sequence. Also, it is used for timing the current limit latchoff as explained in the Current Limit section. The current limit timer is set to 4 times the delay timer.

The delay timer is programmed using Bits <2:0> of the Ton Delay command (0xD4). The delay can be programmed between 0.5 msec and 4 msec. Table 1 provides the programmable delay times.

Table 1. Delay Codes

Code	Delay (msec)
000	0.5
001	1
010	1.5
011	2 = default
100	2.5
101	3
110	3.5
111	4

Soft−Start

The Soft−Start slope for the output voltage is set by an internal timer. The default value is 0.5 V/msec, which can be programmed through the PMBus interface. After TD1 and the phase detection cycle have been completed, the SS time (TD2 in Figure 2) starts. The SS circuit uses the internal VID DAC to increase the output voltage in 6.25 mV steps up to the 1.1 V boot voltage.

Once the SS circuit has reached the boot voltage, the boot voltage delay time (TD3) is started. The end of the boot voltage delay time signals the beginning of the second soft−start time (TD4). The SS voltage changes from the boot voltage to the programmed VID DAC voltage (either higher or lower) using 6.25 mV steps.

The soft−start slew rate is programmed using Bits <2:0> of the Ton_Rise (0xD5) command code. Table 2 provides the soft−start values.

Table 2. Slew Rate Codes

Code	Slew Rate (V/msec)
000	0.1
001	0.3
010	0.5 = default
011	0.7
100	0.9
101	1.1
110	1.3
111	1.5

Figure 8 shows typical startup waveforms for the NCP4200.

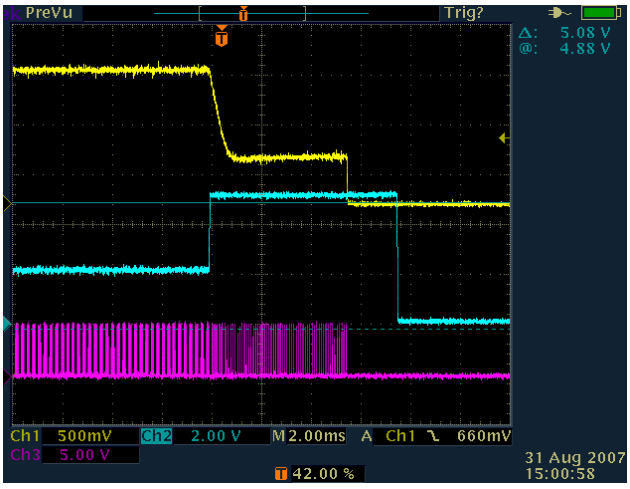


Figure 8. Typical Startup Waveforms

Phase Detection

During startup, the number of operational phases and their phase relationship is determined by the internal circuitry that monitors the PWM outputs. Normally, the NCP4200 operates as a 4−phase PWM controller.

To operate as a 3−Phase Controller: connect PWM4 to V_{CC}.

To operate as a 2−Phase Controller: connect PWM3 and PWM4 to V_{CC}.

To operate as a single phase controller: connect PMW2, PWM3, and PWM4 to V_{CC}.

Prior to soft−start, while EN is high the PWM4, PWM3 and PWM2 pins sink approximately 100 μA each. An internal comparator checks each pin's voltage vs. a threshold of 3.0 V. If the pin is tied to V_{CC}, it is above the threshold. Otherwise, an internal current sink pulls the pin to GND, which is below the threshold. PWM1 is low during the phase detection interval that occurs during the first six clock cycles of TD2. After this time, if the remaining PWM outputs are not pulled to V_{CC}, the 100 μA current sink is removed, and they function as normal PWM outputs. If they are pulled to V_{CC}, the 100 μA current source is removed, and the outputs are put into a high impedance state.

The PWM outputs are logic−level devices intended for driving fast response external gate drivers such as the ADP3121. Because each phase is monitored independently, operation approaching 100% duty cycle is possible. In addition, more than one output can be on at the same time to allow overlapping phases.

Master Clock Frequency

The clock frequency of the NCP4200 is set with an external resistor connected from the RT pin to ground. The frequency follows the graph in Figure 3. To determine the frequency per phase, the clock is divided by the number of phases in use. If all phases are in use, divide by 4. If 2 phases are in use then divide by 2.

Output Voltage Differential Sensing

The NCP4200 combines differential sensing with a high accuracy VID DAC and reference, and a low offset error amplifier. This maintains a worst−case specification of ±9 mV differential sensing error over its full operating output voltage and temperature range. The output voltage is sensed between the FB pin and FBRTN pin. FB is connected through a resistor, R_B, to the regulation point, usually the remote sense pin of the microprocessor. FBRTN is connected directly to the remote sense ground point. The internal VID DAC and precision reference are referenced to FBRTN, which has a minimal current of 70 μA to allow accurate remote sensing. The internal error amplifier compares the output of the DAC to the FB pin to regulate the output voltage.

Output Current Sensing

The NCP4200 provides a dedicated Current Sense Amplifier (CSA) to monitor the total output current for proper voltage positioning vs. load current, for the I_{MON} output and for current limit detection. Sensing the load current at the output gives the total real time current being delivered to the load, which is an inherently more accurate method than peak current detection or sampling the current across a sense element such as the low−side MOSFET. This amplifier can be configured in several ways, depending on the objectives of the system, as follows:

- Output inductor DCR sensing without a thermistor for lower cost.
- Output inductor DCR sensing with a thermistor for improved accuracy with inductor temperature tracking.
- Sense resistors for highest accuracy measurements.

The positive input of the CSA is connected to the CSREF pin, which is connected to the average output voltage. The inputs to the amplifier are summed together through resistors from the sensing element, such as the switch node side of the output inductors, to the inverting input CSSUM. The feedback resistor between CSCOMP and CSSUM sets the gain of the amplifier and a filter capacitor is placed in parallel with this resistor. The gain of the amplifier is programmable by adjusting the feedback resistor. This difference signal is used internally to offset the VID DAC for voltage positioning. This difference signal can be adjusted between 50% and 150% of the external value using the PMBus Load−line Calibration (0xDE) and Load−line Set (0xDF) commands. The difference between CSREF and CSCOMP is used as a differential input for the current limit comparator.

To provide the best accuracy for sensing current, the CSA is designed to have a low offset input voltage. Also, the sensing gain is determined by external resistors to make it extremely accurate.

The CPU current can also be monitored over the PMBus. The current limit and the load−line can be adjusted from the circuit component values over the PMBus.

Current Limit Set−Point

The current limit threshold on the NCP4200 is programmed by a resistor between the I_{LIMFS} pin and the CSCOMP pin. The I_{LIMFS} current, I_{ILIMFS}, is compared with an internal current reference of 20 μA. If I_{ILIMFS} exceeds 20 μA then the output current has exceeded the limit and the current limit protection is tripped.

$$I_{ILIMFS} = \frac{V_{ILIMFS} - V_{CSCOMP}}{R_{ILIMFS}} \quad \text{(eq. 1)}$$

Where $V_{ILIMFS} = V_{CSREF}$

$$I_{ILIMFS} = \frac{V_{CSREF} - V_{CSCOMP}}{R_{ILIMFS}} \quad \text{(eq. 2)}$$

$$V_{CSREF} - V_{CSCOMP} = \frac{R_{CS}}{R_{PH}} \times R_L \times I_{LOAD}$$

Assuming that:

$$\frac{R_{CS}}{R_{PH}} \times R_L = 1\ m\Omega \quad \text{(eq. 3)}$$

i.e. the external circuit is set up for a 1 mΩ load−line then the R_{ILIMFS} is calculated as follows:

$$I_{ILIMFS} = \frac{1\ m\Omega \times I_{LOAD}}{R_{ILIMITFS}} \quad \text{(eq. 4)}$$

Assuming we want a current limit of 150 A that means that I_{LIMFS} must equal 20 μA at that load.

$$20\ \mu A = \frac{1\ m\Omega \times 150\ A}{R_{ILIMITFS}} = 7.5\ k\Omega \quad \text{(eq. 5)}$$

Solving this equation for $R_{LIMITFS}$ we get 7.5 kΩ.

The current limit threshold can be modified from the resistor programmed value by using the PMBus interface using Bits <4:0> of the Current Limit Threshold command (0xE2). The limit is programmable between 50% of the external limit and 146.7% of the external limit. The resolution is 3.3%. Table 3 gives some examples codes.

Table 3. Current Limit

Code	Current Limit (% of External Limit)
0 0000	50%
0 0001	53.3%
1 0000	100% = default
1 0001	103.3%
1 1110	143.3%
1 1111	146.7%

Current Limit, Short−Circuit and Latchoff Protection

If the current limit is reached and TD5 has completed, an internal latchoff delay time will start, and the controller will shut down if the fault is not removed. This delay is four times longer than the delay time during the startup sequence. The current limit delay time only starts after TD5 has completed. If there is a current limit during startup, the NCP4200 will go through TD1 to TD5 and then start the latchoff time. Because the controller continues to cycle the phases during the latchoff delay time, if the short is removed before the timer is complete, the controller can return to normal operation.

The latchoff function can be reset by either removing/reapplying the supply voltage to the NCP4200, or by toggling the EN pin low for a short time.

During startup when the output voltage is below 200 mV, a secondary current limit is active. This is necessary because the voltage swing of CSCOMP cannot go below ground. This secondary current limit limits the internal COMP voltage to the PWM comparators to 1.5 V. This limits the voltage drop across the low−side MOSFETs through the current balance circuitry. Typical overcurrent latchoff waveforms are shown in Figure 9.

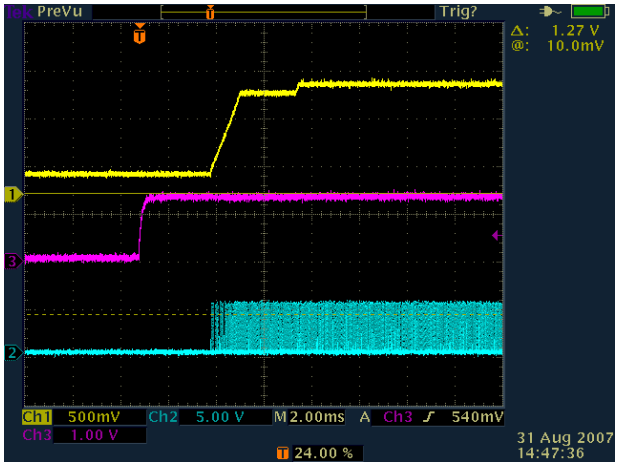


Figure 9. Overcurrent Latchoff Waveforms

An inherent per phase current limit protects individual phases if one or more phases stop functioning because of a faulty component. This limit is based on the maximum normal mode COMP voltage.

Output Current Monitor

I_{MON} is an analog output from the NCP4200 representing the total current being delivered to the load. It outputs an accurate current that is directly proportional to the current set by the I_{LIMFS} resistor.

$$I_{IMON} = 10 \times I_{ILIMFS} \quad \text{(eq. 6)}$$

The current is then run through a parallel RC connected from the I_{MON} pin to the FBRTN pin to generate an accurately scaled and filtered voltage as per the specification. The size of the resistor is used to set the I_{MON} scaling.

The scaling is set such that I_{MON} = 900 mV at the TDC current of the processor. This means that the R_{IMON} resistor should be chosen as follows.

From the Current Limit Set−point paragraph we know the following:

$$I_{ILIMFS} = \frac{1\ m\Omega \times I_{LOAD}}{R_{LIMIFS}} \quad \text{(eq. 7)}$$

$$I_{IMON} = 10 \times \frac{1\ m\Omega \times I_{LOAD}}{R_{LIMFS}}$$

For a 150 A current limit R_{LIMFS} = 7.5 kΩ. Assuming the TDC = 135 A then V_{MON} should equal 900 mV when I_{LOAD} = 135 A.

When I_{LOAD} = 135 A, I_{MON} equals:

$$I_{IMON} = 10 \times \frac{1\ m\Omega \times 135\ A}{7.5\ k\Omega} = 180\ \mu A \quad \text{(eq. 8)}$$

$$V_{IMON} = 900\ mV = 180\ \mu A \times R_{MON}$$

This gives a value of 5 kΩ for R_{MON}.

If the TDC and OCP limit for the processor have to be changed the because the $I_{LIMITFS}$ resistor sets up both the current limit and also the current out of the I_{MON} pin, as explained earlier.

The I_{MON} pin also includes an active clamp to limit the I_{MON} voltage to 1.15 V MAX while maintaining accuracy at 900 mV full scale.

Active Impedance Control Mode

For controlling the dynamic output voltage droop as a function of output current, the CSA gain and load−line programming can be scaled to be equal to the droop impedance of the regulator times the output current. This droop voltage is then used to set the input control voltage to the system. The droop voltage is subtracted from the DAC reference input voltage directly to tell the error amplifier where the output voltage should be. This allows enhanced feed forward response.

Load Line Setting

The load−line is programmable over the PMBus on the NCP4200. It is programmed using the Load−line Calibration (0xDE) and Load−line Set (0xDF) commands. The load−line can be adjusted between 0% and 100% of the external R_{CSA}. In this example R_{CSA} = 1 mΩ R_O needs to 0.8 mΩ therefore programming the Load−line Calibration + Load−line Set register to give a combined percentage of 80% will set the R_O to 0.8 mΩ

Table 4. Load−line Commands

Code	Load−line (as a percentage of R_{CSA})
0 0000	0%
0 0001	3.226%
1 0000	51.6% = default
1 0001	53.3%
1 1110	96.7%
1 1111	100%

Current Control Mode and Thermal Balance

The NCP4200 has individual inputs (SW1 to SW4) for each phase that are used for monitoring the per phase current. This information is combined with an internal ramp to create a current balancing feedback system that has been optimized for initial current balance accuracy and dynamic thermal balancing during operation. This current balance information is independent of the average output current information used for positioning. The magnitude of the internal ramp can be set to optimize the transient response of the system. It also monitors the supply voltage for feed−forward control for changes in the supply. A resistor connected from the power input voltage to the RAMPADJ pin determines the slope of the internal PWM ramp.

The balance between the phases can be programmed using the PMBus Phase Bal SW(x) commands (0xE3 to 0xE6). This allows each phase to be adjusted if there is a difference in temperature due to layout and airflow considerations. The phase balance can be adjusted from a default gain of 5 (Bits 4:0 = 10000). The minimum gain programmable is 3.75 (Bits 4:0 = 00000) and the max gain is 6.25 (Bits 4:0 = 11111).

Voltage Control Mode

A high gain, high bandwidth, voltage mode error amplifier is used for the voltage mode control loop. The control input voltage to the positive input is set via the VID logic according to the voltages listed in Table 10. The VID code is set using the VID Input pins or it can be programmed over the PMBus using the VOUT_Command. By default, the NCP4200 outputs a voltage corresponding to the VID Inputs. To output a voltage following the VOUT_Command the user first needs to program the required VID Code. Then the VID_EN Bits need to be enabled. The following is the sequence:

1. Program the required VID Code to the VOUT_Command code (0x21).
2. Set the VID_EN bit (Bit 3) in the VR Config 1 A (0xD2) and on the VR Config 1B (0xD3).
   This voltage is also offset by the droop voltage for active positioning of the output voltage as a function of current, commonly known as active voltage positioning. The output of the amplifier is the COMP pin, which sets the termination voltage for the internal PWM ramps.
   The negative input (FB) is tied to the output sense location with Resistor R_B and is used for sensing and controlling the output voltage at this point. A current source (equal to IREF) from the FB pin flowing through R_B is used for setting the no load offset voltage from the VID voltage. The no load voltage is negative with respect to the VID DAC for Intel CPU's.

The value of R_B can be found using the following equation:

$$R_B = \frac{V_{VID} - V_{ONL}}{I_{FB}} \quad \text{(eq. 9)}$$

An offset voltage can be added to the control voltage over the serial interface. This is done using Bits <5:0> of the VOUT_TRIM (0xDB) and VOUT_CAL (0xDC) Commands. The max offset that can be applied is ±193.75 mV (even if the sum of the offsets > 193.75 mV). The LSB size is 6.25 mV. A positive offset is applied when Bit 5 = 0. A negative offset is applied when Bit 5 = 1.

Table 5. Offset Codes

VOUT_ TRIM CODE	TRIM OFFSET VOLTAGE	VOUT_ CAL CODE	CAL OFFSET VOLTAGE	TOTAL OFFSET VOLTAGE
00 1000	50 mV	00 0010	12.5 mV	62.5 mV
10 0001	−6.25 mV	10 1110	−87.5 mV	−93.75 mV
00 1111	93.75 mV	10 0001	−6.25 mV	87.5 mV

Dynamic VID

The NCP4200 has the ability to respond to dynamically changing VID inputs while the controller is running. This allows the output voltage to change while the supply is running and supplying current to the load. This is commonly referred to as Dynamic VID (DVID). A DVID can occur under either light or heavy load conditions. The processor signals the controller by changing the VID inputs (or by programming a new VOUT_Command) in a single or multiple steps from the start code to the finish code. This change can be positive or negative.

When a VID bit changes state, the NCP4200 detects the change and ignores the DAC inputs for a minimum of 200 ns. This time prevents a false code due to logic skew while the VID inputs are changing. Additionally, the first VID change initiates the PWRGD and CROWBAR blanking functions for a minimum of 100 μs to prevent a false PWRGD or CROWBAR event. Each VID change resets the internal timer.

If a VID off code is detected the NCP4200 will wait for 5 μsec to ensure that the code is correct before initiating a shutdown of the controller.

The NCP4200 also uses the TON_Transition command code (0xD6) to limit the DVID slew rates. These can be encountered when the system does a large single VID step for power state changes, thus the DVID slew rate needs to be limited to prevent large inrush currents.

The transition slew rate is programmed using Bits <2:0> of the Ton_Transition (0xD6) command code. Table 6 provides the soft−start values.

Table 6. Transition Rate Codes

Code	Transition Rate (V/msec)
000	1
001	3
010	5 = default
011	7
100	9
101	11
110	13
111	15

Enhanced Transients Mode

The NCP4200 incorporates enhanced transient response for both load step up and load release. For load step up it senses the output of the error amp to determine if a load step up has occurred and then sequences on the appropriate number of phases to ramp up the output current.

For load release, it also senses the output of the error amp and uses the load release information to trigger the TRDET pin, which is then used to adjust the error amp feedback for optimal positioning. This is especially important during high frequency load steps.

Additional information is used during load transients to ensure proper sequencing and balancing of phases during high frequency load steps as well as minimizing the stress on components such as the input filter and MOSFETs.

Reference Current

The I_{REF} pin is used to set an internal current reference. This reference current sets I_{FB}. A resistor to ground programs the current based on the 1.8 V output.

$$I_{REF} = \frac{1.8\ V}{R_{IREF}} \quad \text{(eq. 10)}$$

Typically, R_{IREF} is set to 121 kΩ to program I_{REF} = 15 μA.

$$I_{FB} = I_{REF} = 15\ \mu A \quad \text{(eq. 11)}$$

Power Good Monitoring

The power good comparator monitors the output voltage via the CSREF pin. The PWRGD pin is an open−drain output whose high level (when connected to a pullup resistor) indicates that the output voltage is within the nominal limits. The nominal limits specified in the specifications above based on the VID voltage setting. PWRGD goes low if the output voltage is outside of this specified range, if the VID DAC inputs are in no CPU mode, or whenever the EN pin is pulled low. PWRGD is blanked during a DVID event for a period of 100 μs to prevent false signals during the time the output is changing.

The PWRGD circuitry also incorporates an initial turn−on delay time (TD5). Prior to the SS voltage reaching the programmed VID DAC voltage and the PWRGD masking time finishing, the PWRGD pin is held low. Once the SS circuit reaches the programmed DAC voltage, the internal timer operates.

The default range for the PWRGD comparator is +300 mV and −500 mV. However these values can be adjusted over the PMBus. The high limit is programmed using Bits <1:0> of Command Code 0xE0 and the low limit is programmed using Bits <2:0> of Command code 0xE1. The following is a table of the programmable values.

Table 7. PWRGD High Limits

Code	PWRGD High Limits
00	+300mV (default)
01	+250 mV
10	+200 mV
11	+150 mV

Table 8. PWRGD Low Limits

Code	PWRGD Low Limits
000	−500mV (default)
001	−450 mV
010	−400 mV
011	−350 mV
100	−300 mV
101	−250 mV
110	−200 mV
111	−150 mV

Power State Indicator

The $\overline{\text{PSI}}$ pin is an input used to determine the operating state of the load. If this input is pulled low, the load is in a low power state and the controller asserts the $\overline{\text{ODN}}$ pin low, which can be used to disable phases and maintain better efficiency at lighter loads.

The sequencing into and out of low power operation is maintained to minimize output deviations as well as providing full power load transients immediately after exiting a low power state.

The user can program how many phases are enabled when $\overline{\text{PSI}}$ is asserted. By default only phase 1 is enabled. The number of phases enabled can be changed over the PMBus. However extreme care should be taken to ensure that $\overline{\text{OD1}}$ is connected to all phases enabled during $\overline{\text{PSI}}$. The number of phases enabled during $\overline{\text{PSI}}$ is programmed using Bits 6 and 7 of the MFR Config Command (0xD1).

Table 9. # Phases Enabled During $\overline{\text{PSI}}$

Code	PWRGD High Limits
00	1−Phase (default)
01	2−Phases
10	1−Phase
11	1−Phase

The actual phases enabled, depends upon how many phases are enabled for normal operation. For example if 4 phases are enabled normally and 2 during $\overline{\text{PSI}}$, then Phase 1 and Phase 3 will be enabled during $\overline{\text{PSI}}$.

Output Crowbar

As part of the protection for the load and output components of the supply, the PWM outputs are driven low (turning on the low−side MOSFETs) when the output voltage exceeds the upper crowbar threshold. This crowbar action stops once the output voltage falls below the release threshold of approximately 300 mV. The value for the crowbar limit follows the programmable PWRGD high limit.

Turning on the low−side MOSFETs pulls down the output as the reverse current builds up in the inductors. If the output overvoltage is due to a short in the high−side MOSFET, this action current limits the input supply, or blows its fuse protecting the microprocessor from being destroyed.

Output Enable and UVLO

For the NCP4200 to begin switching the input, supply current to the controller must be higher than the UVLO threshold and the EN pin must be higher than its 0.8 V threshold. This initiates a system startup sequence. If either UVLO or EN is less than their respective thresholds, the NCP4200 is disabled. This holds the PWM outputs at ground and forces PWRGD, $\overline{\text{ODN}}$ and $\overline{\text{OD1}}$ signals low.

In the application circuit (see Figure 2), the $\overline{\text{OD1}}$ pin should be connected to the $\overline{\text{OD}}$ inputs of the external drivers for the phases that are always on. The $\overline{\text{ODN}}$ pin should be connected to the $\overline{\text{OD}}$ inputs of the external drivers on the phases that are shut down during low power operation.

Grounding the driver $\overline{\text{OD}}$ inputs disables the drivers such that both DRVH and DRVL are grounded. This feature is important in preventing the discharge of the output capacitors when the controller is shut off. If the driver outputs are not disabled, a negative voltage can be generated during output due to the high current discharge of the output capacitors through the inductors.

Voltage Monitoring

The NCP4200 can monitor the voltage on the EN pin and reports this back in a register. The ADC range for the voltage measurements is 0 V to 2.0 V. Voltages greater than 2.0 V can be monitored using a resistor divider network. Voltage measurements are 10 bits wide.

Shunt Resistor

The NCP4200 uses a shunt to generate 5.0 V from the 12 V supply range. A trade−off can be made between the power dissipated in the shunt resistor and the UVLO threshold.

Figure 10 shows the typical resistor value needed to realize certain UVLO voltages. It also gives the maximum power dissipated in the shunt resistor for these UVLO voltages.

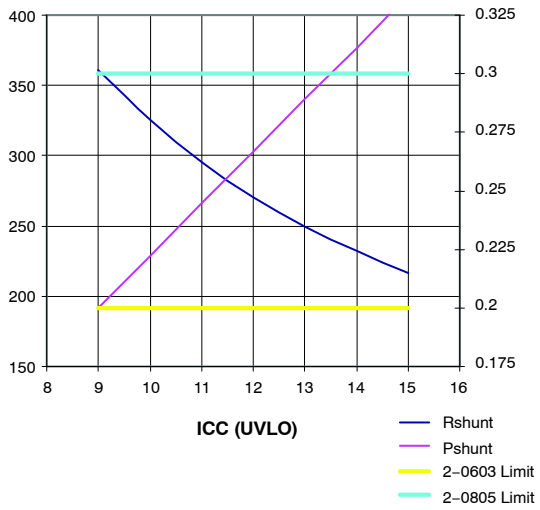


Figure 10. Typical Shunt Resistor Value and Power Dissipation for Different UVLO Voltage

The maximum power dissipated is calculated using Equation:

$$P_{MAX} = \frac{\left(V_{IN(MAX)} - V_{CC(MIN)}\right)^2}{R_{SHUNT}} \quad \text{(eq. 12)}$$

where:

$V_{IN(MAX)}$ is the maximum voltage from the 12 V input supply (if the 12 V input supply is 12 V ±5%, $V_{IN(MAX)}$ = 12.6 V; if the 12 V input supply is 12 V ±10%, $V_{IN(MAX)}$ = 13.2 V).

$V_{CC(MIN)}$ is the minimum V_{CC} voltage of the NCP4200. This is specified as 4.75 V.

R_{SHUNT} is the shunt resistor value.

The CECC standard specification for power rating in surface−mount resistors is: 0603 = 0.1 W, 0805 = 0.125 W, 1206 = 0.25 W.

PMBus Interface

Control of the NCP4200 is carried out using the PMBus Interface. The physical protocol for PMBus closely matches that of SMBus. The NCP4200 is connected to this bus as a slave device, under the control of a master controller.

Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low−to−high transition when the clock is high might be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse; this is known as No Acknowledge. The master takes the data line low during the low period before the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the NCP4200, write operations contain one, two or three bytes, and read operations contain one or two bytes. The command code or register address determines the number of bytes to be read or written, See the Register Map for more information.

To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed (i.e. command code), and then data can be written to that register or read from it. The first byte of a read or write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

This write byte operation is shown in Figure 12. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to be written to, which is stored in the address pointer register. The second data byte is the data to be written to the internal data register.

1. The read byte operation is shown in Figure 13. First the command code needs to be written to the NCP4200 so that the required data is sent back. This is done by performing a write to the NCP4200 as before, but only the data byte containing the register address is sent, because no data is written to the register. A repeated start is then issued and a read operation is then performed consisting of the serial bus address; R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register.
2. It is not possible to read or write a data byte from a data register without first writing to the address pointer register, even if the address pointer register is already at the correct value.
3. In addition to supporting the send byte, the NCP4200 also supports the read byte, write byte, read word and write word protocols. (See System Management Bus Specifications Rev. 2.0 and the PMBus Specification Rev 1.1 Part I and Part II for more information.)

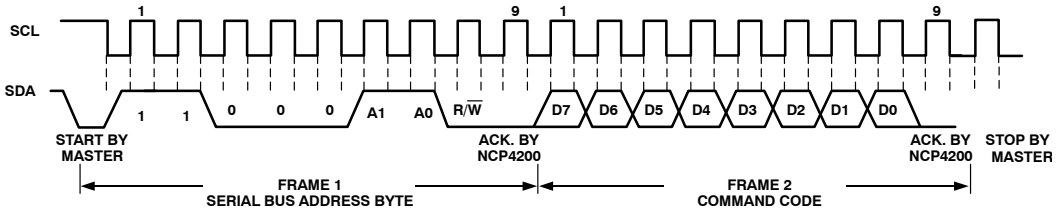


Figure 11. Send Byte

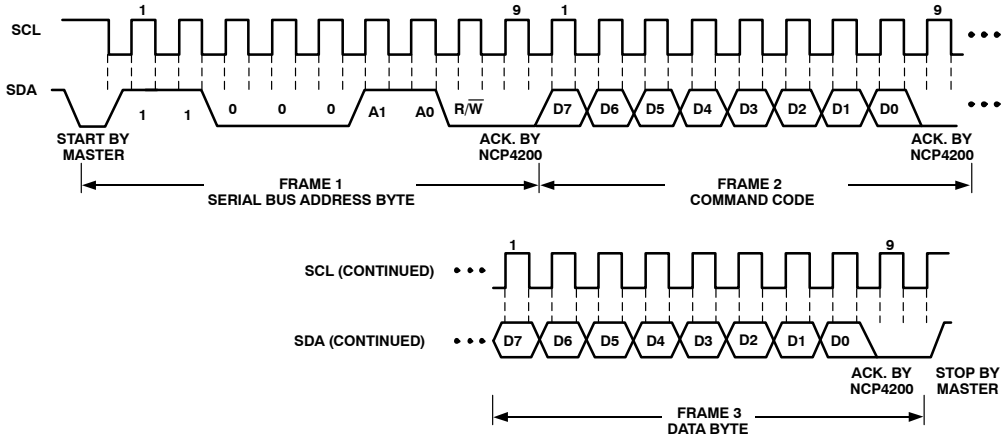


Figure 12. Write Byte

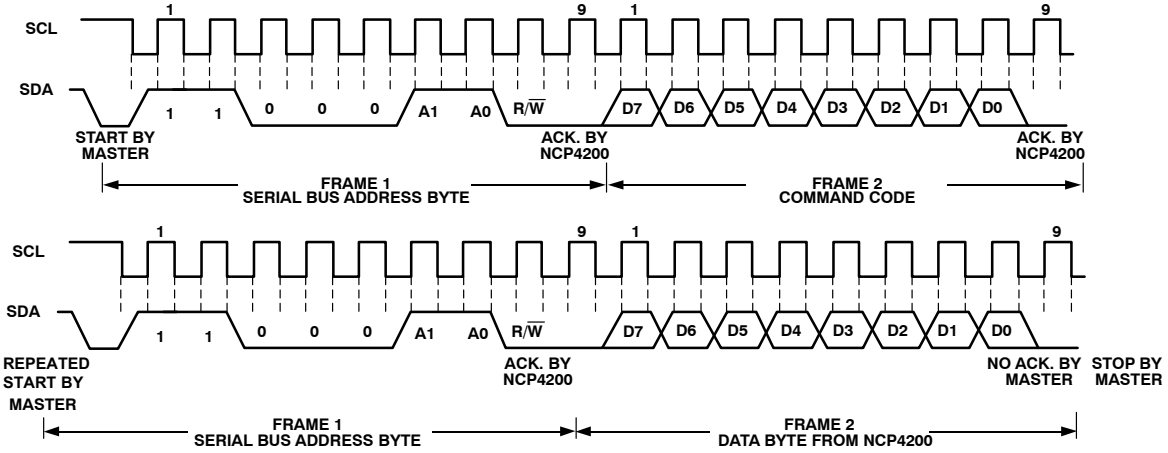


Figure 13. Read Byte

Write Operations

The PMBus specification defines several protocols for different types of read and writes operations. The ones used in the NCP4200 are discussed in this section. The following abbreviations are used in the diagrams:

S—START
P—STOP
R—READ
W—WRITE
A—ACKNOWLEDGE
$\overline{A}$—NO ACKNOWLEDGE

The NCP4200 uses the following PMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

For the NCP4200, the send byte protocol is used to clear faults. This operation is shown in Figure 14.

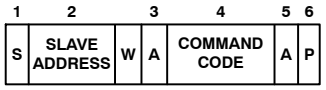


Figure 14. Send Byte Command

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA and the transaction ends.

The byte write operation is shown in Figure 15.

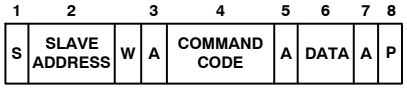


Figure 15. Single Byte Write to a Register

Write Word

In this operation, the master device sends a command byte and two data bytes to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends the first data byte.
7. The slave asserts ACK on SDA.
8. The master sends the second data byte.
9. The slave asserts ACK on SDA.
10. The master asserts a stop condition on SDA and the transaction ends.

The word write operation is shown in Figure 16.

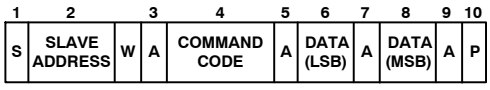


Figure 16. Single Word Write to a Register

Block Write

In this operation, the master device sends a command byte and a byte count followed by the stated number of data bytes to the slave device as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code
5. The slave asserts ACK on SDA
6. The master sends the byte count N
7. The slave asserts ACK on SDA
8. The master sends the first data byte
9. The slave asserts ACK on SDA
10. The master sends the second data byte.
11. The slave asserts ACK on SDA
12. The master sends the remainder of the data byes
13. The slave asserts an ACK on SDA after each data byte.
14. After the last data byte the master asserts a STOP condition on SDA

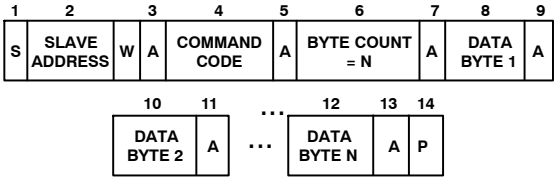


Figure 17. Block Write to a Register

Read Operations

The NCP4200 uses the following PMBus read protocols.

Read Byte

In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserted ACK on SDA.
6. The master sends a repeated start condition on SDA.
7. The master sends the 7 bit slave address followed by the read bit (high).
8. The slave asserts ACK on SDA.
9. The slave sends the Data Byte.
10. The master asserts NO ACK on SDA.
11. The master asserts a stop condition on SDA and the transaction ends.

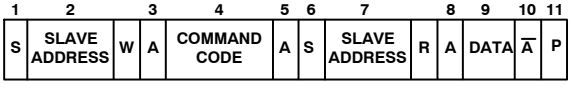


Figure 18. Single Byte Read from a Register

Read Word

In this operation, the master device receives two data bytes from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserted ACK on SDA.
6. The master sends a repeated start condition on SDA.
7. The master sends the 7 bit slave address followed by the read bit (high)
8. The slave asserts ACK on SDA.
9. The slave sends the first Data Byte (low Data Byte).
10. The master asserts ACK on SDA.
11. The slave sends the second Data Byte (high Data Byte).
12. The masters asserts a No ACK on SDA.
13. The master asserts a stop condition on SDA and the transaction ends.

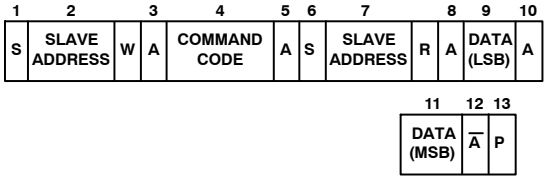


Figure 19. Word Read from a Command Code

Block Read

In this operation, the master device sends a command byte, the slave sends a byte count followed by the stated number of data bytes to the master device as follows:

1. The master device asserts a START condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a REPEATED START condition on SDA.
5. The master sends the 7−bit slave address followed by the read bit (high).
6. The slave asserts ACK on SDA.
7. The slave sends the byte count N.
8. The master asserts ACK on SDA.
9. The slave sends the first data byte.
10. The master asserts ACK on SDA.
11. The slave sends the remainder of the data byes, the master asserts an ACK on SDA after each data byte.
12. After the last data byte the master asserts a No ACK on SDA.
13. The master asserts a STOP condition on SDA.

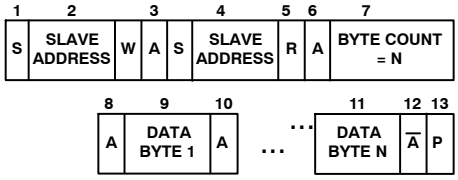


Figure 20. Block Write to a Command Coder

PMBus Timeout

The NCP4200 includes a PMBus timeout feature. If there is no PMBus activity for 35 ms, the NCP4200 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the PMBus expecting data. Some PMBus controllers cannot handle the PMBus timeout feature, so it can be disabled.

Configuration Register 1 (0xD1)

Bit 3 SMB_TO_EN = 1; PMBus timeout enabled.

Bit 3 TODIS = 0; PMBus timeout disabled (default).

Virus Protection

To prevent rogue programs or viruses from accessing critical NCP4200 register settings, the lock bit can be set. Setting Bit 0 of the Lock/Reset sets the lock bit and locks critical registers. In this mode, certain registers can no longer be written to until the NCP4200 is powered down and powered up again. For more information on which registers are locked see the Register Map.

Table 10. VR11.1 and VR11 x VID CODES for the NCP4200

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
OFF	0	0	0	0	0	0	0	0
OFF	0	0	0	0	0	0	0	1
1.60000	0	0	0	0	0	0	1	0
1.59375	0	0	0	0	0	0	1	1
1.58750	0	0	0	0	0	1	0	0
1.58125	0	0	0	0	0	1	0	1
1.57500	0	0	0	0	0	1	1	0
1.56875	0	0	0	0	0	1	1	1
1.56250	0	0	0	0	1	0	0	0

Table 10. VR11.1 and VR11 x VID CODES for the NCP4200

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.55625	0	0	0	0	1	0	0	1
1.55000	0	0	0	0	1	0	1	0
1.54375	0	0	0	0	1	0	1	1
1.53750	0	0	0	0	1	1	0	0
1.53125	0	0	0	0	1	1	0	1
1.52500	0	0	0	0	1	1	1	0
1.51875	0	0	0	0	1	1	1	1
1.51250	0	0	0	1	0	0	0	0
1.50625	0	0	0	1	0	0	0	1
1.50000	0	0	0	1	0	0	1	0
1.49375	0	0	0	1	0	0	1	1
1.48750	0	0	0	1	0	1	0	0
1.48125	0	0	0	1	0	1	0	1
1.47500	0	0	0	1	0	1	1	0
1.46875	0	0	0	1	0	1	1	1
1.46250	0	0	0	1	1	0	0	0
1.45625	0	0	0	1	1	0	0	1
1.45000	0	0	0	1	1	0	1	0
1.44375	0	0	0	1	1	0	1	1
1.43750	0	0	0	1	1	1	0	0
1.43125	0	0	0	1	1	1	0	1
1.42500	0	0	0	1	1	1	1	0
1.41875	0	0	0	1	1	1	1	1
1.41250	0	0	1	0	0	0	0	0
1.40625	0	0	1	0	0	0	0	1
1.40000	0	0	1	0	0	0	1	0
1.39375	0	0	1	0	0	0	1	1
1.38750	0	0	1	0	0	1	0	0
1.38125	0	0	1	0	0	1	0	1
1.37500	0	0	1	0	0	1	1	0
1.36875	0	0	1	0	0	1	1	1
1.36250	0	0	1	0	1	0	0	0
1.35625	0	0	1	0	1	0	0	1
1.35000	0	0	1	0	1	0	1	0
1.34375	0	0	1	0	1	0	1	1
1.33750	0	0	1	0	1	1	0	0
1.33125	0	0	1	0	1	1	0	1
1.32500	0	0	1	0	1	1	1	0
1.31875	0	0	1	0	1	1	1	1
1.31250	0	0	1	1	0	0	0	0
1.30625	0	0	1	1	0	0	0	1
1.30000	0	0	1	1	0	0	1	0
1.29375	0	0	1	1	0	0	1	1

Table 10. VR11.1 and VR11 x VID CODES for the NCP4200

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.28750	0	0	1	1	0	1	0	0
1.28125	0	0	1	1	0	1	0	1
1.27500	0	0	1	1	0	1	1	0
1.26875	0	0	1	1	0	1	1	1
1.26250	0	0	1	1	1	0	0	0
1.25625	0	0	1	1	1	0	0	1
1.25000	0	0	1	1	1	0	1	0
1.24375	0	0	1	1	1	0	1	1
1.23750	0	0	1	1	1	1	0	0
1.23125	0	0	1	1	1	1	0	1
1.22500	0	0	1	1	1	1	1	0
1.21875	0	0	1	1	1	1	1	1
1.21250	0	1	0	0	0	0	0	0
1.20625	0	1	0	0	0	0	0	1
1.20000	0	1	0	0	0	0	1	0
1.19375	0	1	0	0	0	0	1	1
1.18750	0	1	0	0	0	1	0	0
1.18125	0	1	0	0	0	1	0	1
1.17500	0	1	0	0	0	1	1	0
1.16875	0	1	0	0	0	1	1	1
1.16250	0	1	0	0	1	0	0	0
1.15625	0	1	0	0	1	0	0	1
1.15000	0	1	0	0	1	0	1	0
1.14375	0	1	0	0	1	0	1	1
1.13750	0	1	0	0	1	1	0	0
1.13125	0	1	0	0	1	1	0	1
1.12500	0	1	0	0	1	1	1	0
1.11875	0	1	0	0	1	1	1	1
1.11250	0	1	0	1	0	0	0	0
1.10625	0	1	0	1	0	0	0	1
1.10000	0	1	0	1	0	0	1	0
1.09375	0	1	0	1	0	0	1	1
1.08750	0	1	0	1	0	1	0	0
1.08125	0	1	0	1	0	1	0	1
1.07500	0	1	0	1	0	1	1	0
1.06875	0	1	0	1	0	1	1	1
1.06250	0	1	0	1	1	0	0	0
1.05625	0	1	0	1	1	0	0	1
1.05000	0	1	0	1	1	0	1	0
1.04375	0	1	0	1	1	0	1	1
1.03750	0	1	0	1	1	1	0	0
1.03125	0	1	0	1	1	1	0	1
1.02500	0	1	0	1	1	1	1	0

Table 10. VR11.1 and VR11 x VID CODES for the NCP4200

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
1.01875	0	1	0	1	1	1	1	1
1.01250	0	1	1	0	0	0	0	0
1.00625	0	1	1	0	0	0	0	1
1.00000	0	1	1	0	0	0	1	0
0.99375	0	1	1	0	0	0	1	1
0.98750	0	1	1	0	0	1	0	0
0.98125	0	1	1	0	0	1	0	1
0.97500	0	1	1	0	0	1	1	0
0.96875	0	1	1	0	0	1	1	1
0.96250	0	1	1	0	1	0	0	0
0.95625	0	1	1	0	1	0	0	1
0.95000	0	1	1	0	1	0	1	0
0.94375	0	1	1	0	1	0	1	1
0.93750	0	1	1	0	1	1	0	0
0.93125	0	1	1	0	1	1	0	1
0.92500	0	1	1	0	1	1	1	0
0.91875	0	1	1	0	1	1	1	1
0.91250	0	1	1	1	0	0	0	0
0.90625	0	1	1	1	0	0	0	1
0.90000	0	1	1	1	0	0	1	0
0.89375	0	1	1	1	0	0	1	1
0.88750	0	1	1	1	0	1	0	0
0.88125	0	1	1	1	0	1	0	1
0.87500	0	1	1	1	0	1	1	0
0.86875	0	1	1	1	0	1	1	1
0.86250	0	1	1	1	1	0	0	0
0.85625	0	1	1	1	1	0	0	1
0.85000	0	1	1	1	1	0	1	0
0.84375	0	1	1	1	1	0	1	1
0.83750	0	1	1	1	1	1	0	0
0.83125	0	1	1	1	1	1	0	1
0.82500	0	1	1	1	1	1	1	0
0.81875	0	1	1	1	1	1	1	1
0.81250	1	0	0	0	0	0	0	0
0.80625	1	0	0	0	0	0	0	1
0.80000	1	0	0	0	0	0	1	0
0.79375	1	0	0	0	0	0	1	1
0.78750	1	0	0	0	0	1	0	0
0.78125	1	0	0	0	0	1	0	1
0.77500	1	0	0	0	0	1	1	0
0.76875	1	0	0	0	0	1	1	1
0.76250	1	0	0	0	1	0	0	0
0.75625	1	0	0	0	1	0	0	1

Table 10. VR11.1 and VR11 x VID CODES for the NCP4200

OUTPUT	VID7	VID6	VID5	VID4	VID3	VID2	VID1	VID0
0.75000	1	0	0	0	1	0	1	0
0.74375	1	0	0	0	1	0	1	1
0.73750	1	0	0	0	1	1	0	0
0.73125	1	0	0	0	1	1	0	1
0.72500	1	0	0	0	1	1	1	0
0.71875	1	0	0	0	1	1	1	1
0.71250	1	0	0	1	0	0	0	0
0.70625	1	0	0	1	0	0	0	1
0.70000	1	0	0	1	0	0	1	0
0.69375	1	0	0	1	0	0	1	1
0.68750	1	0	0	1	0	1	0	0
0.68125	1	0	0	1	0	1	0	1
0.67500	1	0	0	1	0	1	1	0
0.66875	1	0	0	1	0	1	1	1
0.66250	1	0	0	1	1	0	0	0
0.65625	1	0	0	1	1	0	0	1
0.65000	1	0	0	1	1	0	1	0
0.64375	1	0	0	1	1	0	1	1
0.63750	1	0	0	1	1	1	0	0
0.63125	1	0	0	1	1	1	0	1
0.62500	1	0	0	1	1	1	1	0
0.61875	1	0	0	1	1	1	1	1
0.61250	1	0	1	0	0	0	0	0
0.60625	1	0	1	0	0	0	0	1
0.60000	1	0	1	0	0	0	1	0
0.59375	1	0	1	0	0	0	1	1
0.58750	1	0	1	0	0	1	0	0
0.58125	1	0	1	0	0	1	0	1
0.57500	1	0	1	0	0	1	1	0
0.56875	1	0	1	0	0	1	1	1
0.56250	1	0	1	0	1	0	0	0
0.55625	1	0	1	0	1	0	0	1
0.55000	1	0	1	0	1	0	1	0
0.54375	1	0	1	0	1	0	1	1
0.53750	1	0	1	0	1	1	0	0
0.53125	1	0	1	0	1	1	0	1
0.52500	1	0	1	0	1	1	1	0
0.51875	1	0	1	0	1	1	1	1
0.51250	1	0	1	1	0	0	0	0
0.50625	1	0	1	1	0	0	0	1
0.50000	1	0	1	1	0	0	1	0
OFF	1	1	1	1	1	1	1	0
OFF	1	1	1	1	1	1	1	1

Table 11. PMBus Commands for the NCP4200

Cmd Code	R/W	Default	Description	# Bytes	Comment
0x01	R/W	0x80	Operation	1	00xx xxxx – Immediate Off 01xx xxxx – Soft Off 1000 xxxx – On (slew rate set by soft–start) – Default 1001 10xx – Margin Low (Act on Fault) 1010 10xx – Margin High (Act on Fault)
0x02	R/W	0x17	ON_OFF_Config	1	Configures how the controller is turned on and off.

Bit	Default	Comment
7:5	000	Reserved for Future Use
4	1	This bit is read only. Switching starts when commanded by the Control Pin and the Operation Command, as set in Bits 3:0.
3	0	0: Unit ignores OPERATION commands over the PMBus 1: Unit responds to OPERATION command, powerup may also depend upon Control input, as described in Bit 2
2	1	0: Unit ignores EN pin 1: Unit responds EN pin, powerup may also depend upon the Operation Register, as described for Bit 3
1	1	Control Pin polarity 0 = Active Low 1 = Active High
0	1	This bit is read only. 1: means that when the controller is disabled it will either immediately turn off or soft off (as set in the Operation Command)

0x03	W	NA	Clear_Faults	0	Writing any value to this command code will clear all Status Bits immediately. The SMBus $\overline{\text{ALERT}}$ is deasserted on this command. If the fault is still present the fault bit shall immediately be asserted again.
0x10	R/W	0x00	Write Protect	1	The Write_Protect command is used to control writing to the PMBus device. There is also a lock bit in the Manufacture Specific Registers that once set will disable writes to all commands until the power to the NCP4200 is cycled.

Data Byte	Comment
1000 0000	Disables all writes except to the Write_Protect Command
0100 0000	Disables all writes except to the Write_Protect and Operation Commands
0010 0000	Disables all writes except to the Write_Protect, Operation, ON_OFF_Config and VOUT_COMMAND Commands
0000 0000	Enables writes to all commands
0001 0000	Disables all writes except to WRITE_PROTECT, PAGE and all MFR–SPECIFIC Commands

0x19	R	0xB0	Capability	1	This command allows the host to get some information on the PMBus device.

Bit	Default	Comment
7	1	PEC (Packet Error Checking is supported)
6:5	01	Max supported bus speed is 400 kHz
4	1	NCP4200 has an SMBus $\overline{\text{ALERT}}$ pin and ARA is supported
3:0	000	Reserved for future use

0x20	R	0x20	VOUT_MODE	1	The NCP4200 supports VID mode for programming the output voltage.
0x21	R/W	0x00	VOUT_COMMAND	2	Sets the output voltage using VID.
0x25	R/W	0x0020	VOUT_MARGIN_HIGH	2	Sets the output voltage when operation command is set to Margin High. Programmed in VID Mode.

Cmd Code	R/W	Default	Description	# Bytes	Comment
0x26	R/W	0x00B2	VOUT_MARGIN_LOW	2	Sets the output voltage when operation command is set to Margin Low. Programmed in VID Mode.
0x38	R/W	0x0001	IOUT_CAL_GAIN	2	Sets the ratio of voltage sensed to current output. Scale is Linear and is expressed in 1/Ω
0x39	R/W	0x0000	IOUT_CAL_OFFSET	2	This offset is used to null out any offsets in the output current sensing circuitry. Units are Amps
0x4A	R/W	0x0064	IOUT_OC_WARN_LIMIT	2	This sets the high current limit. Once this limit is exceeded IOUT_OC_WARN_LIMIT bit is set in the Status_IOUT register and an $\overline{\text{ALERT}}$ is generated. This limit is set in Amps.
0x68	R/W	0x012C	POUT_OP_FAULT_LIMIT	2	This sets the output power over power fault limit. Once exceeded Bit 1 of the Status I_{OUT} Command gets set and the $\overline{\text{FAULT}}$ output gets asserted (if not masked).
0x6A	R/W	0x012C	POUT_OP_WARN LIMIT	2	This sets the output power over power warn limit. Once exceeded Bit 0 of the Status I_{OUT} Command gets set and the $\overline{\text{ALERT}}$ output gets asserted (if not masked)
0x78	R	0x00	STATUS BYTE	1	**Bit** / **Name** / **Description**
					7 / BUSY / A fault was declared because the NCP4200 was busy and unable to respond.
					6 / OFF / This bit is set whenever the NCP4200 is not switching.
					5 / VOUT_OV / This bit gets set whenever the NCP4200 goes into OVP mode.
					4 / IOUT_OC / This bit gets set whenever the NCP4200 latches off due to an overcurrent event.
					3 / Res /
					2 / Res /
					1 / CML / A Communications, memory or logic fault has occurred.
					0 / None of the Above / A fault has occurred which is not one of the above.
0x79	R	0x0000	STATUS WORD	2	**Byte** / **Bit** / **Name** / **Description**
					Low / 7 / Res /
					Low / 6 / OFF / This bit is set whenever the NCP4200 is not switching.
					Low / 5 / VOUT_OV / This bit gets set whenever the NCP4200 goes into OVP mode.
					Low / 4 / IOUT_OC / This bit gets set whenever the NCP4200 latches off due to an overcurrent event.
					Low / 3 / Res /
					Low / 2 / Res /
					Low / 1 / CML / A Communications, memory or logic fault has occurred.
					High / 0 / None of the Above / A fault has occurred which is not one of the above.
					High / 7 / V_{OUT} / This bit gets set whenever the measured output voltage goes outside its power good limits or an OVP event has taken place, i.e. any bit in Status V_{OUT} is set.
					High / 6 / I_{OUT}/P_{OUT} / This bit gets set whenever the measured output current or power exceeds its warning limit or goes into OCP. i.e. any bit in Status I_{OUT} is set.
					High / 5 / Res /
					High / 4 / MFR / A manufacturer specific warning or fault has occurred.

Cmd Code	R/W	Default	Description	# Bytes	Comment			
					High	3	$\overline{\text{POWER_GOOD}}$	The Power−Good signal is deasserted. Same as Power−Good in General Status.
					High	2	Res	
					High	1	OTHER	A Status bit in Status Other is asserted.
					High	0	Res	
0x7A	R	0x00	STATUS VOUT	1	**Bit**	**Name**	**Description**	
					7	VOUT_OVER VOLTAGE FAULT	This bit gets set whenever OVP event takes place.	
					6	VOUT_OVER VOLTAGE WARNING	This bit gets set whenever the measured output voltage goes above its power−good limit.	
					5	VOUT_UNDER VOLTAGE WARNING	This bit gets set whenever the measured output voltage goes below its power−good limit.	
					4	VOUT_UNDER VOLTAGE FAULT	Not applicable.	
					3	Res		
					2	Res		
					1	Res		
					0	Res		
0x7B	R	0x00	STATUS IOUT	1	**Bit**	**Name**	**Description**	
					7	I_{OUT} Overcurrent Fault	This bit gets set if the NCP4200 latches off due to an OCP Event.	
					6	Res		
					5	I_{OUT} Overcurrent Warning	This bit gets set if I_{OUT} exceeds its programmed high warning limit.	
					4	Res		
					3	Res		
					2	Res		
					1	P_{OUT} Over Power Warning	This bit gets set if the measured P_{OUT} exceeds the $\overline{\text{FAULT}}$ Limit.	
					0	P_{OUT} Over Power Warning Fault	This bit gets set if the measured P_{OUT} exceeds the Warn Limit.	
0x7E	R	0x00	STATUS CML	1	**Bit**	**Desc**	**Name**	
					7	Supported	Invalid or Unsupported Command Received.	
					6	Supported	Invalid or Unsupported Data Received.	
					5	Supported	PEC Failed.	
					4	Not supported	Memory Fault Detected.	
					3	Not supported	Processor Fault Detected.	
					2	Not supported		
					1	Supported	A communication fault other than the ones listed has occurred.	
					0	Not supported	Other memory or Logic Fault has occurred.	

Cmd Code	R/W	Default	Description	# Bytes	Comment		
0x80	R	0x00	STATUS_ALERT	1	**Bit**	**Name**	**Description**
					7	Res	
					6	Res	
					5	Res	
					4	Res	
					3	Res	
					2	V_{MON} WARN	Gets asserted when V_{MON} exceeds it programmed WARN limits.
					1	V_{MON} $\overline{FAULT}$	Gets asserted when V_{MON} exceeds it programmed $\overline{FAULT}$ limits.
					0	Res	
0x88	R	0x00		2			
0x8B	R	0x00	READ_VOUT	2	Read−back output voltage. Voltage is read back in VID Mode.		
0x8C	R	0x00	READ_IOUT	2	Read−back output current. Current is read back in Linear Mode (Amps).		
0x8D	R	0x00		2			
0x96	R	0x00	READ_POUT	2	Read−back Output Power, read back in Linear Mode in W's.		
0x99	R	0x4101	MFR_ID	1	0x4101		
0x9A	R	0x0002	MFR_MODEL	2	0x0002		
0x9B	R	0x0301	MFR_REVISION	1	0x0301		

Table 12. Manufacturer Specific Command Codes for the NCP4200

Cmd Code	R/W	Default	Description	# Bytes	Comment		
0xDO	R/W	0x00	Lock/Reset	1	**Bit**	**Name**	**Description**
					1	Reset	Resets all registers to their POR Value. Has no effect if Lock bit is set.
					0	Lock	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read−only and cannot be modified until the NCP4200 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. (Lockable).
0xD1	R/W	0x07	Mfr Config	1	**Bit**	**Name**	**Description**
					7:6	$\overline{PSI}$	These bits sets the number of phases turned on during $\overline{PSI}$. 00 = CL set for 1 Phase (default) 01 = CL set for 2 Phases 10 = CL set for 1 Phase 11 = CL set for 1 Phase
					5	Res	
					4	Res	
					3	PMB_TO_EN	PMBus Timeout Enable. When the PMB_TO_EN bit is set to 1, the PMBus Timeout feature is enabled. In this state if, at any point during an PMBus transaction involving the NCP4200, activity ceases for more than 35 ms, the NCP4200 assumes the bus is locked and releases the bus. This allows the NCP4200 to be used with SMBus controllers that cannot handle SMBus timeouts. (Lockable).
					2	$\overline{FAULT}$_EN	Enable the $\overline{FAULT}$ pin, Default = 1.
					1	$\overline{ALERT}$_EN	Enable the $\overline{ALERT}$ pin.
					0	ENABLE_ $\overline{MONITOR}$	When the ENABLE_MONITOR bit is set to 1, the NCP4200 starts conversions with the ADC and monitors the voltages.

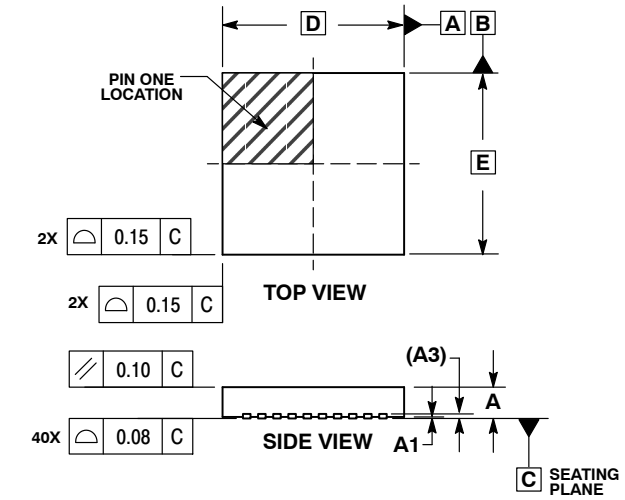
Cmd Code	R/W	Default	Description	# Bytes	Comment		
0xD2	R/W	0x52	VR Config. 1A	1	**Bit**	**Name**	**Description**
					6:4	Phase Enable Bits	000 = Phase 1 100 = Phase 2 010 = Phase 3 110 = Phase 4
					3	VID_EN	When the VID_EN bit is set to 1, the VID code in the VOUT_COMMAND register sets the output voltage. When VID_EN is set to 0, the output voltage follows the VID input pins.
					2	LOOP_EN	When the LOOP_EN bit is set to 1 in both registers, the control loop test function is enabled. This allows measurement of the control loop AC gain and phase response with appropriate instrumentation. The control loop signal insertion pin is I_{MON}. The control loop output pin is COMP.
					1	CLIM_EN	When CLIM_EN is set to 1, the current limit time out latchoff functions normally. When this bit is set to 0 in both registers, the current limit latchoff is disabled. In this state, the part can be in current limit indefinitely.
					0	Res	
0xD3	R/W	0x52	VR Config. 1B	1	This register is for security reasons. It has the same format as register 0xD2. Bits need to be set in both registers for the function to take effect.		
0xD4	R/W	0x03	Ton Delay	1	This resister sets TD1, TD3 and TD5 delays for the soft−start sequence. The current limit latchoff timer is 4 times the programmed delay time: 000 = 0.5 ms 001 = 1 ms 010 = 1.5 ms 011 = 2 ms = default 100 = 2.5 ms 101 = 3 ms 110 = 3.5 ms 111 = 4 ms		
0xD5	R/W	0x02	Ton Rise	1	This register sets the soft−start voltage slew rate, and hence TD2 and TD4, of the soft−start sequence: 000 = 0.1 V/ms 001 = 0.3 V/ms 010 = 0.5 V/ms = default 011 = 0.7 V/ms 100 = 0.9 V/ms 101 = 1.1 V/ms 110 = 1.3 V/ms 111 = 1.5 V/ms		
0xD6	R/W	0x01	Ton Transition	1	This register sets the slew rate during dynamic VID.		
0xD8	R	0x00	EN/VTT Voltage	2	This is a 16 bit value that reports back the voltage on the VTT Pin. Voltage is reported using Linear Mode.		
0xDA	R	0x00	VMON Voltage	1	This is a 16 bit value that reports back the voltage measured between FB and FBRTN. Voltage is reported using Linear Mode.		
0xDB	R/W	0x00	VOUT_TRIM	1	Offset Command Code for V_{OUT}, max ±200 mV.		
0xDC	R/W	0x00	VOUT_CAL	1	Offset Command Code for V_{OUT}, max ±200 mV.		
0xDE	R/W	0x10	Load−line Calibration	1	This value sets the internal load−line attenuation DAC calibration value. The maximum load−line is controlled externally by setting the gain of the current sense amplifier as explained in the applications section. This maximum load−line can then be adjusted from 100% to 0% in 30 steps. Each LSB represents a 3.226% change in the load−line. 00000 = No load−line 10000 = 51.6% of external load−line 11111 = 100% of external load−line		

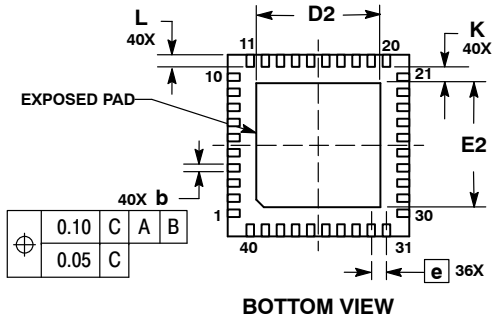
Cmd Code	R/W	Default	Description	# Bytes	Comment
0xDF	R/W	0x00	Load−line Set	1	This value sets the internal load−line attenuation DAC value. The maximum load−line is controlled externally by setting the gain of the current sense amplifier as explained in the applications section. This maximum load−line can then be adjusted from 100% to 0% in 30 steps. Each LSB represents a 3.226% change in the load−line. 00000 = No load−line 10000 = 51.613% of external load−line 11111 = 100% of external load−line
0xE0	R/W	0x00	PWRGD Hi Threshold	1	This value sets the PWRGD Hi Threshold and the CROWBAR Threshold: Code = 00, PWRGD HI = 300 mV (default) Code = 01, PWRGD HI = 250 mV Code = 10, PWRGD HI = 200 mV Code = 11, PWRGD HI = 150 mV
0xE1	R/W	0x00	PWRGD Lo Threshold	1	This value sets the PWRGD Lo Threshold: Code = 000, PWRGD Lo = −500 mV (default) Code = 001, PWRGD Lo = −450 mV Code = 010, PWRGD Lo = −400 mV Code = 011, PWRGD Lo = −350 mV Code = 100, PWRGD Lo = −300 mV Code = 101, PWRGD Lo = −250 mV Code = 110, PWRGD Lo = −200 mV Code = 111, PWRGD Lo = −150 mV
0xE2	R/W	0x10	Current Limit Threshold	1	This value sets the internal current limit adjustment value. The default current limit is programmed using a resistor to ground on the LIMIT pin. The value of this register adjusts this value by a percentage between 50% and 146.7%. Each LSB represents a 3.33% change in the current limit threshold. 11111 = 146.7% of external current limit 10000 = 100% of external current limit (default) 00000 = 50% of external current limit
0xE3	R/W	0x10	Phase Bal SW1	1	These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by ±25% from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25
0xE4	R/W	0x10	Phase Bal SW2	1	These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by ±25% from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25
0xE5	R/W	0x10	Phase Bal SW3	1	These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by ±25% from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25
0xE6	R/W	0x10	Phase Bal SW4	1	These values adjust the gain of the internal phase balance amplifiers. The nominal gain is set to 5. These registers can adjust the gain by ±25% from 3.75 to 6.25. Code = 00000, Gain of 3.75 Code = 10000, Gain of 5 (default) Code = 11111, Gain of 6.25
0xF5	R/W	0x0002	V_{MON} $\overline{FAULT}$ Limit	2	V_{MON} $\overline{FAULT}$ Limit
0xF6	R/W	0x0002	V_{MON} Warn Limit	2	V_{MON} Warn Limit
0xF9	R/W	0x00	Mask $\overline{ALERT}$	1	**Bit** / **Name** / **Description** 7 / Mask V_{OUT} / Masks any $\overline{ALERT}$ caused by bits in Status V_{OUT} Register. 6 / Mask I_{OUT} / Masks any $\overline{ALERT}$ caused by bits in Status I_{OUT} Register. 5 / Res / 4 / Res /

Cmd Code	R/W	Default	Description	# Bytes	Comment		
					3	Mask CML	Masks any $\overline{\text{ALERT}}$ caused by bits in Status CML Register.
					2	V_{MON}	Masks any $\overline{\text{ALERT}}$ caused by V_{MON} exceeding its high or low limit.
					1	Res	
					0	Mask P_{OUT}	Masks any $\overline{\text{ALERT}}$ caused by P_{OUT} exceeding its programmed limit.
0xFA	R/W	0x00	Mask $\overline{\text{FAULT}}$	1	**Bit**	**Name**	**Description**
					7	Mask V_{OUT}	Masks any $\overline{\text{FAULT}}$ caused by bits in Status V_{OUT} Register.
					6	Mask I_{OUT}	Masks any $\overline{\text{FAULT}}$ caused by bits in Status I_{OUT} Register.
					5	Res	
					4	Res	
					3	Mask CML	Masks any $\overline{\text{FAULT}}$ caused by bits in Status CML Register.
					2	V_{MON}	Masks any $\overline{\text{ALERT}}$ caused by V_{MON} exceeding its high or low limit.
					1	Res	
					0	Mask P_{OUT}	Masks any $\overline{\text{FAULT}}$ caused by P_{OUT} exceeding its programmed limit.
0xFB	R	0x00	General Status	1	**Bit**	**Name**	**Description**
					7	$\overline{\text{FAULT}}$	
					6	$\overline{\text{ALERT}}$	
					5	$\overline{\text{POWER_GOOD}}$	Replaced by Bit 3 of the Status Word Command
					4	RDY	
0xFC	R	0x00	Phase Status	1	**Bit**	**Name**	**Description**
					5	Phase 4	This bit is set to 1 when Phase 4 is enabled.
					4	Phase 3	This bit is set to 1 when Phase 3 is enabled.
					3	Phase 2	This bit is set to 1 when Phase 2 is enabled.
					2	$\overline{\text{PSI}}$	This bit is set to 1 when $\overline{\text{PSI}}$ is asserted.

PACKAGE DIMENSIONS

QFN40 6x6, 0.5P
CASE 488AR−01
ISSUE A

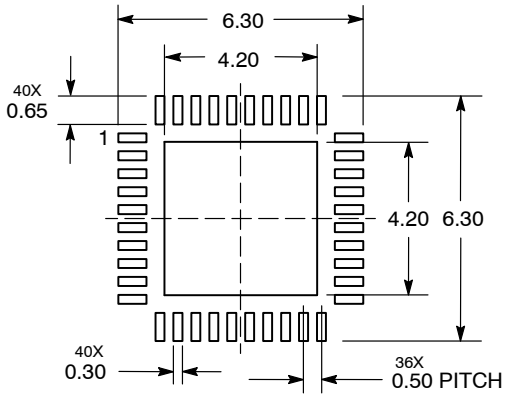




NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

	MILLIMETERS	
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	4.00	4.20
E	6.00 BSC	
E2	4.00	4.20
e	0.50 BSC	
L	0.30	0.50
K	0.20	−−−

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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