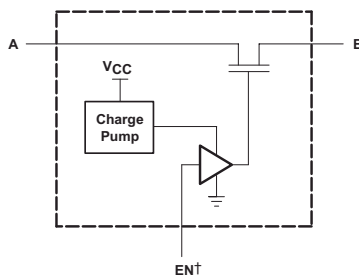


SN74CB3Q16211 24 位开关、2.5V/3.3V 低压 FET 总线开关

1 特性

- 德州仪器 (TI)
Widebus® 系列产品
- 高带宽数据路径 (高达 500MHz⁽¹⁾)
- 可耐受 5V 电压并支持器件上电或断电的 I/O
- 在运行范围内具有平缓的低通态电阻 (r_{on}) 特性 (r_{on} 典型值 = 5 Ω)
- 支持在数据 I/O 端口进行轨到轨开关
 - 3.3V V_{CC} 时, 开关范围为 0V 至 5V
 - 2.5V V_{CC} 时, 开关范围为 0V 至 3.3V
- 具有接近零传播延迟的双向数据流
- 低输入和输出电容可更大程度减小负载和信号失真 ($C_{io(OFF)}$ 典型值 = 4pF)
- 快速开关频率 (f_{OE} 最大值 = 20MHz)
- 数据与控制输入提供下冲钳位二极管
- 低功耗 (I_{CC} 典型值 = 1mA)
- V_{CC} 工作范围为 2.3V 至 3.6V
- 数据 I/O 支持 0V 至 5V 信号电平 (0.8V、1.2V、1.5V、1.8V、2.5V、3.3V、5V)
- 控制输入可由 TTL 或 5V/3.3V CMOS 输出驱动
- I_{off} 支持局部断电模式运行
- 闩锁性能超过 100mA, 符合 JESD 78 II 类规范
- ESD 性能测试符合 JESD 22 标准
 - 2000V 人体放电模型 (A114-B, II 类)
 - 1000V 充电器件模型 (C101)
- 支持数字和模拟应用: PCI 接口、差分信号接口、内存交错、总线隔离、低失真信号门控¹



† EN 是应用于开关的内部使能信号。

每个 FET 开关 (SW) 的简化版原理图

2 应用

- AV 接收器
- 蓝光录像机和播放器
- 嵌入式 PC
- 便携式音频接口盒
- DLP 正投系统

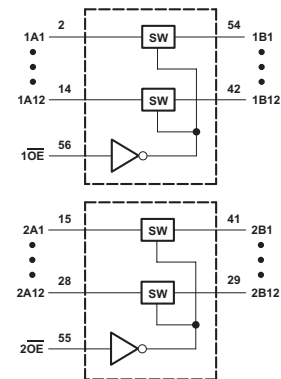
3 说明

SN74CB3Q16211 器件是一款高带宽 FET 总线开关, 此开关利用一个电荷泵来提升传输晶体管的栅极电压, 从而提供一个平缓的低通态电阻 (r_{on})。平缓的低通态电阻可实现超小的传播延迟, 并且支持在数据输入/输出 (I/O) 端口上进行轨到轨开关。该器件还具有低的数据 I/O 电容, 以更大限度地减少数据总线上的容性负载和信号失真。SN74CB3Q16211 器件专为支持高带宽应用而设计, 提供优化的接口解决方案, 非常适合宽带通信、网络和数据密集型计算系统。

器件信息⁽¹⁾

器件型号	封装	封装尺寸
SN74CB3Q16211	TSSOP (56)	14.00mm × 6.10mm
	TVSOP (56)	11.30mm × 4.40mm
	SSOP (56)	18.40mm × 7.49mm
	BGA MICROSTAR JUNIOR (56)	7.00mm × 4.50mm

(1) 如需了解所有可用封装, 请参阅数据表末尾的可订购产品附录。



所示终端编号适用于 DGG、DGV 和 DL 封装。

逻辑图 (正逻辑)

¹ 有关 CB3Q 系列性能特性的其他信息, 请参阅 TI 应用报告 [CBT-C](#)、[CB3T](#) 和 [CB3Q 信号开关系列](#)。



Table of Contents

1 特性.....	1	7.6 Typical Characteristics.....	6
2 应用.....	1	8 Parameter Measurement Information.....	7
3 说明.....	1	9 Device and Documentation Support.....	8
4 Revision History.....	2	9.1 Documentation Support.....	8
5 说明 (续).....	2	9.2 接收文档更新通知.....	8
6 Pin Configuration and Functions.....	3	9.3 支持资源.....	8
7 Specifications.....	4	9.4 Trademarks.....	8
7.1 Absolute Maximum Ratings.....	4	9.5 Electrostatic Discharge Caution.....	8
7.2 Handling Ratings.....	4	9.6 术语表.....	8
7.3 Recommended Operating Conditions.....	4	10 Mechanical, Packaging, and Orderable Information.....	8
7.4 Electrical Characteristics.....	5		
7.5 Switching Characteristics.....	5		

4 Revision History

注：以前版本的页码可能与当前版本的页码不同

Changes from Revision * (May 2004) to Revision A (July 2022)	Page
• 将文档更新为新的 TI 数据表格式 - 无规格变化.....	1
• 删除了“订购信息”表.....	1
• 添加了“应用”.....	1
• 添加了“器件信息”表.....	1
• 更新了整个文档中的表格、图和交叉参考的编号格式.....	1
• Changed the BGA package from: GQL to: ZQL in the <i>Pin Configuration and Functions</i> section.....	3
• Moved T_{stg} to Handling Ratings table.....	4
• Added Mechanical, Packaging, and Orderable Information section.....	8

5 说明 (续)

SN74CB3Q16211 器件配置为两个具有独立输出使能 (1 $\overline{OE}$ 、2 $\overline{OE}$) 输入的 12 位总线开关。它即可用作 24 个 12 位总线开关，也可用作 1 个 2 位总线开关。当 $\overline{OE}$ 为低电平时，相关 12 位总线开关打开，并且 A 端口被连接至 B 端口，从而实现两个端口之间的双向数据流。当 $\overline{OE}$ 为高电平时，相关 12 位总线开关关闭，并且在 A 与 B 端口之间存在高阻抗状态。

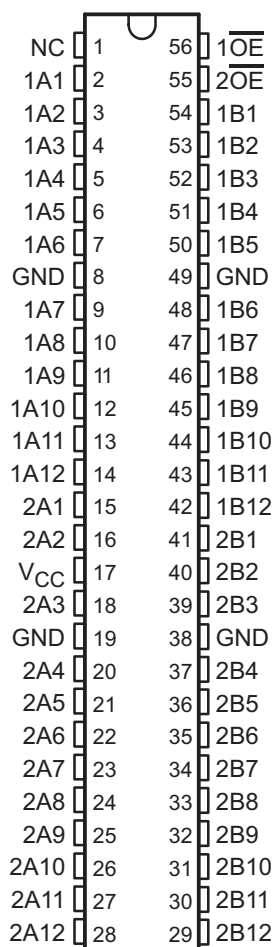
该器件完全符合使用 I_{off} 的部分断电应用的规范要求。 I_{off} 电路可防止在器件断电时电流回流对器件造成损坏。

为了确保加电或断电期间的高阻抗状态， $\overline{OE}$ 应通过一个上拉电阻器被连接至 V_{CC} ；该电阻器的最小值由驱动器的电流灌入能力来决定。

表 5-1. 功能表
(每个 12 位总线开关)

输入 $\overline{OE}$	输入/输出 A	功能
L	B	端口 A = 端口 B
H	Z	断开

6 Pin Configuration and Functions



NC – No internal connection

图 6-1. DGG, DGV, or DL Package, 56-Pin TSSOP and TVSOP (Top View)

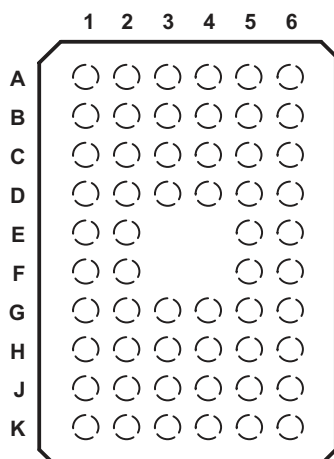


图 6-2. ZQL Package, 56-Pin BGA (Top View)

	1	2	3	4	5	6
A	1A2	1A1	NC	1OE	2OE	1B1
B	1A5	1A4	1A3	1B2	1B3	1B4
C	1A7	GND	1A6	1B5	GND	1B6
D	1A10	1A8	1A9	1B8	1B7	1B9
E	1A12	1A11			1B10	1B11
F	2A1	2A2			2B1	1B12
G	VCC	GND	2A3	2B3	GND	2B2
H	2A4	2A5	2A6	2B6	2B5	2B4
J	2A7	2A8	2A9	2B9	2B8	2B7
K	2A10	2A11	2A12	2B12	2B11	2B10

NC – No internal connection

图 6-3. Functions Table

7 Specifications

7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage range ⁽²⁾	– 0.5	4.6	V
V _{IN}	Control input voltage range ^{(2) (3)}	– 0.5	7	V
V _{I/O}	Switch I/O voltage range ^{(2) (3) (4)}	– 0.5	7	V
I _{IK}	Control input clamp current	V _{IN} < 0		– 50 mA
I _{I/OK}	I/O port clamp current	V _{I/O} < 0		– 50 mA
I _{I/O}	ON-state switch current ⁽⁵⁾			±64 mA
Continuous current through V _{CC} or GND terminals				±100 mA
θ _{JA}	Package thermal impedance ⁽⁶⁾	DGG package		64
		DGV package		48
		DL package		56
		GQL package		42

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to ground unless otherwise specified.
- (3) The input and output voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (4) V_I and V_O are used to denote specific conditions for V_{I/O}.
- (5) I_I and I_O are used to denote specific conditions for I_{I/O}.
- (6) The package thermal impedance is calculated in accordance with JESD 51-7.

7.2 Handling Ratings

PARAMETER	DEFINITION	MIN	MAX	UNIT
T _{stg}	Storage temperature range	– 65	150	°C

7.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)⁽¹⁾

		MIN	MAX	UNIT
V _{CC}	Supply voltage	2.3	3.6	V
V _{IH}	High-level control input voltage	V _{CC} = 2.3 V to 2.7 V	1.7	5.5
		V _{CC} = 2.7 V to 3.6 V	2	5.5
V _{IL}	Low-level control input voltage	V _{CC} = 2.3 V to 2.7 V	0	0.7
		V _{CC} = 2.7 V to 3.6 V	0	0.8
V _{I/O}	Data input/output voltage	0	5.5	V
T _A	Operating free-air temperature	– 40	85	°C

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number [SCBA004](#).

7.4 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS		MIN	TYP ⁽²⁾	MAX	UNIT
V_{IK}		$V_{CC} = 3.6\text{ V}$,	$I_I = -18\text{ mA}$			-1.8	V
I_{IN}	Control inputs	$V_{CC} = 3.6\text{ V}$,	$V_{IN} = 0\text{ to }5.5\text{ V}$			± 1	μA
I_{OZ} ⁽³⁾		$V_{CC} = 3.6\text{ V}$,	$V_O = 0\text{ to }5.5\text{ V}$, $V_I = 0$			± 1	μA
I_{off}		$V_{CC} = 0$,	$V_O = 0\text{ to }5.5\text{ V}$, $V_I = 0$			1	μA
I_{CC}		$V_{CC} = 3.6\text{ V}$,	$I_{I/O} = 0$,		1	3	mA
ΔI_{CC} ⁽⁴⁾	Control inputs	$V_{CC} = 3.6\text{ V}$,	One input at 3 V, Other inputs at V_{CC} or GND			30	μA
I_{CCD} ⁽⁵⁾	Per control input	$V_{CC} = 3.6\text{ V}$,	A and B ports open, Control input switching at 50% duty cycle		0.15	0.25	mA/ MHz
C_{in}	Control inputs	$V_{CC} = 3.3\text{ V}$,	$V_{IN} = 5.5\text{ V}$, 3.3 V, or 0		3.5	5	pF
$C_{io(OFF)}$		$V_{CC} = 3.3\text{ V}$,	$V_{IN} = V_{CC}$ or GND, Switch OFF, $V_{I/O} = 5.5\text{ V}$, 3.3 V, or 0		4	5	pF
$C_{io(ON)}$		$V_{CC} = 3.3\text{ V}$,	$V_{IN} = V_{CC}$ or GND, Switch ON, $V_{I/O} = 5.5\text{ V}$, 3.3 V, or 0		10	12.5	pF
r_{on} ⁽⁶⁾	$V_{CC} = 2.3\text{ V}$, TYP at $V_{CC} = 2.5\text{ V}$	$V_I = 0$,	$I_O = 30\text{ mA}$		5	8	Ω
		$V_I = 1.7\text{ V}$,	$I_O = -15\text{ mA}$		5	9	
	$V_{CC} = 3\text{ V}$	$V_I = 0$,	$I_O = 30\text{ mA}$		5	6.5	
		$V_I = 2.4\text{ V}$,	$I_O = -15\text{ mA}$		5	8	

- (1) V_{IN} and I_{IN} refer to control inputs. V_I , V_O , I_I , and I_O refer to data pins.
- (2) All typical values are at $V_{CC} = 3.3\text{ V}$ (unless otherwise noted), $T_A = 25^\circ\text{C}$.
- (3) For I/O ports, the parameter I_{OZ} includes the input leakage current.
- (4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.
- (5) This parameter specifies the dynamic power-supply current associated with the operating frequency of a single control input (see [Figure 7-2](#)).
- (6) Measured by the voltage drop between the A and B terminals at the indicated current through the switch. ON-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

7.5 Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 8-1](#))

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			MIN	MAX	MIN	MAX	
f_{OE} ⁽¹⁾	$\overline{OE}$	A or B		10		20	MHz
t_{pd} ⁽²⁾	A or B	B or A		0.15		0.25	ns
t_{en}	$\overline{OE}$	A or B	1.5	8	1.5	8	ns
t_{dis}	$\overline{OE}$	A or B	1	7.5	1	7.5	ns

- (1) Maximum switching frequency for control input ($V_O > V_{CC}$, $V_I = 5\text{ V}$, $R_L \geq 1\text{ M}\Omega$, $C_L = 0$).
- (2) The propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).

7.6 Typical Characteristics

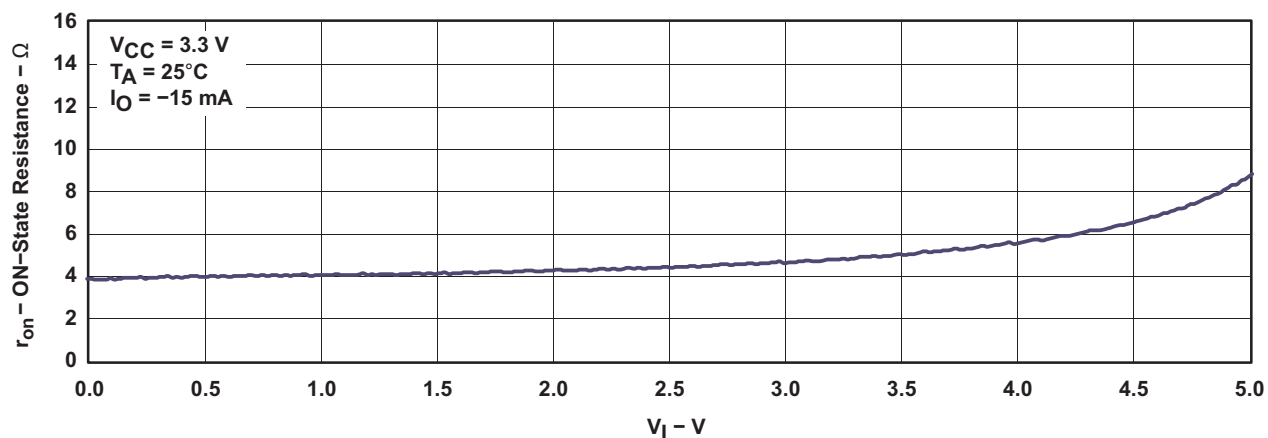


图 7-1. Typical r_{on} vs V_I

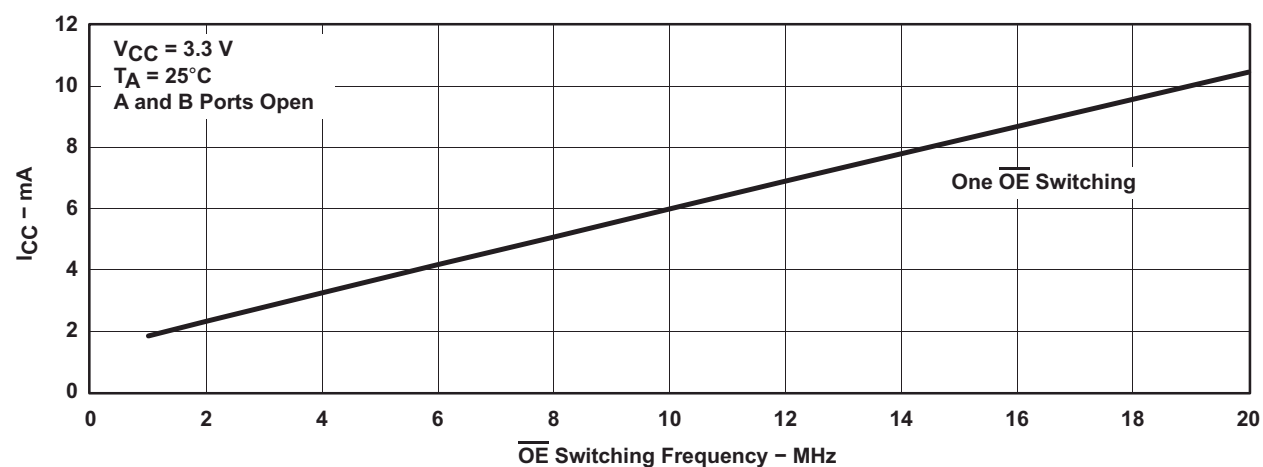
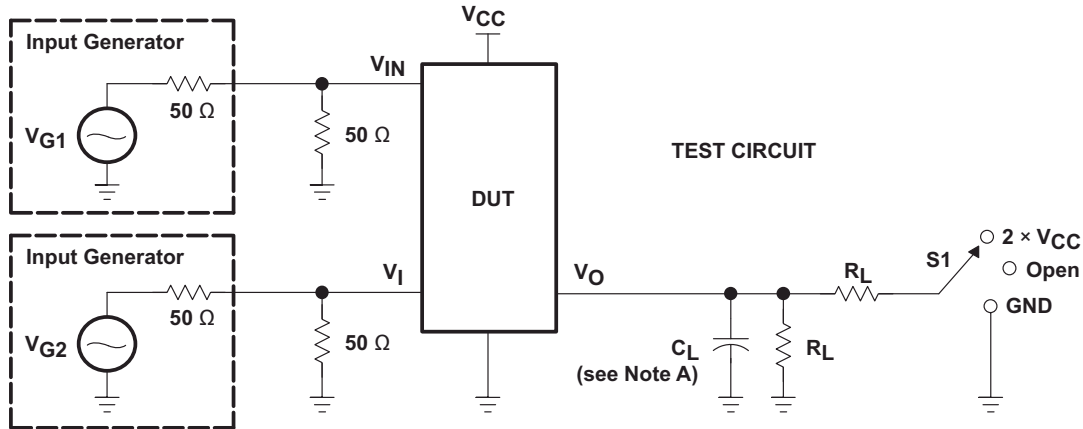
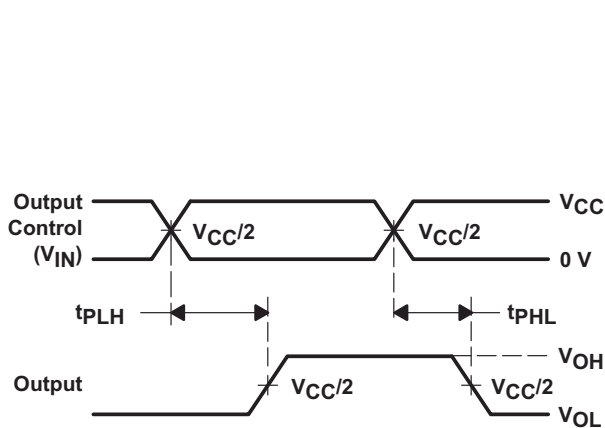


图 7-2. Typical I_{CC} vs $\overline{OE}$ Switching Frequency

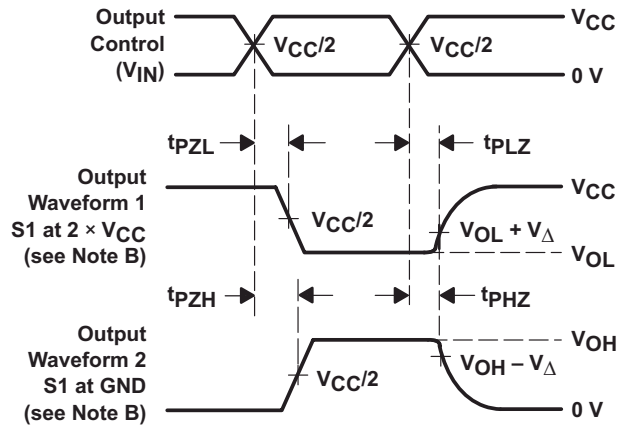
8 Parameter Measurement Information



TEST	V _{CC}	S1	R _L	V _I	C _L	V _Δ
t _{pd} (s)	2.5 V ± 0.2 V	Open	500 Ω	V _{CC} or GND	30 pF	
	3.3 V ± 0.3 V	Open	500 Ω	V _{CC} or GND	50 pF	
t _{PLZ} /t _{PZL}	2.5 V ± 0.2 V	2 × V _{CC}	500 Ω	GND	30 pF	0.15 V
	3.3 V ± 0.3 V	2 × V _{CC}	500 Ω	GND	50 pF	0.3 V
t _{PHZ} /t _{PZH}	2.5 V ± 0.2 V	GND	500 Ω	V _{CC}	30 pF	0.15 V
	3.3 V ± 0.3 V	GND	500 Ω	V _{CC}	50 pF	0.3 V



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES (t_{pd}(s))



VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: PRR ≤ 10 MHz, Z_O = 50 Ω, t_r ≤ 2.5 ns, t_f ≤ 2.5 ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis}.
 - t_{PZL} and t_{PZH} are the same as t_{en}.
 - t_{PLH} and t_{PHL} are the same as t_{pd}(s). The t_{pd} propagation delay is the calculated RC time constant of the typical ON-state resistance of the switch and the specified load capacitance, when driven by an ideal voltage source (zero output impedance).
 - All parameters and waveforms are not applicable to all devices.

图 8-1. Test Circuit and Voltage Waveforms

9 Device and Documentation Support

9.1 Documentation Support

9.1.1 Related Documentation

For related documentation, see the following:

- Texas Instruments, [CBT-C, CB3T, and CB3Q Signal-Switch Families application report](#)

9.2 接收文档更新通知

要接收文档更新通知，请导航至 [ti.com](#) 上的器件产品文件夹。点击 [订阅更新](#) 进行注册，即可每周接收产品信息更改摘要。有关更改的详细信息，请查看任何已修订文档中包含的修订历史记录。

9.3 支持资源

[TI E2E™ 支持论坛](#) 是工程师的重要参考资料，可直接从专家获得快速、经过验证的解答和设计帮助。搜索现有解答或提出自己的问题可获得所需的快速设计帮助。

链接的内容由各个贡献者“按原样”提供。这些内容并不构成 TI 技术规范，并且不一定反映 TI 的观点；请参阅 TI 的《使用条款》。

9.4 Trademarks

TI E2E™ is a trademark of Texas Instruments.

Widebus® is a registered trademark of Texas Instruments.

所有商标均为其各自所有者的财产。

9.5 Electrostatic Discharge Caution



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

9.6 术语表

[TI 术语表](#) 本术语表列出并解释了术语、首字母缩略词和定义。

10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical packaging and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser based versions of this data sheet, refer to the left hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74CB3Q16211DGGR	ACTIVE	TSSOP	DGG	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3Q16211	Samples
SN74CB3Q16211DGVR	ACTIVE	TVSOP	DGV	56	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	BW211	Samples
SN74CB3Q16211DL	ACTIVE	SSOP	DL	56	20	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3Q16211	Samples
SN74CB3Q16211DLR	ACTIVE	SSOP	DL	56	1000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	CB3Q16211	Samples

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSELETE: TI has discontinued the production of the device.

⁽²⁾ **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

⁽³⁾ MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

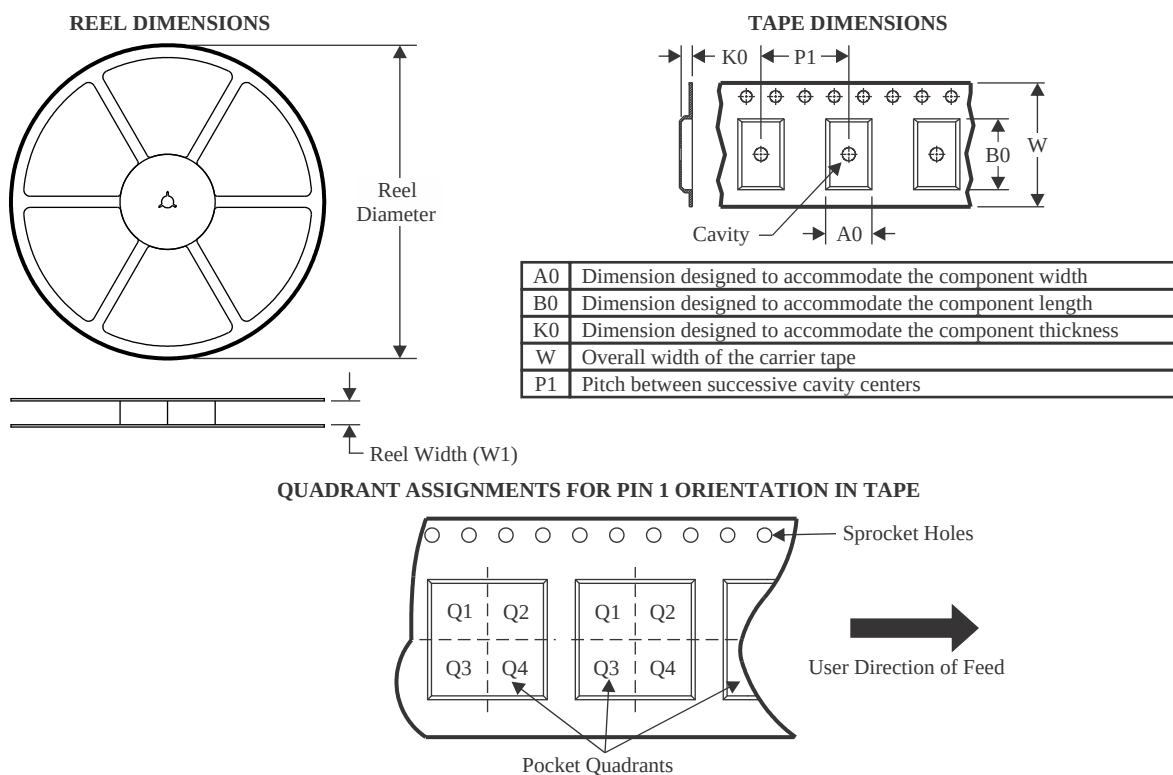
⁽⁶⁾ Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

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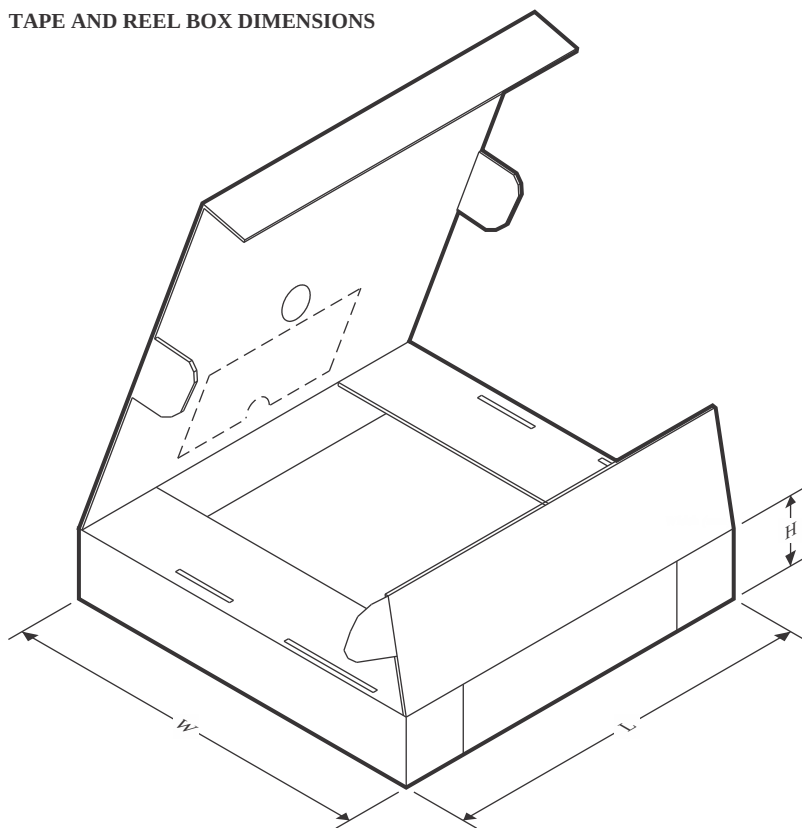
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74CB3Q16211DGGR	TSSOP	DGG	56	2000	330.0	24.4	8.6	15.6	1.8	12.0	24.0	Q1
SN74CB3Q16211DGVR	TVSOP	DGV	56	2000	330.0	24.4	6.8	11.7	1.6	12.0	24.0	Q1
SN74CB3Q16211DLR	SSOP	DL	56	1000	330.0	32.4	11.35	18.67	3.1	16.0	32.0	Q1

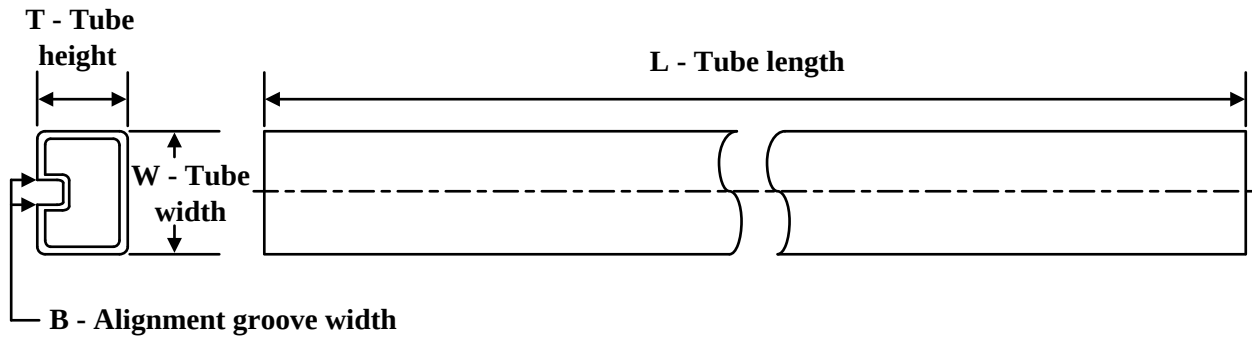
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74CB3Q16211DGGR	TSSOP	DGG	56	2000	367.0	367.0	45.0
SN74CB3Q16211DGVR	TVSOP	DGV	56	2000	367.0	367.0	45.0
SN74CB3Q16211DLR	SSOP	DL	56	1000	367.0	367.0	55.0

TUBE



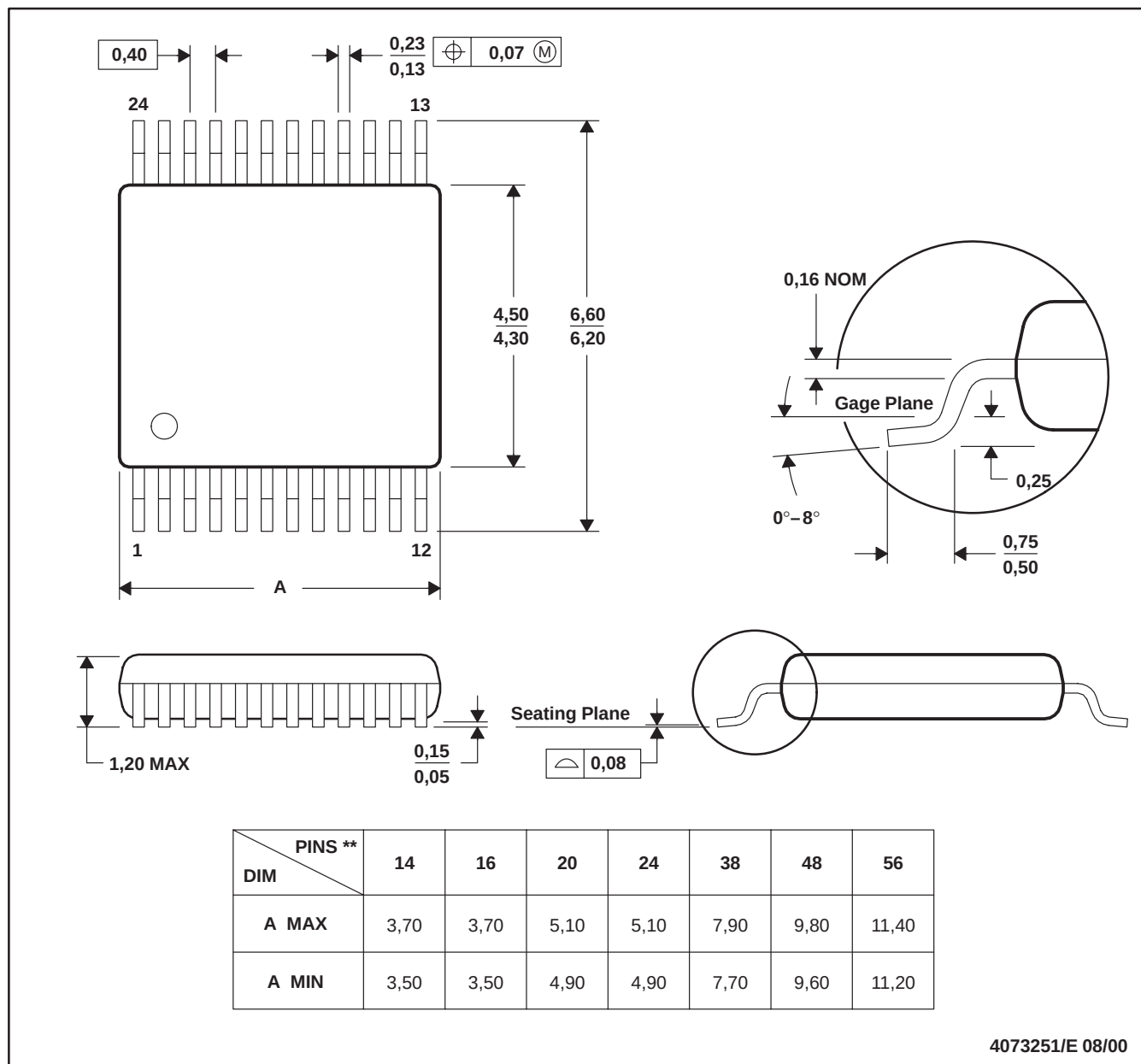
*All dimensions are nominal

Device	Package Name	Package Type	Pins	SPQ	L (mm)	W (mm)	T (μm)	B (mm)
SN74CB3Q16211DL	DL	SSOP	56	20	473.7	14.24	5110	7.87

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



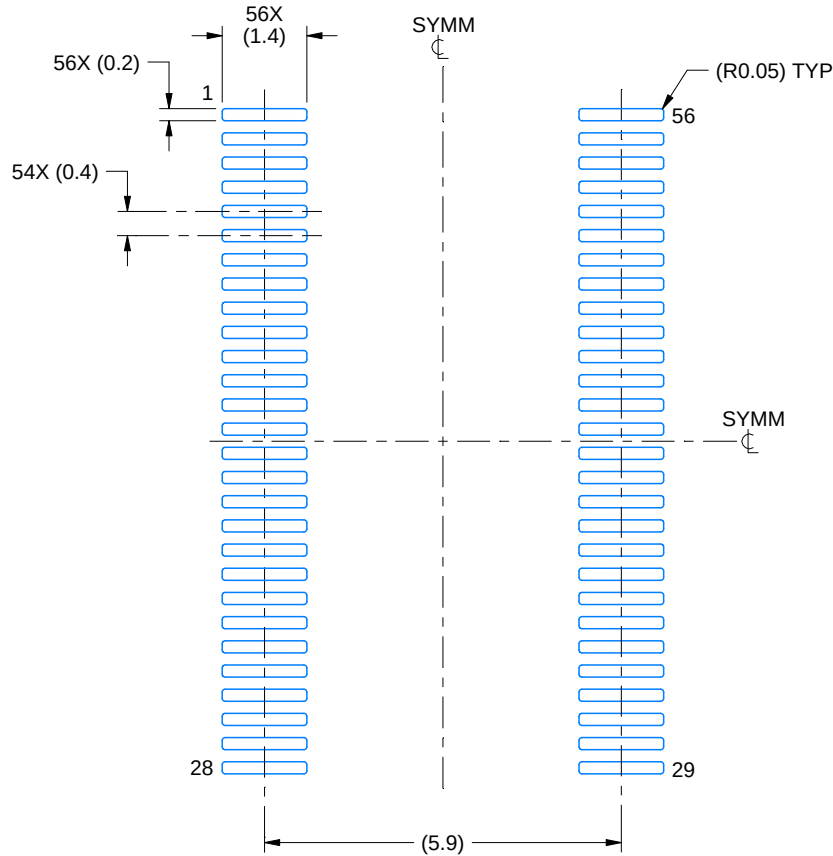
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

EXAMPLE BOARD LAYOUT

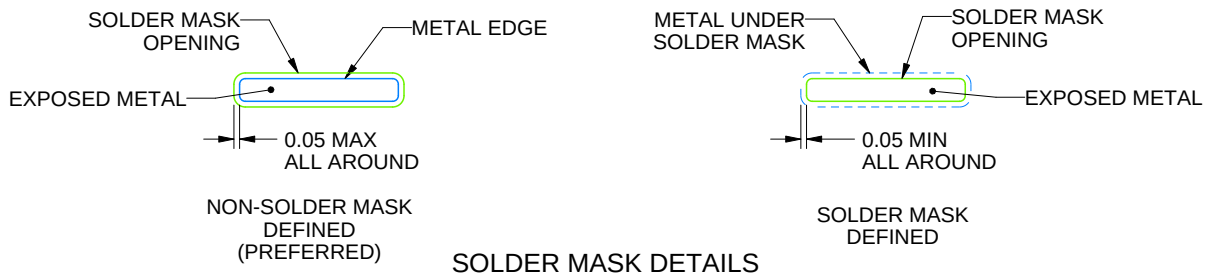
DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 8X



4220240/B 12/2020

NOTES: (continued)

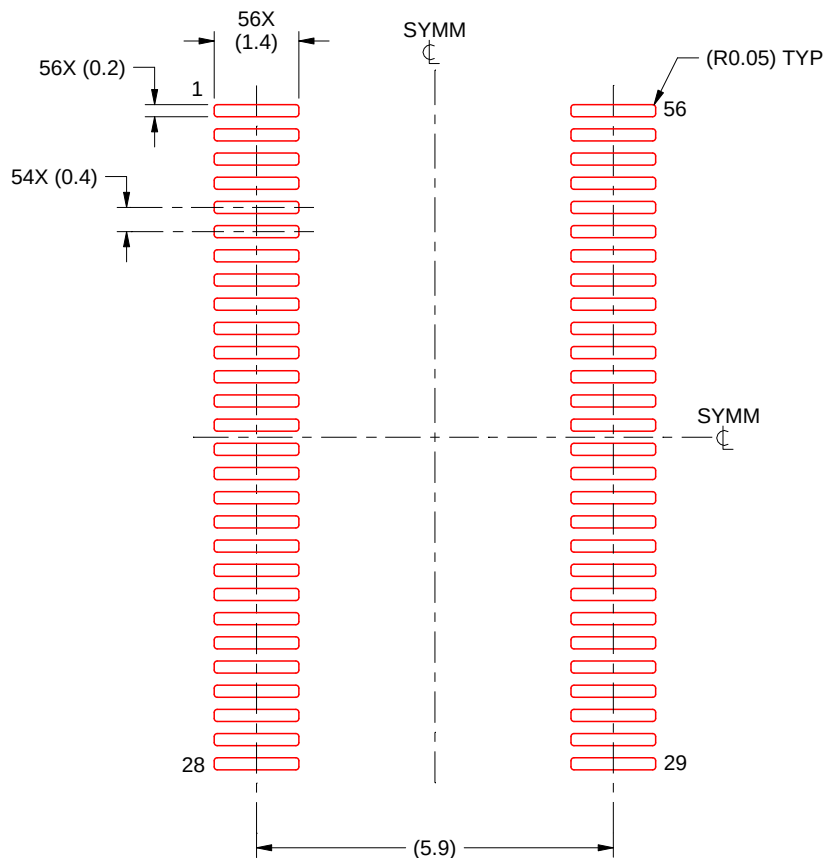
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGV0056A

TVSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



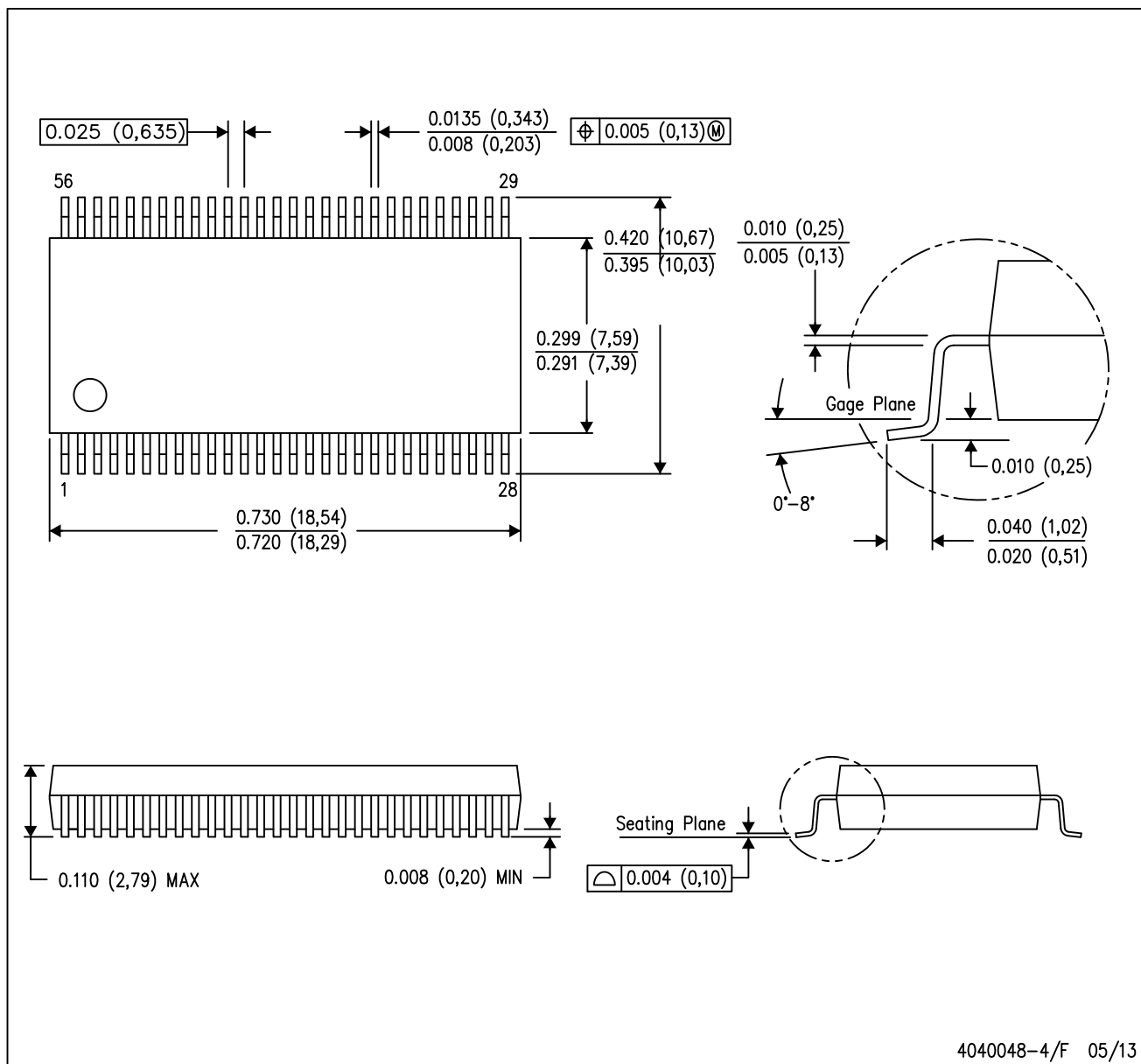
4220240/B 12/2020

NOTES: (continued)

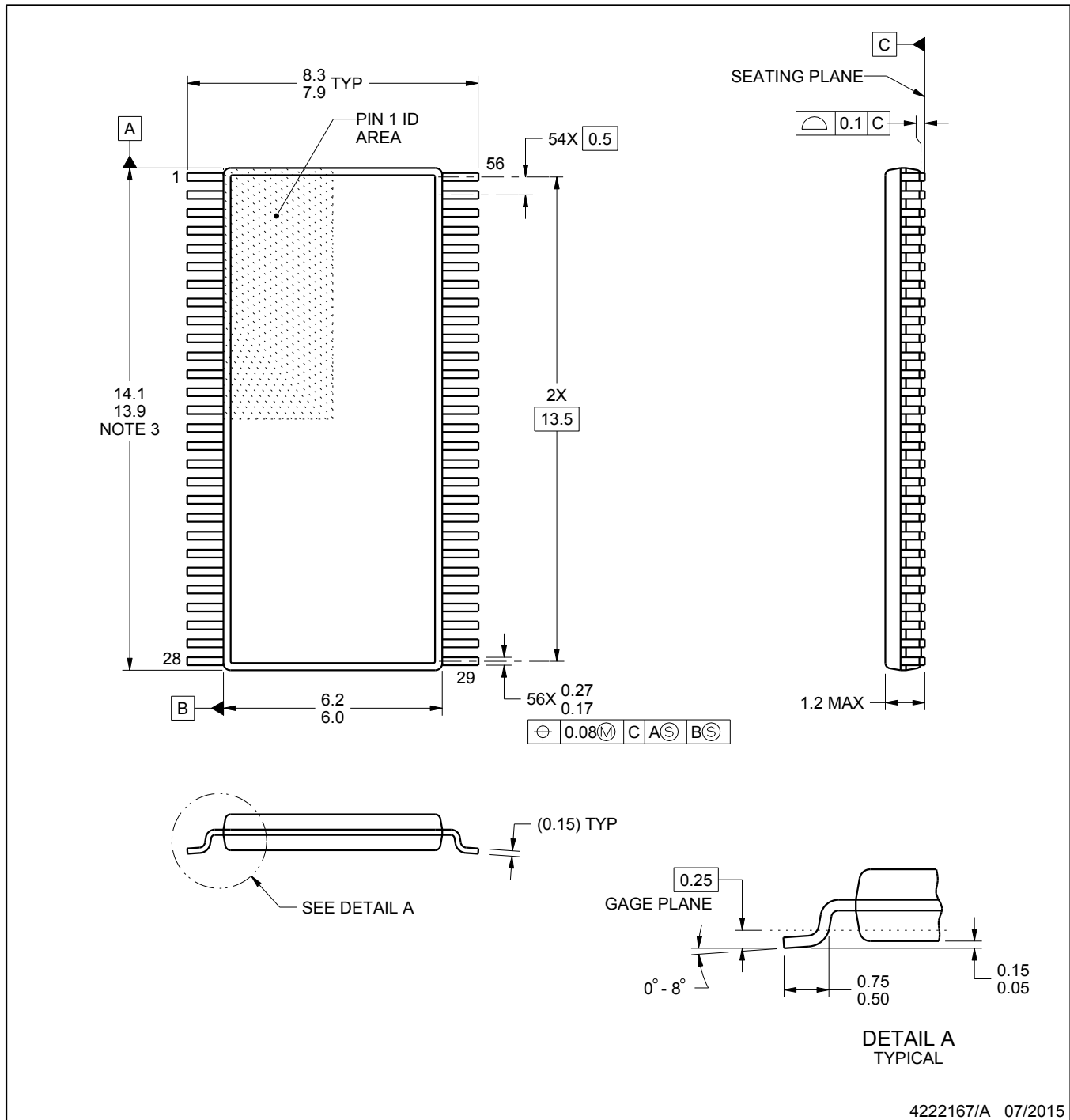
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

DL (R-PDSO-G56)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 - Falls within JEDEC MO-118



4222167/A 07/2015

NOTES:

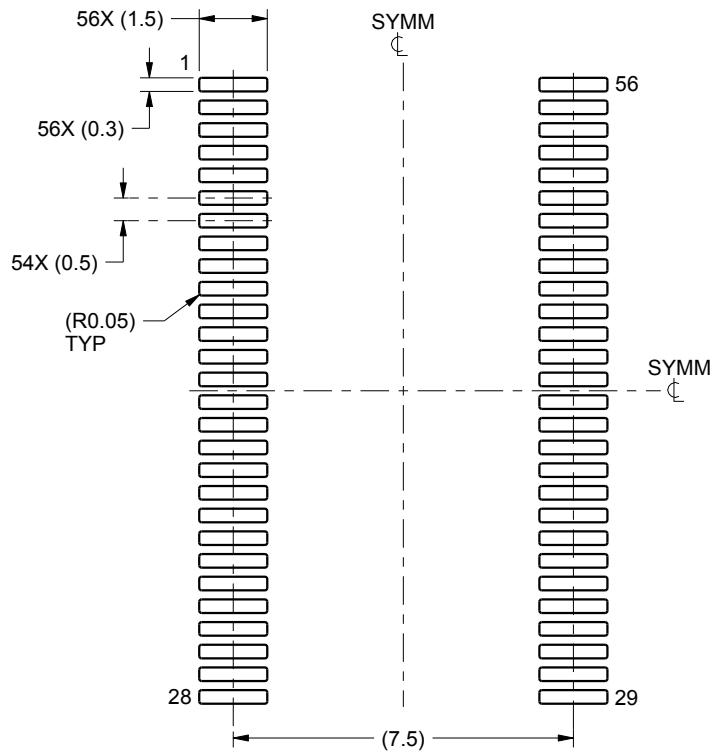
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- Reference JEDEC registration MO-153.

EXAMPLE BOARD LAYOUT

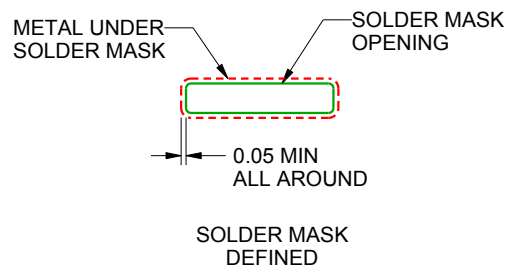
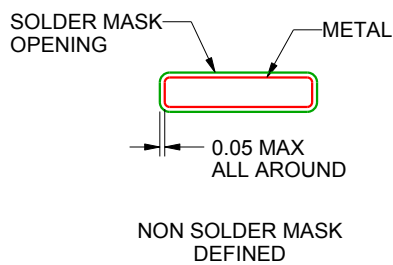
DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
SCALE:6X



SOLDER MASK DETAILS

4222167/A 07/2015

NOTES: (continued)

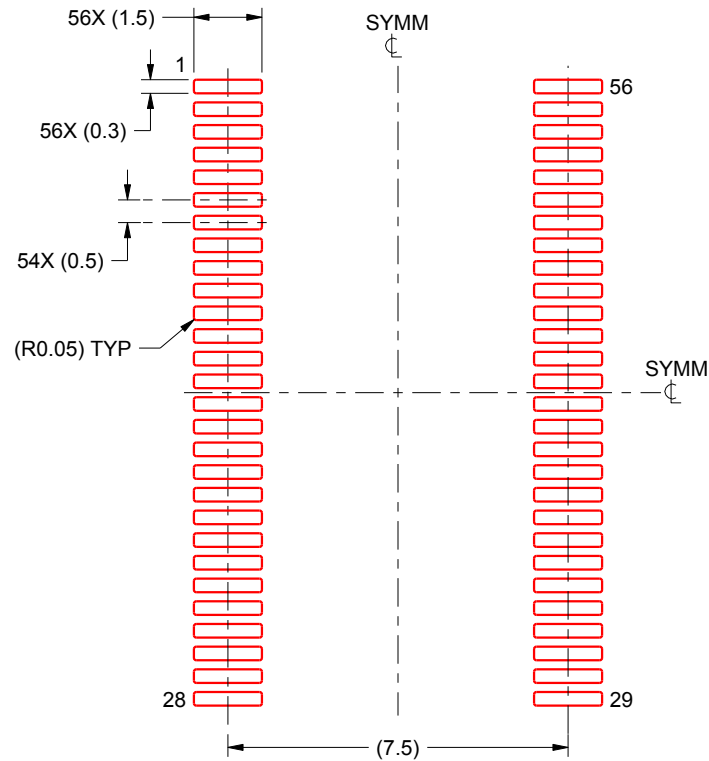
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DGG0056A

TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4222167/A 07/2015

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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