ATA00501

AGC Transimpedance Amplifier
SONET OC-1

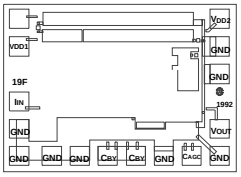
PRELIMINARY DATA SHEET-Rev 1.5

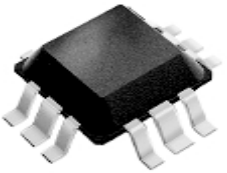
FEATURES

- Single +5 Volt Supply
- Automatic Gain Control
- -43 dBm Sensitivity
- 0 dBm Optical Overload
- 70 MHz Bandwidth

APPLICATIONS

- OC-1 Receiver
- FITL
- Low Noise RF Amplifier





D1C	S2 12 Pin 4 Sided SQFP Package

PRODUCT DESCRIPTION

The ANADIGICS ATA00501 is a 5V low noise transimpedance amplifier with AGC designed to be used in OC-1 fiber optic links. The device is used in conjunction with a photodetector (PIN diode or avalanche photodiode) to convert an optical signal into an output voltage. The ATA00501 has a bandwidth of 70MHz and a dynamic range in excess of 40dB. It is manufactured in a GaAs MESFET process and available in bare die form or a 12 pin SQFP package.

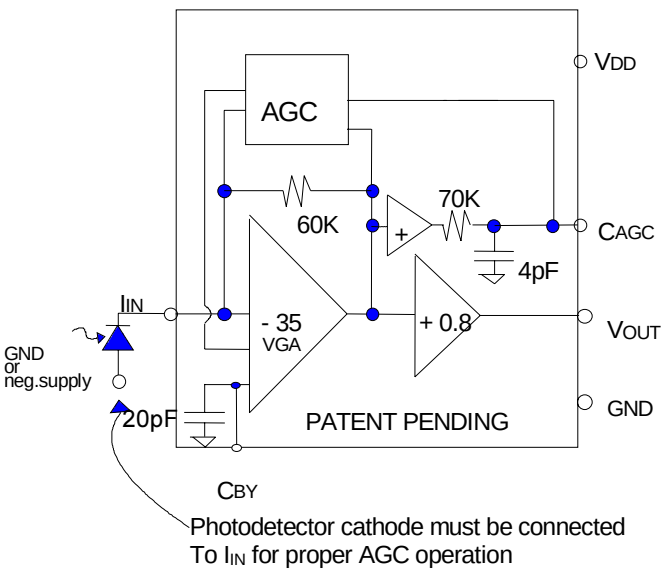


Figure 1: ATA00501 Equivalent Circuit

Table 1: ATA00501D1C Pad Description (Die Only)

PAD	DESCRIPTION	COMMENT
VDD1	VDD1	Positive supply for input gain stage
VDD2	VDD2	Positive supply for second gain stage
IIN	TIA Input Current	Connect detector cathode for proper operation
VOUT	TIA Output Voltage	Requires external DC block
CAGC	External AGC Capacitor	70K * CAGC= AGC time constant
CBY	Input gain stage bypass capacitor	>56 pF

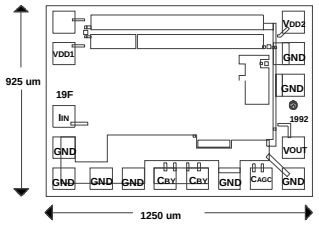


Figure 2: Bonding Pad Layout (Die Only)

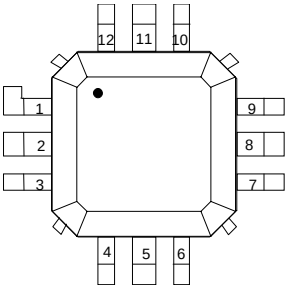


Figure 3: Pin Layout

Table 2:ATA00501S2C Pin Description

PIN	DESCRIPTION	PIN	DESCRIPTION
1	NC	7	V_{OUT}
2	GND	8	GND
3	I_{IN}	9	NC
4	C_{BY}	10	V_{DD}
5	GND	11	GND
6	C_{AGC}	12	NC

ELECTRICAL CHARACTERISTICS

Table 3: Absolute Maximum Ratings

V_{DD1}	7.0 V
V_{DD2}	7.0 V
I_{IN}	5 mA
T_A	Operating Temp. - 40 ° C to 125 ° C
T_S	Storage Temp. - 65 ° C to 150 ° C

Stresses in excess of the absolute ratings may cause permanent damage. Functional operation is not implied under these conditions. Exposure to absolute ratings for extended periods of time may adversely affect reliability.

Table 4: Electrical Specifications

PARAMETER	MIN	TYP	MAX	UNIT
Transresistance(RL=∞,Idc<500nA)		55		KΩ
Transresistance (R_L=50) (1)	15	28		KΩ
Bandwith -3dB	50	70		MHz
Input Resistance (2)		1500		Ω
Output Resistance	30	50	60	Ω
Input Offset Voltage	1.5	1.6	1.9	Volts
Output Offset Voltage		1.8		Volts
Offset Voltage Drift		1		mV/°C
AGC Threshold (I_{IN}) (3)	5	10		μA
Optical Overload (4)	-3	0		dBm
AGC Time Constant (6)		16		μsec
Optical Sensitivity - DIE (7)		- 43		dBm
Optical Sensitivity - SQFP (7)		-41		dBm
Supply Current		30	45	mA
Operating Voltage Range	+ 4.5	+ 5.0	+ 6.0	Volts
Operating Temperature Range	- 40		85	°C

Notes:

(1) f=50MHz

(2) Measured with I_{IN} below AGC Threshold. During AGC, input impedance will decrease proportionally to I_{IN}

(3) Defined as the I_{IN} where Transresistance has decreased by 50%.

(4) See note on "Indirect Measurement of Optical Overload".

(5) See note on "Measurement of Input Referred Noise Current".

(6) C_{AGC} = 56 pF

(7) Parameter is guaranteed (not tested) by design and characterization data @ 51Mb/s, assuming detector responsivity of 0.9

APPLICATION INFORMATION

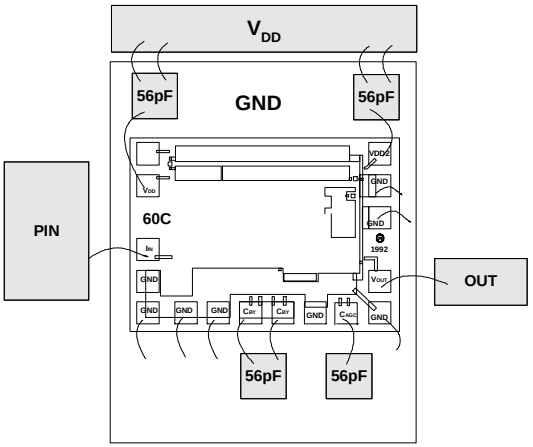


Figure 4: ATA 00501D1C Typical Bonding

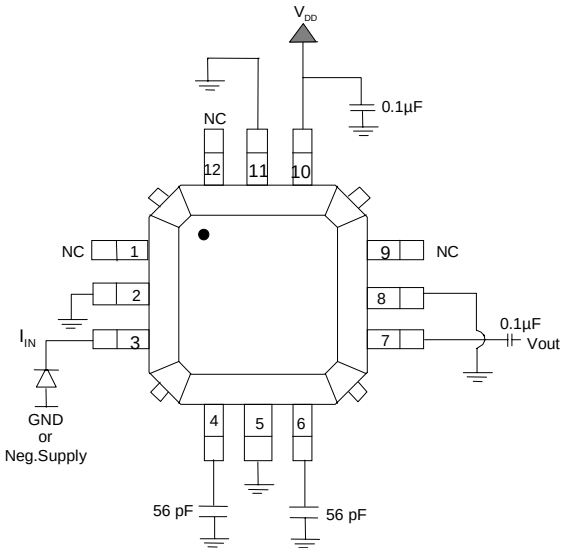


Figure 5: ATA 00501S2C External Circuit

Power Supplies and General Layout Considerations

The ATA00501S2C may be operated from a positive supply as low as + 4.5 V and as high as + 6.0 V. Below + 4.5 V, bandwidth, overload and sensitivity will degrade, while at + 6.0 V, bandwidth, overload and sensitivity improve (see “Bandwidth vs. Temperature” curves). Use of surface mount, low inductance power supply bypass capacitors (>=56pF) are essential for good high frequency and low noise performance. The power supply bypass capacitors should be mounted on or connected to a good low inductance ground plane.

General Layout Considerations

Since the gain stages of the transimpedance amplifier have an open loop bandwidth in excess of 1.0 GHz, it is essential to maintain good high frequency layout practices. To prevent oscillations, a low inductance RF ground plane should be made available for power supply bypassing. Traces that can be made short should be made short, and the utmost care should be taken to maintain very low capacitance at the photodiode-TIA interface (I_{IN}), excess capacitance at this node will cause a degradation in bandwidth and sensitivity (see Bandwidth vs. C_T curves).

Figure 6: Bandwidth vs. Temperature

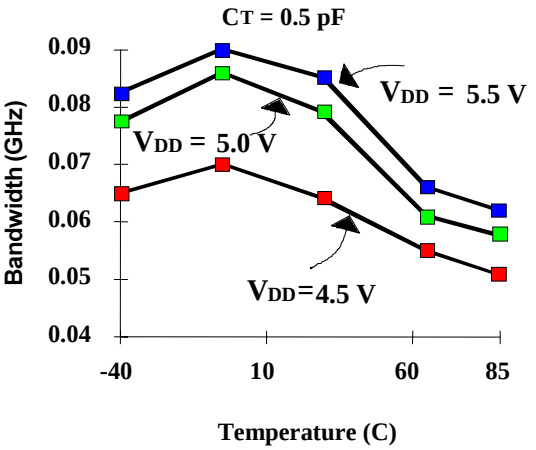
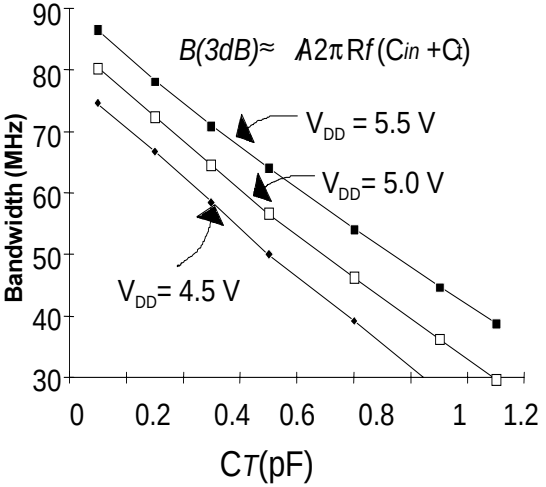


Figure 7: Bandwidth vs. CT



Note: All performance curves are typical @ T_A =25 °C unless otherwise noted.

I_{IN} Connection

(Refer to the equivalent circuit diagram.) Bonding the detector cathode to I_{IN} (and thus drawing current from the ATA00501) improves the dynamic range. Although the detector may be used in the reverse direction for input currents not exceeding 25µA, the specifications for optical overload will not be met.

Figure 8: Transimpedance vs. IIN

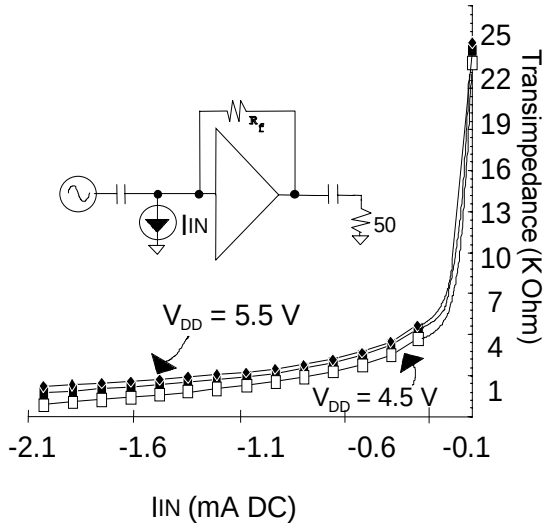
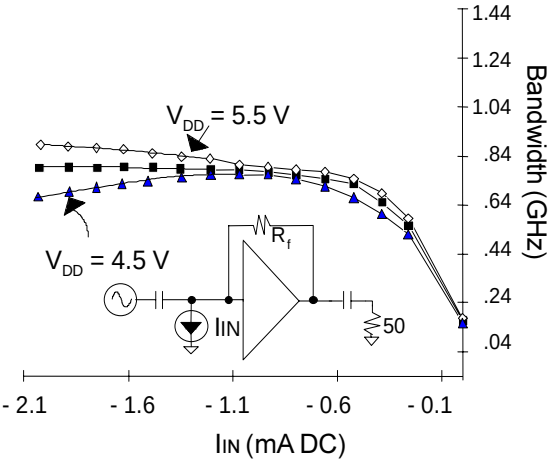


Figure 9: Bandwidth vs. IIN



V_{OUT} Connection

The output pad should be connected via a coupling capacitor to the next stage of the receiver channel (filter or decision circuits), as the output buffers are not designed to drive a DC coupled 50 ohm load (this would require an output bias current of approximately 36 mA to maintain a quiescent 1.8 Volts across the output load). If V_{OUT} is connected to a high input impedance decision circuit (>500 ohms), then a coupling capacitor may not be required, although caution should be exercised since DC offsets of the photo detector/TIA combination may cause clipping of subsequent gain or decision circuits.

Figure 10: VOUT vs. IIN

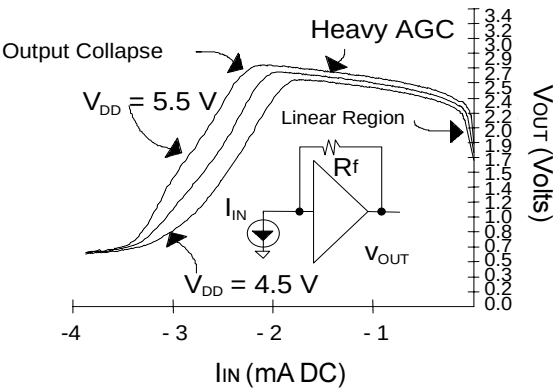
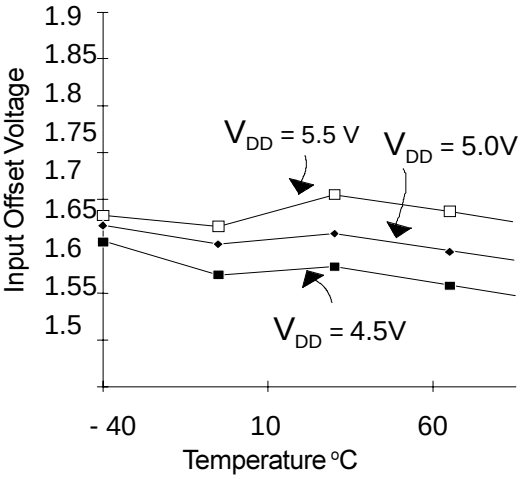


Figure 11: Input Offset Voltage vs. Temperature



C_{BY} Connection

The C_{BY} pad must be connected via a low inductance path to a surface mount capacitor of at least 56pF (additional capacitance can be added in parallel with the 56 pF or 220 pF capacitors to improve low frequency response and noise performance). Referring to the equivalent circuit diagram and the typical bonding diagram, it is critical that the connection from CBY to the bypass capacitor use two bond wires for low inductance, since any high frequency impedance at this node will be fed back to the open loop amplifier with a resulting loss of transimpedance bandwidth. Two pads are provided for this purpose.

Sensitivity and Bandwidth

In order to guarantee sensitivity and bandwidth performance, the TIA is subjected to a comprehensive series of tests at the die sort level (100% testing at 25 ^{O}C) to verify the DC parametric performance and the high frequency performance (i.e. adequate |S21|) of the amplifier. Acceptably high |S21| of the internal gain stages will ensure low amplifier input capacitance and hence low input referred noise current. Transimpedance sensitivity and bandwidth are then guaranteed by design and correlation with RF and DC die sort test results.

Indirect Measurement of Optical Overload

Optical overload can be defined as the maximum optical power above which the BER (bit error rate) increases beyond 1 error in 10^{10} bits. The ATA00501D1C is 100% tested at die sort by a DC measurement which has excellent correlation with an PRBS optical overload measurement. The measurement consists of sinking a negative current (see V_{OUT} vs I_{IN} figure) from the TIA and determining the point of output voltage collapse. Also the input node virtual ground during “heavy AGC” is checked to verify that the linearity (i.e. pulse width distortion) of the amplifier has not been compromised.

Measurement of Input Referred Noise Current

The “Input Noise Current” is directly related to sensitivity . It can be defined as the output noise voltage (Vout), with no input signal, (including a 30 MHz lowpass filter at the output of the TIA) divided by the AC transresistance.

Figure 12: Input Referred Noise Spectral Density

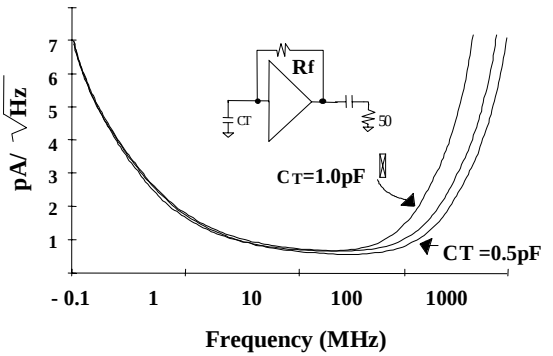
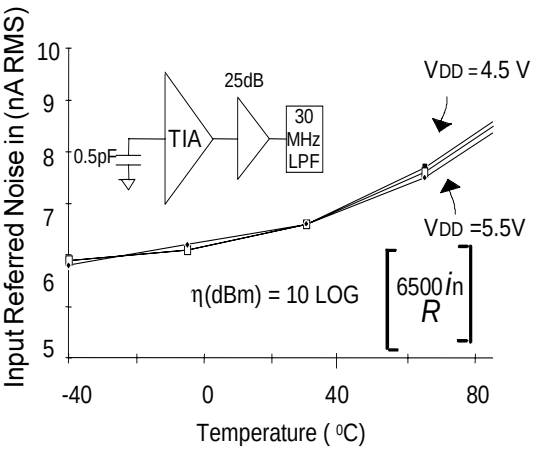


FIgure 13: Input Referred Noise vs Temperature



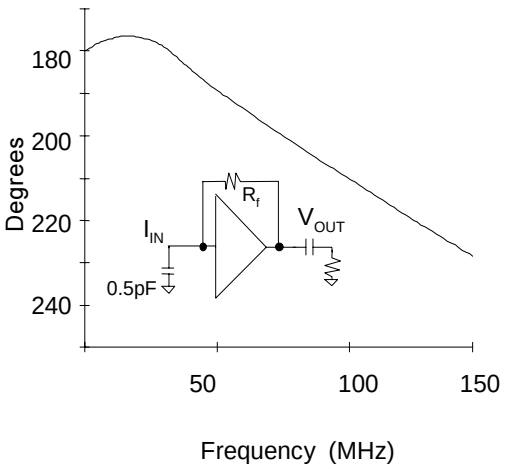
AGC Capacitor

It is important to select an external AGC capacitor of high quality and appropriate size. The ATA00501D1C has an on-chip 70 KΩ resistor with a shunt 4 pF capacitor to ground. Without external capacitance the chip will provide an AGC time constant of 280 nS. For the best performance in a typical 51MB/s SONET receiver, a minimum AGC capacitor of 56pF is recommended. This will provide the minimum amount of protection against pattern sensitivity and pulse width distortion on repetitive data sequences during high average optical power conditions. Conservative design practices should be followed when selecting an AGC capacitor, since unit to unit variability of the internal time constant and various data conditions can lead to data errors if the chosen value is too small.

Phase Response

At frequencies below the 3dB bandwidth of the device, the transimpedance phase response is characteristic of a single pole transfer function (as shown in the Phase vs Frequency curve). The output impedance is essentially resistive up to 1000 MHz.

Figure 14: Phase (I_{IN} to V_{OUT})



PACKAGE OUTLINE

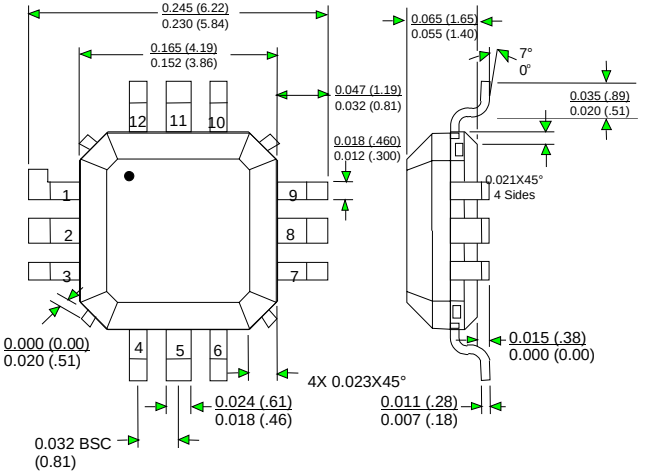


Figure 15: ATA00501S2C Package Pin-Out (S2C)
Dimensions in Inches (Millimeters)

ORDERING INFORMATION

PART NUMBER	PACKAGE OPTION	PACKAGE DESCRIPTION
ATA00501D1C	D1C	Die
ATA00501S2C	S2C	12 Pin 4 Sided SQFP Package

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