

## Stereo Audio Volume Control

### FEATURES

- **DIGITALLY-CONTROLLED ANALOG VOLUME CONTROL:**
  - Two Independent Audio Channels
  - Serial Control Interface
  - Zero Crossing Detection
  - Mute Function
- **WIDE GAIN AND ATTENUATION RANGE:**
  - +31.5dB to -95.5dB with 0.5dB Steps
- **LOW NOISE AND DISTORTION:**
  - 120dB Dynamic Range
  - 0.0004% THD+N at 1kHz
- **LOW INTERCHANNEL CROSSTALK:**
  - 126dBFS
- **NOISE-FREE LEVEL TRANSITIONS**
- **POWER SUPPLIES: ±15V Analog, +5V Digital**
- **AVAILABLE IN DIP-16 AND SOL-16 PACKAGES**
- **PIN AND SOFTWARE COMPATIBLE WITH THE PGA2311 AND CIRRUS LOGIC CS3310™**

### APPLICATIONS

- **AUDIO AMPLIFIERS**
- **MIXING CONSOLES**
- **MULTI-TRACK RECORDERS**
- **BROADCAST STUDIO EQUIPMENT**
- **MUSICAL INSTRUMENTS**
- **EFFECTS PROCESSORS**
- **A/V RECEIVERS**
- **CAR AUDIO SYSTEMS**

### DESCRIPTION

The PGA2310 is a high-performance, stereo audio volume control designed for professional and high-end consumer audio systems. The ability to operate from  $\pm 15V$  analog power supplies enables the PGA2310 to process input signals with large voltage swings, thereby preserving the dynamic range available in the overall signal path. Using high performance operational amplifier stages internal to the PGA2310 yields low noise and distortion, while providing the capability to drive  $600\Omega$  loads directly without buffering. The three-wire serial control interface allows for connection to a wide variety of host controllers, in addition to support for daisy-chaining of multiple PGA2310 devices.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

# PGA2310

SBOS207B – OCTOBER 2001 – REVISED JUNE 2004



This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted<sup>(1)</sup>

		PGA2310	UNIT
Supply voltage	V <sub>A+</sub>	+16.0	V
	V <sub>A-</sub>	-16.0	V
	V <sub>D+</sub>	+6.5	V
Analog input voltage		0 to V <sub>A+</sub> , V <sub>A-</sub>	V
Digital input voltage		-0.3 to V <sub>D+</sub>	V
Operating temperature range		-55 to +125	°C
Storage temperature range		-65 to +150	°C
Junction temperature		+150	°C
Lead temperature (soldering, 10s)		+300	°C
Package temperature (IR, reflow, 10s)		+235	°C

<sup>(1)</sup> Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. Exposure to absolute maximum conditions for extended periods may degrade device reliability. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those specified is not implied.

## ORDERING INFORMATION<sup>(1)</sup>

PRODUCT	PACKAGE-LEAD	PACKAGE DESIGNATOR	SPECIFIED TEMPERATURE RANGE	PACKAGE MARKING	ORDERING NUMBER	TRANSPORT MEDIA, QUANTITY
PGA2310	DIP-16	N	-40°C to +85°C	PGA2310PA	PGA2310PA	Rails, 25
	SOL-16	DW		PGA2310UA	PGA2310UA	Rails, 48
				PGA2310UA	PGA2310UA/1K	Tape and Reel, 1000

<sup>(1)</sup> For the most current package and ordering information, see the Package Option Addendum located at the end of this data sheet.

**ELECTRICAL CHARACTERISTICS**

At  $T_A = +25^\circ\text{C}$ ,  $V_{A+} = +15\text{V}$ ,  $V_{A-} = -15\text{V}$ ,  $V_{D+} = +5\text{V}$ ,  $R_L = 100\text{k}\Omega$ ,  $C_L = 20\text{pF}$ , BW measure = 10Hz to 20kHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	PGA2310			UNIT
		MIN	TYP	MAX	
<b>DC CHARACTERISTICS</b>					
Step Size			0.5		dB
Gain Error	Gain Setting = 31.5dB		$\pm 0.05$		dB
Gain Matching			$\pm 0.05$		dB
Input Resistance			10		$\text{k}\Omega$
Input Capacitance			7		pF
<b>AC CHARACTERISTICS</b>					
THD+N	$V_{IN} = 10\text{V}_{pp}$ , $f = 1\text{kHz}$		0.0004	0.001	%
Dynamic Range	$V_{IN} = \text{AGND}$ , Gain = 0dB	116	120		dB
Voltage Range, Input and Output		$(V_{A-}) + 1.5$		$(V_{A-}) - 1.5$	V
Output Noise	$V_{IN} = \text{AGND}$ , Gain = 0dB		9.5	13.5	$\mu\text{V}_{RMS}$
Interchannel Crosstalk	$f = 1\text{kHz}$		-126		dBFS
<b>OUTPUT BUFFER</b>					
Offset Voltage	$V_{IN} = \text{AGND}$ , Gain = 0dB		0.5	3	mV
Load Capacitance Stability			1000		pF
Short-Circuit Current			35		mA
Unity-Gain Bandwidth, Small Signal			1.5		MHz
<b>DIGITAL CHARACTERISTICS</b>					
High-Level Input Voltage, $V_{IH}$		+2.0		$V_{D+}$	V
Low-Level Input Voltage, $V_{IL}$		-0.3		0.8	V
High-Level Output Voltage, $V_{OH}$	$I_O = 200\mu\text{A}$	$(V_{D+}) - 1.0$			V
Low-Level Output Voltage, $V_{OL}$	$I_O = -3.2\text{mA}$			0.4	V
Input Leakage Current			1	10	$\mu\text{A}$
<b>SWITCHING CHARACTERISTICS</b>					
Serial Clock (SCLK) Frequency	$t_{SCLK}$	0		6.25	MHz
Serial Clock (SCLK) Pulse Width Low	$t_{PH}$	80			ns
Serial Clock (SCLK) Pulse Width High	$t_{PL}$	80			ns
MUTE Pulse Width Low	$t_{MI}$	2.0			ms
<b>Input Timing</b>					
SDI Setup Time	$t_{SDS}$	20			ns
SDI Hold Time	$t_{SDH}$	20			ns
$\overline{\text{CS}}$ Falling to SCLK Rising	$t_{CSCR}$	90			ns
SCLK Falling to $\overline{\text{CS}}$ Rising	$t_{CFCS}$	35			ns
<b>Output Timing</b>					
$\overline{\text{CS}}$ Low to SDO Active	$t_{CSO}$			35	ns
SCLK Falling to SDO Data Valid	$t_{CFDO}$			60	ns
$\overline{\text{CS}}$ High to SDO High Impedance	$t_{CSZ}$			100	ns
<b>POWER SUPPLY</b>					
Operating Voltage					
$V_{A+}$		+4.5	+15	+15.5	V
$V_{A-}$		-4.5	-15	-15.5	V
$V_{D+}$		+4.5	+5	+5.5	V
Quiescent Current					
$I_{A+}$	$V_{A+} = +15\text{V}$		7.5	10	mA
$I_{A-}$	$V_{A-} = -15\text{V}$		7.7	10	mA
$I_{D+}$	$V_{D+} = +5\text{V}$		0.8	1.5	mA

# PGA2310

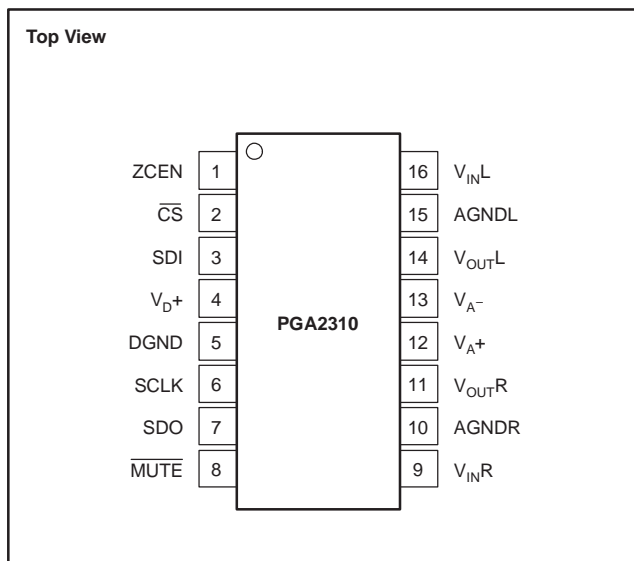
SBOS207B – OCTOBER 2001 – REVISED JUNE 2004

## ELECTRICAL CHARACTERISTICS (continued)

 At  $T_A = +25^\circ\text{C}$ ,  $V_{A+} = +15\text{V}$ ,  $V_{A-} = -15\text{V}$ ,  $V_{D+} = +5\text{V}$ ,  $R_L = 100\text{k}\Omega$ ,  $C_L = 20\text{pF}$ , BW measure = 10Hz to 20kHz, unless otherwise noted.

PARAMETER	TEST CONDITIONS	PGA2310			UNIT
		MIN	TYP	MAX	
<b>TEMPERATURE RANGE</b>					
Specified Range		-40		+85	$^\circ\text{C}$
Operating Range		-55		+125	$^\circ\text{C}$
Storage Range		-65		+150	$^\circ\text{C}$
Thermal Resistance, $\theta_{JC}$					
DIP-16			60		$^\circ\text{C}/\text{W}$
SOL-16			50		$^\circ\text{C}/\text{W}$

## PIN CONFIGURATION

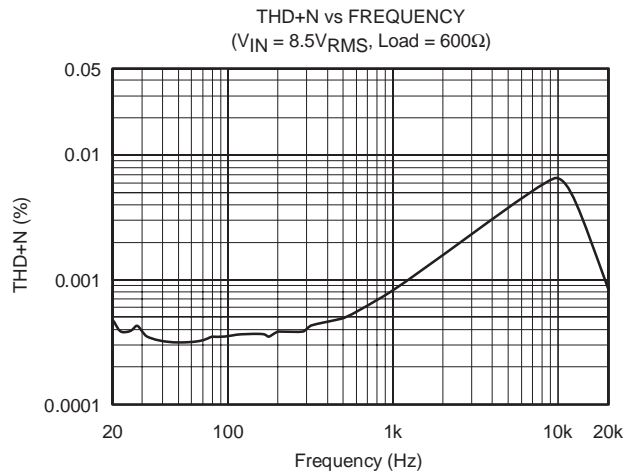
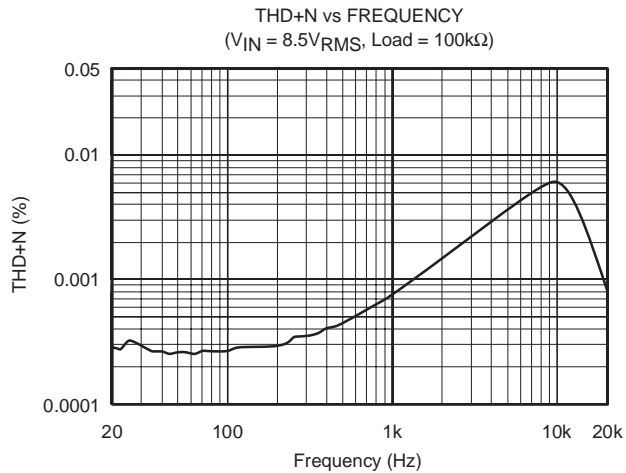
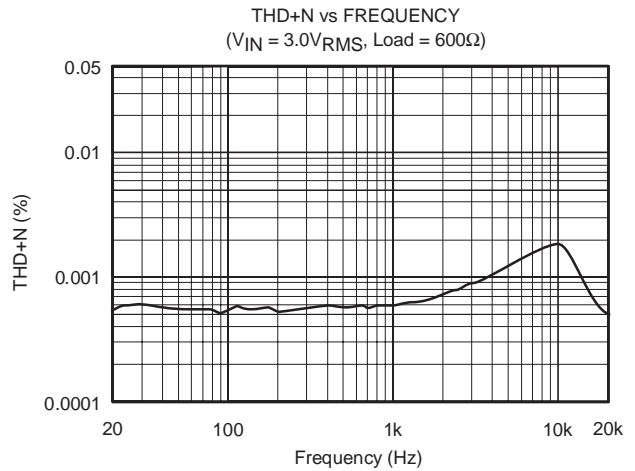
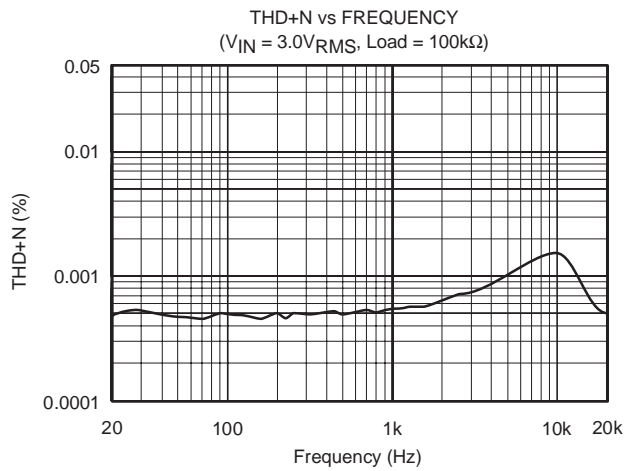
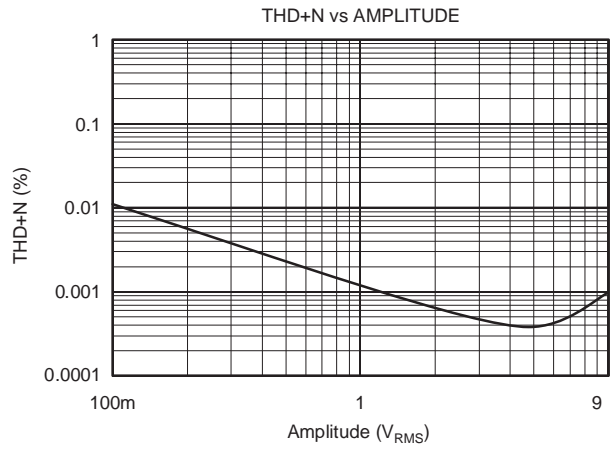
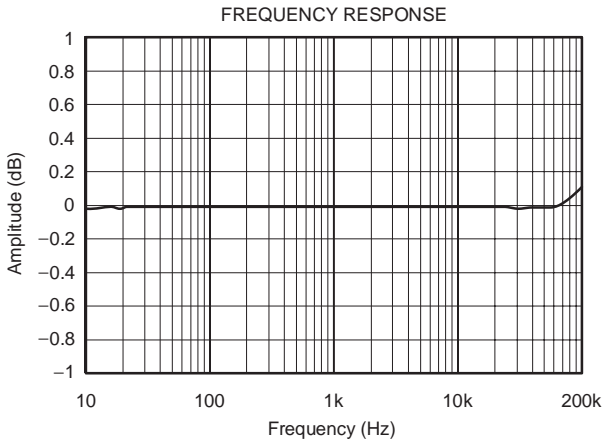


## PIN ASSIGNMENTS

PIN	NAME	FUNCTION
1	ZCEN	Zero Crossing Enable Input (Active High)
2	$\overline{\text{CS}}$	Chip Select Input (Active Low)
3	SDI	Serial Data input
4	$V_{D+}$	Digital Power Supply, +5V
5	DGND	Digital Ground
6	SCLK	Serial Clock Input
7	SDO	Serial Data Output
8	$\overline{\text{MUTE}}$	Mute Control Input (Active Low)
9	$V_{INR}$	Analog Input, Right Channel
10	AGNDR	Analog Ground, Right Channel
11	$V_{OUTR}$	Analog Output, Right Channel
12	$V_{A+}$	Analog Power Supply, +15V
13	$V_{A-}$	Analog Power Supply, -15V
14	$V_{OUTL}$	Analog Output, Left Channel
15	AGNDL	Analog Ground, Left Channel
16	$V_{INL}$	Analog Input, Left Channel

**TYPICAL CHARACTERISTICS**

At  $T_A = +25^\circ\text{C}$ ,  $V_{A+} = +15\text{V}$ ,  $V_{A-} = -15\text{V}$ ,  $V_{D+} = +5\text{V}$ ,  $R_L = 100\text{k}\Omega$ ,  $C_L = 20\text{pF}$ , BW measure = 10Hz to 20kHz, unless otherwise noted.

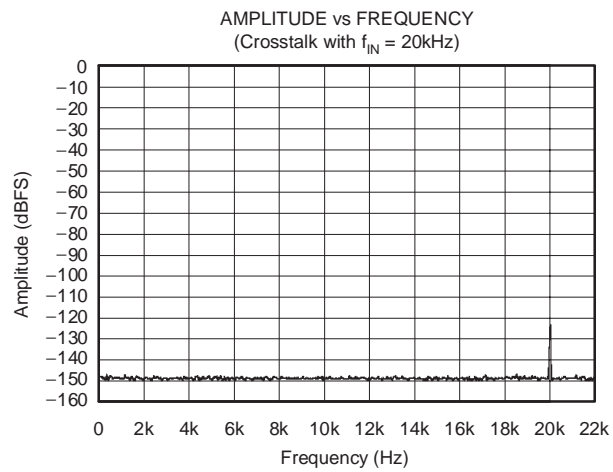
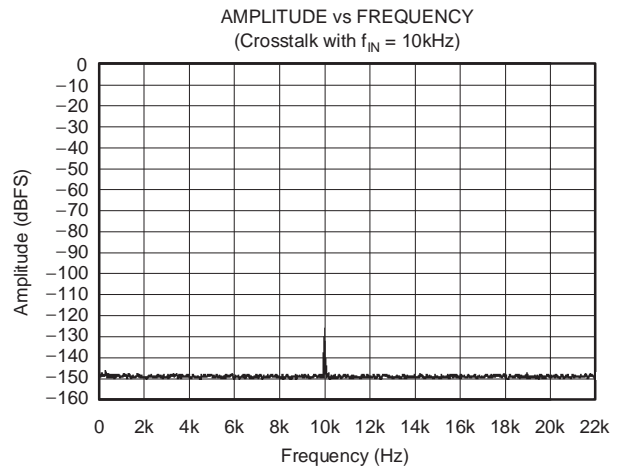
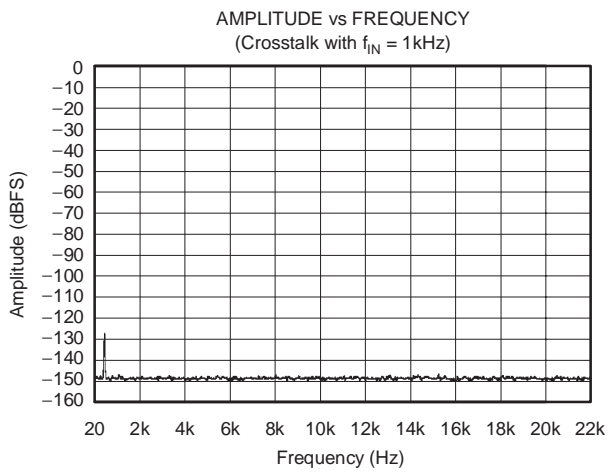


# PGA2310

SBOS207B – OCTOBER 2001 – REVISED JUNE 2004

## TYPICAL CHARACTERISTICS (continued)

At  $T_A = +25^\circ\text{C}$ ,  $V_{A+} = +15\text{V}$ ,  $V_{A-} = -15\text{V}$ ,  $V_{D+} = +5\text{V}$ ,  $R_L = 100\text{k}\Omega$ ,  $C_L = 20\text{pF}$ , BW measure = 10Hz to 20kHz, unless otherwise noted.



## GENERAL DESCRIPTION

The PGA2310 is a stereo audio volume control. It may be used in a wide array of professional and consumer audio equipment. The PGA2310 is fabricated in a mixed-signal BiCMOS process, as to take advantage of the superior analog characteristics for which it offers.

The heart of the PGA2310 is a resistor network, an analog switch array, and a high-performance bipolar op amp stage. The switches are used to select taps in the resistor network that, in turn, determine the gain of the amplifier stage. Switch selections are programmed using a serial control port. The serial port allows connection to a wide variety of host controllers. Figure 1 shows a functional block diagram of the PGA2310.

## POWER-UP STATE

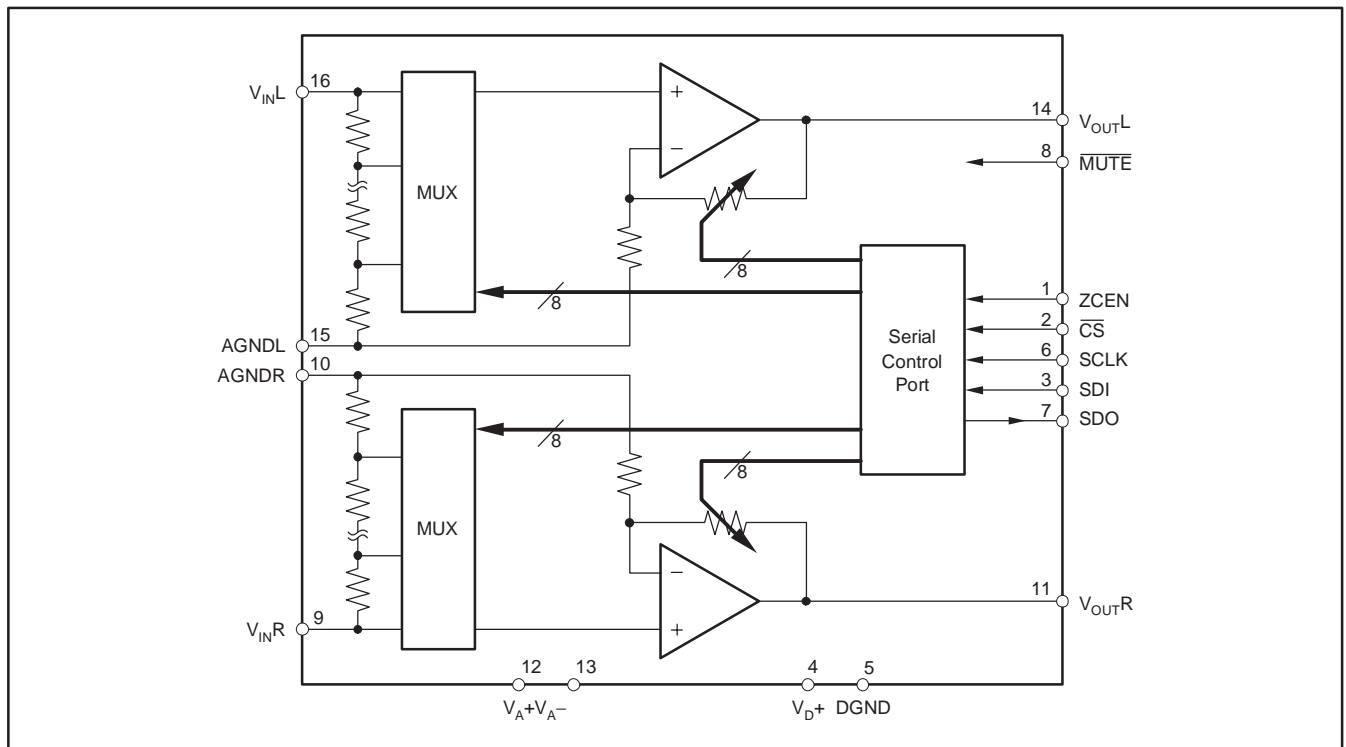
On power up, all internal flip-flops are reset. The gain byte value for both the left and right channels are set to 00<sub>HEX</sub>, or mute condition. The gain will remain at this setting until the host controller programs new settings for each channel via the serial control port.

## ANALOG INPUTS AND OUTPUTS

The PGA2310 includes two independent channels, referred to as the left and right channels. Each channel has a corresponding input and output pin. The input and output pins are unbalanced, or referenced to analog ground (either AGNDR or AGNDL). The inputs are named  $V_{INR}$  (pin 9) and  $V_{INL}$  (pin 16), while the outputs are named  $V_{OUTR}$  (pin 11) and  $V_{OUTL}$  (pin 14).

The input and output pins may swing within 1.5V of the analog power supplies,  $V_{A+}$  (pin 12) and  $V_{A-}$  (pin 13). Given  $V_{A+} = +15V$  and  $V_{A-} = -15V$ , the maximum input or output voltage range is 27V<sub>PP</sub>.

It is important to drive the PGA2310 with a low source impedance. If a source impedance of greater than 600Ω is used, the distortion performance of the PGA2310 will begin to degrade.



**Figure 1. PGA2310 Block Diagram**

## SERIAL CONTROL PORT

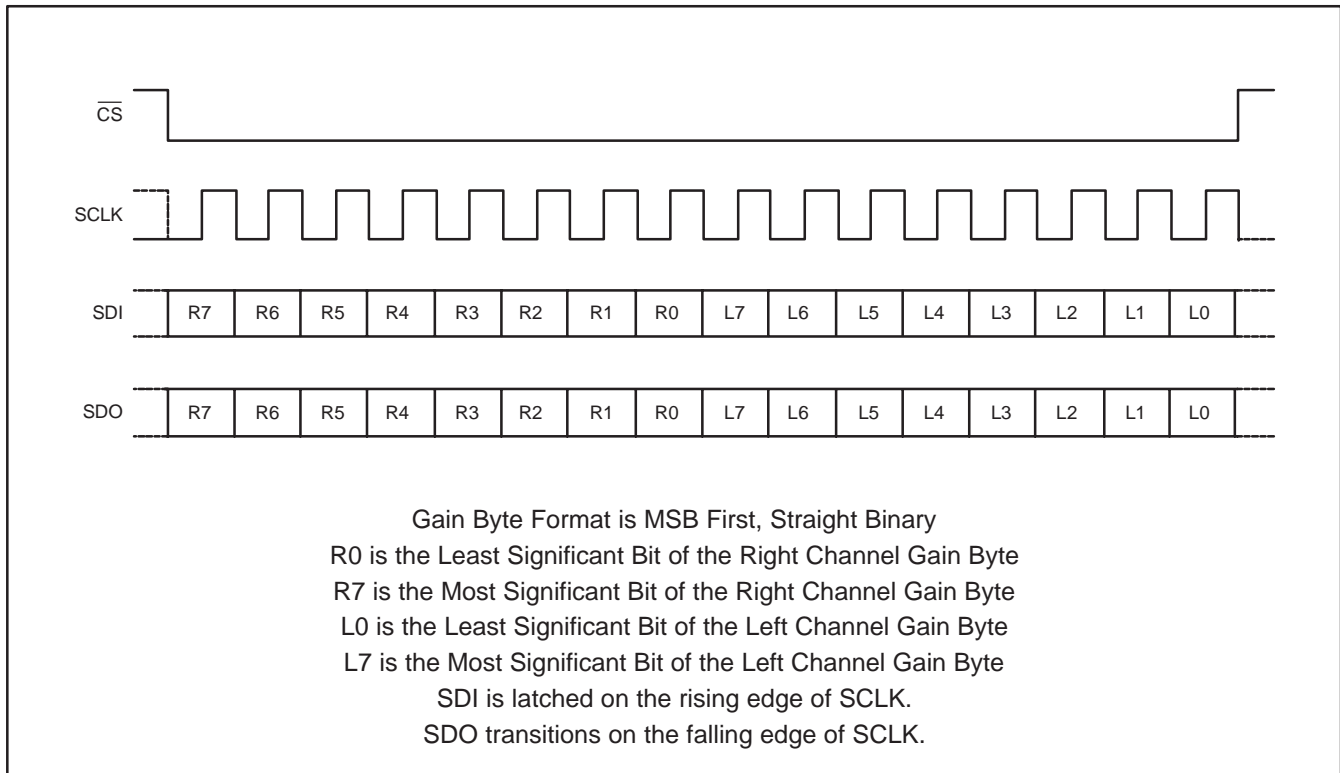
The serial control port is utilized to program the gain settings for the PGA2310. The serial control port includes three input pins and one output pin. The inputs include  $\overline{CS}$  (pin 2), SDI (pin 3), and SCLK (pin 6). The sole output pin is SDO (pin 7).

The  $\overline{CS}$  pin functions as the chip select input. Data may be written to the PGA2310 only when  $\overline{CS}$  is low. SDI is the serial data input pin. Control data is provided as a 16-bit word at the SDI pin, 8 bits each for the left and right channel

gain settings. Data is formatted as MSB first, straight binary code. SCLK is the serial clock input. Data is clocked into SDI on the rising edge of SCLK.

SDO is the serial data output pin, and is used when daisy-chaining multiple PGA2310 devices. Daisy-chain operation is described in detail later in this section. SDO is a tristate output, and assumes a high impedance state when  $\overline{CS}$  is high.

The protocol for the serial control port is shown in Figure 2. See Figure 3 for detailed timing specifications of the serial control port.



**Figure 2. Serial Interface Protocol**



## GAIN SETTINGS

The gain for each channel is set by its corresponding 8-bit code, either R[7:0] or L[7:0], see Figure 2. The gain code data is straight binary format. If we let N equal the decimal equivalent of R[7:0] or L[7:0], then the following relationships exist for the gain settings:

### For N = 0:

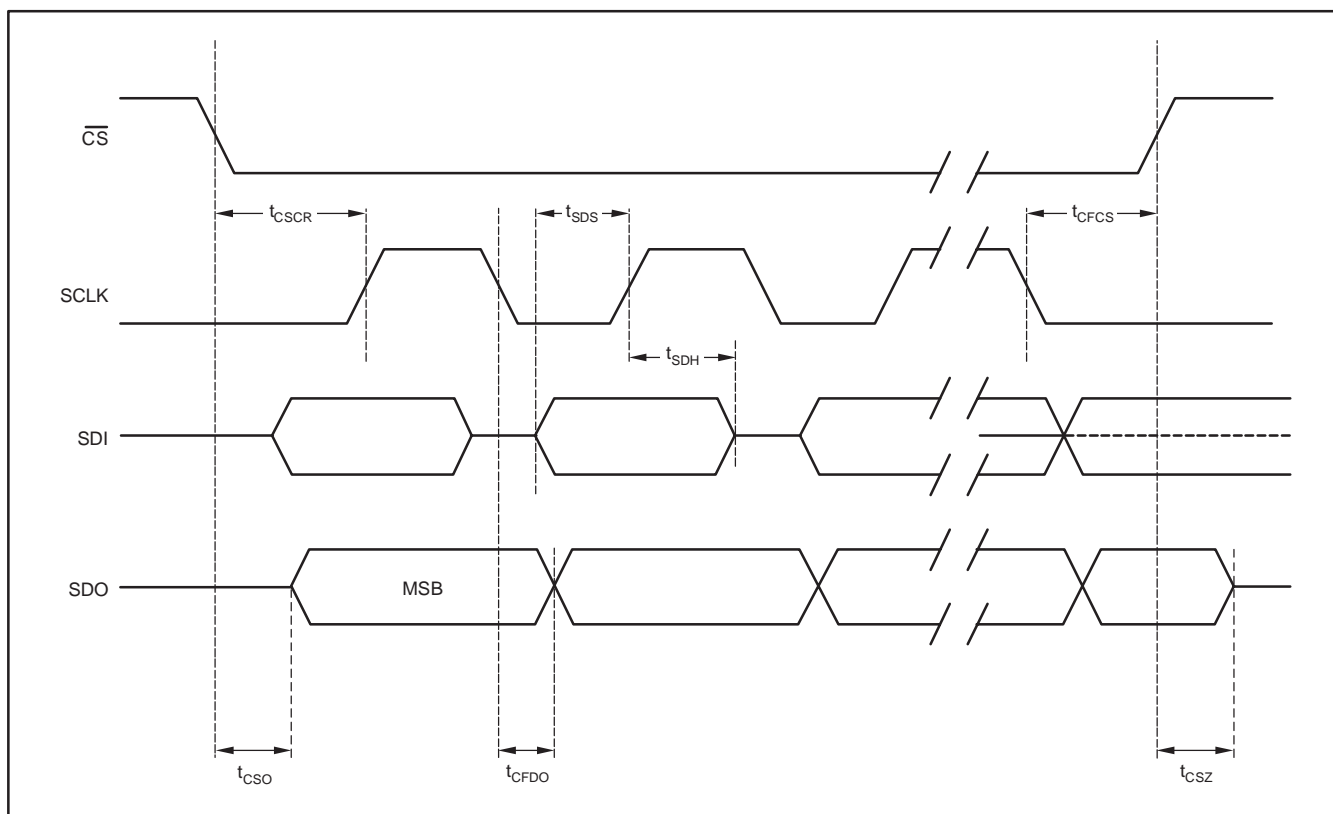
**Mute Condition.** The input multiplexer is connected to analog ground (AGNDR or AGNDL).

### For N = 1 to 255:

$$\text{Gain (dB)} = 31.5 - [0.5 \cdot (255 - N)]$$

This results in a gain range of +31.5dB (with N = 255) to -95.5dB (with N = 1).

Changes in gain setting may be made with or without zero crossing detection. The operation of the zero crossing detector and timeout circuitry is discussed later in this data sheet.



**Figure 3. Serial Interface Timing Requirements**

## DAISY-CHAINING MULTIPLE PGA2310 DEVICES

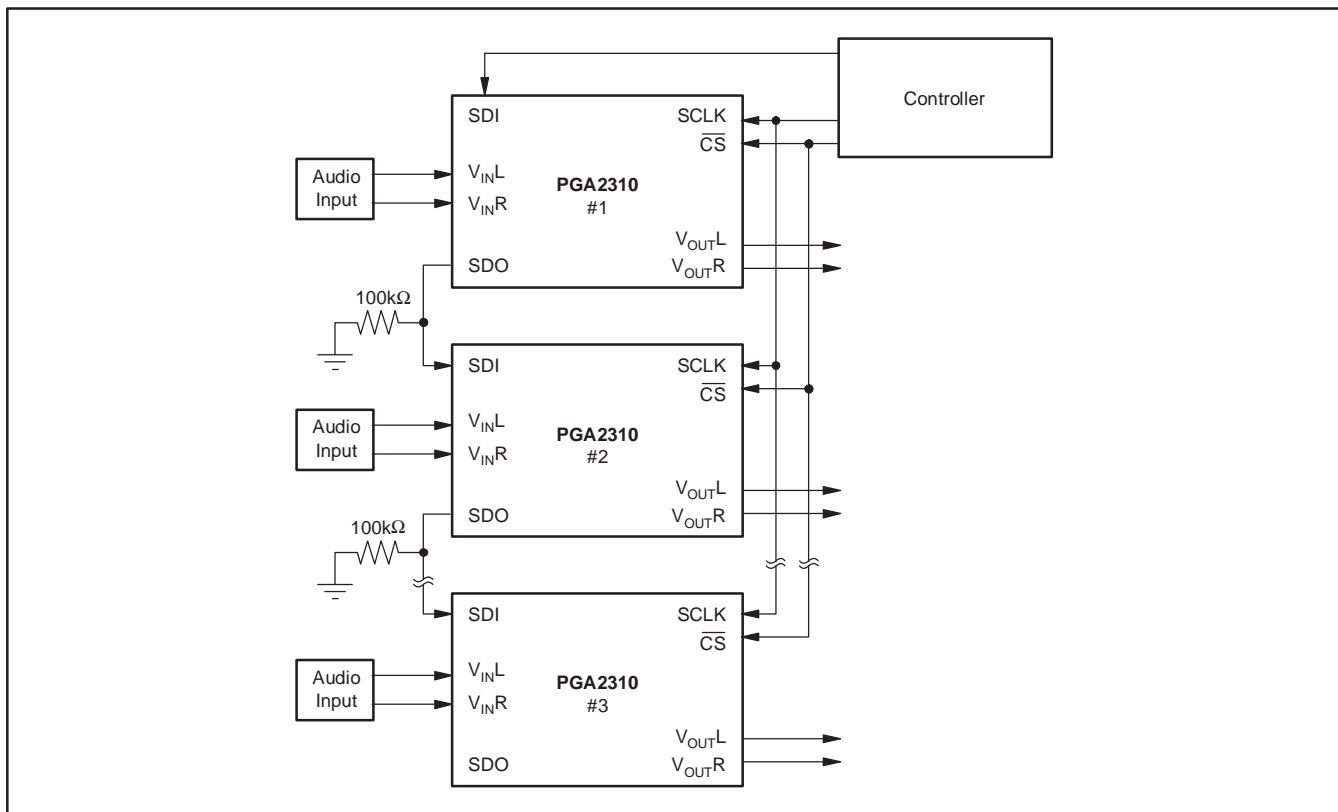
In order to reduce the number of control signals required to support multiple PGA2310 devices on a printed circuit board, the serial control port supports daisy-chaining of multiple PGA2310 devices. Figure 4 shows the connection requirements for daisy-chain operation. This arrangement allows a three-wire serial interface to control many PGA2310 devices.

As shown in Figure 4, the SDO pin from device #1 is connected to the SDI input of device #2, and is repeated for additional devices. This in turn forms a large shift register, in which gain data may be written for all PGA2310s connected to the serial bus. The length of the shift register is  $16 \times N$  bits, where  $N$  is equal to the number of PGA2310s connected to the serial bus. The length of the shift register is  $16 \times N$  bits, where  $N$  is equal to the number of PGA2310 devices included in the chain. The  $\overline{CS}$  input must remain low for  $16 \times N$  SCLK periods, where  $N$  is the number of devices connected in the chain, in order to allow enough SCLK cycles to load all devices.

## ZERO CROSSING DETECTION

The PGA2310 includes a zero crossing detection function that can provide for noise-free level transitions. The concept is to change gain settings on a zero crossing of the input signal, thus minimizing audible glitches. This function is enabled or disabled using the ZCEN input (pin 1). When ZCEN is low, zero crossing detection is disabled. When ZCEN is high, zero crossing detection will be enabled.

The zero crossing detection takes effect with a change in gain setting for a corresponding channel. The new gain setting will not be latched until either two zero crossings are detected, or a timeout period of 16ms has elapsed without detecting two zero crossings. In the case of a timeout, the new gain setting takes effect with no attempt to minimize audible artifacts.



**Figure 4. Daisy-Chaining Multiple PGA2310 Devices**

## MUTE FUNCTION

The PGA2310 includes a mute function. This function may be activated by either the  $\overline{\text{MUTE}}$  input (pin 8), or by setting the gain byte value for one or both channels to 00<sub>HEX</sub>. The  $\overline{\text{MUTE}}$  pin may be used to mute both channels, while the gain setting may be used to selectively mute the left and right channels. Muting is accomplished by switching the input multiplexer to analog ground (AGNDR or AGNDL) with zero crossing enabled.

The  $\overline{\text{MUTE}}$  pin is active low. When  $\overline{\text{MUTE}}$  is low, each channel will be muted following the next zero crossing event or timeout that occurs on that channel. If  $\overline{\text{MUTE}}$  becomes active while  $\overline{\text{CS}}$  is also active, the mute will take effect once the  $\overline{\text{CS}}$  pin goes high. When the  $\overline{\text{MUTE}}$  pin is high, the PGA2310 operates normally, with the mute function disabled.

## APPLICATIONS INFORMATION

This section includes additional information that is pertinent to designing the PGA2310 into an end application.

### RECOMMENDED CONNECTION DIAGRAM

Figure 5 depicts the recommended connections for the PGA2310. Power-supply bypass capacitors should be placed as close to the PGA2310 package as physically possible.

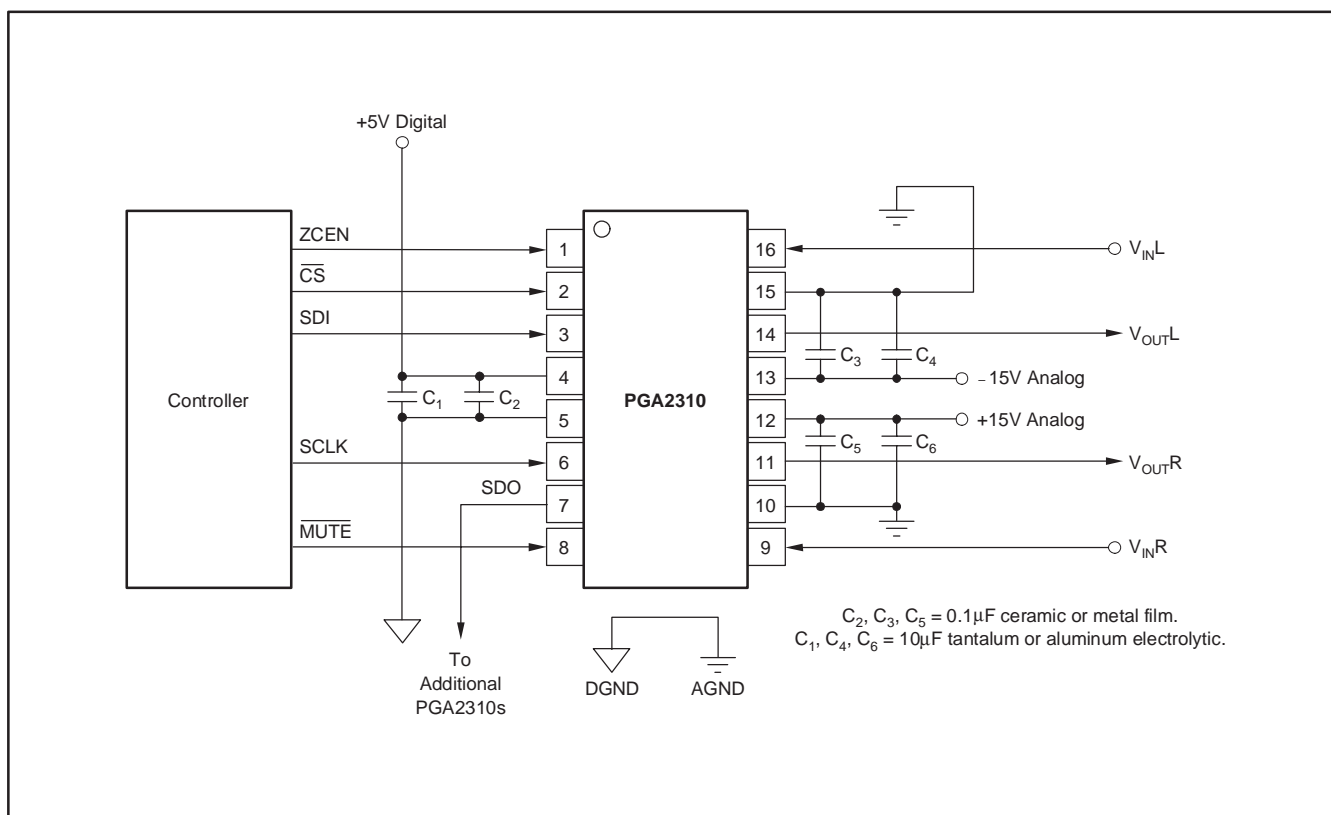


Figure 5. Recommended Connection Diagram

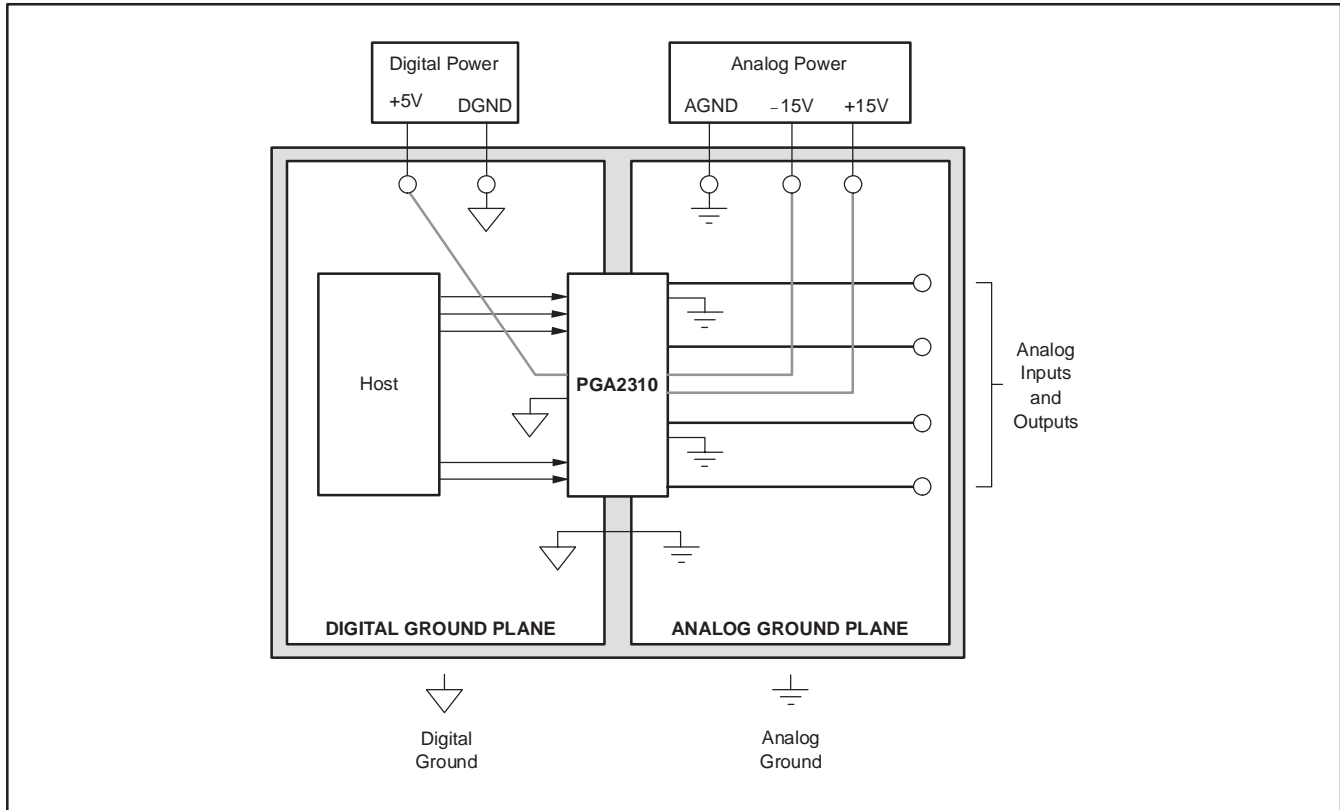
# PGA2310

SBOS207B – OCTOBER 2001 – REVISED JUNE 2004

## PRINTED CIRCUIT BOARD LAYOUT GUIDELINES

It is recommended that the ground planes for the digital and analog sections of the printed circuit board (PCB) be separate from one another. The planes should be connected at a single point. Figure 6 shows the recommended PCB floor plan for the PGA2310.

The PGA2310 is mounted so that it straddles the split between the digital and analog ground planes. Pins 1 through 8 are oriented to the digital side of the board, while pins 9 through 16 are on the analog side of the board.



**Figure 6. Typical PCB Layout Floor Plan**

## PACKAGING INFORMATION

ORDERABLE DEVICE	STATUS(1)	PACKAGE TYPE	PACKAGE DRAWING	PINS	PACKAGE QTY
PGA2310PA	ACTIVE	PDIP	N	16	25
PGA2310UA	ACTIVE	SOIC	DW	16	48
PGA2310UA/1K	ACTIVE	SOIC	DW	16	1000

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

---

N (R-PDIP-T\*\*)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN

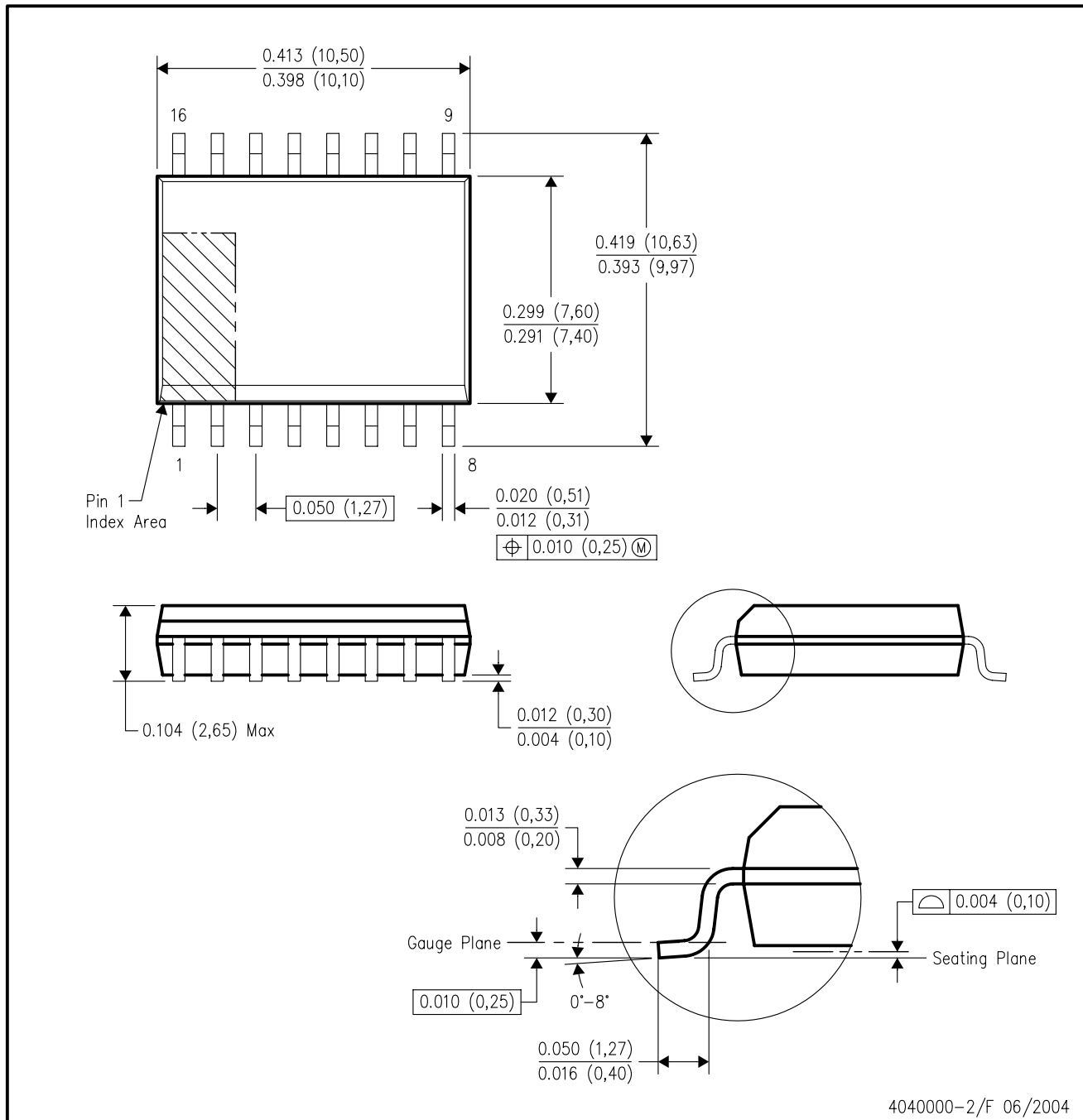


- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - $\triangle C$  Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
  - $\triangle D$  The 20 pin end lead shoulder width is a vendor option, either half or full width.

4040049/E 12/2002

DW (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040000-2/F 06/2004

- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-013 variation AA.

## IMPORTANT NOTICE

Texas Instruments Incorporated and its subsidiaries (TI) reserve the right to make corrections, modifications, enhancements, improvements, and other changes to its products and services at any time and to discontinue any product or service without notice. Customers should obtain the latest relevant information before placing orders and should verify that such information is current and complete. All products are sold subject to TI's terms and conditions of sale supplied at the time of order acknowledgment.

TI warrants performance of its hardware products to the specifications applicable at the time of sale in accordance with TI's standard warranty. Testing and other quality control techniques are used to the extent TI deems necessary to support this warranty. Except where mandated by government requirements, testing of all parameters of each product is not necessarily performed.

TI assumes no liability for applications assistance or customer product design. Customers are responsible for their products and applications using TI components. To minimize the risks associated with customer products and applications, customers should provide adequate design and operating safeguards.

TI does not warrant or represent that any license, either express or implied, is granted under any TI patent right, copyright, mask work right, or other TI intellectual property right relating to any combination, machine, or process in which TI products or services are used. Information published by TI regarding third-party products or services does not constitute a license from TI to use such products or services or a warranty or endorsement thereof. Use of such information may require a license from a third party under the patents or other intellectual property of the third party, or a license from TI under the patents or other intellectual property of TI.

Reproduction of information in TI data books or data sheets is permissible only if reproduction is without alteration and is accompanied by all associated warranties, conditions, limitations, and notices. Reproduction of this information with alteration is an unfair and deceptive business practice. TI is not responsible or liable for such altered documentation.

Resale of TI products or services with statements different from or beyond the parameters stated by TI for that product or service voids all express and any implied warranties for the associated TI product or service and is an unfair and deceptive business practice. TI is not responsible or liable for any such statements.

Following are URLs where you can obtain information on other Texas Instruments products and application solutions:

<b>Products</b>		<b>Applications</b>	
Amplifiers	<a href="http://amplifier.ti.com">amplifier.ti.com</a>	Audio	<a href="http://www.ti.com/audio">www.ti.com/audio</a>
Data Converters	<a href="http://dataconverter.ti.com">dataconverter.ti.com</a>	Automotive	<a href="http://www.ti.com/automotive">www.ti.com/automotive</a>
DSP	<a href="http://dsp.ti.com">dsp.ti.com</a>	Broadband	<a href="http://www.ti.com/broadband">www.ti.com/broadband</a>
Interface	<a href="http://interface.ti.com">interface.ti.com</a>	Digital Control	<a href="http://www.ti.com/digitalcontrol">www.ti.com/digitalcontrol</a>
Logic	<a href="http://logic.ti.com">logic.ti.com</a>	Military	<a href="http://www.ti.com/military">www.ti.com/military</a>
Power Mgmt	<a href="http://power.ti.com">power.ti.com</a>	Optical Networking	<a href="http://www.ti.com/opticalnetwork">www.ti.com/opticalnetwork</a>
Microcontrollers	<a href="http://microcontroller.ti.com">microcontroller.ti.com</a>	Security	<a href="http://www.ti.com/security">www.ti.com/security</a>
		Telephony	<a href="http://www.ti.com/telephony">www.ti.com/telephony</a>
		Video & Imaging	<a href="http://www.ti.com/video">www.ti.com/video</a>
		Wireless	<a href="http://www.ti.com/wireless">www.ti.com/wireless</a>

Mailing Address: Texas Instruments  
Post Office Box 655303 Dallas, Texas 75265