# S-24C16C (WLP PRODUCT)

www.ablic.com

## 2-WIRE SERIAL E$^2$PROM

© ABLIC Inc., 2016

Rev.1.0_01_H

The S-24C16C is a 2-wire, low current consumption and wide range operation serial E$^2$PROM. The S-24C16C has the capacity of 16 K-bit, and the organization is 2048 words × 8-bit. Page write and sequential read are available.

**Caution This product is intended to use in general electronic devices such as consumer electronics, office equipment, and communications devices. Before using the product in medical equipment or automobile equipment including car audio, keyless entry and engine control unit, contact to ABLIC Inc. is indispensable.**

## ■ Features

- Operating voltage range — Read: 1.6 V to 5.5 V; Write: 1.7 V to 5.5 V
- Page write: 16 bytes / page
- Sequential read
- Operation frequency: 400 kHz (1.6 V to 5.5 V)
- Write time: 5.0 ms max.
- Noise suppression: Schmitt trigger and noise filter on input pins (SCL, SDA)
- Write protect function during the low power supply voltage
- Endurance: $10^6$cycles / word[*1] (Ta = +25°C)
- Data retention: 100 years (Ta = +25°C)
- Memory capacity: 16 K-bit
- Write protect: 100%
- Initial delivery data: FFh
- Lead-free, halogen-free

***1.** For each address (Word: 8-bit)

## ■ Package

- WLP-6J

## ■ Pin Configuration

### 1. WLP-6J

WLP-6J
Bottom view

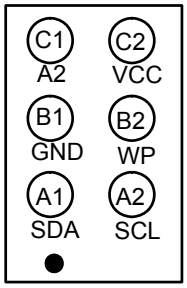



**Figure 1**

S-24C16CI-H6T3S3

**Table 1**

| Pin No | Symbol | Description |
|---|---|---|
| A1 | SDA*2 | Serial data I/O |
| A2 | SCL*2 | Serial clock input |
| B1 | GND | Ground |
| B2 | WP | Write protect input<br>Connected to $V_{CC}$: Protection valid<br>Open or connected to GND: Protection invalid |
| C1 | A2*1 | TEST pin |
| C2 | VCC | Power supply |

***1.** Connect to GND.
***2.** Do not use it in high impedance.

**Remark** Refer to the "**Package drawings**" for the details.

## ■ Block Diagram

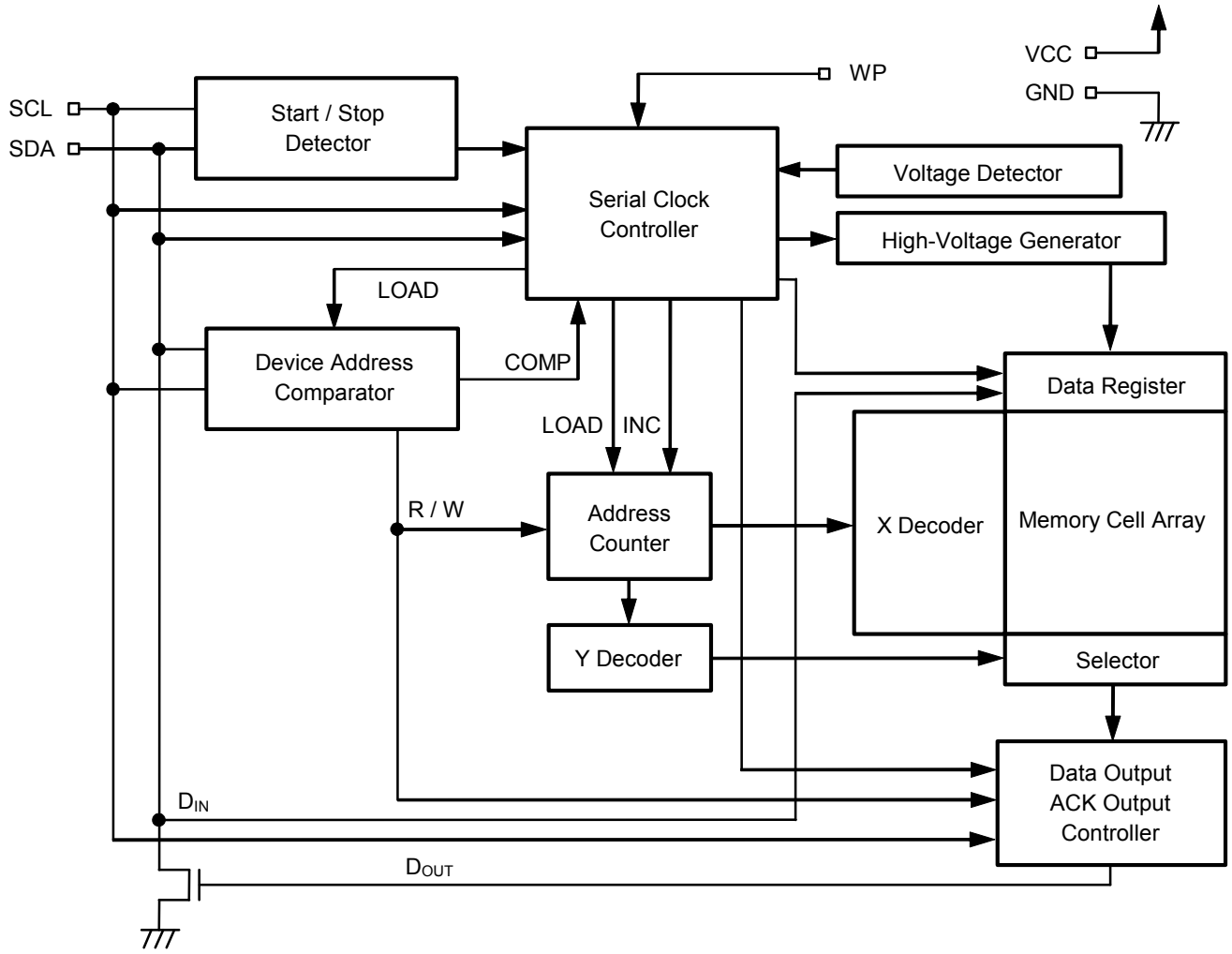



**Figure 2**

## ■ Absolute Maximum Ratings

**Table 2**

| Item | Symbol | Absolute Maximum Ratings | Unit |
|---|---|---|---|
| Power supply voltage | $V_{CC}$ | −0.3 to +6.5 | V |
| Input voltage | $V_{IN}$ | −0.3 to +6.5 | V |
| Output voltage | $V_{OUT}$ | −0.3 to +6.5 | V |
| Operation ambient temperature | $T_{opr}$ | −40 to +85 | °C |
| Storage temperature | $T_{stg}$ | −65 to +150 | °C |

**Caution The absolute maximum ratings are rated values exceeding which the product could suffer physical damage. These values must therefore not be exceeded under any conditions.**

## ■ Recommended Operating Conditions

**Table 3**

| Item | Symbol | Condition | Ta = −40°C to +85°C | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| Power supply voltage | $V_{CC}$ | Read | 1.6 | 5.5 | V |
| | | Write | 1.7 | 5.5 | V |
| High level input voltage | $V_{IH}$ | $V_{CC}$ = 1.6 V to 5.5 V | 0.7 × $V_{CC}$ | 5.5 | V |
| Low level input voltage | $V_{IL}$ | $V_{CC}$ = 1.6 V to 5.5 V | −0.3 | 0.3 × $V_{CC}$ | V |

## ■ Pin Capacitance

**Table 4**

(Ta = +25°C, f = 1.0 MHz, $V_{CC}$ = 5.0 V)

| Item | Symbol | Condition | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Input capacitance | $C_{IN}$ | $V_{IN}$ = 0 V (SCL, A2, WP) | − | 10 | pF |
| I/O capacitance | $C_{I/O}$ | $V_{I/O}$ = 0 V (SDA) | − | 10 | pF |

## ■ Endurance

**Table 5**

| Item | Symbol | Operation Ambient Temperature | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Endurance | $N_W$ | Ta = +25°C | $10^6$ | − | cycles / word*1 |

***1.** For each address (Word: 8 bits)

## ■ Data Retention

**Table 6**

| Item | Symbol | Operation Ambient Temperature | Min. | Max. | Unit |
|---|---|---|---|---|---|
| Data retention | − | Ta = +25°C | 100 | − | year |

## ■ DC Electrical Characteristics

**Table 7**

| Item | Symbol | Condition | Ta = –40°C to +85°C<br>$V_{CC}$ = 1.6 V to 5.5 V<br>$f_{SCL}$ = 400 kHz | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| Current consumption (READ) | $I_{CC1}$ | – | – | 0.8 | mA |

**Table 8**

| Item | Symbol | Condition | Ta = –40°C to +85°C<br>$V_{CC}$ = 1.7 V to 5.5 V<br>$f_{SCL}$ = 400 kHz | | Unit |
|---|---|---|---|---|---|
| | | | Min. | Max. | |
| Current consumption (WRITE) | $I_{CC2}$ | – | – | 2.5 | mA |

**Table 9**

| Item | Symbol | Condition | Ta = –40°C to +85°C | | | | | | Unit |
|---|---|---|---|---|---|---|---|---|---|
| | | | $V_{CC}$ = 2.5 V to 5.5 V | | $V_{CC}$ = 1.8 V to 5.5 V | | $V_{CC}$ = 1.6 V to 1.8 V | | |
| | | | Min. | Max. | Min. | Max. | Min. | Max. | |
| Standby current consumption | $I_{SB}$ | $V_{IN}$ = $V_{CC}$ or GND | – | 3.5 | – | 3.5 | – | 2.0 | μA |
| Input leakage current 1 | $I_{LI1}$ | SCL, SDA, A2<br>$V_{IN}$ = GND to $V_{CC}$ | – | 1.0 | – | 1.0 | – | 1.0 | μA |
| Output leakage current | $I_{LO}$ | SDA<br>$V_{OUT}$ = GND to $V_{CC}$ | – | 1.0 | – | 1.0 | – | 1.0 | μA |
| Input current 1 | $I_{IL}$ | WP<br>$V_{IN}$ < 0.3 × $V_{CC}$ | – | 50.0 | – | 50.0 | – | 50.0 | μA |
| Input current 2 | $I_{IH}$ | WP<br>$V_{IN}$ > 0.7 × $V_{CC}$ | – | 2.0 | – | 2.0 | – | 2.0 | μA |
| Input Impedance 1 | $Z_{IL}$ | WP<br>$V_{IN}$ = 0.3 × $V_{CC}$ | 30 | – | 30 | – | 30 | – | kΩ |
| Input Impedance 2 | $Z_{IH}$ | WP<br>$V_{IN}$ = 0.7 × $V_{CC}$ | 500 | – | 500 | – | 500 | – | kΩ |
| Low level output voltage | $V_{OL}$ | $I_{OL}$ = 3.2 mA | – | 0.4 | – | – | – | – | V |
| | | $I_{OL}$ = 1.5 mA | – | 0.3 | – | 0.3 | – | 0.3 | V |
| | | $I_{OL}$ = 0.7 mA | – | 0.2 | – | 0.2 | – | 0.2 | V |

## ■ AC Electrical Characteristics

**Table 10 Measurement Conditions**

| | |
|---|---|
| Input pulse voltage | $0.2 \times V_{CC}$ to $0.8 \times V_{CC}$ |
| Input pulse rising / falling time | 20 ns or less |
| Output reference voltage | $0.3 \times V_{CC}$ to $0.7 \times V_{CC}$ |
| Output load | 100 pF |

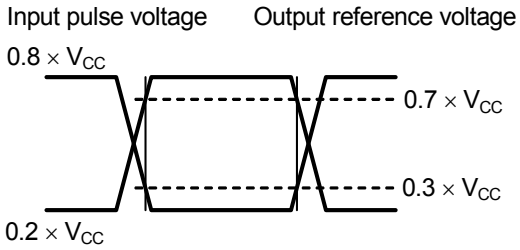



**Figure 3 I/O Waveform during AC Measurement**

**Table 11**

| Item | Symbol | Ta = −40°C to +85°C, $V_{CC}$ = 1.6 V to 5.5 V | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| SCL clock frequency | $f_{SCL}$ | 0 | 400 | kHz |
| SCL clock time "L" | $t_{LOW}$ | 1.3 | – | µs |
| SCL clock time "H" | $t_{HIGH}$ | 0.6 | – | µs |
| SDA output delay time | $t_{AA}$ | 0.1 | 0.9 | µs |
| SDA output hold time | $t_{DH}$ | 50 | – | ns |
| Start condition setup time | $t_{SU.STA}$ | 0.6 | – | µs |
| Start condition hold time | $t_{HD.STA}$ | 0.6 | – | µs |
| Data input setup time | $t_{SU.DAT}$ | 100 | – | ns |
| Data input hold time | $t_{HD.DAT}$ | 0 | – | ns |
| Stop condition setup time | $t_{SU.STO}$ | 0.6 | – | µs |
| SCL, SDA rising time | $t_R$ | – | 0.3 | µs |
| SCL, SDA falling time | $t_F$ | – | 0.3 | µs |
| WP setup time | $t_{WS1}$ | 0 | – | µs |
| WP hold time | $t_{WH1}$ | 0 | – | µs |
| WP release setup time | $t_{WS2}$ | 0 | – | µs |
| WP release hold time | $t_{WH2}$ | 0 | – | µs |
| Bus release time | $t_{BUF}$ | 1.3 | – | µs |
| Noise suppression time | $t_I$ | – | 50 | ns |

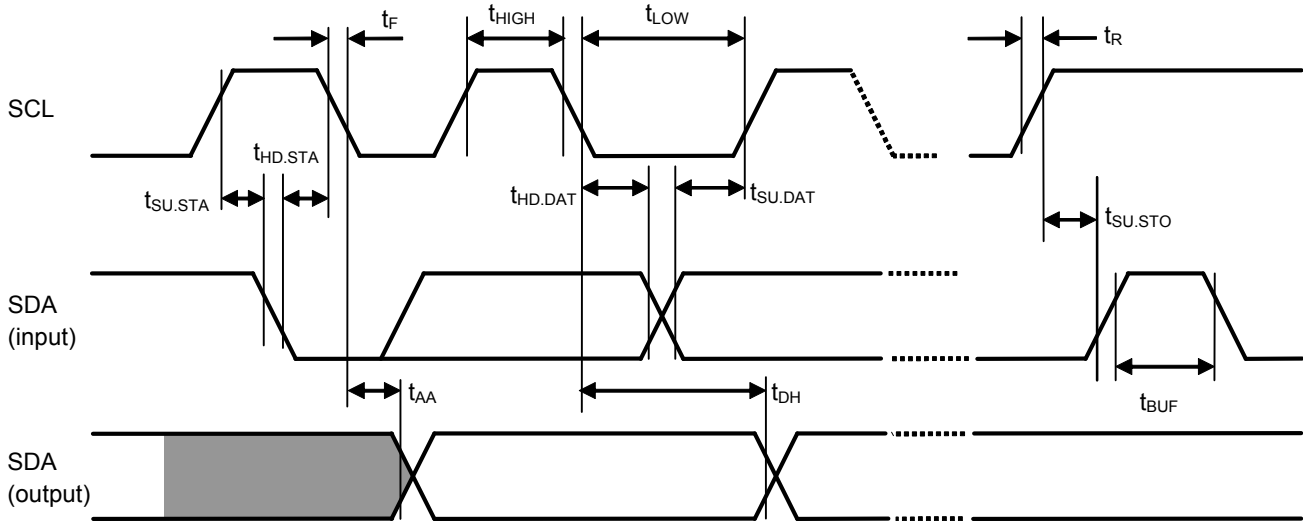



**Figure 4 Bus Timing**

**Table 12**

| Item | Symbol | Ta = –40°C to +85°C<br>$V_{CC}$ = 1.7 V to 5.5 V | | Unit |
|---|---|---|---|---|
| | | Min. | Max. | |
| Write time | $t_{WR}$ | – | 5.0 | ms |

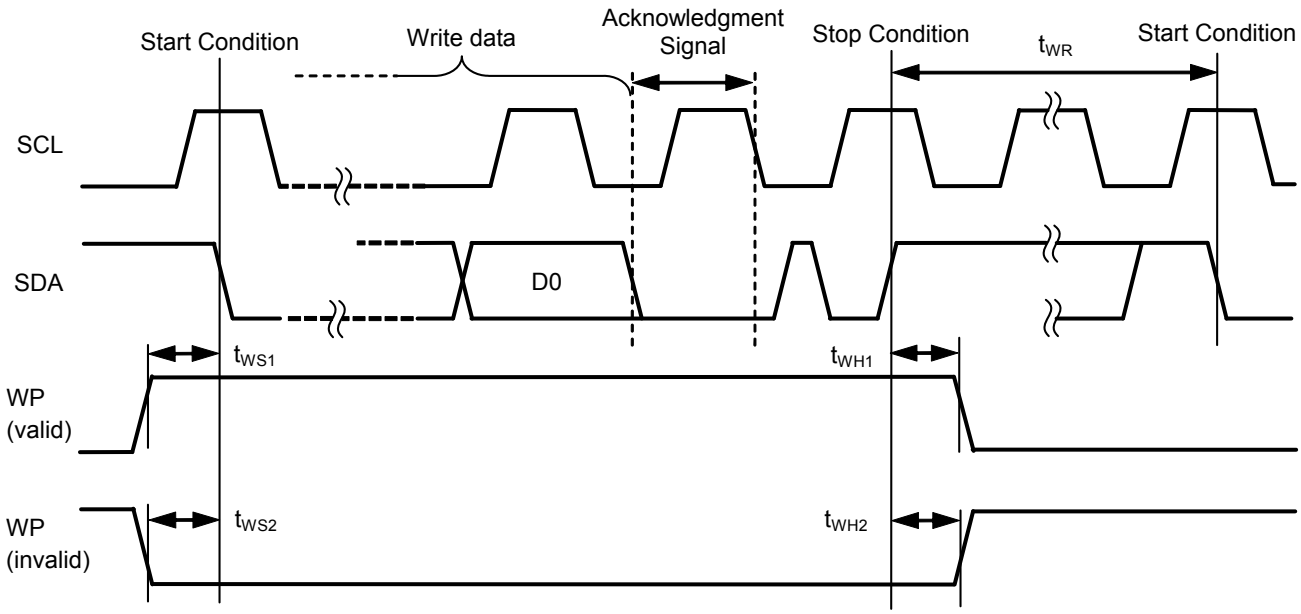



**Figure 5 Write Cycle Timing**

## ■ Pin Functions

### 1. A2 (Test) pin

The slave address can not be assigned in the S-24C16C since addressing function is removed.
The A2 pin should be connected to the GND.

### 2. SDA (Serial data input / output) pin

The SDA pin is used for the bi-directional transmission of serial data. This pin is a signal input pin, and an Nch open drain output pin.
In use, generally, connect the SDA line to any other device which has the open-drain or open-collector output with Wired-OR connection by pulling up to $V_{CC}$ by a resistor (**Figure 6** shows the relation with an output load).

### 3. SCL (Serial clock input) pin

The SCL pin is used for the serial clock input. Since the signals are processed at a rising or falling edge of the SCL clock, pay attention to the rising and falling time and comply with the specification.

### 4. WP (Write protect input) pin

The write protect is enabled by connecting the WP pin to $V_{CC}$. When not using the write protect, connect this pin to GND or set in open.

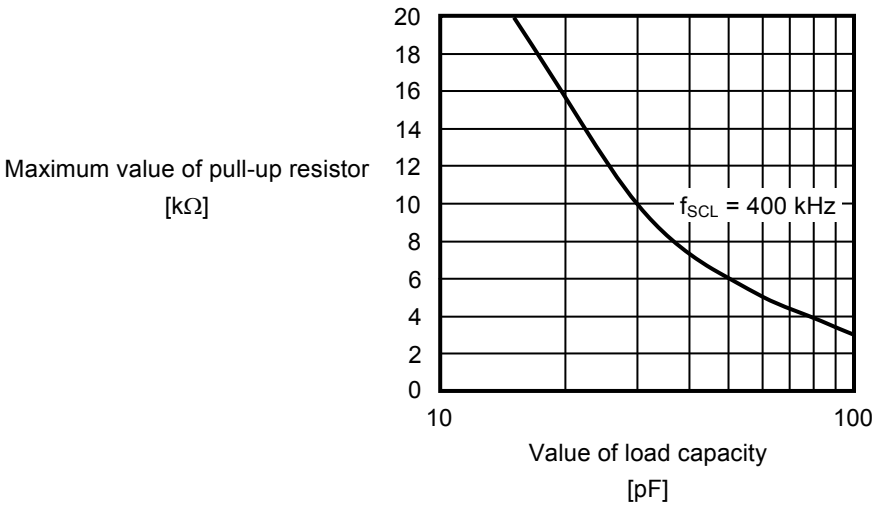



**Figure 6 Output Load**

## ■ Initial Delivery Data

Initial delivery data of all addresses is “FFh”.

## ■ Operation

### 1. Start condition

Start is identified by a high to low transition of the SDA line while the SCL line is stable at high.
Every operation begins from a start condition.

### 2. Stop condition

Stop is identified by a low to high transition of the SDA line while the SCL line is stable at high.
When a device receives a stop condition during a read sequence, the read operation is interrupted, and the device enters standby mode.
When a device receives a stop condition during a write sequence, the reception of the write data is halted, and the S-24C16C initiates a write cycle.

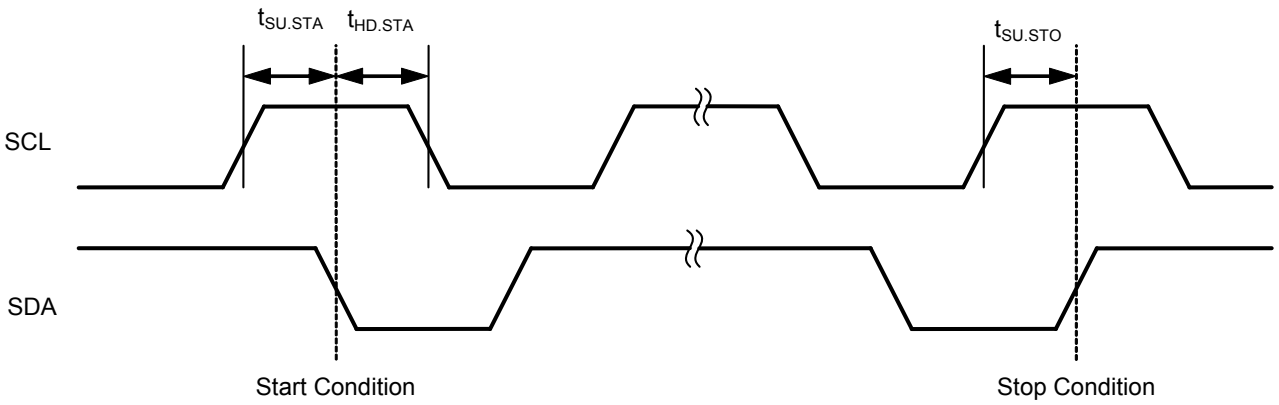



**Figure 7 Start / Stop Conditions**

### 3. Data transmission

Changing the SDA line while the SCL line is low, data is transmitted.
Changing the SDA line while the SCL line is high, a start or stop condition is recognized.

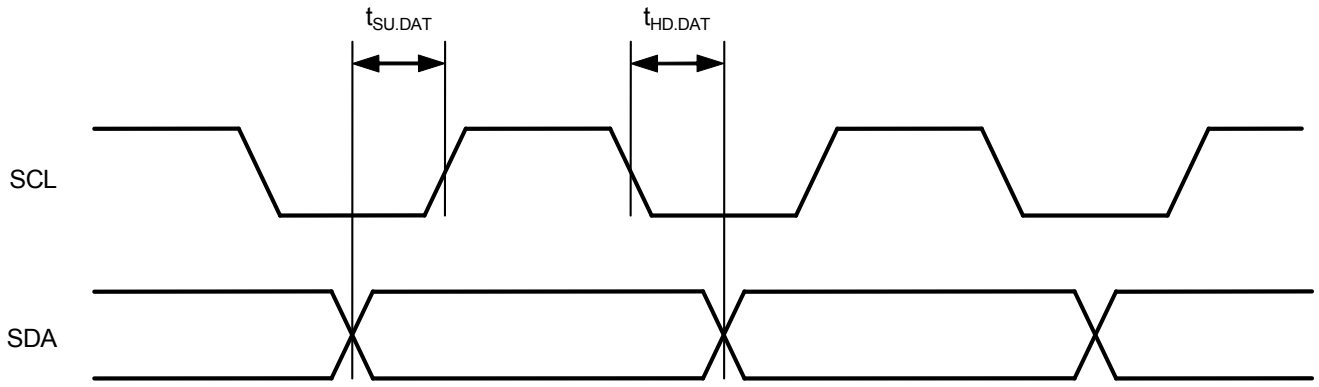



**Figure 8 Data Transmission Timing**

### 4. Acknowledge

The unit of data transmission is 8 bits. During the 9th clock cycle period the receiver on the bus pulls down the SDA line to acknowledge the receipt of the 8-bit data.
When an internal write cycle is in progress, the device does not generate an acknowledge.

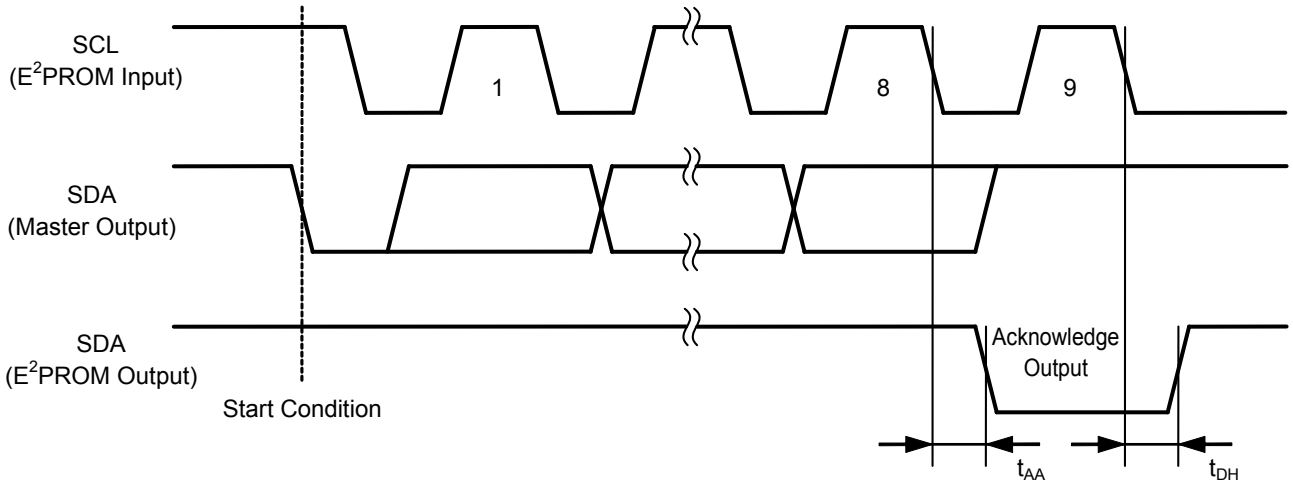



**Figure 9 Acknowledge Output Timing**

## 5. Device addressing

To start communication, the master device on the system generates a start condition to the bus line. Next, the master device sends 7-bit device address and a 1-bit read / write instruction code on to the SDA bus.
The upper 4 bits of the device address are the “Device Code”, and are fixed to “1010”.

In the S-24C16C, successive 3 bits (P2, P1, P0) are “Page Address”. Choose the 8 memory blocks of 256-byte (Adress 000h to 0FFh, 100h to 1FFh, 200h to 2FFh, 300h to 3FFh, 400h to 4FFh, 500h to 5FFh, 600h to 6FFh, and 700h to 7FFh).

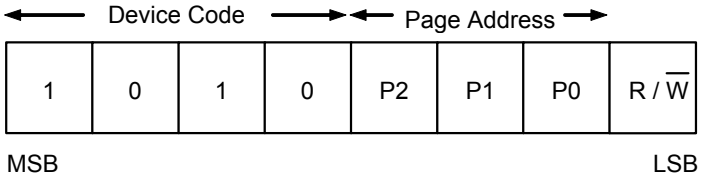



**Figure 10 Device Address**

## 6. Write

### 6. 1 Byte write

When the master sends a 7-bit device address and a 1-bit read / write instruction code set to “0”, following a start condition, the S-24C16C acknowledges it. And the S-24C16C receives 8-bit word address and responds with an acknowledge. After the S-24C16C receives 8-bit write data and responds with an acknowledge, it receives a stop condition and that initiates the write cycle at the addressed memory.
During the write cycle all operations are forbidden and no acknowledge is generated.

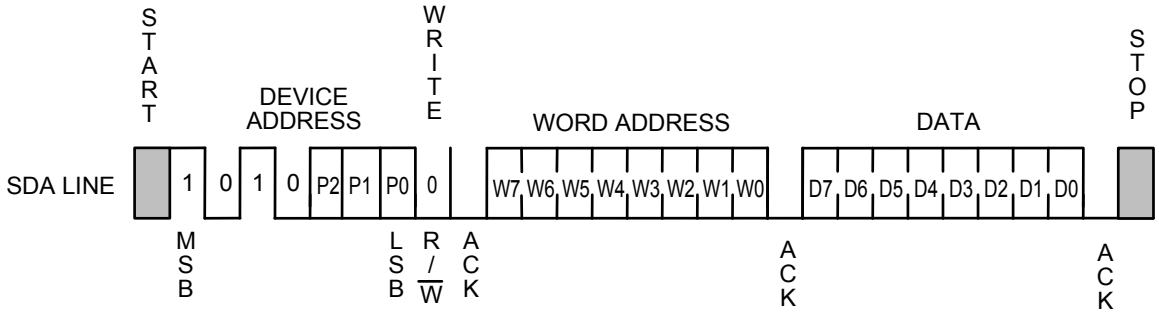



**Figure 11 Byte Write**

### 6. 2 Page write

The page write mode allows up to 16 bytes to be written in a single write operation in the S-24C16C.
Its basic process to transmit data is as same as byte write, but it operates page write by sequentially receiving 8-bit write data as much data as the page size has.
When the S-24C16C receives a 7-bit device address and a 1-bit read / write instruction code set to “0”, following a start condition, it generates an acknowledge. And the S-24C16C receives 8-bit word address and responds with an acknowledge. After the S-24C16C receives 8-bit write data and responds with an acknowledge, it receives 8-bit write data corresponding to the next word address, and generates an acknowledge. The S-24C16C repeats reception of 8-bit write data and generation of acknowledge in succession. The S-24C16C can receive as many write data as the maximum page size.
Receiving a stop condition initiates a write cycle of the area starting from the designated memory address and having the page size equal to the received write data.

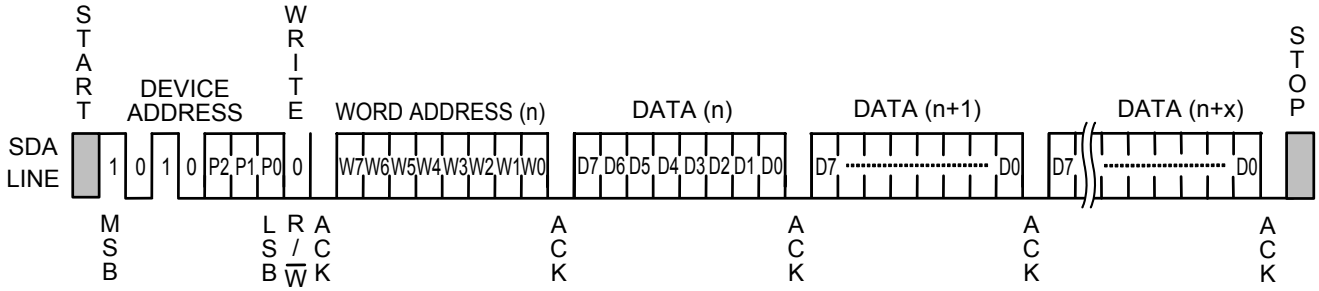



**Figure 12 Page Write**

In the S-24C16C, the lower 4 bits of the word address are automatically incremented every time when the S-24C16C receives 8-bit write data. If the size of the write data exceeds 16 bytes, the upper 4 bits of the word address and page address (P2, P1, P0) remain unchanged, and the lower 4 bits are rolled over and the last 16-byte data that the S-24C16C received will be overwritten.

### 6. 3 Write protect

Write protect is available in the S-24C16C. When the WP pin is connected to the $V_{CC}$, write operation to memory area is inhibited.
When the WP pin is connected to GND or set in open, the write protect is invalid, and write operation in all memory area is available.
Fix the level of the WP pin from start condition in the write operation (byte write, page write) until stop condition. If the WP pin changes during this time, the address data being written at this time is not guaranteed. Regarding the timing of write protect, refer to **Figure 5**.
In not using the write protect, connect the WP pin to GND or set it open. The write protect is valid in the range of operation power supply voltage.
As seen in **Figure 13** when the write protect is valid, the S-24C16C does not generate an acknowledgment signal after data input.

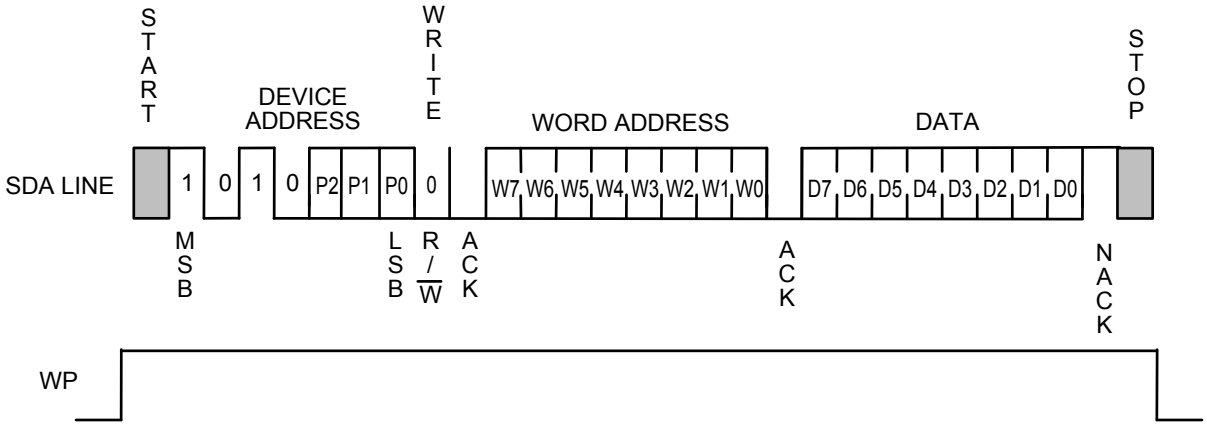
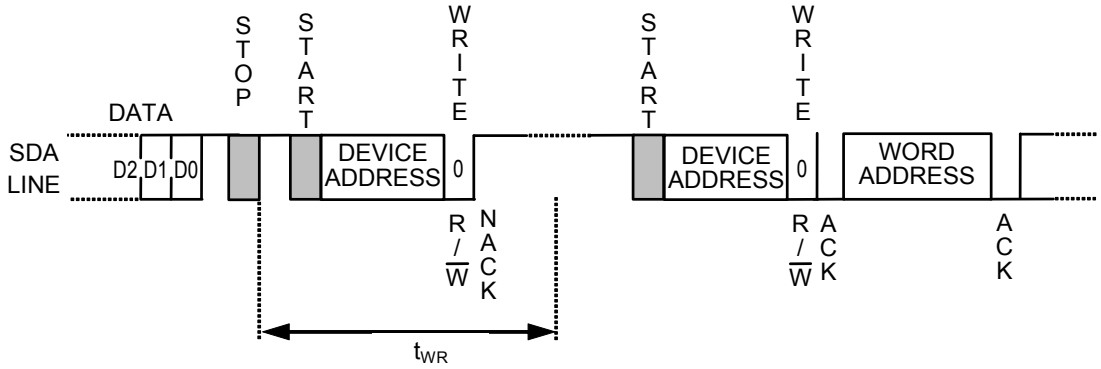



**Figure 13 Write Protect**

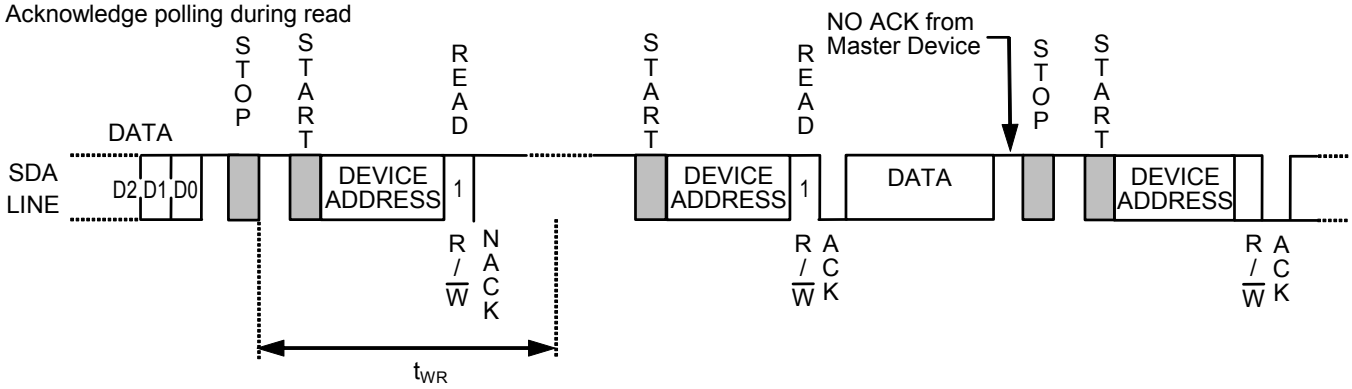
### 6. 4 Acknowledge polling

Acknowledge polling is used to know the completion of the write cycle in the S-24C16C.
After the S-24C16C receives a stop condition and once starts the write cycle, all operations are inhibited and no response is made to the signal transmitted by the master device.
Accordingly the master device can recognize the completion of the write cycle in the S-24C16C by detecting a response from the slave device after transmitting the start condition, the device address and the read / write instruction code to the S-24C16C (slave device).
That is, if the S-24C16C does not generate an acknowledgment signal, the write cycle is in progress and if the S-24C16C generates an acknowledgment signal, the write cycle has been completed.
It is recommended to use the read instruction "1" as the read / write instruction code transmitted by the master device.

Acknowledge polling during write




Acknowledge polling during read




**Remark** Users are able to input word address and data after ACK output in acknowledge polling during write.
Users are able to read data after ACK output in acknowledge polling during read. However, after that users input the write instruction, a start condition may not be input during data output. Input a stop condition and the next instruction after data output and ACK output.

**Figure 14 Usage Example of Acknowledge Polling**

## 7. Read

### 7. 1 Current address read

Either in writing or in reading the S-24C16C holds the last accessed memory address. The memory address is maintained as long as the power voltage does not decrease less than the operating voltage.
The master device can read the data at the memory address of the current address pointer without assigning the word address as a result, when it recognizes the position of the address pointer in the S-24C16C. This is called "Current Address Read".
In the following the address counter in the S-24C16C is assumed to be "n".
When the S-24C16C receives a 7-bit device address and a 1-bit read / write instruction code set to "1" following a start condition, it responds with an acknowledge.
Next, an 8-bit data at the address "n" is sent from the S-24C16C synchronous to the SCL clock. The address counter is incremented and the content of the address counter becomes n+1.
The master device outputs stop condition not an acknowledge, the reading of S-24C16C is ended.

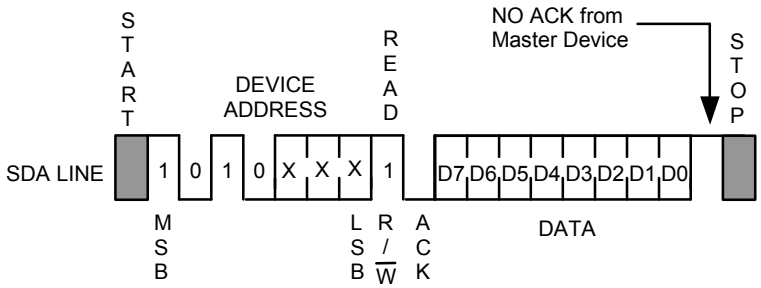



**Figure 15 Current Address Read**

Attention should be paid to the following point on the recognition of the address pointer in the S-24C16C.
In Read, the memory address counter in the S-24C16C is automatically incremented after output of the 8th bit of the data. In Write, on the other hand, the upper bits of the memory address (the upper bits of the word address and the page address[*1]) are left unchanged and are not incremented.

***1.** S-24C16C is the upper 4bits of the word address and the page address P2, P1 and P0.

### 7. 2 Random read

Random read is used to read the data at an arbitrary memory address.
A dummy write is performed to load the memory address into the address counter.
When the S-24C16C receives a 7-bit device address and a 1-bit read / write instruction code set to “0” following a start condition, it responds with an acknowledge.
And the S-24C16C receives 8-bit word address and responds with an acknowledge. The memory address is loaded to the address counter in the S-24C16C by these operations. Reception of write data does not follow in a dummy write whereas reception of write data follows in byte write and in page write.
Since the memory address is loaded into the memory address counter by dummy write, the master device can read the data starting from the arbitrary memory address by transmitting a new start condition and performing the same operation in the current address read.
That is, when the S-24C16C receives a 7-bit device address and a 1-bit read / write instruction code set to “1”, following a start condition signal, it responds with an acknowledge. Next, 8-bit data is transmitted from the S-24C16C in synchronous to the SCL clock. The master device outputs stop condition not an acknowledge, the reading of S-24C16C is ended.

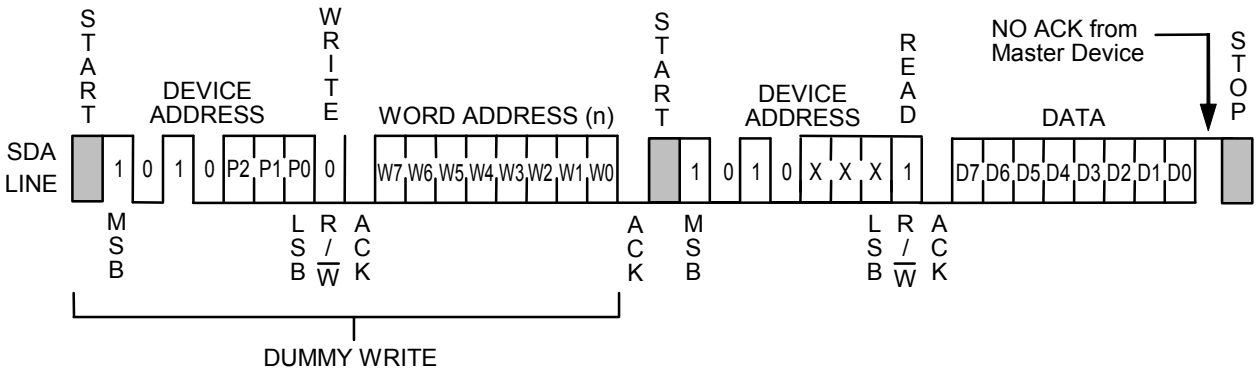



**Figure 16 Random Read**

### 7. 3 Sequential read

When the S-24C16C receives a 7-bit device address and a 1-bit read / write instruction code set to “1” following a start condition both in current address read and random read, it responds with an acknowledge.
When an 8-bit data is output from the S-24C16C synchronous to the SCL clock, the address counter is automatically incremented.
When the master device responds with an acknowledge, the data at the next memory address is transmitted. Response with an acknowledge by the master device has the memory address counter in the S-24C16C incremented and makes it possible to read data in succession. This is called “Sequential Read”.
The master device outputs stop condition not an acknowledge, the reading of S-24C16C is ended.
Data can be read in succession in the sequential read mode. When the memory address counter reaches the last word address, it rolls over to the first word address.

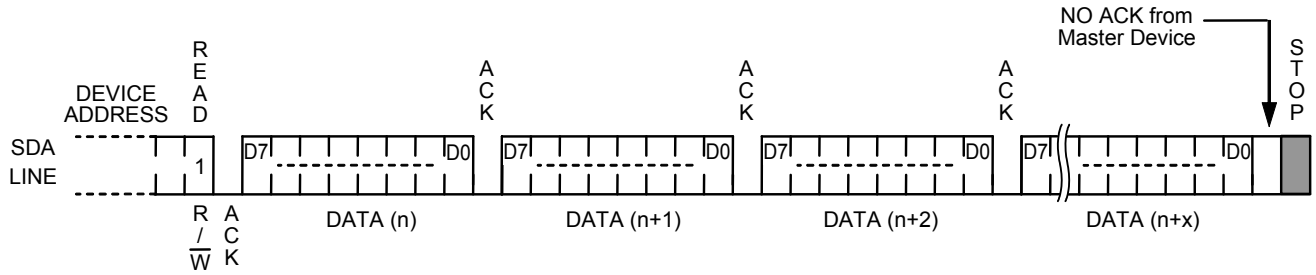



**Figure 17 Sequential Read**

## ■ Write Protect Function during the Low Power Supply Voltage

The S-24C16C has a built-in detection circuit which operates with the low power supply voltage, cancels Write when the power supply voltage drops and power-on. Its detection and release voltages are 1.20 V typ. (Refer to **Figure 18**).
The S-24C16C cancels Write by detecting a low power supply voltage when it receives a stop condition.
In the data trasmission and the Write operation, data in the address written during the low power supply voltage is not assurable.

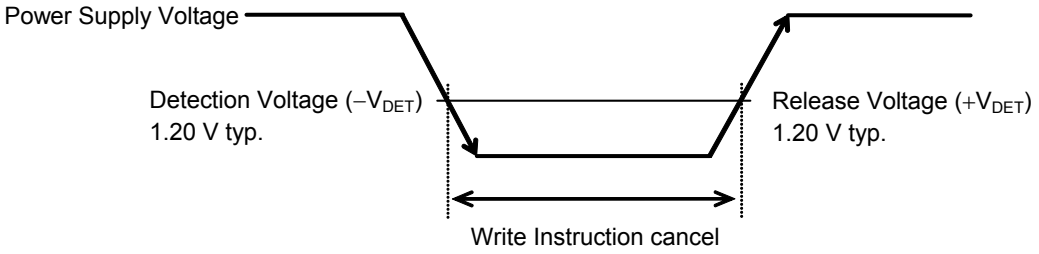



**Figure 18 Operation during Low Power Supply Voltage**

## ■ Using S-24C16C

### 1. Adding a pull-up resistor to SDA I/O pin and SCL input pin

In consideration of I$^2$C-bus protocol function, the SDA I/O pins should be connected with a pull-up resistor.
The S-24C16C cannot transmit normally without using a pull-up resistor.

In case that the SCL input pin of the S-24C16C is connected to the Nch open drain output pin of the master device, connect the SCL pin with a pull-up resistor. As well, in case the SCL input pin of the S-24C16C is connected to the tri-state output pin of the master device, connect the SCL pin with a pull-up resistor in order not to set it in high impedance. This prevents the S-24C16C from error caused by an uncertain output (high impedance) from the tri-state pin when resetting the master device during the voltage drop.

### 2. Equivalent circuit of input and I/O pin

The SCL pin and the SDA pin do not have a built-in pull-down or pull-up resistor.
The WP pin has a built-in pull-down resistor.The SDA pin has an open-drain output.
The followings are equivalent circuits of the pins.

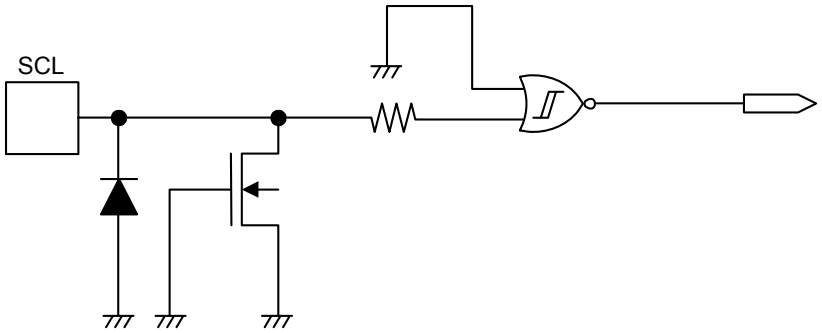



**Figure 19 SCL Pin**

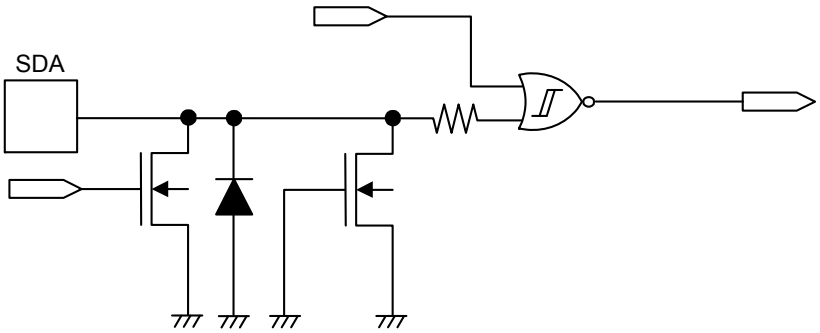



**Figure 20 SDA Pin**

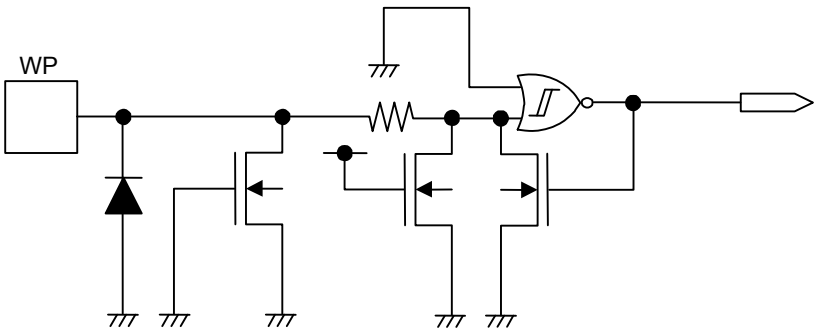



**Figure 21 WP Pin**

### 3. Phase adjustment during S-24C16C access

The S-24C16C does not have a pin to reset (the internal circuit). The users cannot forcibly reset it externally. If the communication to the S-24C16C interrupted, the users need to handle it as you do for software.
In the S-24C16C, users are able to reset the internal circuit by inputting a start condition and a stop condition.
Although the reset signal is input to the master device, the S-24C16C's internal circuit does not go in reset, but it does by inputting a stop condition to the S-24C16C. The S-24C16C keeps the same status thus cannot do the next operation. Especially, this case corresponds to that only the master device is reset when the power supply voltage drops.
If the power supply voltage restored in this status, input the instruction after resetting (adjusting the phase with the master device) the S-24C16C. How to reset is shown below.

**[How to reset S-24C16C]**

The S-24C16C is able to be reset by a start and stop instructions. When the S-24C16C is reading data "0" or is outputting the acknowledgment signal, outputs "0" to the SDA line. In this status, the master device cannot output an instruction to the SDA line. In this case, terminate the acknowledgment output operation or the Read operation, and then input a start instruction. **Figure 22** shows this procedure.
First, input a start condition. Then transmit 9 clocks (dummy clock) of SCL. During this time, the master device sets the SDA line to "H". By this operation, the S-24C16C interrupts the acknowledgment output operation or data output, so input a start condition*1. When a start condition is input, the S-24C16C is reset. To make doubly sure, input the stop condition to the S-24C16C. The normal operation is then possible.

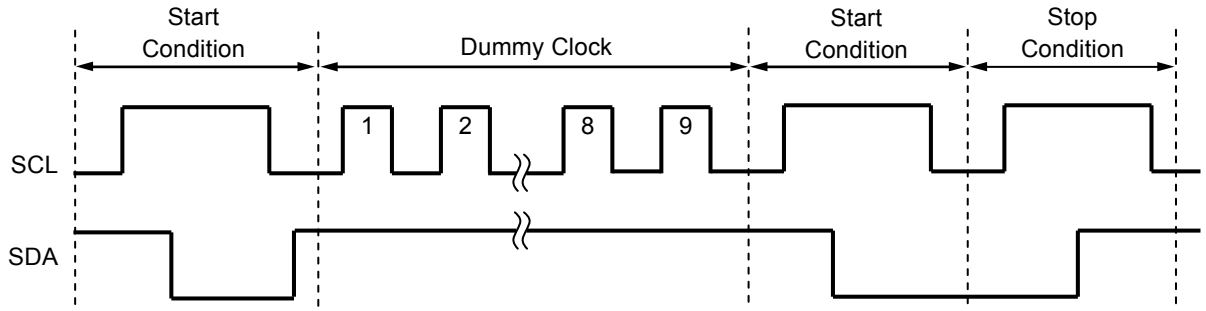



**Figure 22 Resetting S-24C16C**

***1.** After 9 clocks (dummy clock), if the SCL clock continues to being output without inputting a start condition, S-24C16C may go in the write operation when it receives a stop condition. To prevent this, input a start condition after 9 clocks (dummy clock).

**Remark** Regarding this reset procedure with dummy clock, it is recommended to perform at the system initialization after applying the power supply voltage.

## 4. Acknowledge check

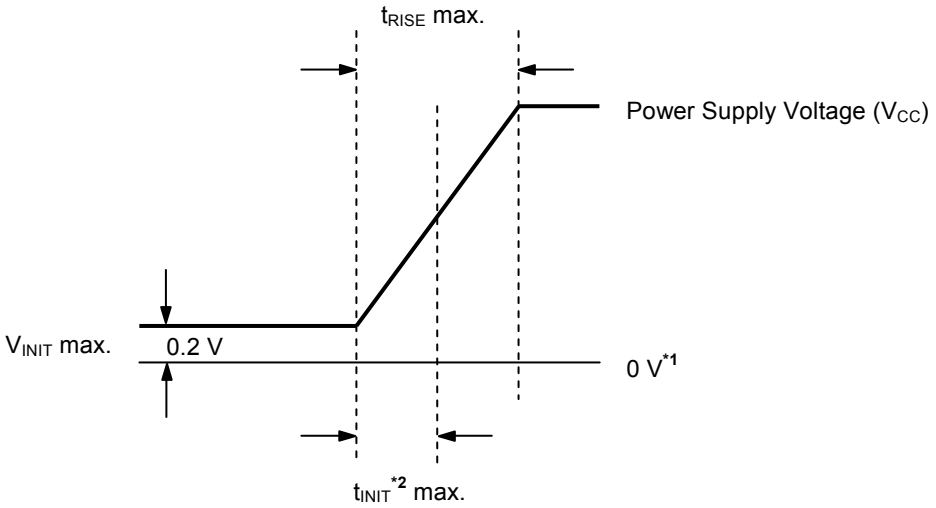
The $I^2C$-bus protocol includes an acknowledge check function as a handshake function to prevent a communication error. This function allows detection of a communication failure during data communication between the master device and S-24C16C. This function is effective to prevent malfunction, so it is recommended to perform an acknowledge check with the master device.

## 5. Built-in power-on-clear circuit

The S-24C16C has a built-in power-on-clear circuit that initializes itself at the same time during power-on. Unsuccessful initialization may cause a malfunction. To operate the power-on-clear circuit normally, the following conditions must be satisfied to raise the power supply voltage.

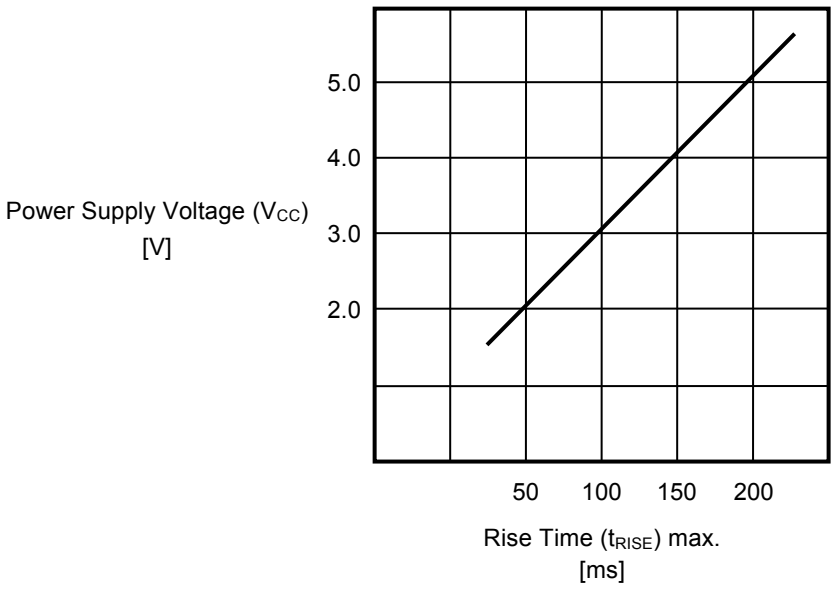
### 5. 1 Raising power supply voltage

Shown in **Figure 23**, raise the power supply voltage from 0.2 V max., within the time defined as $t_{RISE}$ which is the time required to reach the power supply voltage to be set.
For example, if the power supply voltage is 5.0 V, $t_{RISE}$ = 200 ms seen in **Figure 24**. The power supply voltage must be raised within 200 ms.




***1.** 0 V means there is no difference in potential between the VCC pin and the GND pin of the S-24C16C.
***2.** $t_{INIT}$ is the time required to initialize the S-24C16C. No instructions are accepted during this time.

**Figure 23 Raising Power Supply Voltage**




For example: If the supply voltage = 5.0 V, raise the power supply voltage to 5.0 V within 200 ms.

**Figure 24 Rise Time of Power Supply Voltage**

When initialization is successfully completed by the power-on-clear circuit, the S-24C16C enters the standby status.
If the power-on-clear circuit does not operate;
The S-24C16C has not completed initialization, an instruction previously input is still valid or an instruction may be inappropriately recognized. In this case, S-24C16C may perform the Write operation.
The voltage drops due to power off while the S-24C16C is being accessed. Even if the master device is reset due to the low power voltage, the S-24C16C may malfunction unless the power-on-clear operation conditions of S-24C16C are satisfied.

When not using this rise time seen in **Figure 24**, adjust the phase (reset) to reset the internal circuit in the S-24C16C normally.

### 5. 2 Initialization time

The S-24C16C initializes at the same time when the power supply voltage is raised. Input instructions to the S-24C16C after initialization. S-24C16C does not accept any instruction during initialization.
**Figure 25** shows the initialization time of the S-24C16C.

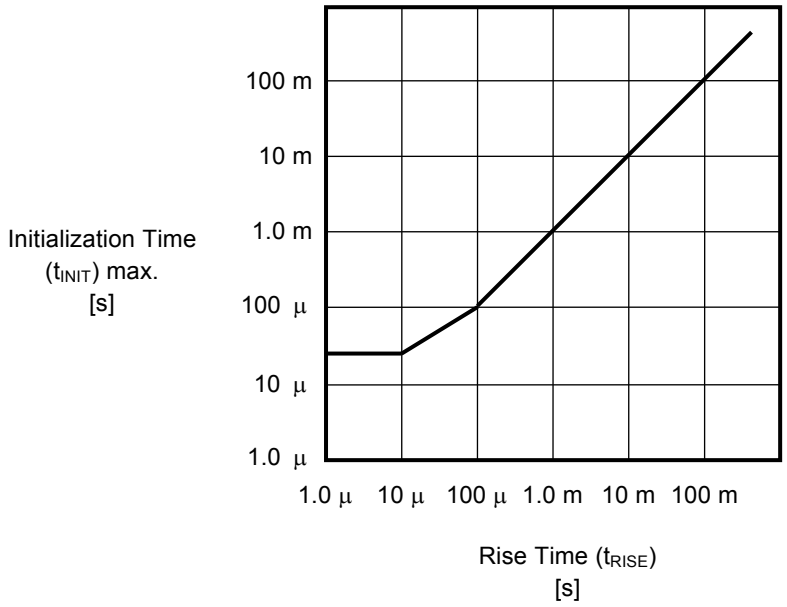



**Figure 25 Initialization Time of S-24C16C**

### 6. Data hold time ($t_{HD.DAT}$ = 0 ns)

If SCL and SDA of the S-24C16C are changed at the same time, it is necessary to prevent a start / stop condition from being mistakenly recognized due to the effect of noise.
The S-24C16C may error if it does not recognize a start / stop condition correctly during transmission.
It is recommended to set the delay time of 0.3 μs minimum from a falling edge of SCL for the SDA.
This is to prevent S-24C16C from going in a start / stop condition due to the time lag caused by the load of the bus line.

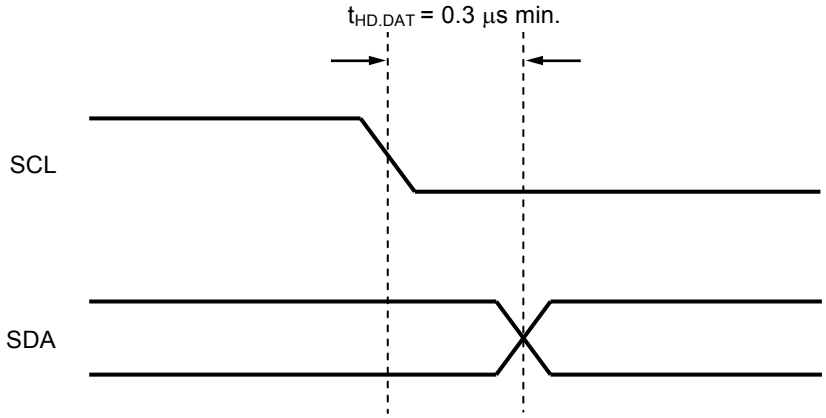



**Figure 26 S-24C16C Data Hold Time**

### 7. SDA pin and SCL pin noise suppression time

The S-24C16C includes a built-in low-pass filter at the SDA and SCL pins to suppress noise. This means that if the power supply voltage is 5.0 V, noise with a pulse width of 130 ns or less can be suppressed.
For details of the assurable value, refer to noise suppression time ($t_I$) in **Table 11**.

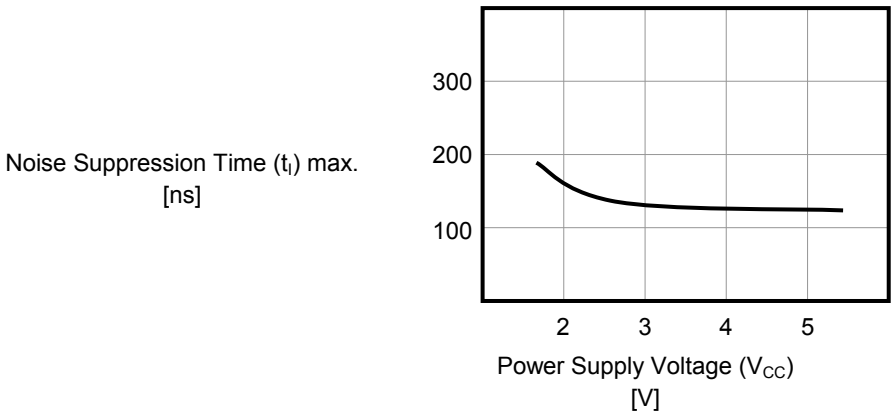



**Figure 27 Noise Suppression Time for SDA and SCL Pins**

### 8. Operation when input stop condition during input write data

The S-24C16C does the write operation only when it receives data of 1 byte or more and receives a stop condition immediately after ACK output.
Refer to **Figure 28** regarding details.

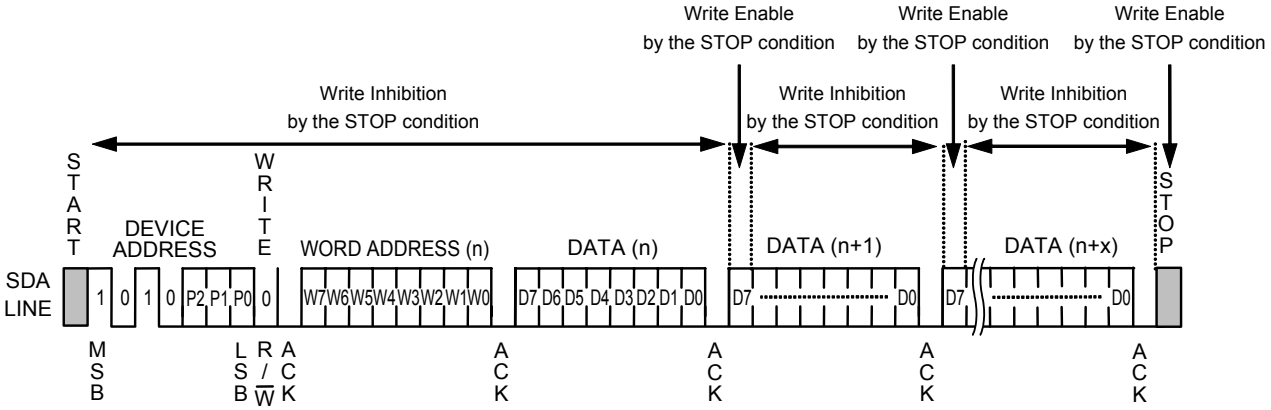



**Figure 28 Write Operation by Inputting Stop Condition during Write**

### 9. Command cancel by start condition

By a start condition, users are able to cancel command which is being input. However, adjust the phase while the S-24C16C is outputting “L” because users are not able to input a start condition. When users cancel the command, there may be a case that the address will not be identified. Use random read for the read operation, not current address read.

### 10. Precaution for use

Absolute maximum ratings: Do not operate these ICs in excess of the absolute maximum ratings (as listed on the data sheet). Exceeding the supply voltage rating can cause latch-up.

Operations with moisture on the S-24C16C pins may occur malfunction by short-circuit between pins. Especially, in occasions like picking the S-24C16C up from low temperature tank during the evaluation. Be sure that not remain frost on the S-24C16C’s pins to prevent malfunction by short-circuit.
Also attention should be paid in using on environment, which is easy to dew for the same reason.

## ■ Precautions

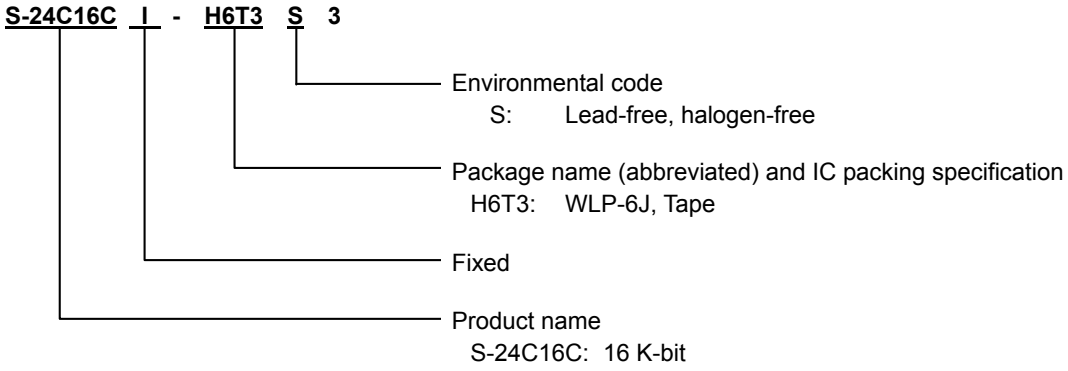
- Do not apply an electrostatic discharge to this IC that exceeds the performance ratings of the built-in electrostatic protection circuit.
- ABLIC Inc. claims no responsibility for any and all disputes arising out of or in connection with any infringement of the products including this IC upon patents owned by a third party.

## ■ Precautions for WLP package

- The side of device silicon substrate is exposed to the marking side of device package. Since this portion has lower strength against the mechanical stress than the standard plastic package, chip, crack, etc should be careful of the handing of a package enough. Moreover, the exposed side of silicon has electrical potential of device substrate, and needs to be kept out of contact with the external potential.
- In this package, the overcoat of the resin of translucence is carried out on the side of device area. Keep it mind that it may affect the characteristic of a device when exposed a device in the bottom of a high light source.

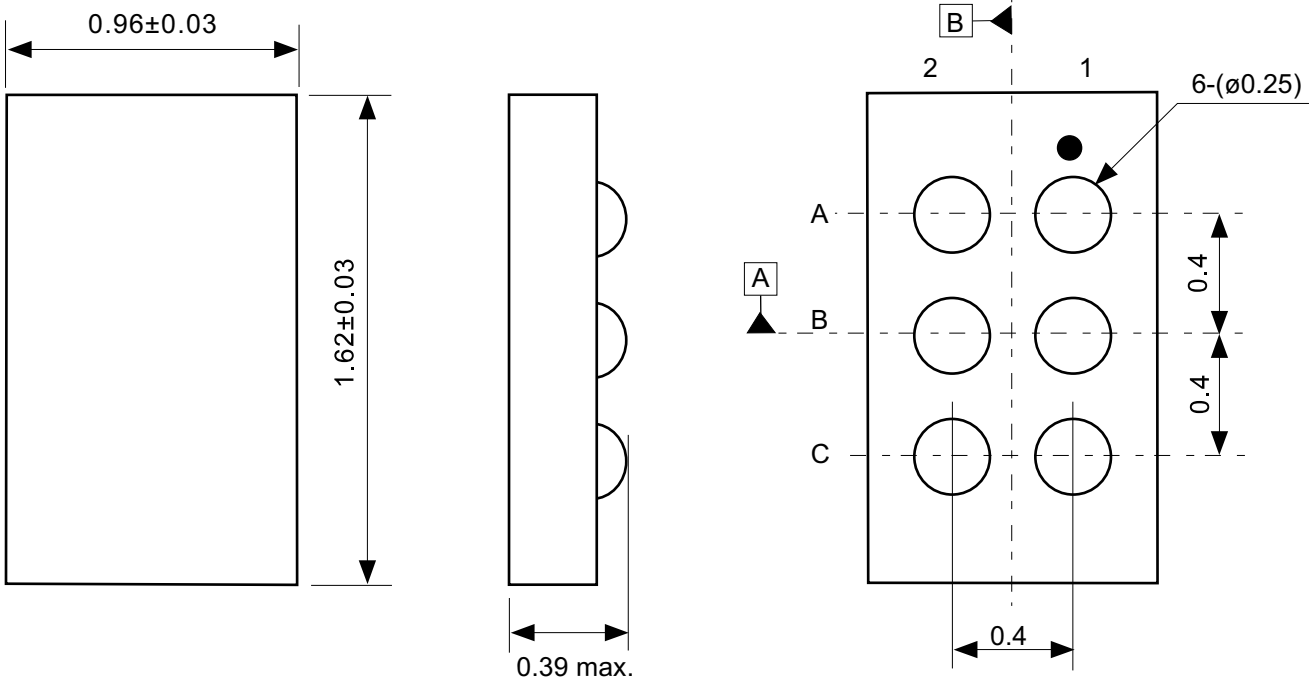
## ■ Product Name Structure

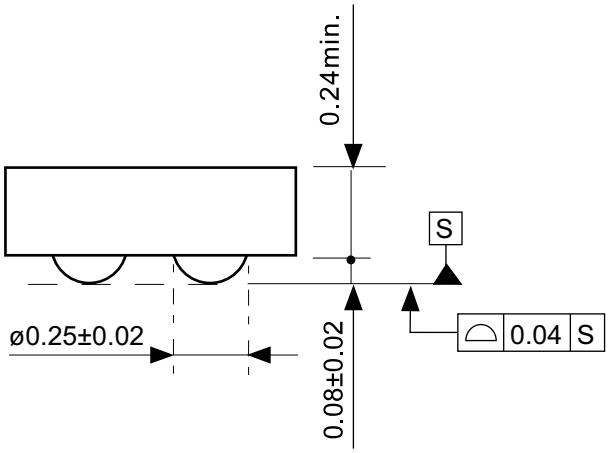
### 1. Product name




### 2. Package

| Package Name | Drawing Code | | |
|---|---|---|---|
| | Package | Tape | Reel |
| WLP-6J | HJ006-C-P-SD | HJ006-C-C-SD | HJ006-C-R-SD |

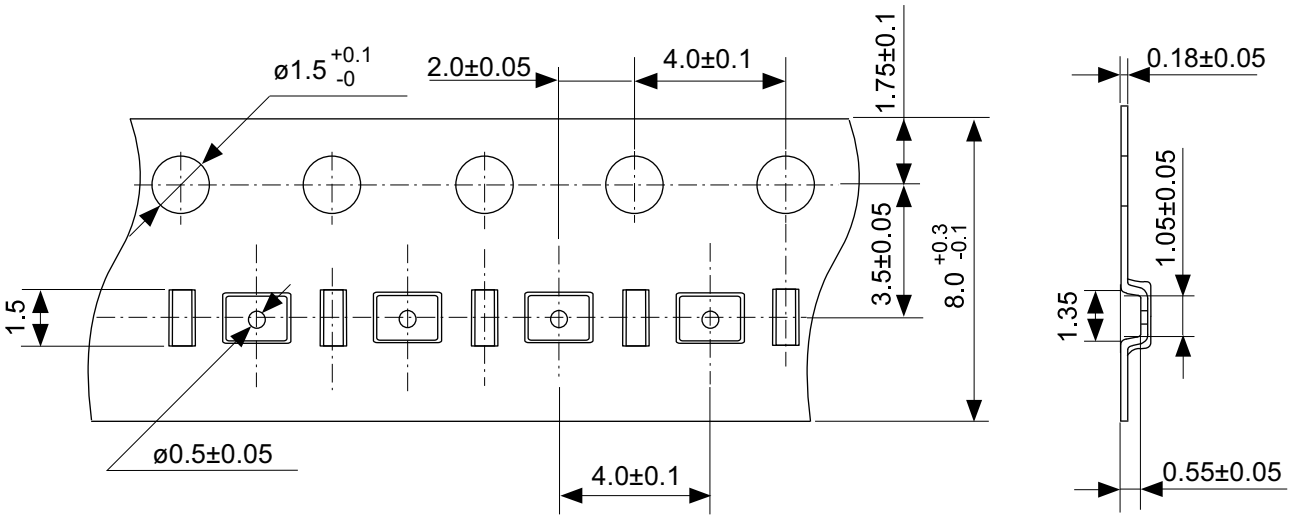


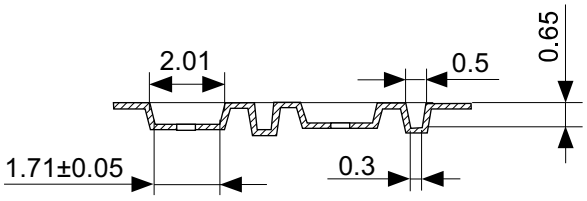



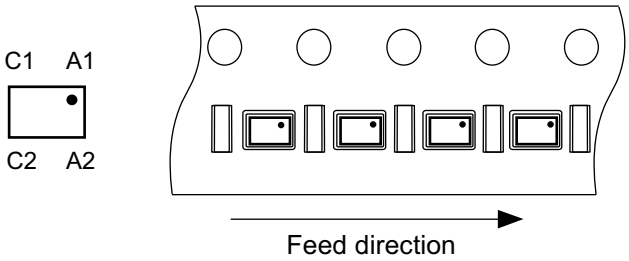

| Pin No. | Symbol |
|---|---|
| A1 | SDA |
| B1 | GND |
| C1 | A2 |
| A2 | SCL |
| B2 | WP |
| C2 | VCC |

No. HJ006-C-P-SD-2.0

| | |
|---|---|
| TITLE | WLP-6J-C-PKG Dimensions (S-24C16C) |
| No. | HJ006-C-P-SD-2.0 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |

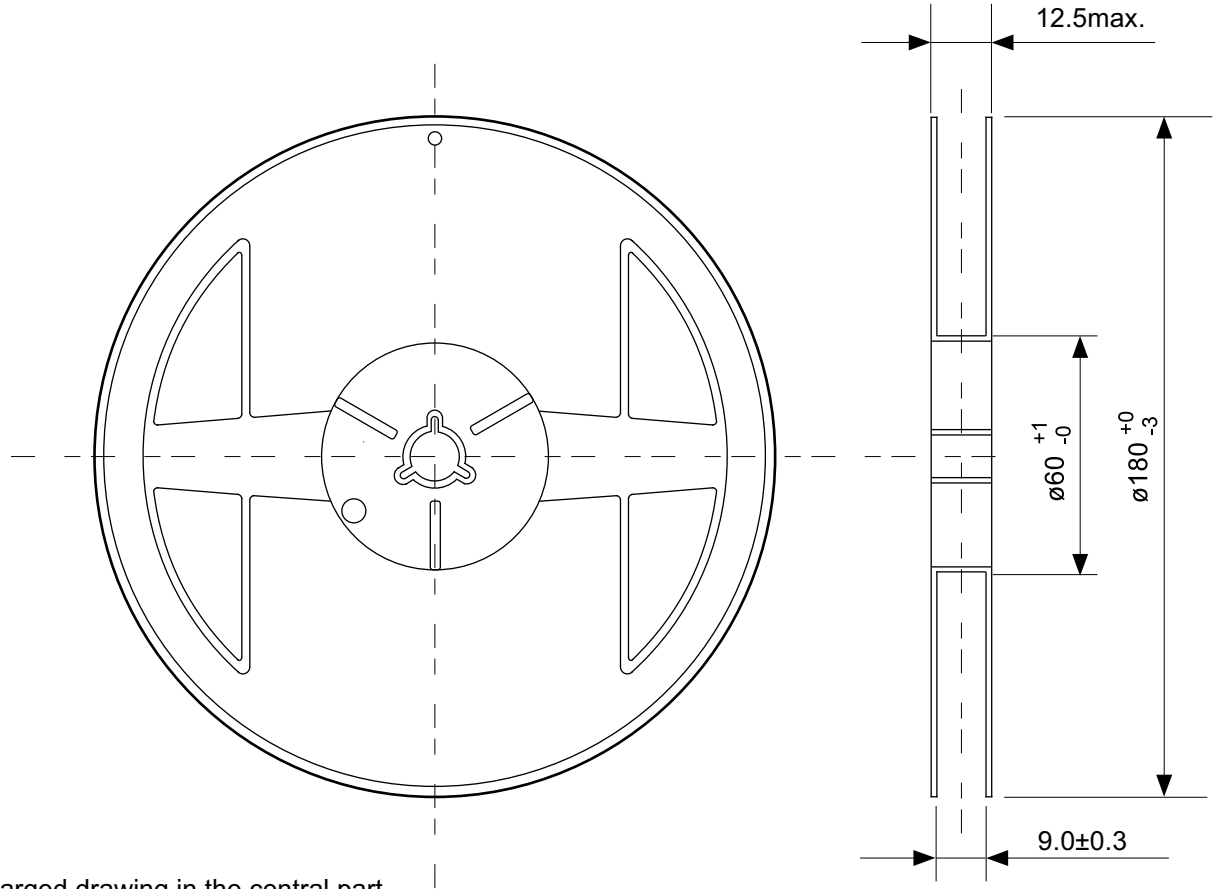


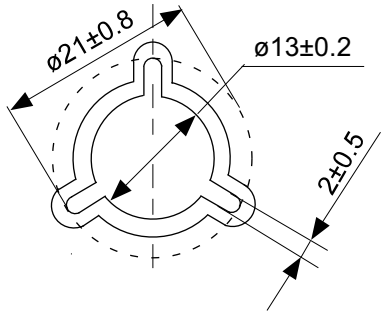




No. HJ006-C-C-SD-1.0

| | |
|---|---|
| TITLE | WLP-6J-C-Carrier Tape (S-24C16C) |
| No. | HJ006-C-C-SD-1.0 |
| ANGLE | |
| UNIT | mm |
| | |
| **ABLIC Inc.** | |




Enlarged drawing in the central part




No. HJ006-C-R-SD-1.0

| | | | |
|---|---|---|---|
| TITLE | WLP-6J-C-Reel (S-24C16C) | | |
| No. | HJ006-C-R-SD-1.0 | | |
| ANGLE | | QTY. | 3,000 |
| UNIT | mm | | |
| | | | |
| **ABLIC Inc.** | | | |

## Disclaimers (Handling Precautions)

1. All the information described herein (product data, specifications, figures, tables, programs, algorithms and application circuit examples, etc.) is current as of publishing date of this document and is subject to change without notice.
2. The circuit examples and the usages described herein are for reference only, and do not guarantee the success of any specific mass-production design.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the reasons other than the products described herein (hereinafter "the products") or infringement of third-party intellectual property right and any other right due to the use of the information described herein.
3. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by the incorrect information described herein.
4. Be careful to use the products within their ranges described herein. Pay special attention for use to the absolute maximum ratings, operation voltage range and electrical characteristics, etc.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by failures and / or accidents, etc. due to the use of the products outside their specified ranges.
5. Before using the products, confirm their applications, and the laws and regulations of the region or country where they are used and verify suitability, safety and other factors for the intended use.
6. When exporting the products, comply with the Foreign Exchange and Foreign Trade Act and all other export-related laws, and follow the required procedures.
7. The products are strictly prohibited from using, providing or exporting for the purposes of the development of weapons of mass destruction or military use. ABLIC Inc. is not liable for any losses, damages, claims or demands caused by any provision or export to the person or entity who intends to develop, manufacture, use or store nuclear, biological or chemical weapons or missiles, or use any other military purposes.
8. The products are not designed to be used as part of any device or equipment that may affect the human body, human life, or assets (such as medical equipment, disaster prevention systems, security systems, combustion control systems, infrastructure control systems, vehicle equipment, traffic systems, in-vehicle equipment, aviation equipment, aerospace equipment, and nuclear-related equipment), excluding when specified for in-vehicle use or other uses by ABLIC, Inc. Do not apply the products to the above listed devices and equipments.
   ABLIC Inc. is not liable for any losses, damages, claims or demands caused by unauthorized or unspecified use of the products.
9. In general, semiconductor products may fail or malfunction with some probability. The user of the products should therefore take responsibility to give thorough consideration to safety design including redundancy, fire spread prevention measures, and malfunction prevention to prevent accidents causing injury or death, fires and social damage, etc. that may ensue from the products' failure or malfunction.
   The entire system in which the products are used must be sufficiently evaluated and judged whether the products are allowed to apply for the system on customer's own responsibility.
10. The products are not designed to be radiation-proof. The necessary radiation measures should be taken in the product design by the customer depending on the intended use.
11. The products do not affect human health under normal use. However, they contain chemical substances and heavy metals and should therefore not be put in the mouth. The fracture surfaces of wafers and chips may be sharp. Be careful when handling these with the bare hands to prevent injuries, etc.
12. When disposing of the products, comply with the laws and ordinances of the country or region where they are used.
13. The information described herein contains copyright information and know-how of ABLIC Inc. The information described herein does not convey any license under any intellectual property rights or any other rights belonging to ABLIC Inc. or a third party. Reproduction or copying of the information from this document or any part of this document described herein for the purpose of disclosing it to a third-party is strictly prohibited without the express permission of ABLIC Inc.
14. For more details on the information described herein or any other questions, please contact ABLIC Inc.'s sales representative.
15. This Disclaimers have been delivered in a text using the Japanese language, which text, despite any translations into the English language and the Chinese language, shall be controlling.

2.4-2019.07