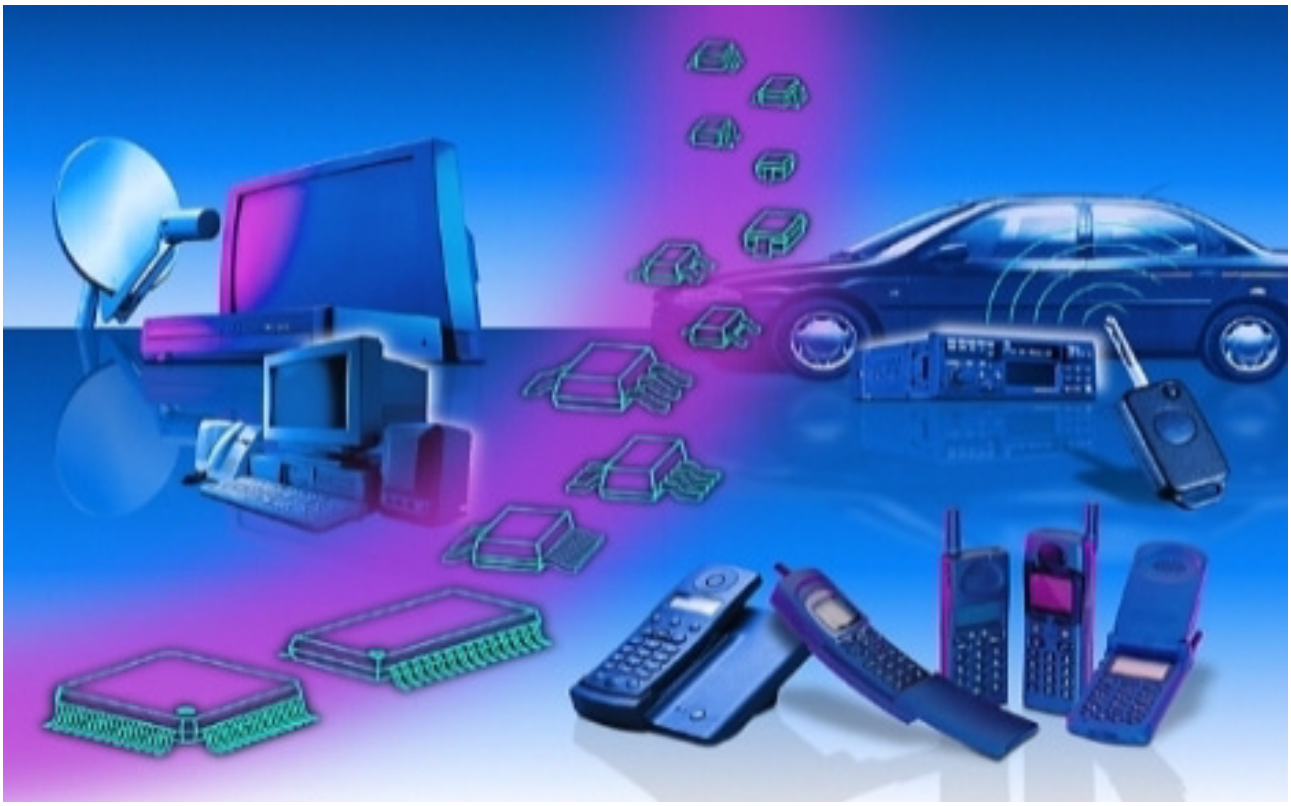


Wireless Components

315 MHz ASK/FSK Transmitter in 10-pin Package

TDK 5101 F Version 0.1

Target Specification July 2003

Confidential

Preliminary

Confidential **Revision History**		
Current Version: Version 0.1 as of July 2003		
Previous Version:		
Page (in previous Version)	Page (in current Version)	Subjects (major changes since last revision)

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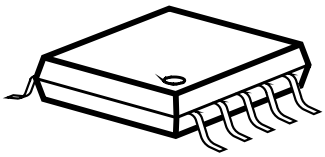
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Product Info

General Description

The TDK 5101 F is a single chip ASK/FSK transmitter for the frequency band 311-317 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery life. Additional features are a power down mode and a divided clock output.

Package



Features

- fully integrated frequency synthesizer
- VCO without external components
- ASK and FSK modulation
- frequency range 311-317 MHz
- high efficiency power amplifier (typically 5 dBm)
- low supply current (typically 7mA)
- voltage supply range 2.1 - 4 V
- temperature range –40 ... +125°C
- power down mode
- crystal oscillator 9.84 MHz
- FSK-switch
- divided clock output for µC
- low external component count

Applications

- Tire pressure monitoring systems
- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

Ordering Information

Type	Ordering Code	Package
TDK 5101 F	t.b.d.	P-TSSOP-10
available on tape and reel		

1 Product Description

Contents of this Chapter

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1.2 Applications 1-2
1.3 Features 1-2
1.4 Package Outlines 1-3

1.1 Overview

The TDK 5101 F is a single chip ASK/FSK transmitter for the frequency band 311-317 MHz. The IC offers a high level of integration and needs only a few external components. The device contains a fully integrated PLL synthesizer and a high efficiency power amplifier to drive a loop antenna. A special circuit design and an unique power amplifier design are used to save current consumption and therefore to save battery life. Additional features are a power down mode and a divided clock output.

The IC can be used for both ASK and FSK modulation.

1.2 Applications

- Tire pressure monitoring systems
- Keyless entry systems
- Remote control systems
- Alarm systems
- Communication systems

1.3 Features

- fully integrated frequency synthesizer
- VCO without external components
- ASK and FSK modulation
- switchable frequency range 311-317 MHz
- high efficiency power amplifier (typically 5 dBm)
- low supply current (typically 7 mA)
- voltage supply range 2.1 - 4 V
- temperature range –40°C ... 125°C
- power down mode
- crystal oscillator 9.84 MHz
- FSK-switch
- divided clock output for µC
- low external component count

1.4 Package Outlines

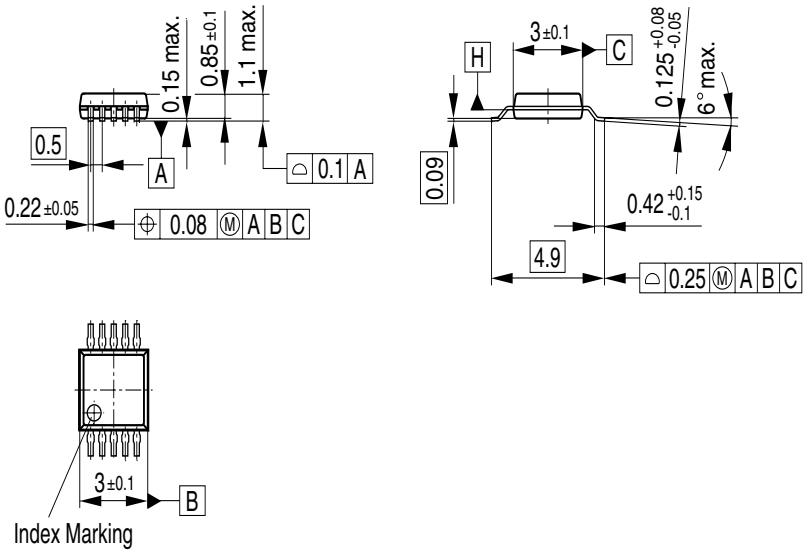


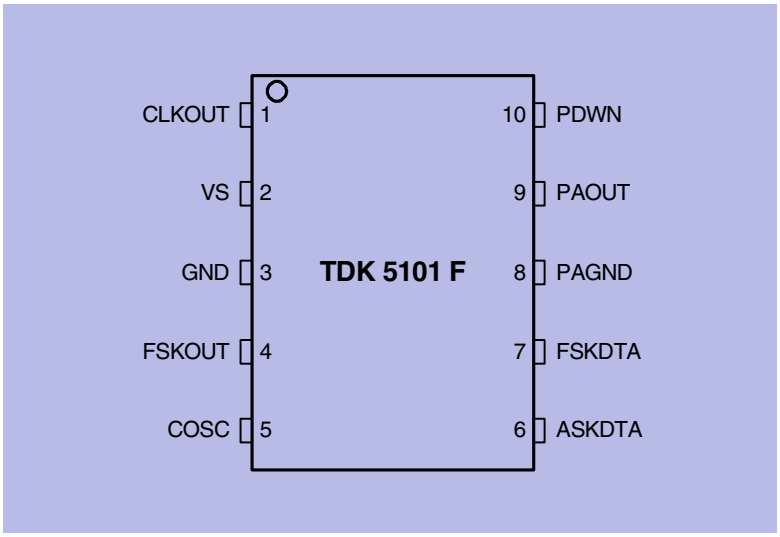
Figure 1-1 P-TSSOP-10

2 Functional Description

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2.1 Pin Configuration



Pin_config.wmf

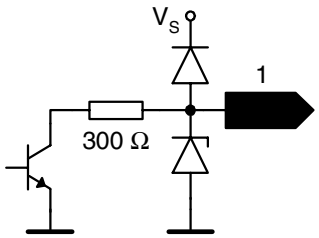
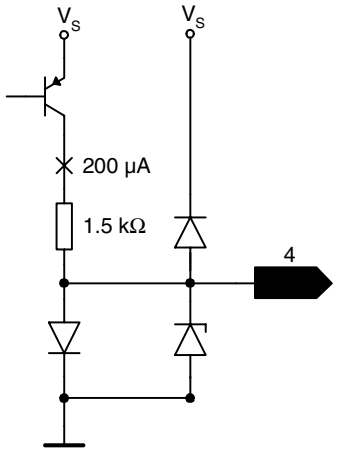
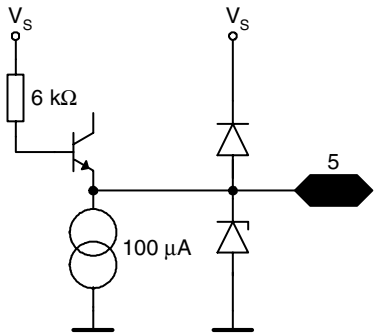
Figure 2-1 IC Pin Configuration

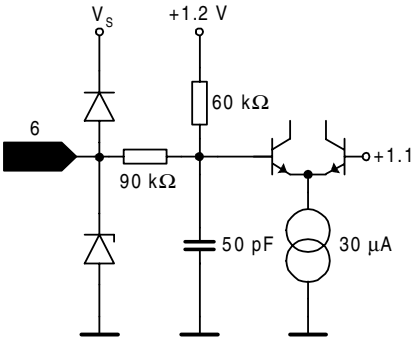
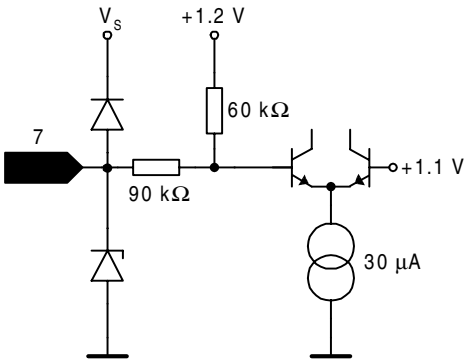
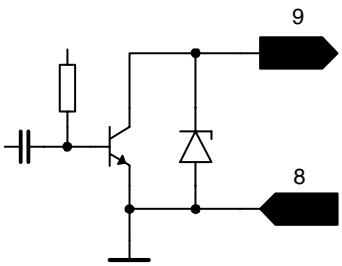
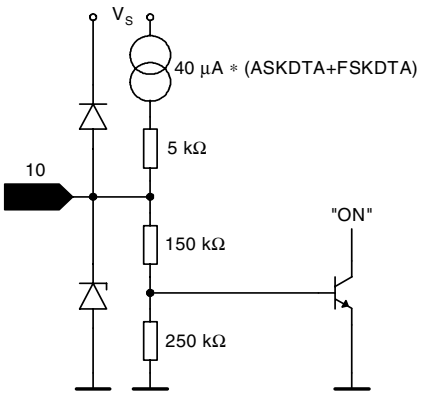
Table 2-1

Pin No.	Symbol	Function
1	CLKOUT	Clock Driver Output (615.2 kHz)
2	VS	Voltage Supply
3	GND	Ground
4	FSKOUT	Frequency Shift Keying Switch Output
5	COSC	Crystal Oscillator Input (9.84 MHz)
6	ASKDTA	Amplitude Shift Keying Data Input
7	FSKDTA	Frequency Shift Keying Data Input
8	PAGND	Power Amplifier Ground
9	PAOUT	Power Amplifier Output (315 MHz)
10	PDWN	Power Down Mode Control

2.2 Pin Definitions and Functions

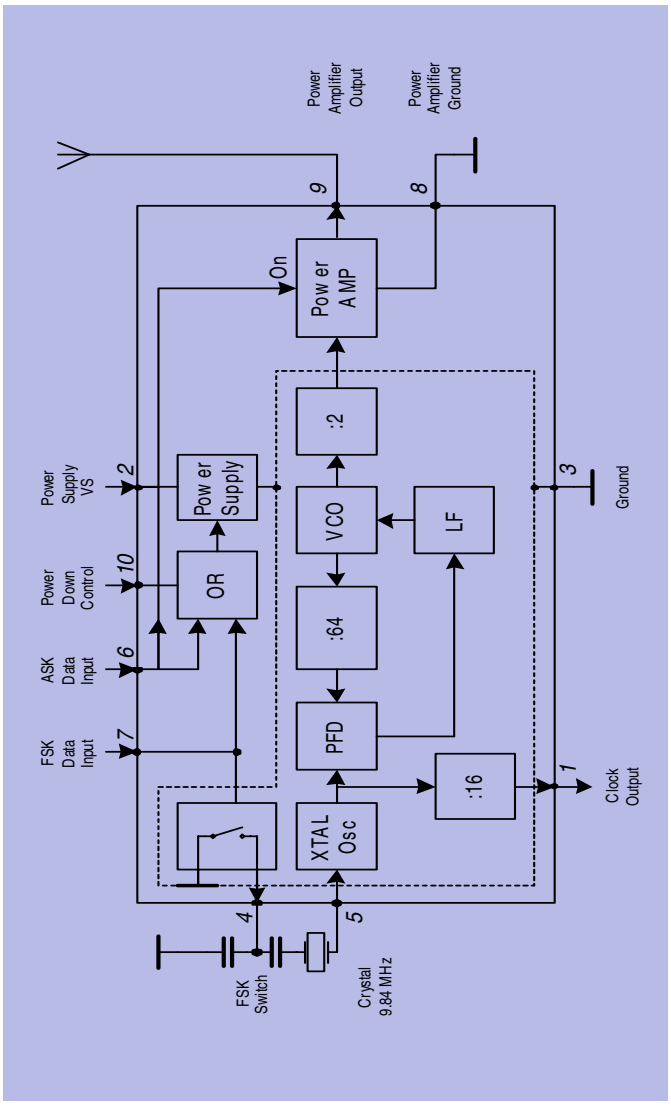
Table 2-2

Pin No.	Symbol	Interface Schematic[1)]	Function
1	CLKOUT		Clock output to supply an external device. An external pull-up resistor has to be added in accordance to the driving requirements of the external device. The clock frequency is 615.2 kHz.
2	VS		This pin is the positive supply of the transmitter electronics. An RF bypass capacitor should be connected directly to this pin and returned to GND (pin 3) as short as possible.
3	GND		General ground connection.
4	FSKOUT		This pin is connected to a switch to GND (pin 3). The switch is closed when the signal at FSKDTA (pin 7) is in a logic low state. The switch is open when the signal at FSKDTA (pin 7) is in a logic high state. FSKOUT can switch an additional capacitor to the reference crystal network to pull the crystal frequency by an amount resulting in the desired FSK frequency shift of the transmitter output frequency.
5	COSC		This pin is connected to the reference oscillator circuit. The reference oscillator is working as a negative impedance converter. It presents a negative resistance in series to an inductance at the COSC pin.

6	ASKDTA		Digital amplitude modulation can be imparted to the Power Amplifier through this pin. A logic high (ASKDTA > 1.5 V or open) enables the Power Amplifier. A logic low (ASKDTA < 0.5 V) disables the Power Amplifier.
7	FSKDTA		Digital frequency modulation can be imparted to the Xtal Oscillator by this pin. The VCO-frequency varies in accordance to the frequency of the reference oscillator. A logic high (FSKDTA > 1.5V or open) sets the FSK switch to a high impedance state. A logic low (FSKDTA < 0.5 V) closes the FSK switch from FSKOUT (pin 4) to GND (pin 3). A capacitor can be switched to the reference crystal network this way. The Xtal Oscillator frequency will be shifted giving the designed FSK frequency deviation.
8	PAGND		Ground connection of the power amplifier. The RF ground return path of the power amplifier output PAOUT (pin 9) has to be concentrated to this pin.
9	PAOUT		RF output pin of the transmitter. A DC path to the positive supply VS has to be supplied by the antenna matching network.
10	PDWN		Disable pin for the complete transmitter circuit. A logic low (PDWN < 0.7 V) turns off all transmitter functions. A logic high (PDWN > 1.5 V) gives access to all transmitter functions. PDWN input will be pulled up by 40 µA internally by either setting FSKDTA or ASKDTA to a logic high-state.

1) Indicated voltages and currents apply for PLL Enable Mode and Transmit Mode. In Power Down Mode, the values are zero or high-ohmic.

2.3 Functional Block diagram



Blockdiagram.wmf

Figure 2-2 Functional Block diagram

2.4 Functional Blocks

2.4.1 PLL Synthesizer

The Phase Locked Loop synthesizer consists of a Voltage Controlled Oscillator (VCO), an asynchronous divider chain, a phase detector, a charge pump and a loop filter. It is fully implemented on chip. The tuning circuit of the VCO consisting of spiral inductors and varactor diodes is on chip, too. Therefore no additional external components are necessary. The nominal center frequency of the VCO is 630 MHz. The oscillator signal is fed both, to the synthesizer divider chain and to the power amplifier. The overall division ratio of the asynchronous divider chain is 64. The phase detector is a Type IV PD with charge pump. The passive loop filter is realized on chip.

2.4.2 Crystal Oscillator

The crystal oscillator operates at 9.84 MHz.

The crystal frequency is divided by 16. The resulting 615.2 kHz are available at the clock output CLKOUT (pin1) to drive the clock input of a micro controller.

To achieve FSK transmission, the oscillator frequency can be detuned by a fixed amount by switching an external capacitor via FSKOUT (pin 4).

The condition of the switch is controlled by the signal at FSKDTA (pin 7).

Table 2-3

FSKDTA (pin7)	FSK Switch
Low[1)]	CLOSED
Open[2)], High[3)]	OPEN

1) Low: Voltage at pin < 0.5 V
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

2.4.3 Power Amplifier

The VCO frequency is divided by 2 and fed to the Power Amplifier.

The Power Amplifier can be switched on and off
by the signal at ASKDTA (pin 6).

Table 2-4

ASKDTA (pin 6)	Power Amplifier
Low[1)]	OFF
Open[2)], High[3)]	ON

1) Low: Voltage at pin < 0.5 V
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

The Power Amplifier has an Open Collector output at PAOUT (pin 9) and requires an external pull-up coil to provide bias. The coil is part of the tuning and matching LC circuitry to get best performance with the external loop antenna. To achieve the best power amplifier efficiency, the high frequency voltage swing at PAOUT (pin 9) should be twice the supply voltage.

The power amplifier has its own ground pin PAGND (pin 8) in order to reduce the amount of coupling to the other circuits.

2.4.4 Power Modes

The IC provides three power modes, the POWER DOWN MODE, the PLL ENABLE MODE and the TRANSMIT MODE.

2.4.4.1 Power Down Mode

In the POWER DOWN MODE the complete chip is switched off.

The current consumption is typically 0.3 nA at 3 V 25°C.

This current doubles every 8°C. The values for higher temperatures are typically 14 nA at 85°C and typically 600 nA at 125°C.

2.4.4.2 PLL Enable Mode

In the PLL ENABLE MODE the PLL is switched on but the power amplifier is turned off to avoid undesired power radiation during the time the PLL needs to settle. The turn on time of the PLL is determined mainly by the turn on time of the crystal oscillator and is less than 1 msec when the specified crystal is used.

The current consumption is typically 3.5 mA.

2.4.4.3 Transmit Mode

In the TRANSMIT MODE the PLL is switched on and the power amplifier is turned on too.

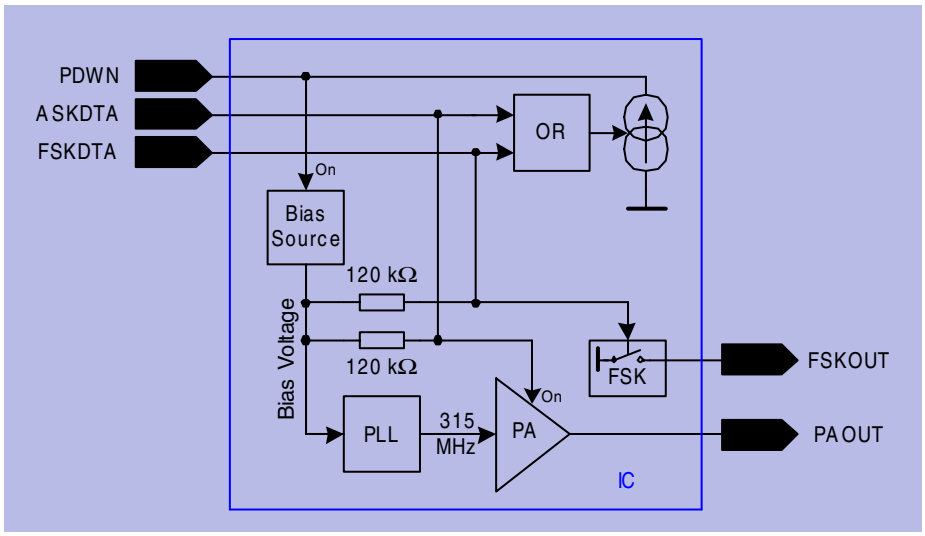
The current consumption of the IC is typically 7 mA when using a proper transforming network at PAOUT, see Figure 3-1.

2.4.4.4 Power mode control

The bias circuitry is powered up via a voltage V > 1.5 V at the pin PDWN (pin10). When the bias circuitry is powered up, the pins ASKDTA and FSKDTA are pulled up internally.
Forcing the voltage at the pins low overrides the internally set state.

Alternatively, if the voltage at ASKDTA or FSKDTA is forced high externally, the PDWN pin is pulled up internally via a current source. In this case, it is not necessary to connect the PDWN pin, it is recommended to leave it open.

The principle schematic of the power mode control circuitry is shown in Figure 2-5.



Power_Mode.wmf

Figure 2-5 Power mode control circuitry

Table 2-5 provides a listing of how to get into the different power modes

Table 2-5

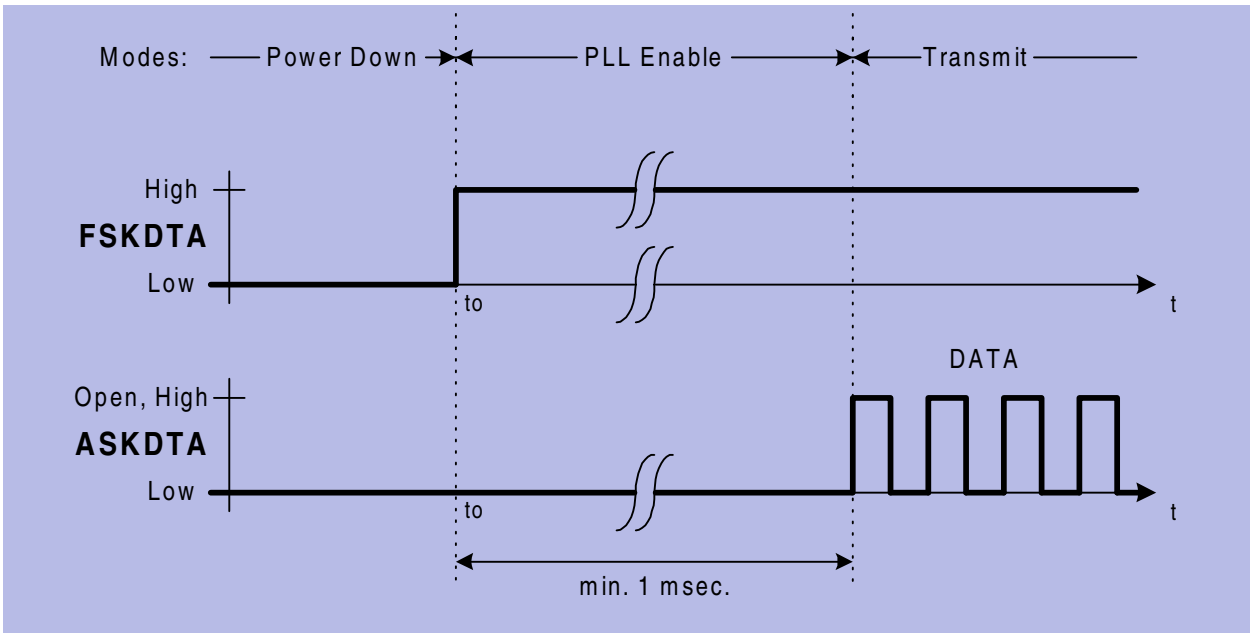
PDWN	FSKDTA	ASKDTA	MODE
Low[1)]	Low, Open	Low, Open	POWER DOWN
Open[2)]	Low	Low	
High[3)]	Low, Open, High	Low	PLL ENABLE
Open	High	Low	
High	Low, Open, High	Open, High	TRANSMIT
Open	High	Open, High	
Open	Low, Open, High	High	

1) Low: Voltage at pin < 0.7 V (PDWN)
Voltage at pin < 0.5 V (FSKDTA, ASKDTA)
2) Open: Pin open
3) High: Voltage at pin > 1.5 V

Other combinations of the control pins PDWN, FSKDTA and ASKDTA are not recommended.

2.4.5 Recommended Timing Diagrams for ASK- and FSK-Modulation

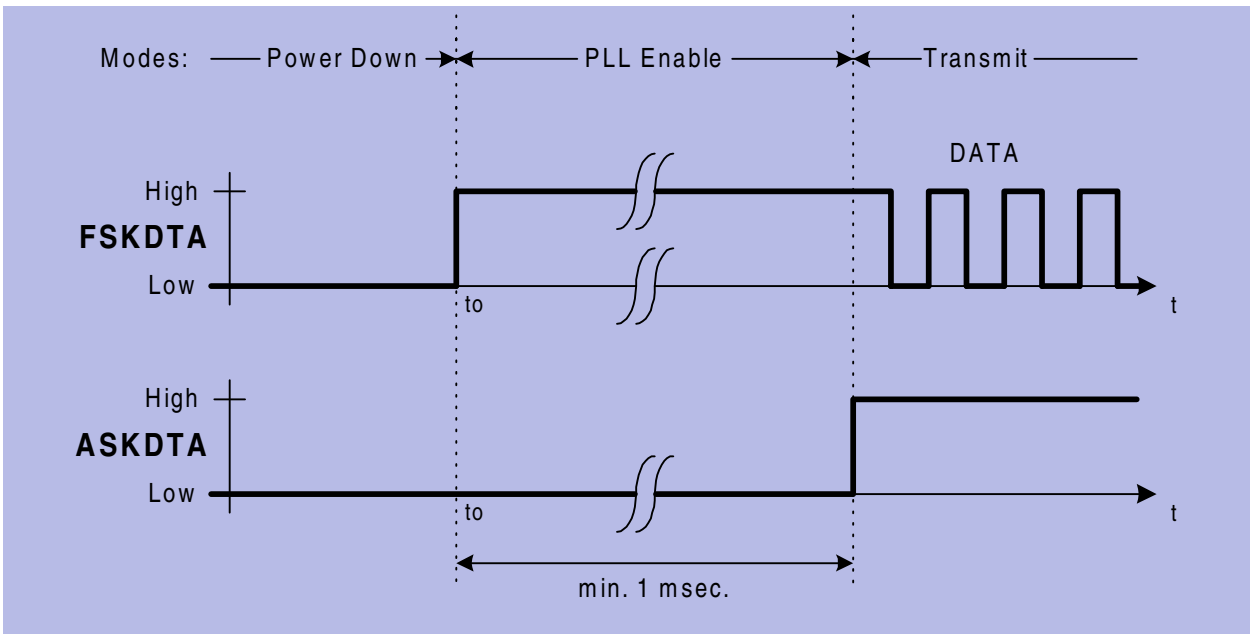
ASK Modulation using FSKDTA and ASKDTA, PDWN not connected



ASK_mod.wmf

Figure 2-6 ASK Modulation

FSK Modulation using FSKDTA and ASKDTA, PDWN not connected



FSK_mod.wmf

Figure 2-7 FSK Modulation

Alternative ASK Modulation, FSKDTA not connected.

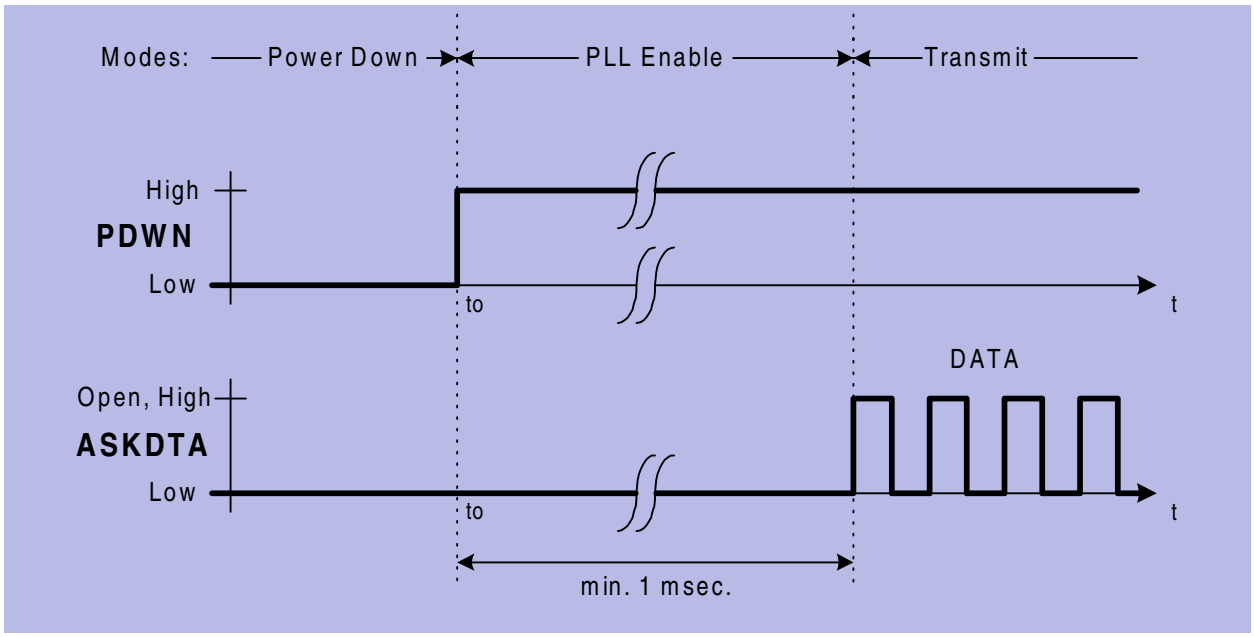


Figure 2-8 Alternative ASK Modulation

Alternative FSK Modulation

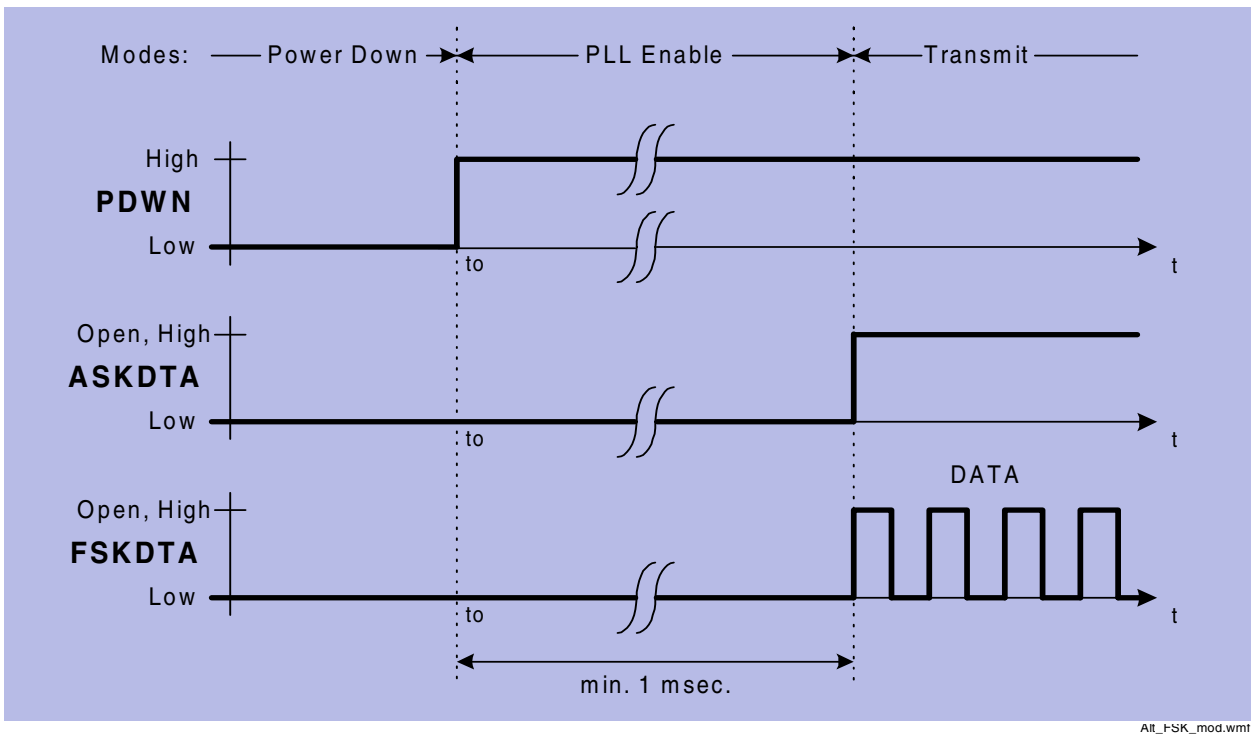


Figure 2-9 Alternative FSK Modulation

3 Applications

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3.1 50 Ohm-Output Testboard Schematic 3-2
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3.3 Bill of material (50 Ohm-Output Testboard) 3-4
3.4 Application Hints on the Crystal Oscillator 3-5
3.5 Design Hints on the Clock Output (CLKOUT). 3-7
3.6 Application Hints on the Power-Amplifier 3-8

3.1 50 Ohm-Output Testboard Schematic

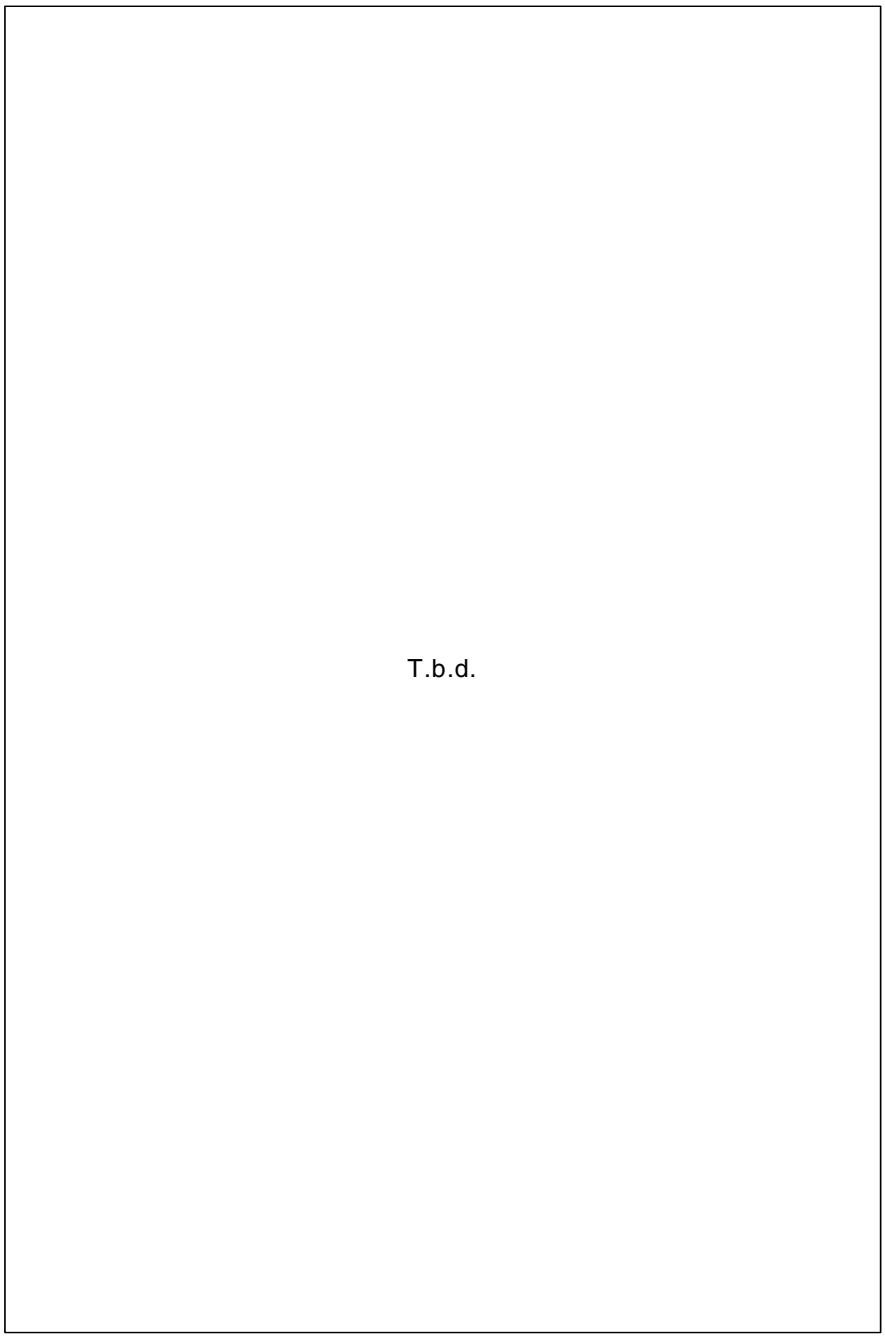


Figure 3-1 50Ω-output testboard schematic

3.2 50 Ohm-Output Testboard Layout

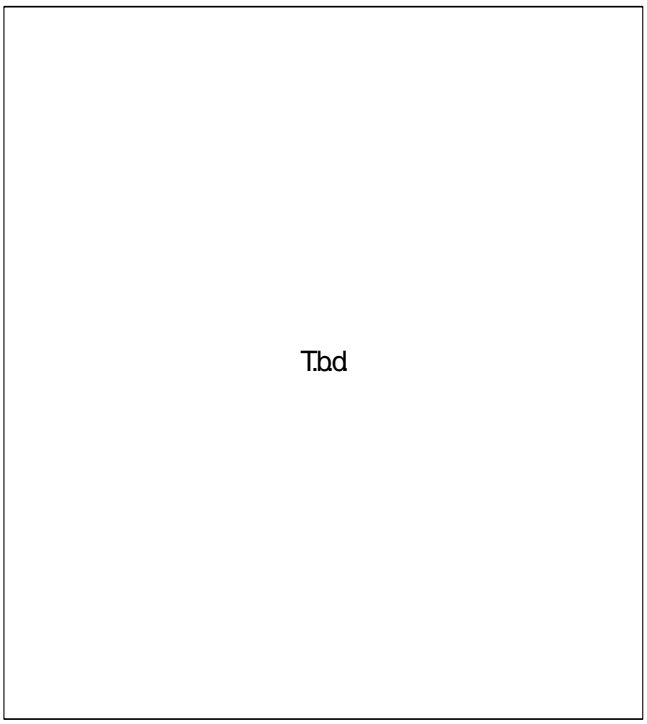


Figure 3-2 Top Side of TDK 5101 F-Testboard with 50 Ω-Output

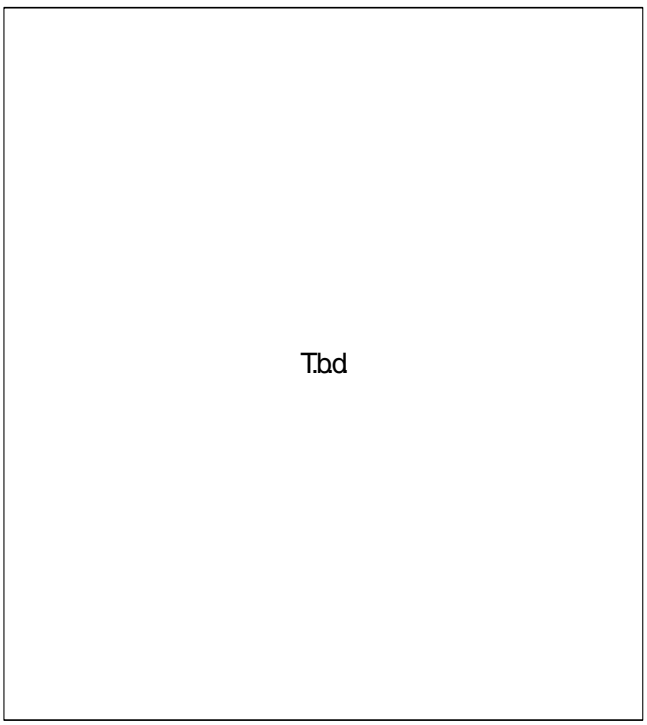


Figure 3-3 Bottom Side of TDK 5101 F-Testboard with 50 Ω-Output

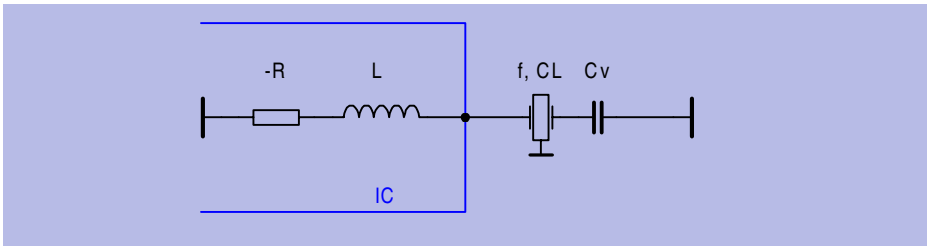
3.3 Bill of material (50 Ohm-Output Testboard)

The bill of materials is to be determined.

3.4 Application Hints on the Crystal Oscillator

1. Application Hints on the crystal oscillator

The crystal oscillator achieves a turn on time less than 1 msec when the specified crystal is used. To achieve this, a NIC oscillator type is implemented in the TDK 5101 F. The input impedance of this oscillator is a negative resistance in series to an inductance. Therefore the load capacitance of the crystal CL (specified by the crystal supplier) is transformed to the capacitance Cv.



$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 L}$$ Formula 1)

CL: crystal load capacitance for nominal frequency

ω: angular frequency

L: inductance of the crystal oscillator

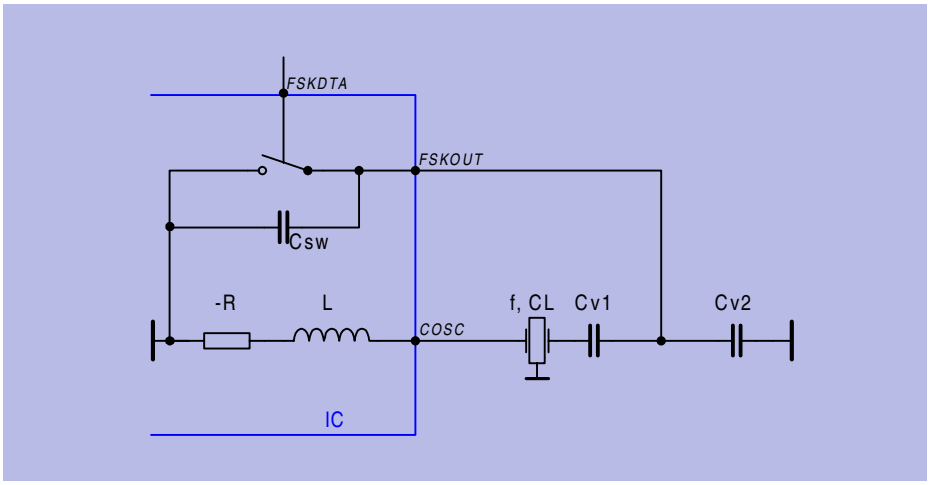
Example for the ASK-Mode:

Referring to the application circuit, in ASK-Mode the capacitance C7 is replaced by a short to ground. Assume a crystal frequency of 9.84 MHz and a crystal load capacitance of CL = 12 pF. The inductance L at 9.84 MHz is about 4.4 µH. Therefore C6 is calculated to 10 pF.

$$Cv = \frac{1}{\frac{1}{CL} + \omega^2 L} = C6$$

Example for the FSK-Mode:

FSK modulation is achieved by switching the load capacitance of the crystal as shown below.



The frequency deviation of the crystal oscillator is multiplied with the divider factor N of the Phase Locked Loop to the output of the power amplifier. In case of small frequency deviations (up to +/- 1000 ppm), the two desired load capacitances can be calculated with the formula below.

$$CL\pm = \frac{CL \mp C0\frac{\Delta f}{N * f1}(1+\frac{2(C0 \mp CL)}{C1})}{1 \pm \frac{\Delta f}{N * f1}(1+\frac{2(C0+CL)}{C1})}$$

C_L: crystal load capacitance for nominal frequency
C_0: shunt capacitance of the crystal
f: frequency
ω: $\omega = 2\pi f$: angular frequency
N: division ratio of the PLL
df: peak frequency deviation

Because of the inductive part of the TDK 5101 F, these values must be corrected by Formula 1. The value of Cv± can be calculated.

$$Cv\pm = \frac{1}{\frac{1}{CL\pm} + \omega^2 L}$$

If the FSK switch is closed, Cv_ is equal to Cv1 (C6 in the application diagram). If the FSK switch is open, Cv2 (C7 in the application diagram) can be calculated.

$$Cv2 = C7 = \frac{Csw * Cv1 - (Cv+) * (Cv1 + Csw)}{(Cv+) - Cv1}$$

Csw: parallel capacitance of the FSK switch (3 pF incl. layout parasitics)

Remark: These calculations are only approximations. The necessary values depend on the layout also and must be adapted for the specific application board.

3.5 Design Hints on the Clock Output (CLKOUT)

The CLKOUT pin is an open collector output. An external pull up resistor (RL) should be connected between this pin and the positive supply voltage. The value of RL is depending on the clock frequency and the load capacitance CLD (PCB board plus input capacitance of the microcontroller). RL can be calculated to:

$$RL = \frac{1}{fCLKOUT * 8 * CLD}$$

Table 3-1

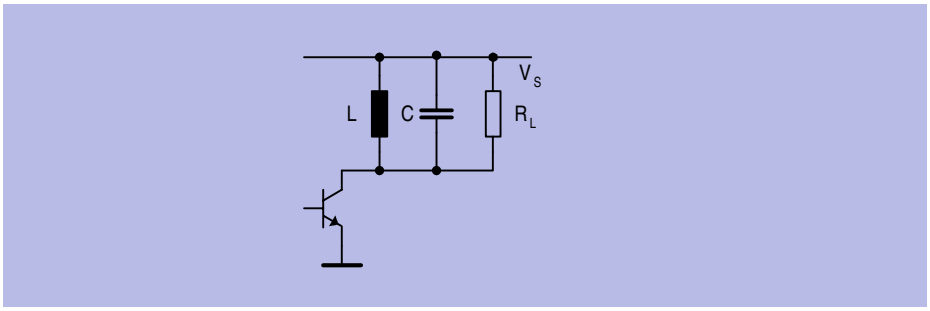
fCLKOUT = 615.2 kHz	
CL[pF]	RL[kOhm]
5	39
10	18
20	10

Remark: To achieve a low current consumption and a low spurious radiation, the largest possible RL should be chosen.

Even harmonics of the signal at CLKOUT can interact with the crystal oscillator input COSC preventing the start-up of oscillation. Care must be taken in layout by sufficient separation of the signal lines to ensure sufficiently small coupling.

3.6 Application Hints on the Power-Amplifier

The power amplifier operates in a high efficient class C mode. This mode is characterized by a pulsed operation of the power amplifier transistor at a current flow angle of $\theta << \pi$. A frequency selective network at the amplifier output passes the fundamental frequency component of the pulse spectrum of the collector current to the load. The load and its resonance transformation to the collector of the power amplifier can be generalized by the equivalent circuit of Figure 3-4. The tank circuit L//C//RL in parallel to the output impedance of the transistor should be in resonance at the operating frequency of the transmitter.



Equivalent_power_wmf.

Figure 3-4 Equivalent power amplifier tank circuit

The optimum load at the collector of the power amplifier for “critical” operation under idealized conditions at resonance is:

$$R_{LC} = \frac{V_S^2}{2 * P_O}$$

The theoretical value of R_{LC} for an RF output power of P_o= 5 dBm (3.16 mW) is:

$$R_{LC} = \frac{3^2}{2 * 0.00316} = 1423\,\Omega$$

“Critical” operation is characterized by the RF peak voltage swing at the collector of the PA transistor to just reach the supply voltage V_S.
The high degree of efficiency under “critical” operating conditions can be explained by the low power losses at the transistor. During the conducting phase of the transistor, its collector voltage is very small. This way the power loss of the transistor, equal to $i_C * u_{CE}$, is minimized. This is particularly true for small current flow angles of $\theta << \pi$.
In practice the RF-saturation voltage of the PA transistor and other parasitics reduce the “critical” R_{LC}.

The output power P_o is reduced by operating in an “overcritical” mode characterised by $R_L > R_{LC}$.
The power efficiency (and the bandwidth) increase when operating at a slightly higher R_L, as shown in Figure 3-5.
The collector efficiency E is defined as

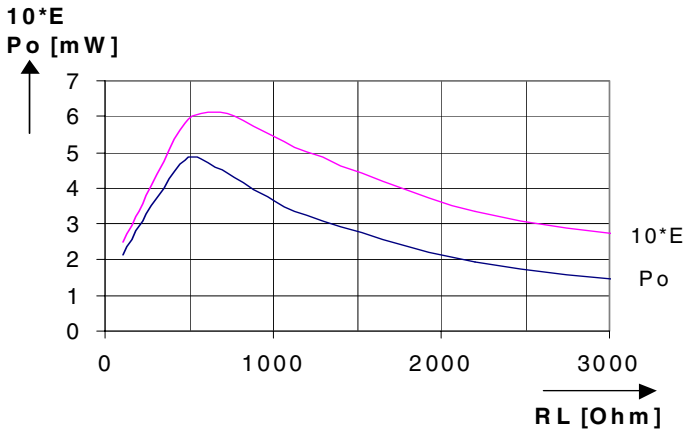
$$E = \frac{P_O}{V_S I_C}$$

The diagram of Figure 3-5 was measured directly at the PA-output at V_S = 3 V. Losses in the matching circuitry decrease the output power by about 1.5 dB. As can be seen from the diagram, 550 Ω is the optimum impedance for operation at 3 V. For an approximation of R_{OPT} and P_{OUT} at other supply voltages those two formulas can be used:

$$R_{OPT} \sim V_S$$

and

$$P_{OUT} \sim R_{OPT}$$

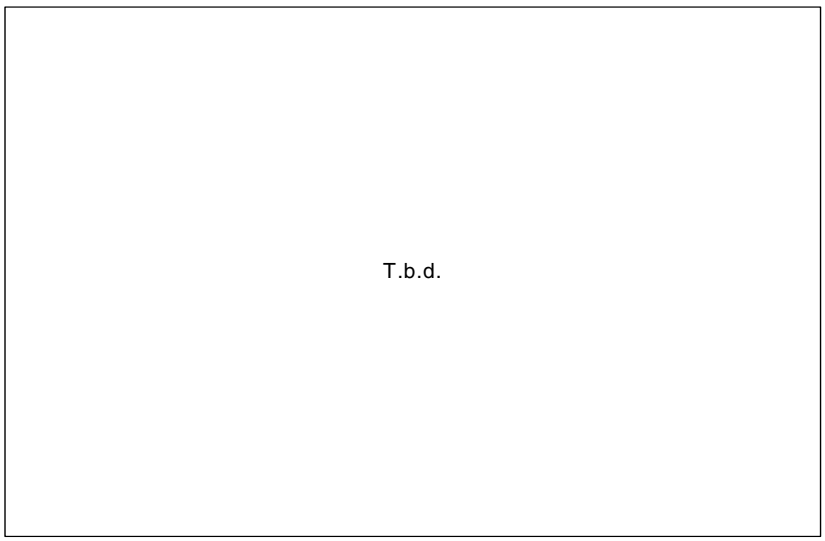


Power_output.wmf

Figure 3-5 Output power P_o (mW) and collector efficiency E vs. load resistor R_L.

The DC collector current I_c of the power amplifier and the RF output power P_o vary with the load resistor R_L. This is typical for overcritical operation of class C amplifiers. The collector current will show a characteristic dip at the resonance frequency for this type of “overcritical” operation. The depth of this dip will increase with higher values of R_L.

As Figure 3-6 shows, detuning beyond the bandwidth of the matching circuit results in an increase of the collector current of the power amplifier and in some loss of output power. This diagram shows the data for the circuit of the test board at the frequency of 315 MHz The effective load resistance of this circuit is R_L =550 Ω, which is the optimum impedance for operation at 3 V. This will lead to a dip of the collector current of approx. 40%.



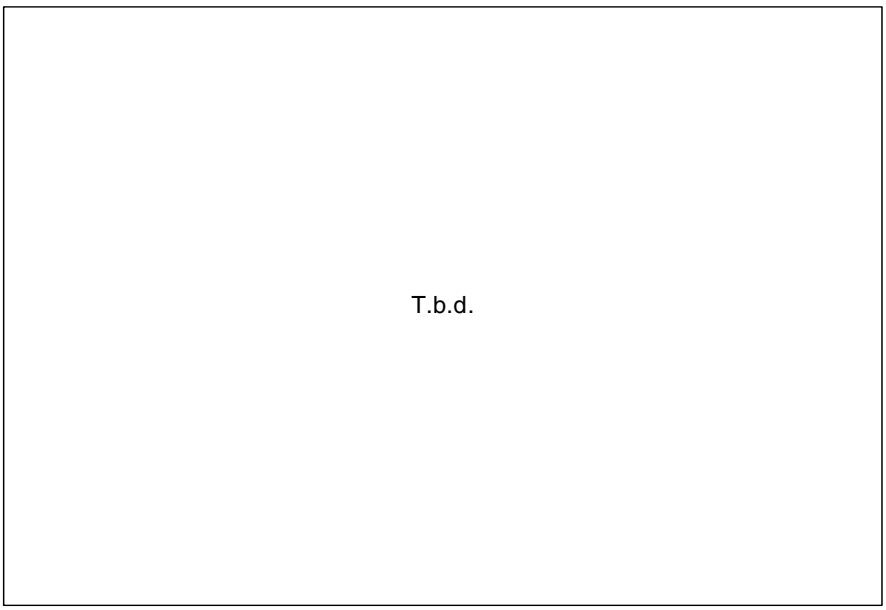
tbd.wmf

Figure 3-6 Output power and collector current vs. frequency

C3, L2-C2 and C8 are the main matching components which are used to transform the 50 Ω load at the SMA-RF-connector to a higher impedance at the PA-output (550 Ω @ 3 V). L1 can be used for some finetuning of the resonant frequency but should not become too small in order to keep its losses low.

The transformed impedance of 550+j0 Ω at the PA-output-pin can be verified with a network analyzer using the following measurement procedure:

1. Calibrate your network analyzer.
2. Connect some short, low-loss 50 Ω cable to your network analyzer with an open end on one side. Semirigid cable works best.
3. Use the „Port Extension“ feature of your network analyzer to shift the reference plane of your network analyzer to the open end of the cable.
4. Connect the center-conductor of the cable to the solder pad of the pin „PA“ of the IC. The outer conductor has to be grounded. Very short connections have to be used. Do not remove the IC or any part of the matching-components!
5. Screw a 50 Ω dummy-load on the RF-I/O-SMA-connector
6. Be sure that your network analyzer is AC-coupled and turn on the power supply of the IC. The TDK 5101 F must not be in Transmit-Mode.
7. Measure the S-parameter S11



tbd.wmf

Figure 3-7 S-parameters of the load at the PA-output

Above you can see the measurement of the evalboard with a span of 100 MHz. The evalboard has been optimized for 3 V. The load is about 550+j0 Ω at the transmit frequency.

A tuning-free realization requires a careful design of the components within the matching network. A simple linear CAE-tool will help to see the influence of tolerances of matching components.

Suppression of spurious harmonics may require some additional filtering within the antenna matching circuit. The total spectrum of a typical 50 Ω-Output testboard can be summarized as:

Table 3-2

Frequency	Output Power 315 MHz Testboard
Fundamental	+5 dBm
Fund – 9.84 MHz	t.b.d.
Fund + 9.84 MHz	t.b.d.
2^{nd} harmonic	t.b.d.
3^{rd} harmonic	t.b.d.

4 Reference

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4.1 Absolute Maximum Ratings

The AC / DC characteristic limits are not guaranteed. The maximum ratings must not be exceeded under any circumstances, not even momentarily and individually, as permanent damage to the IC may result.

Table 4-1

Parameter	Symbol	Limit Values		Unit	Remarks
		Min	Max		
Junction Temperature	T_J	–40	+150	°C	
Storage Temperature	T_s	–40	+125	°C	
Thermal Resistance	R_{thJA}		t.b.d.	K/W	
Supply voltage	V_S	–0.3	+4.0	V	
Voltage at any pin excluding pin 9	V_{pins}	-0.3	V_S + 0.3	V	
Voltage at pin 9	V_{pin9}	-0.3	2 * V_S	V	No ESD-Diode to V_S
Current into pin 4	I_{pin4}	-10	10	mA	
ESD integrity, all pins	V_{ESD}	-1	+1	kV	JEDEC Standard JESD22-A114-B
ESD integrity, all pins excluding pin 9	V_{ESD}	-2	+2	kV	JEDEC Standard JESD22-A114-B

Ambient Temperature under bias: T_A = –40°C to +125°C

Note: All voltages referred to ground (pins) unless stated otherwise.

Pins 3 and 8 are grounded.

4.2 Operating Range

Within the operational range the IC operates as described in the circuit description.

Table 4-2

Parameter	Symbol	Limit Values		Unit	Test Conditions
		Min	Max		
Supply voltage	V_S	2.1	4.0	V	
Ambient temperature	T_A	-40	125	°C	

4.3 AC/DC Characteristics

4.3.1 AC/DC Characteristics at 3V, 25°C

Table 4-3 Supply Voltage V_S = 3 V, Ambient temperature T_{amb} = 25°C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
Current consumption						
Power Down mode	$I_{S\ PDWN}$		0.3	100	nA	V (Pins 10, 6 and 7) < 0.2 V
PLL Enable mode	$I_{S\ PLL_EN}$		3.5	4.2	mA	
Transmit mode 315 MHz	$I_{S\ TRANSM}$		7		mA	
Output frequency						
Output frequency	f_{OUT}		315		MHz	$f_{OUT} = 32 * f_{COSC}$
Clock Driver Output (Pin 1)						
Output current (High)	I_{CLKOUT}			5	µA	$V_{CLKOUT} = V_S$
Saturation Voltage (Low)[1)]	V_{SATL}			0.56	V	I_{CLKOUT} = 1 mA
FSK Switch Output (Pin 4)						
On resistance	R_{FSKOUT}			250	Ω	V_{FSKDTA} = 0 V
On capacitance	C_{FSKOUT}			6	pF	V_{FSKDTA} = 0 V
Off resistance	R_{FSKOUT}	10			kΩ	$V_{FSKDTA} = V_S$
Off capacitance	C_{FSKOUT}			1.5	pF	$V_{FSKDTA} = V_S$
Crystal Oscillator Input (Pin 5)						
Load capacitance	$C_{COSCmax}$			5	pF	
Serial Resistance of the crystal				100	Ω	f = 9.84 MHz
Input inductance of the COSC pin			4.6		µH	f = 9.84 MHz
ASK Modulation Data Input (Pin 6)						
ASK Transmit disabled	V_{ASKDTA}	0		0.5	V	
ASK Transmit enabled	V_{ASKDTA}	1.5		V_S	V	
Input bias current ASKDTA	I_{ASKDTA}			30	µA	$V_{ASKDTA} = V_S$
Input bias current ASKDTA	I_{ASKDTA}	-20			µA	V_{ASKDTA} = 0 V
ASK data rate	f_{ASKDTA}			20	kHz	

Table 4-3 Supply Voltage V_S = 3 V, Ambient temperature T_{amb} = 25°C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
FSK Modulation Data Input (Pin 7)						
FSK Switch on	V_{FSKDTA}	0		0.5	V	
FSK Switch off	V_{FSKDTA}	1.5		V_S	V	
Input bias current FSKDTA	I_{FSKDTA}			30	µA	$V_{FSKDTA} = V_S$
Input bias current FSKDTA	I_{FSKDTA}	-20			µA	V_{FSKDTA} = 0 V
FSK data rate	f_{FSKDTA}			20	kHz	
Power Amplifier Output (Pin 9)						
Output Power[2] at 315 MHz transformed to 50 Ohm	P_{OUT315}		5		dBm	
Power Down Mode Control (Pin 10)						
Power Down mode	V_{PDWN}	0		0.7	V	$V_{ASKDTA} < 0.2$ V $V_{FSKDTA} < 0.2$ V
PLL Enable mode	V_{PDWN}	1.5		V_S	V	$V_{ASKDTA} < 0.5$ V
Transmit mode	V_{PDWN}	1.5		V_S	V	$V_{ASKDTA} > 1.5$ V
Input bias current PDWN	I_{PDWN}			30	µA	$V_{PDWN} = V_S$

1) Derating linearly to a saturation voltage of max. 140 mV at I_{CLKOUT} = 0 mA
2) Power amplifier in overcritical C-operation
Matching circuitry as used in the 50 Ohm-Output Testboard at the specified frequency.
Tolerances of the passive elements not taken into account.

4.3.2 AC/DC Characteristics at 2.1 V ... 4.0 V, -40°C ... +125°C

Table 4-4 Supply Voltage V_S = 2.1 V ... 4.0 V, Ambient temperature T_{amb} = -40°C ... +125°C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
Current consumption						
Power Down mode	$I_{S\ PDWN}$			4	µA	V (Pins 10, 6 and 7) < 0.2 V
PLL Enable mode	$I_{S\ PLL_EN}$		3.5	4.6	mA	
Transmit mode	$I_{S\ TRANSM}$		7		mA	
Output frequency						
Output frequency[1)]	f_{OUT}		315		MHz	$f_{OUT} = 32 * f_{COSC}$
Clock Driver Output (Pin 1)						
Output current (High)	I_{CLKOUT}			5	µA	$V_{CLKOUT} = V_S$
Saturation Voltage (Low)[2)]	V_{SATL}			0.5	V	I_{CLKOUT} = 0.6 mA
FSK Switch Output (Pin 4)						
On resistance	R_{FSKOUT}			280	Ω	V_{FSKDTA} = 0 V
On capacitance	C_{FSKOUT}			6	pF	V_{FSKDTA} = 0 V
Off resistance	R_{FSKOUT}	10			kΩ	$V_{FSKDTA} = V_S$
Off capacitance	C_{FSKOUT}			1.5	pF	$V_{FSKDTA} = V_S$
Crystal Oscillator Input (Pin 5)						
Load capacitance	$C_{COSCmax}$			5	pF	
Serial Resistance of the crystal				100	Ω	f = 9.84 MHz
Input inductance of the COSC pin			4.6		µH	f = 9.84 MHz
ASK Modulation Data Input (Pin 6)						
ASK Transmit disabled	V_{ASKDTA}	0		0.5	V	
ASK Transmit enabled	V_{ASKDTA}	1.5		V_S	V	
Input bias current ASKDTA	I_{ASKDTA}			33	µA	$V_{ASKDTA} = V_S$
Input bias current ASKDTA	I_{ASKDTA}	-20			µA	V_{ASKDTA} = 0 V
ASK data rate	f_{ASKDTA}			20	kHz	

Table 4-4 Supply Voltage V_S = 2.1 V ... 4.0 V, Ambient temperature T_{amb} = -40°C ... +125°C

Parameter	Symbol	Limit Values			Unit	Test Conditions
		Min	Typ	Max		
FSK Modulation Data Input (Pin 7)						
FSK Switch on	V_{FSKDTA}	0		0.5	V	
FSK Switch off	V_{FSKDTA}	1.5		V_S	V	
Input bias current FSKDTA	I_{FSKDTA}			33	µA	$V_{FSKDTA} = V_S$
Input bias current FSKDTA	I_{FSKDTA}	-20			µA	V_{FSKDTA} = 0 V
FSK data rate	f_{FSKDTA}			20	kHz	
Power Amplifier Output (Pin 9)						
Output Power 3) at 315 MHz transformed to 50 Ohm.	$P_{OUT, 315}$				dBm	V_S = 2.1 V
	$P_{OUT, 315}$		5		dBm	V_S = 3.0 V
	$P_{OUT, 315}$				dBm	V_S = 4.0 V
Power Down Mode Control (Pin 10)						
Power Down mode	V_{PDWN}	0		0.5	V	V_{ASKDTA} < 0.2 V V_{FSKDTA} < 0.2 V
PLL Enable mode	V_{PDWN}	1.5		V_S	V	V_{ASKDTA} < 0.5 V
Transmit mode	V_{PDWN}	1.5		V_S	V	V_{ASKDTA} > 1.5 V
Input bias current PDWN	I_{PDWN}			38	µA	$V_{PDWN} = V_S$

1) a) When the minimum T_A is increased by tbd.°C, the minimum f_{VCO} decreases by 1 MHz.
b) When the maximum T_A is decreased by tbd.°C, the maximum f_{VCO} increases by 1 MHz.
c) When the minimum V_S is increased by tbd. mV, the maximum f_{VCO} increases by 1 MHz.
Restriction of c): The maximum f_{VCO} must not be increased by more than tbd. MHz by increasing V_S.

All three measures can be taken independently and additive.

2) Derating linearly to a saturation voltage of max. 140 mV at I_{CLKOUT} = 0 mA

3) Matching circuitry as used in the 50 Ohm-Output Testboard.
Tolerances of the passive elements not taken into account.
Range @ 2.1 V, +25°C: dBm +/- dBm
Typ. temperature dependency at 2.1 V: + dBm@-40°C and - dBm@+125°C, reference +25°C
Range @ 3.0 V, +25°C: 5.0 dBm +/- dBm
Typ. temperature dependency at 3.0 V: + dBm@-40°C and - dBm@+125°C, reference +25°C
Range @ 4.0 V, +25°C: dBm +/- dBm
Typ. temperature dependency at 4.0 V: + dBm@-40°C and - dBm@+125°C, reference +25°C