

NTZD3152P

Small Signal MOSFET

–20 V, –430 mA, Dual P-Channel
with ESD Protection, SOT–563

Features

- Low $R_{DS(on)}$ Improving System Efficiency
- Low Threshold Voltage
- ESD Protected Gate
- Small Footprint 1.6 x 1.6 mm
- These are Pb-Free Devices

Applications

- Load/Power Switches
- Power Supply Converter Circuits
- Battery Management
- Cell Phones, Digital Cameras, PDAs, Pagers, etc.

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V_{DSS}	–20	V
Gate-to-Source Voltage			V_{GS}	±6.0	V
Continuous Drain Current (Note 1)	Steady State	$T_A = 25^{\circ}\text{C}$	I_D	–430	mA
		$T_A = 85^{\circ}\text{C}$		–310	
Power Dissipation (Note 1)	Steady State		P_D	250	mW
Continuous Drain Current (Note 1)	$t \leq 5\text{ s}$	$T_A = 25^{\circ}\text{C}$	I_D	–455	mA
		$T_A = 85^{\circ}\text{C}$		–328	
Power Dissipation (Note 1)	$t \leq 5\text{ s}$		P_D	280	mW
Pulsed Drain Current	$t_p = 10\text{ }\mu\text{s}$		I_{DM}	–750	mA
Operating Junction and Storage Temperature			T_J , T_{STG}	–55 to 150	$^{\circ}\text{C}$
Source Current (Body Diode)			I_S	–350	mA
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)			T_L	260	$^{\circ}\text{C}$

THERMAL RESISTANCE RATINGS

Parameter	Symbol	Max	Unit
Junction-to-Ambient – Steady State (Note 1)	$R_{\theta JA}$	500	$^\circ\text{C/W}$
Junction-to-Ambient – $t \leq 5\text{ s}$ (Note 1)		447	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

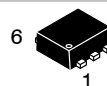
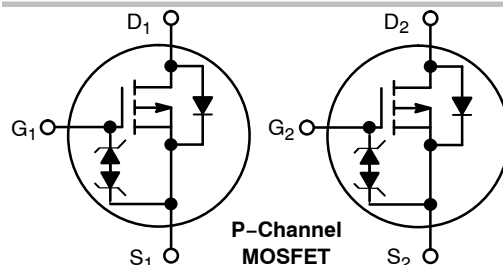
1. Surface mounted on FR4 board using 1 in. sq. pad size
(Cu. area = 1.127 in. sq. [1 oz.] including traces).



ON Semiconductor®

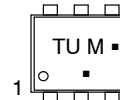
<http://onsemi.com>

$V_{(BR)DSS}$	$R_{DS(on)}$ Typ	I_D Max
–20 V	0.5 Ω @ –4.5 V	–430 mA
	0.6 Ω @ –2.5 V	
	1.0 Ω @ –1.8 V	



SOT–563–6
CASE 463A

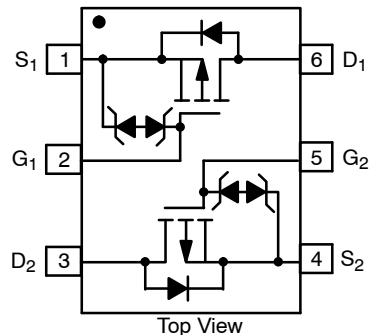
MARKING DIAGRAM



TU = Specific Device Code
M = Date Code
▪ = Pb-Free Package

(Note: Microdot may be in either location)

PINOUT: SOT–563



Top View

ORDERING INFORMATION

Device	Package	Shipping†
NTZD3152PT1G	SOT–563 (Pb-Free)	4000 / Tape & Reel
NTZD3152PT1H		
NTZD3152PT5G	SOT–563 (Pb-Free)	8000 / Tape & Reel
NTZD3152PT5H		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NTZD3152P

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted.)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\text{ }\mu\text{A}$	-20			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			18		mV/°C
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, T_J = 25^\circ\text{C}$			-1.0	μA
		$V_{DS} = -16\text{ V}, T_J = 125^\circ\text{C}$			-2.0	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 4.5\text{ V}$			± 2.0	μA

ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\text{ }\mu\text{A}$	-0.45		-1.0	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-1.9		mV/°C
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -4.5\text{ V}, I_D = -430\text{ mA}$		0.5	0.9	Ω
		$V_{GS} = -2.5\text{ V}, I_D = -300\text{ mA}$		0.6	1.2	
		$V_{GS} = -1.8\text{ V}, I_D = -150\text{ mA}$		1.0	2.0	
Forward Transconductance	g_{FS}	$V_{DS} = -10\text{ V}, I_D = -430\text{ mA}$		1.0		S

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}, V_{DS} = -16\text{ V}$		105	175	pF
Output Capacitance	C_{OSS}			15	30	
Reverse Transfer Capacitance	C_{RSS}			10	20	
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -4.5\text{ V}, V_{DS} = -10\text{ V}, I_D = -215\text{ mA}$		1.7	2.5	nC
Threshold Gate Charge	$Q_{G(TH)}$			0.1		
Gate-to-Source Charge	Q_{GS}			0.3		
Gate-to-Drain Charge	Q_{GD}			0.4		

SWITCHING CHARACTERISTICS (Note 3)

Turn-On Delay Time	$t_{d(on)}$	$V_{GS} = -4.5\text{ V}, V_{DD} = -10\text{ V}, I_D = -215\text{ mA}, R_G = 10\text{ }\Omega$		10		ns
Rise Time	t_r			12		
Turn-Off Delay Time	$t_{d(off)}$			35		
Fall Time	t_f			19		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = -350\text{ mA}$	$T_J = 25^\circ\text{C}$		-0.8	-1.2	V
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, di_{SD}/dt = 100\text{ A}/\mu\text{s}, I_S = -350\text{ mA}$			13		ns

2. Pulse Test: pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.

3. Switching characteristics are independent of operating junction temperatures.

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

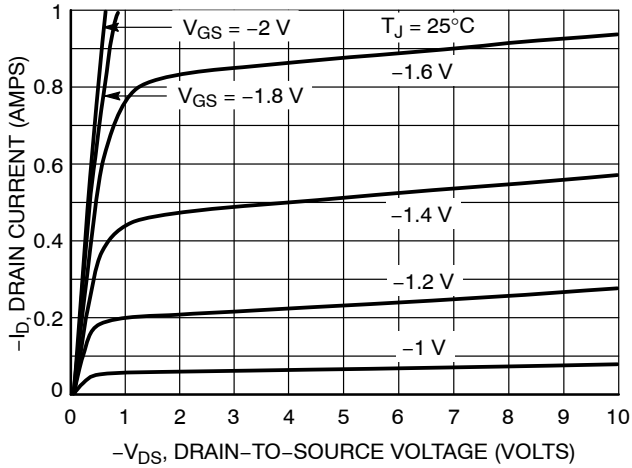


Figure 1. On-Region Characteristics

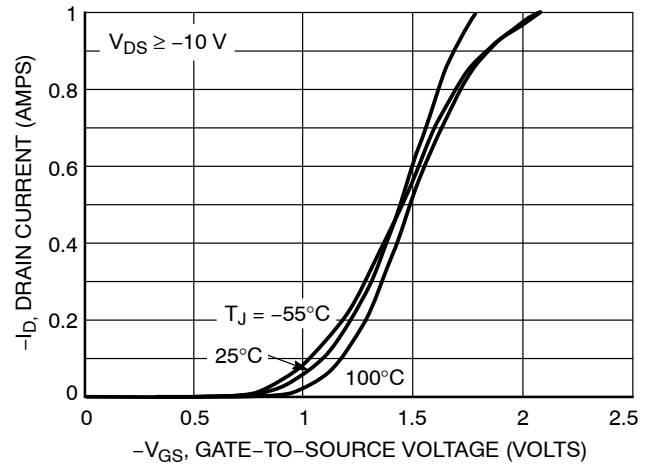


Figure 2. Transfer Characteristics

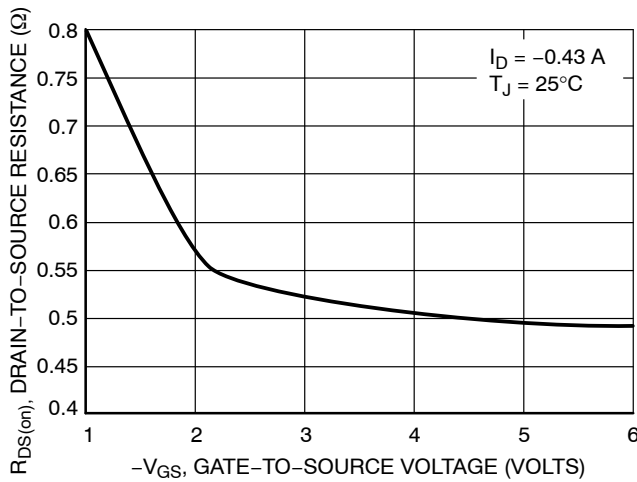


Figure 3. On-Resistance vs. Gate-to-Source Voltage

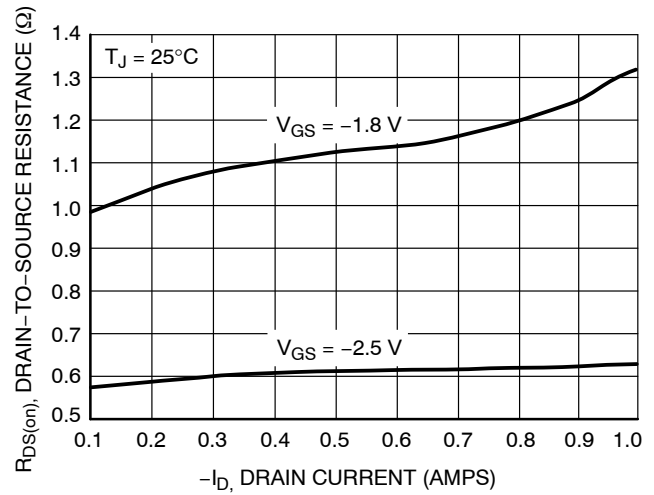


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

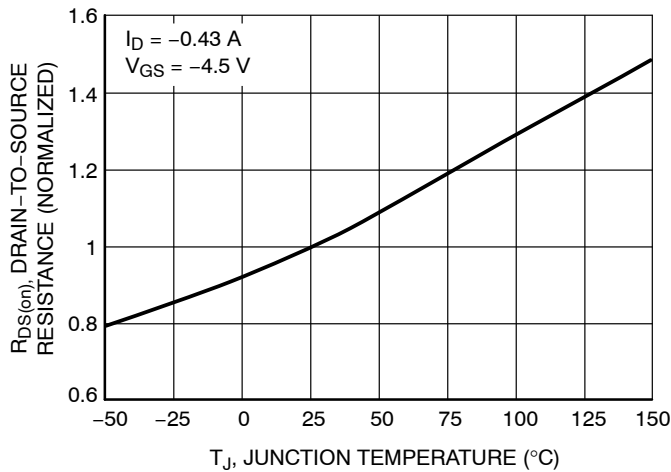


Figure 5. On-Resistance Variation with Temperature

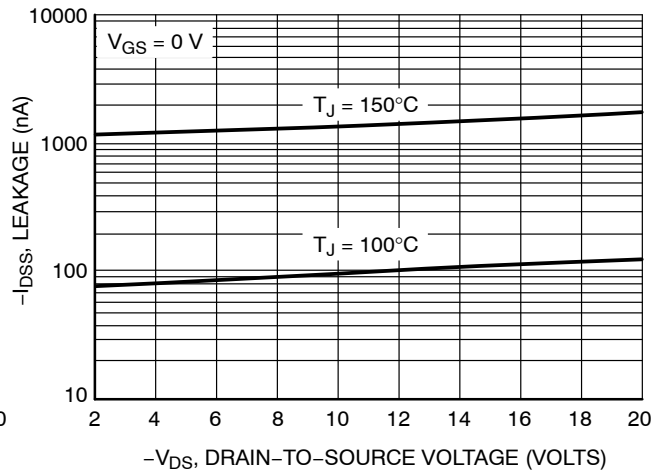


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL PERFORMANCE CURVES ($T_J = 25^\circ\text{C}$ unless otherwise noted)

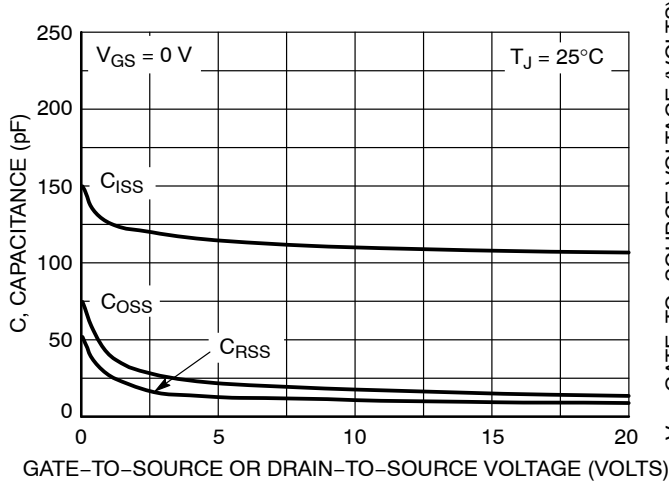


Figure 7. Capacitance Variation

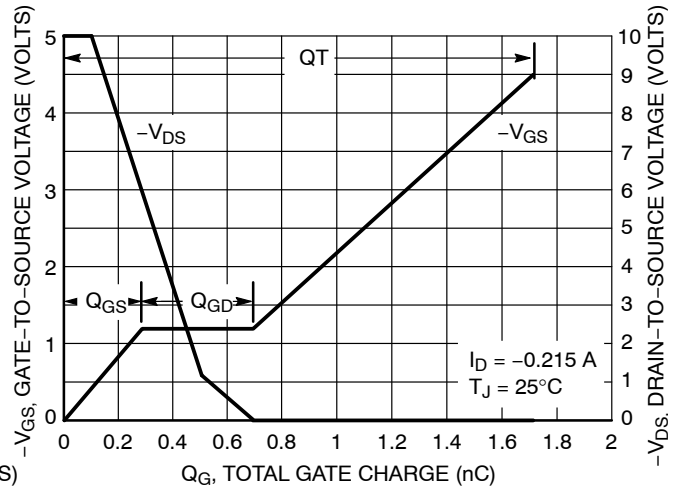


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

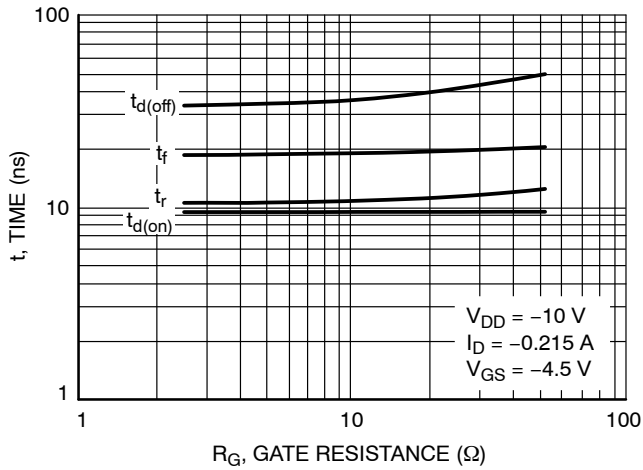


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

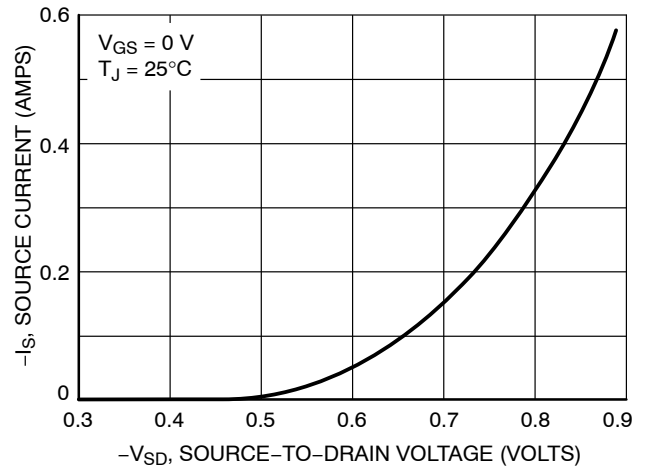
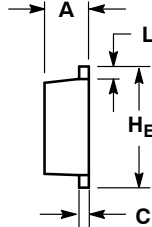
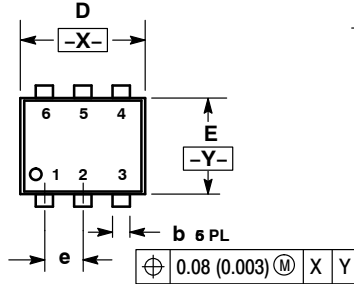


Figure 10. Diode Forward Voltage vs. Current

NTZD3152P

PACKAGE DIMENSIONS

SOT-563, 6 LEAD
CASE 463A-01
ISSUE F

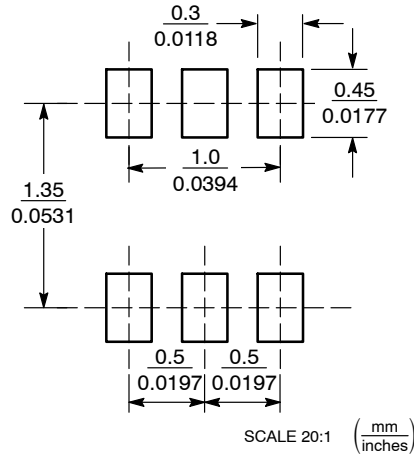


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH THICKNESS. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.50	0.55	0.60	0.020	0.021	0.023
b	0.17	0.22	0.27	0.007	0.009	0.011
C	0.08	0.12	0.18	0.003	0.005	0.007
D	1.50	1.60	1.70	0.059	0.062	0.066
E	1.10	1.20	1.30	0.043	0.047	0.051
e	0.5 BSC			0.02 BSC		
L	0.10	0.20	0.30	0.004	0.008	0.012
H _E	1.50	1.60	1.70	0.059	0.062	0.066

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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