NETWORK SEARCH ENGINE
32K x 72 Entries

Datasheet Brief 75N43102

To request the full IDT75N43102 datasheet, please contact your local IDT Sales Representative or call 1-831-754-4555

Device Description

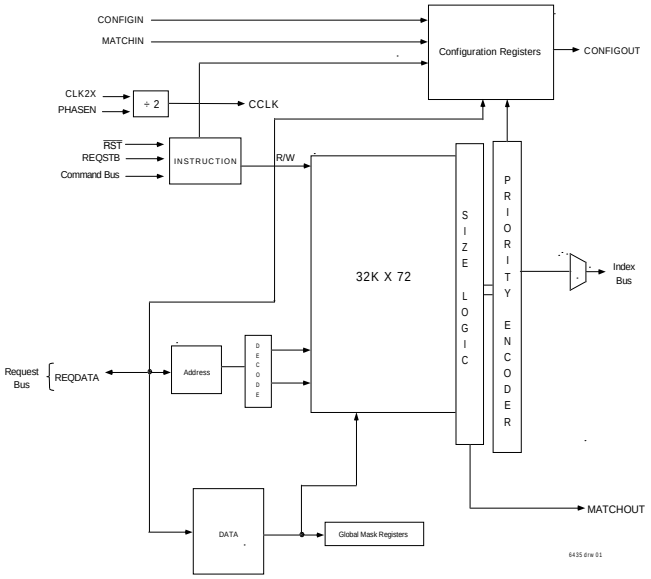
IDT provides proven, industry-leading network search engines (NSEs) that enable and accelerate the intelligent processing of network services in communications equipment. As a part of the complete IDT classification subsystem that includes content inspection engines, the IDT family of NSEs delivers high-performance, feature-rich, easy-to-use, integrated search accelerators.

The IDT 75N43102 is ideally suited for cost-sensitive applications in the enterprise and access markets. It is a full-ternary 32K x 72 entry device where each entry location in the NSE has both a Data entry and an associated Mask entry. The NSE devices integrate content addressable memory (CAM) technology with high-performance logic. The device can perform Lookup operations plus Read and Write maintenance operations.

The IDT 75N43102 NSE device has a bi-directional bus that is a multiplexed address and data bus that can support 62.5 million sustained searches per second. This device can be configured to enable multiple width lookups from 72 to 288 bits wide. The IDT 75N43102 requires a 1.5-volt V_{DD1} supply and a 2.5-volt V_{DD2} supply.

The IDT 75N43102 NSE utilizes the latest high-performance 1.5V CMOS processing technology and is packaged in a JEDEC Standard, 256 pin low profile Ball Grid Array.

Block Diagram

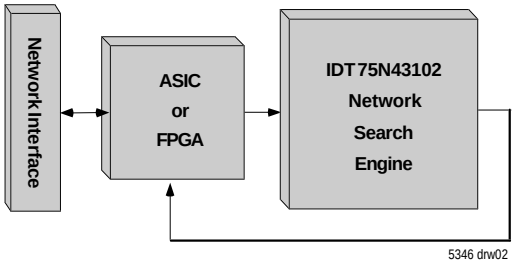


System Configurations

The IDT NSEs are designed to fulfill the needs of various types of networking systems. In solutions requiring data searching such as routers, a system configuration as shown in Figure 1.0 may be realized.

In this compatible configuration, the NSE interfaces directly to an ASIC/ FPGA for lookups and routes an Index directly back to the ASIC/ FPGA. Control of the associated handshake signals is provided by the NSEs for this configuration.

Figure 1.0 ASIC / FPGA Compatible NSE



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Features

- Full Ternary 32K x 72 bit content addressable memory
- Global Mask Registers
- 72/144/288 multiple width lookups
- 62.5M sustained lookups per second at 72 and 144 width lookups
- Dual bus interface
- Cascadable to 2 devices with no glue logic or latency penalty
- Boundary Scan JTAG Interface (IEEE 1149.1 compliant)
- 1.5V match power supply
- 2.5V core and I/O power supply

Functional Highlights

Data and Mask Array

The NSE has Data cell entries and associated Mask cell entries as shown in Fig. 1.1. This combination of Data and Mask cell entries enables the NSE to store 0, 1 or X, making it a full ternary Network Search Engine. During a lookup operation, both arrays are used along with a Global Mask Register to find a match to a requested data word.

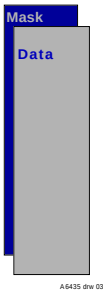


Figure 1.1

Bus Interface

The NSE utilizes a dual bus interface consisting of the NSE Request Bus and the NSE Response Bus.

The NSE Request Bus is comprised of the Command Bus and the Request Data Bus. The Command Bus handles the instruction to the NSE while the Request Data Bus is the main data path to the NSE.

The 72 bit bi-directional Request Data Bus functions as a multiplexed address and data bus, which performs the writing and reading of NSE entries, as well as presenting lookup data to the device.

The NSE Response Bus is comprised of an independent unidirectional Index Bus which drives the result of the lookup (or index) to an ASIC.

Command Bus

The Command Bus loads the specific instructions into the NSE. These include:

- Read or Write

A Read or Write instruction operates on a specified data entry, mask entry, or register.

- Lookup

A lookup can be requested in 72-bit, 144-bit or 288-bit widths. A 36-bit lookup can be accomplished by using two Global Mask Registers.

Registers

There are three basic types of registers supported:

- Configuration Registers are used at initialization to define the segmentation of the entries.
- Global Mask Registers are provided to support Lookup instructions by masking individual bits during a search.
- Reply Width Registers are used with Lookup operations.

Signal Descriptions

Pin Function	I/O	Description
NSE Buses:		
Request Strobe	Input	This input signifies a valid input request and signals the start of an NSE operation cycle.
Command Bus	Input	This defines the instruction to be performed by the NSE and selects a global mask register.
Request Data Bus	Input/Output Three State	The Request Data Bus is a multiplexed address/data bus used to perform reads (and writes) from (to) the NSE, and to present search data for lookups.
Index Bus	Output Three State	This bus is used to drive the Lookup result information directly to the NSE's ASIC/FPGA. The Index Bus contains the encoded location at which the compare was found.
Clock and Initialization:		
Clock Input	Input	All inputs and outputs are referenced to the positive edge of this clock.
Clock Phase Enable	Input	This signal is used to generate an internal clock at ½ the frequency of the input clock.
Reset	Input	This pin will force all outputs to a high impedence condition, as well as clearing the NSE enable bit.
Depth Expansion:		
Configuration	Input	Configures the Device ID at power up.
Configuration	Output	Configures the Device ID at power up.
Match Input	Input	The Match Input signal is driven by the upstream Match Output signal. This indicates to the down stream NSE that a hit in the higher priority NSE has occurred.
Match Output	Output	The Match Output signal signifies that a match has occurred in the NSE. The signal is fed into the Match Input line of the lower priority NSE.

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Revision History

REV	DATE	PAGES	DESCRIPTION
0	7/11/03	p.1-3	Initial release
A	08/14/03	p.4	Updated pinout.
B	04/12/04	All	Updated, removed pinout.