SONY

CXP828P60

CMOS 8-bit Single Chip Microcomputer

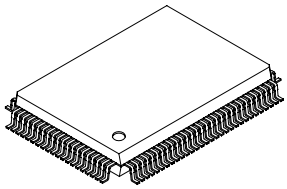
Description

The CXP828P60 is a CMOS 8-bit single chip microcomputer integrating on a single chip an A/D converter, serial interface, timer/counter, time base timer, capture timer/counter, fluorescent display panel controller/driver, remote control reception circuit, and PWM output circuit besides the basic configurations of 8-bit CPU, PROM, RAM, and I/O port.

The CXP828P60 also provides sleep/stop function that enables lower power consumption.

CXP828P60 is the PROM-incorporated version of the CXP82860 with bult-in mask ROM. This provides the additional feature of being able to write directly into the program. Thus, it is most suitable for evaluation use during system development and for small-quantity production.

100 pin QFP (Plastic)



Structure

Silicon gate CMOS IC

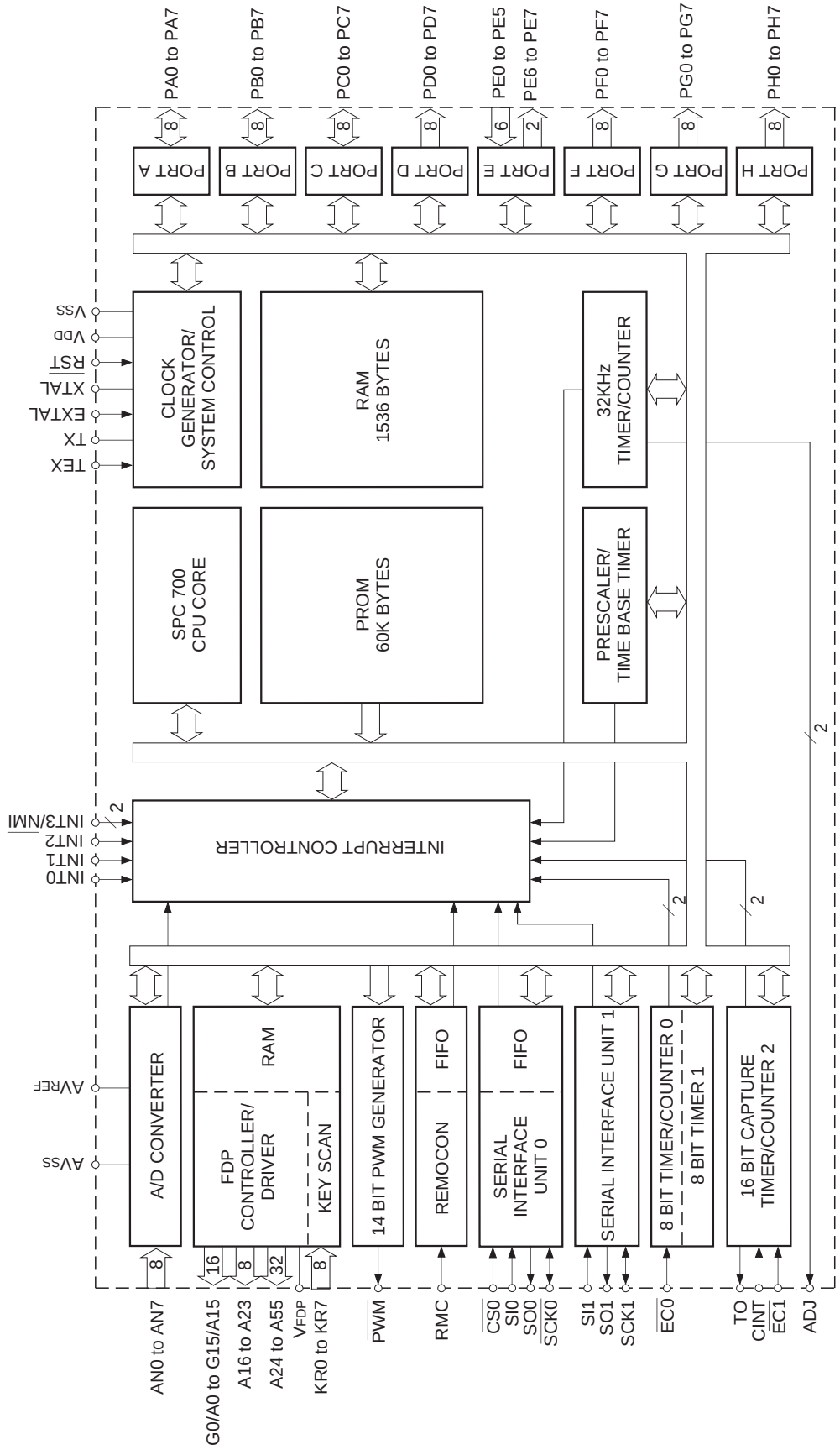
Features

- Wide-range instruction system (213 instructions) to cover various types of data
  — 16-bit arithmetic/multiplication and division/Boolean bit operation instructions
- Minimum instruction cycle — 400ns at 10MHz operation; 122µs at 32kHz operation
- Incorporated PROM capacity — 60K bytes
- Incorporated RAM capacity — 1536 bytes (including fluorescent display area)
- Peripheral functions
  - — A/D converter — 8 bist, 8 channels, successive approximation method (Conversion time of 32µs/10MHz)
  - — Serial interface — 8-bit, 8-stage FIFO incorporated (Auto transfer for 1 to 8 bytes), 1 channel; 8-bit clock synchronized type, 1 channel
  - — Timer — 8-bit timer, 8-bit timer/counter, 19-bit time base timer; 16-bit capture timer/counter, 32kHz timer/counter
  - — Fluorescent display panel controller/driver — Supports the universal grid fluorescent display panel.; High voltage drive output port of 56 pins (40V); Maximum of 640 segments display possible; Display timing number of 1 to 20; Dimmer function; Incorporated pull-down resistor; Hardware key scan function (Maximum of 16 x 8 key matrix supportable)
  - — Remote control reception circuit — 8-bit pulse measurement counter, 6-stage FIFO
  - — PWM output — 14 bits, 1 channel
- Interruption — 16 factors, 15 vectors, multi-interruption possible
- Standby mode — SLEEP/STOP
- Package — 100-pin plastic QFP

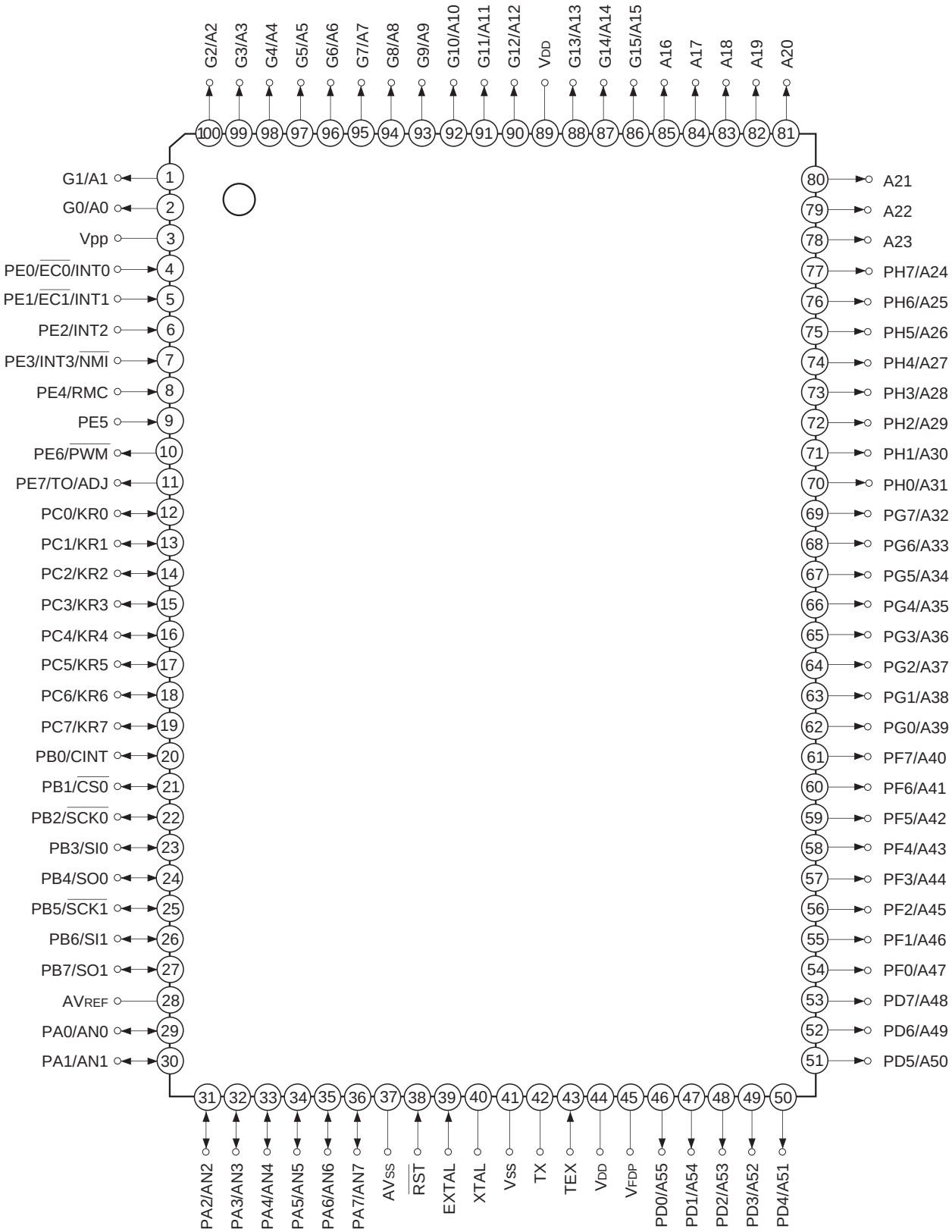
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E95Z36-ST

Block Diagram



Pin Assignment (Top View)



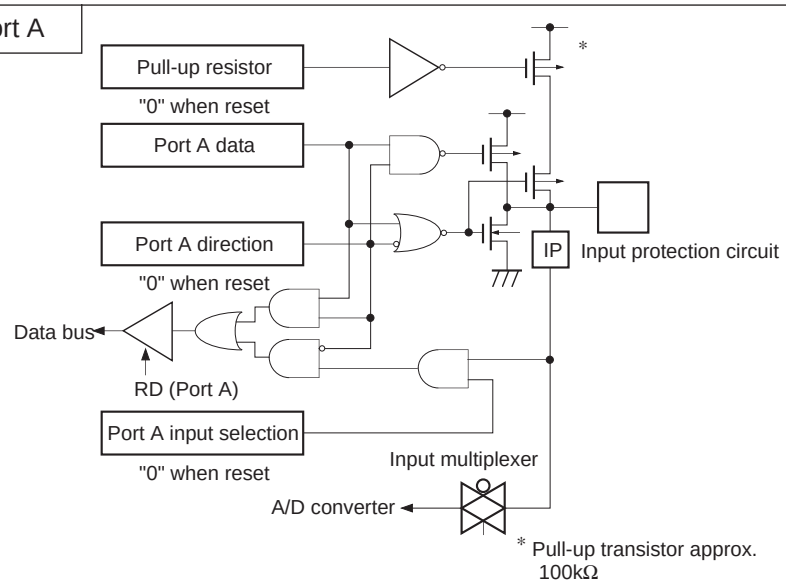
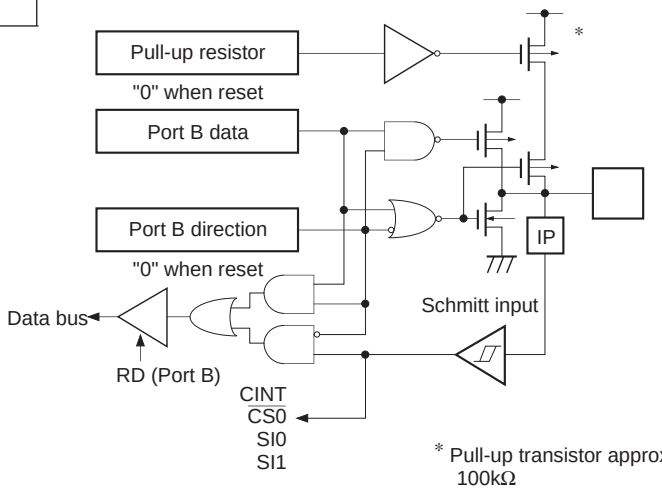
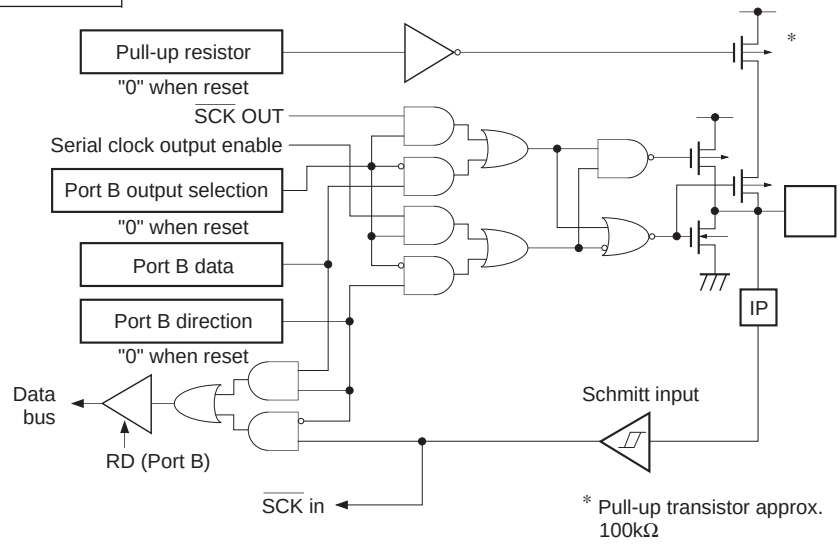
Note) Vpp (Pin 3) must be connected to V_{DD}.

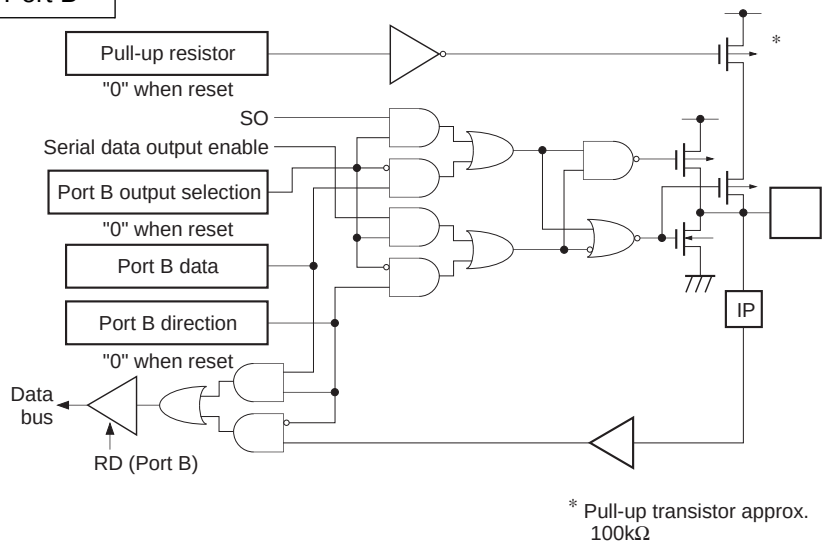
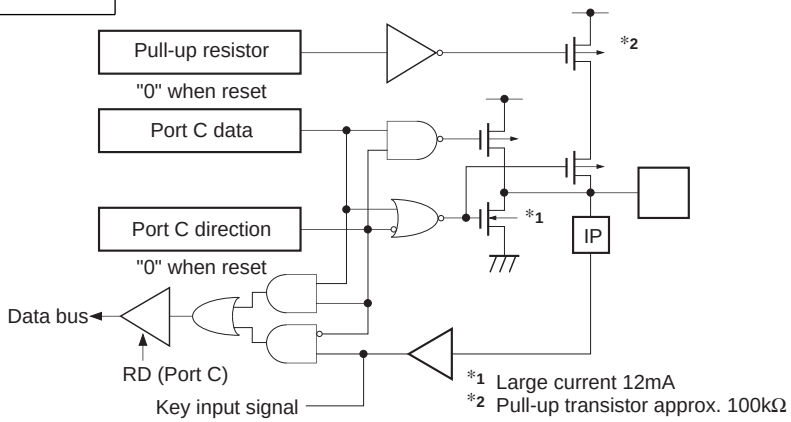
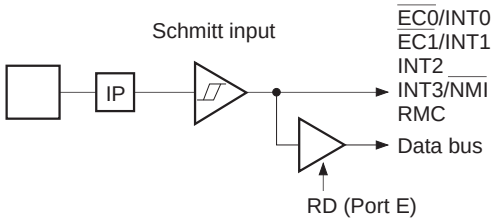
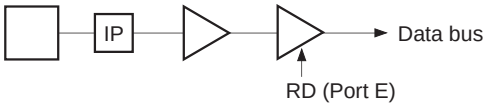
Pin Description

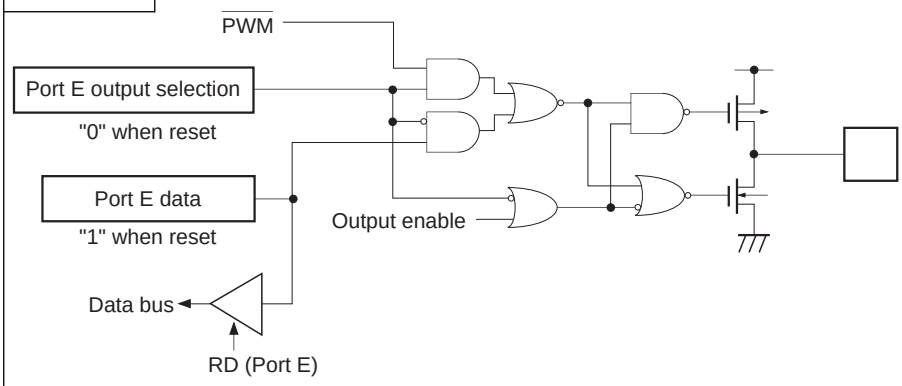
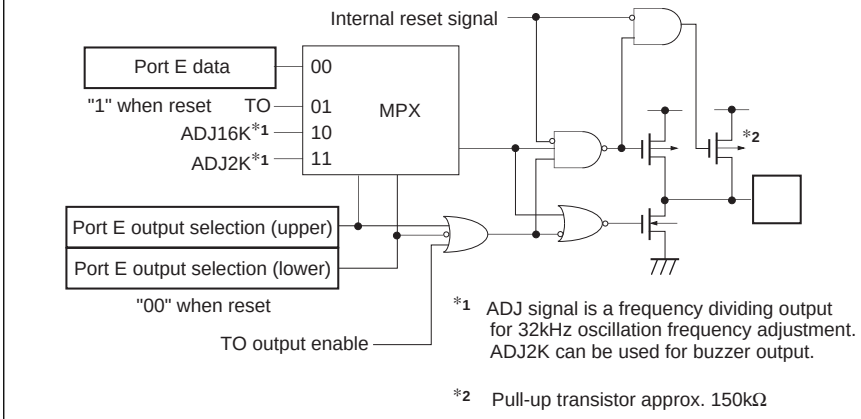
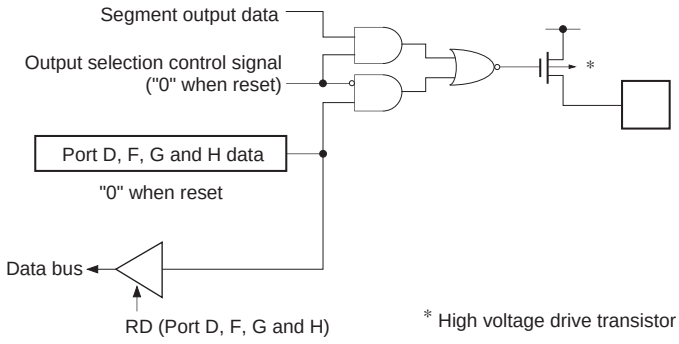
Pin code	I/O	Functions		
PA0/AN0 to PA7/AN7	I/O/ Analog input	(Port A) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8pins)	Analog inputs to A/D converter. (8 pins)	
PB0/CINT	I/O/Input	(Port B) 8-bit I/O port. I/O can be set in a unit of single bits. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Capture input to 16-bit timer/counter.	
PB1/$\overline{CS0}$	I/O/Input		Chip select input for serial interface (CH0).	
PB2/$\overline{SCK0}$	I/O/I/O		Serial clock I/O (CH0).	
PB3/SI0	I/O/Input		Serial data input (CH0).	
PB4/SO0	I/O/Output		Serial data output (CH0).	
PB5/$\overline{SCK1}$	I/O/I/O		Serial clock I/O (CH1).	
PB6/SI1	I/O/Input		Serial data input (CH1).	
PB7/SO1	I/O/Output		Serial data output (CH1).	
PC0/KR0 to PC7/KR7	I/O/Input	(Port C) 8-bit I/O port. I/O can be set in a unit of single bits. Capable of driving 12mA sync current. Incorporation of the pull-up resistance can be set through the software in a unit of 4 bits. (8 pins)	Serves as key return inputs when operating key scan with fluorescent display panel (FDP) segment signal. (8 pins)	
PD0/A55 to PD7/A48	Output/Output	(Port D) 8-bit output port. (8 pins)	FDP segment signal (anode connection) outputs.	
$\overline{PE0}$/INT0/ $\overline{EC0}$	Input/Input/Input	(Port E) 8-bit port. Lower 6 bits are for inputs; upper 2 bits are for outputs. (8 pins)	Inputs for external interruption request. (4 pins)	External event inputs for timer/counter. (2 pins)
$\overline{PE1}$/INT1/ $\overline{EC1}$	Input/Input/Input			
PE2/INT2	Input/Input			
$\overline{PE3}$/INT3/ $\overline{NMI}$	Input/Input/Input			Non-maskable interruption request input.
PE4/RMC	Input/Input		Remote control reception circuit input.	
PE5	Input			
PE6/$\overline{PWM}$	Output/Output		14-bit PWM output.	
PE7/TO/ADJ	Output/Output/ Output		Output for the 16-bit timer/counter rectangular waves, and 32kHz oscillation frequency division.	
PF0/A47 to PF7/A40	Output/Output	(Port F) 8-bit output port. (8pins)	FDP segment signal (anode connection) outputs.	

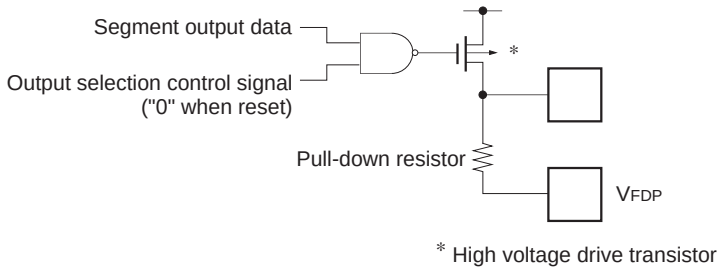
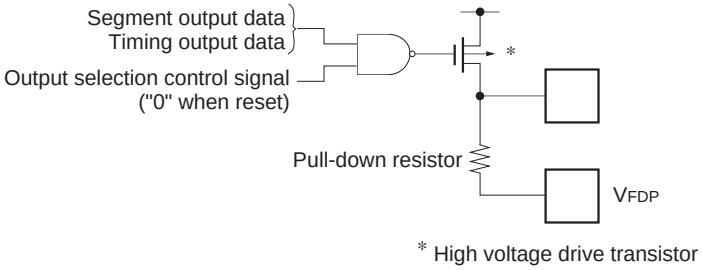
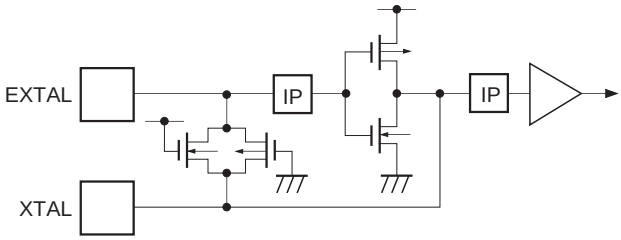
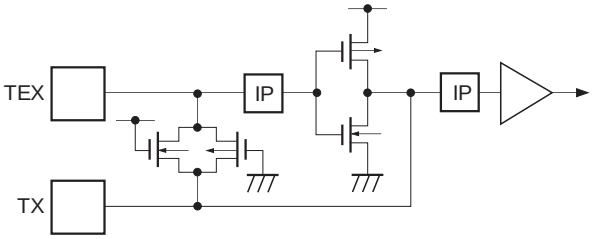
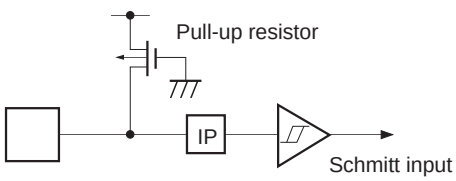
Pin code	I/O	Functions	
PG0/A39 to PG7/A32	Output/Output	(Port G) 8-bit output port. (8 pins)	FDP segment signal (anode connection) outputs.
PH0/A31 to PH7/A24	Output/Output	(Port H) 8-bit output port. (8 pins)	FDP segment signal (anode connection) outputs. (8 pins)
A16 to A23	Output	FDP segment signal (anode connection) outputs. (8 pins)	
G0/A0 to G15/A15	Output/Output	Outputs for FDP timing signals (grid connection)/segment signals (anode connection). (16 pins)	
V_{FDP}		FDP voltage supply for incorporated pull-down (PD) resistor.	
EXTAL	Input	Crystal connectors for system clock oscillation. When the clock is supplied externally, input to EXTAL; opposite phase clock should be input to XTAL.	
XTAL	Output		
TEX	Input	Crystal connectors for 32kHz timer/counter clock oscillation. For usage as event input, input to TEX, and open TX.	
TX	Output		
$\overline{RST}$	Input	Low-level active, system reset.	
AV_{REF}	Input	Reference voltage input for A/D converter.	
AV_{SS}		A/D converter GND.	
V_{DD}		V_{CC} supply.	
Vpp		Vcc supply for incorporated PROM writing. Connect to V_{DD} during normal operation.	
V_{SS}		GND.	

I/O Circuit Format for Pins

Pin	Circuit format	When reset
PA0/AN0 to PA7/AN7 8 pins	Port A 	Hi-Z
PB0/CINT PB1/$\overline{CS0}$ PB3/SI0 PB6/SI1 4 pins	Port B 	Hi-Z
PB2/$\overline{SCK0}$ PB5/$\overline{SCK1}$ 2 pins	Port B 	Hi-Z

Pin	Circuit format	When reset
PB4/SO0 PB7/SO1 2 pins	Port B  	Hi-Z
PC0/KR0 to PC7/KR7 8 pins	Port C  	Hi-Z
PE0/$\overline{EC0}$/INT0 PE1/$\overline{EC1}$/INT1 PE2/INT2 PE3/INT3/$\overline{NMI}$ PE4/RMC 5 pins	Port E  	Hi-Z
PE5 1 pin	Port E  	Hi-Z

Pin	Circuit format	When reset
PE6/$\overline{\text{PWM}}$ 1 pin	Port E 	High level
PE7/TO/ADJ 1 pin	Port E 	High level (with approx. 150kΩ resistor when reset)
PD0/A55 to PD7/A48 PF0/A47 to PF7/A40 PG0/A39 to PG7/A32 PH0/A31 to PH7/A24 32 pins	Port D Port F Port G Port H 	Hi-Z or Low level (when PD resistor is connected)

Pin	Circuit format	When reset
A16 to A23 8 pins		Hi-Z or Low level (when PD resistor is connected)
G0/A0 to G15/A15 16 pins		Hi-Z or Low level (when PD resistor is connected)
EXTAL XTAL 2 pins	 • Diagram shows circuit composition during oscillation. • Feedback resistor is removed and XTAL becomes High level during stop.	Oscillation
TEX TX 2 pins	 • Diagram shows circuit composition during oscillation. • When the operation of the oscillation circuit is stopped by the software, the feedback resistor is removed, and TEX becomes Low level and TX becomes High level.	Oscillation
$\overline{\text{RST}}$ 1 pin		Low level

Absolute Maximum Ratings (Vss = 0V reference)

Item	Symbol	Rating	Unit	Remarks
Supply voltage	V_{DD}	–0.3 to +7.0	V	
	Vpp	–0.3 to +13.0	V	Incorporated PROM
	AVss	–0.3 to +0.3	V	
A/D converter GND voltage	AV_{SS}	–0.3 to +0.3	V	
A/D converter reference voltage	AV_{REF}	–0.3 to +7.0*1	V	
FDP display supply voltage	V_{FDP}	–40*2 to +7.0*1	V	
Input voltage	V_{IN}	–0.3 to +7.0*1	V	
Output voltage	V_{OUT}	–0.3 to +7.0*1	V	
Display output voltage	V_{OD}	–40*2 to +7.0*1	V	
High level output current	I_{OH}	–5	mA	All pins excluding display outputs*3 (value per pin)
	I_{ODH1}	–15	mA	Display outputs A20 to A55 (value per pin)
	I_{ODH2}	–50	mA	Display outputs G0/A0 to G15/A15, and A16 to A19 (value per pin)
High level total output current	$\sum I_{OH}$	–30	mA	Total for all pins excluding display outputs
	$\sum I_{ODH}$	–120	mA	Total for all display outputs
Low level output current	I_{OL}	15	mA	Port (value per pin)
	I_{OLC}	20	mA	Large current port (value per pin)*4
Low level total output current	$\sum I_{OL}$	100	mA	Total for all output pins
Operating temperature	Topr	–20 to +75	°C	
Storage temperature	Tstg	–55 to +150	°C	
Allowable power dissipation	P_D	600	mW	

*1) V_{IN}, V_{OUT}, V_{OD} and AV_{REF} must not exceed V_{DD} + 0.3V.

*2) V_{FDP} and V_{OD} must not exceed V_{DD} – 40V.

*3) Specifies output current of general-purpose I/O ports.

*4) The large current drive transistor is the N-CH transistor of Port C (PC).

Note) Usage exceeding absolute maximum ratings may permanently impair the LSI. Normal operation should be conducted under the recommended operating conditions. Exceeding these conditions may adversely affect the reliability of the LSI.

Recommended Operating Conditions (Vss = 0V reference)

Item	Symbol	Min.	Max.	Unit	Remarks
Supply voltage	V_{DD}	4.5	5.5	V	Guaranteed operation range during high-speed mode (1/2, 1/4 frequency dividing clock)
		3.5	5.5	V	Guaranteed operation range during low-speed mode or SLEEP mode (1/16 frequency dividing clock)
		2.7	5.5	V	Guaranteed operation range with TEX clock
		2.5	5.5	V	Guaranteed data hold range during STOP
High level input voltage	V_{IH}	0.7V_{DD}	V_{DD}	V	*1
	V_{IHS}	0.8V_{DD}	V_{DD}	V	Hysteresis input*2
	V_{IHEX}	V_{DD} – 0.4	V_{DD} + 0.3	V	EXTAL*3
Low level input voltage	V_{IL}	0	0.3V_{DD}	V	*1
	V_{ILS}	0	0.2V_{DD}	V	Hysteresis input*2
	V_{ILEX}	–0.3	0.4	V	EXTAL*3
Operating temperature	Topr	–10	+75	°C	

*1) Value for each pin of normal input port (PA, PB4, PB7, PC).

*2) Value of the following pins: $\overline{RST}$, CINT, $\overline{CS0}$, $\overline{SCK0}$, $\overline{SCK1}$, $\overline{EC0}$/INT0, $\overline{EC1}$/INT1, INT2, INT3/$\overline{NMI}$, RMC.

*3) Specifies only during external clock input.

Electrical Characteristics

DC Characteristics

(Ta = –10 to +75°C, V_{SS} = 0V reference)

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
High level output current	V_{OH}	PA, PB, PC, PE6, PE7	V_{DD} = 4.5V, I_{OH} = –0.5mA	4.0			V
			V_{DD} = 4.5V, I_{OH} = –1.2mA	3.5			V
Low level output current	V_{OL}		V_{DD} = 4.5V, I_{OL} = 1.8mA			0.4	V
			V_{DD} = 4.5V, I_{OL} = 3.6mA			0.6	V
		PC	V_{DD} = 4.5V, I_{OL} = 12.0mA			1.5	V
Input current	I_{IHE}	EXTAL	V_{DD} = 5.5V, V_{IH} = 5.5V	0.5		40	µA
	I_{ILE}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.5		–40	µA
	I_{IHT}	TEX	V_{DD} = 5.5V, V_{IL} = 5.5V	0.1		10	µA
	I_{ILT}		V_{DD} = 5.5V, V_{IL} = 0.4V	–0.1		–10	µA
	I_{ILR}	$\overline{RST}$	V_{DD} = 5.5V, V_{IL} = 0.4V	–1.5		–400	µA
	I_{IL}	PA to PC*1				–50	µA
			V_{DD} = 4.5V, V_{IL} = 4.0V	–3.3			µA
Display output current	I_{OH}	A20 to A55	V_{DD} = 4.5V V_{OH} = V_{DD} –2.5V	–8			mA
		G0/A0 to G15/A15 A16 to A19		–30			mA
Open drain output leakage current (P-CH Tr off state)	I_{LOL}	G0/A0 to G15/A15 A16 to A55	V_{DD} = 5.5V V_{OL} = V_{DD} –35V V_{FDP} = V_{DD} –35V			–20	µA
Pull-down resistance	R_L	G0/A0 to G15/A15 A16 to A55	V_{DD} = 5V V_{OD} –V_{FDP} = 30V	60	100	270	kΩ
I/O leakage current	I_{IZ}	PA to PC*1 PE0 to PE5 $\overline{RST}$	V_{DD} = 5.5V V_I = 0, 5.5V			±10	µA

Item	Symbol	Pins	Conditions	Min.	Typ.	Max.	Unit
Power supply current*2	I_{DD1}	V_{DD}	High-speed mode operation (1/2 frequency dividing clock) V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		22	50	mA
	I_{DD2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		45	130	µA
	I_{DDS1}		SLEEP mode V_{DD} = 5.5V, 10MHz crystal oscillation (C_1 = C_2 = 15pF)		2.3	10	mA
	I_{DDS2}		V_{DD} = 3V, 32kHz crystal oscillation (C_1 = C_2 = 47pF)		11	30	µA
	I_{DDS3}		STOP mode V_{DD} = 5.5V, termination of 10MHz and 32kHz oscillation			30	µA
Input capacity	C_{IN}	PA to AC, PE0 to 5, XTAL, EXTAL, TEX, $\overline{RST}$	Clock 1MHz 0V for all pins excluding measured pins		10	20	pF

*1) PA to PC pins specify the input current when pull-up resistance has been selected; leakage current when no resistance has been selected.

*2) When all pins are open.

AC Characteristics

(1) Clock timing

(Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Conditions	Min.	Typ.	Max.	Unit
System clock frequency	f_C	XTAL EXTAL	Fig. 1, Fig. 2	1		10	MHz
System clock input pulse width	t_{XL} t_{XH}	EXTAL	Fig. 1, Fig. 2 External clock drive	37.5			ns
System clock input rise time, fall time	t_{CR} t_{CF}	EXTAL	Fig. 1, Fig. 2 External clock drive	t_{sys} + 50*1		200	ns
Event count input clock pulse width	t_{EH} t_{EL}	$\overline{EC0}$, $\overline{EC1}$	Fig. 3				ns
Event count input clock rise time, fall time	t_{ER} t_{EF}	$\overline{EC0}$, $\overline{EC1}$	Fig. 3			20	ms
System clock frequency	f_C	TEX TX	V_{DD} = 2.7 to 5.5V Fig. 2 (32kHz clock applied condition)		32.768		kHz
Event count input pulse width	t_{TL} t_{TH}	TEX	Fig. 3	10			µs
Event count input rise time, fall time	t_{TR} t_{TF}	TEX	Fig. 3			20	ms

*1) t_{sys} indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (CLC: 00FE$_H$).
t_{sys} (ns)=2000/fc (upper two bits="00"), 4000/fc (upper two bits="01"), 16000/fc (upper two bits="11")

Fig. 1. Clock timing

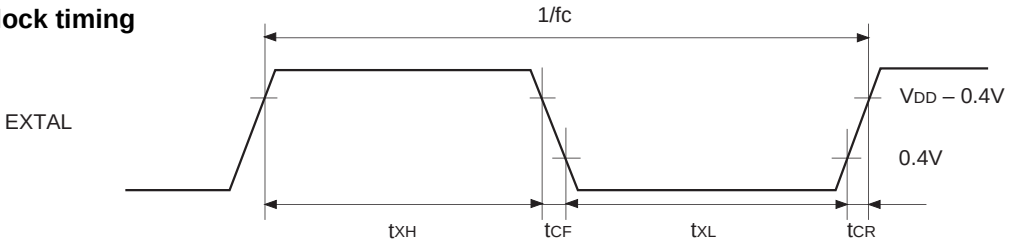


Fig. 2. Clock applied conditions

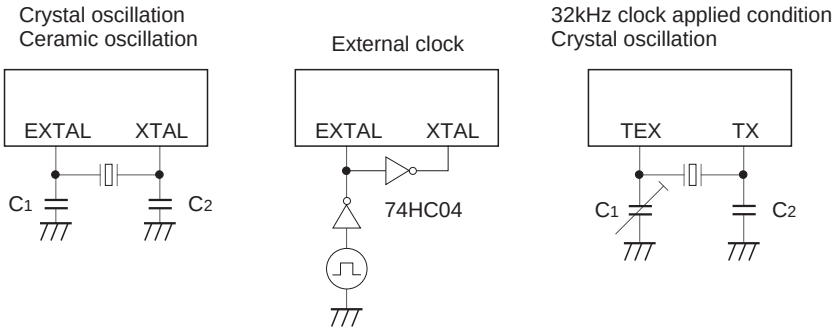
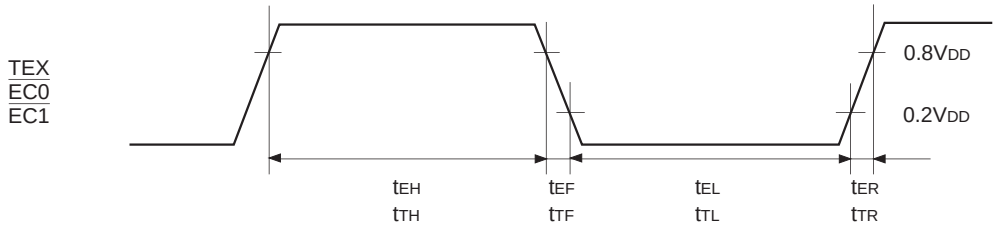


Fig. 3. Event count clock timing



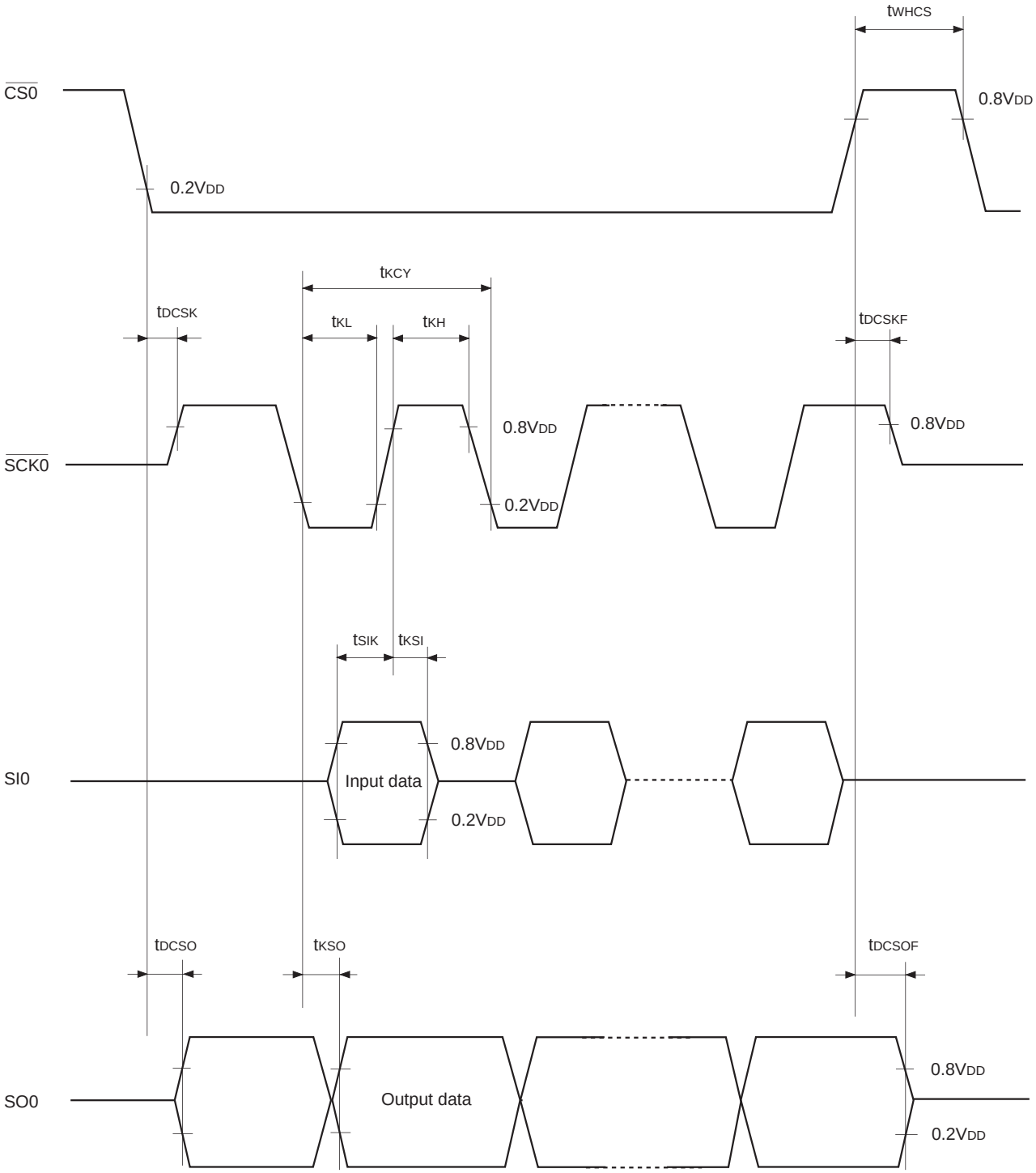
(2) Serial transfer (CH0) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{CS0} \downarrow \rightarrow \overline{SCK0}$ delay time	t_{DCSK}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow \overline{SCK0}$ float delay time	t_{DCSKF}	$\overline{SCK0}$	Chip select transfer mode ($\overline{SCK0}$ = output mode)		tsys + 200	ns
$\overline{CS0} \downarrow \rightarrow$ SO0 delay time	t_{DCSO}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0} \uparrow \rightarrow$ SO0 float delay time	t_{DCSOF}	SO0	Chip select transfer mode		tsys + 200	ns
$\overline{CS0}$ High level width	t_{WHCS}	$\overline{CS0}$	Chip select transfer mode	tsys + 200		ns
$\overline{SCK0}$ cycle time	t_{KCY}	$\overline{SCK0}$	Input mode	2tsys + 200		ns
			Output mode	16000/fc		ns
$\overline{SCK0}$ High, Low level width	t_{KH} t_{KL}	$\overline{SCK0}$	Input mode	tsys + 100		ns
			Output mode	8000/fc–50		ns
SI0 input set-up time (for $\overline{SCK0} \uparrow$)	t_{SIK}	SI0	$\overline{SCK0}$ input mode	100		ns
			$\overline{SCK0}$ output mode	200		ns
SI0 input hold time (for $\overline{SCK0} \uparrow$)	t_{KSI}	SI0	$\overline{SCK0}$ input mode	tsys + 200		ns
			$\overline{SCK0}$ output mode	100		ns
$\overline{SCK0} \downarrow \rightarrow$ SO0 delay time	t_{KSO}	SO0	$\overline{SCK0}$ input mode		tsys + 200	ns
			$\overline{SCK0}$ output mode		100	ns

Note 1) tsys indicates the three values below according to the upper two bits (CPU clock selection) of the control clock register (CLC: $00FE_H$).
tsys (ns)=2000/fc (upper two bits="00"), 4000/fc (upper two bits="01"), 16000/fc (upper two bits="11")

Note 2) The load condition for the $\overline{SCK0}$ output mode, SO0 output delay time is 50pF + 1TTL.

Fig. 4. Serial transfer CH0 timing

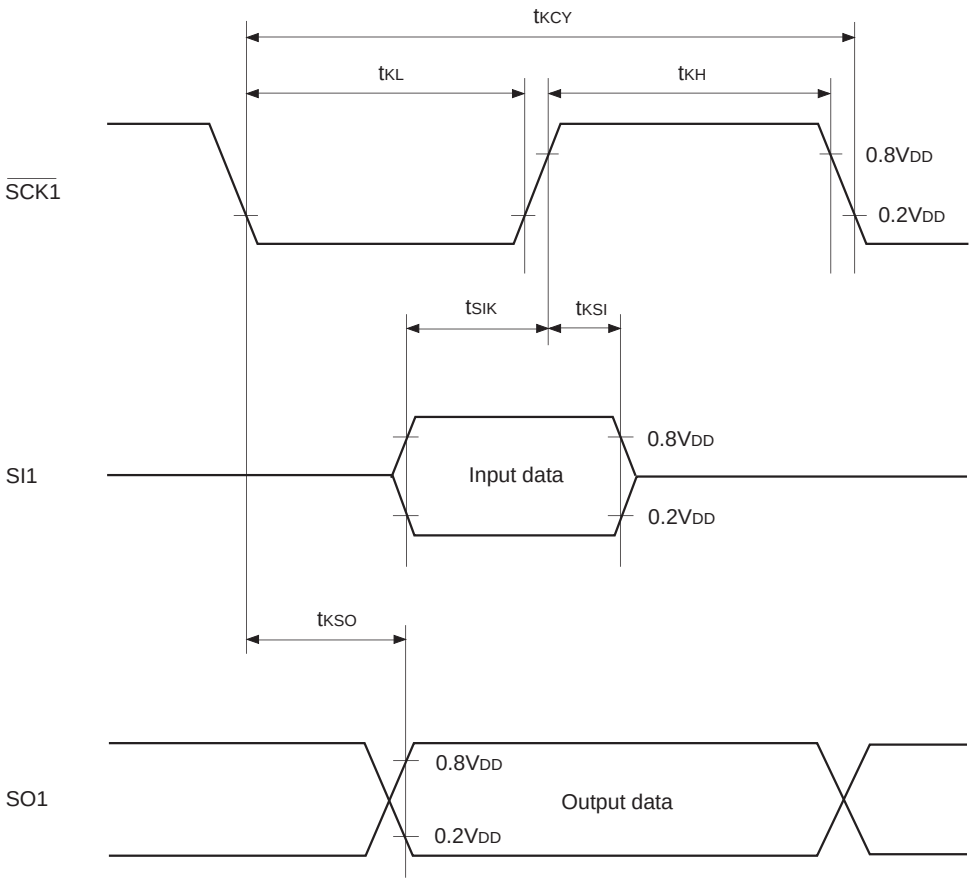


Serial transfer (CH1) (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
$\overline{SCK1}$ cycle time	t_{KCY}	$\overline{SCK1}$	Input mode	1000		ns
			Ouput mode	16000/fc		ns
$\overline{SCK1}$ High, Low level width	t_{KH} t_{KL}	$\overline{SCK1}$	Input mode	400		ns
			Ouput mode	8000/fc–50		ns
SI1 input set-up time (for $\overline{SCK1}$ ↑)	t_{SIK}	SI1	$\overline{SCK1}$ input mode	100		ns
			$\overline{SCK1}$ ouput mode	200		ns
SI1 input hold time (for $\overline{SCK1}$ ↑)	t_{KSI}	SI1	$\overline{SCK1}$ input mode	200		ns
			$\overline{SCK1}$ ouput mode	100		ns
$\overline{SCK1}$ ↓ → SO1 delay time	t_{KSO}	SO1	$\overline{SCK1}$ input mode		200	ns
			$\overline{SCK1}$ ouput mode		100	ns

Note) The load condition for the $\overline{SCK1}$ output mode, SO1 output delay time is 50pF + 1TTL.

Fig. 5. Serial transfer CH1 timing

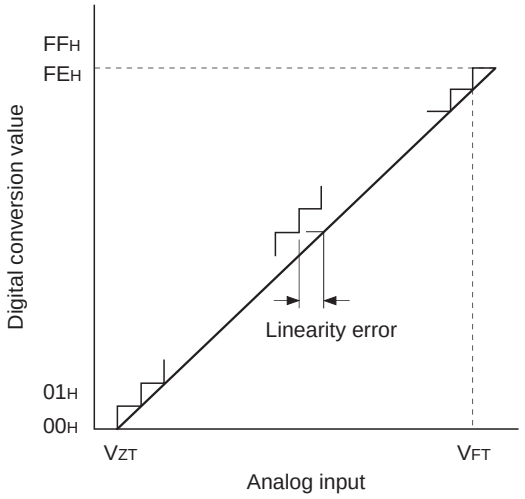


(3) A/D converter characteristics

(Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, AV_{REF} = 4.0 to V_{DD}, Vss = AV_{SS} = 0V reference)

Item	Symbol	Pin	Condition	Min.	Typ.	Max.	Unit
Resolution						8	Bits
Linearity error			Ta = 25°C V_{DD} = AV_{REF} = 5.0V V_{SS} = AV_{SS} = 0V			±3	LSB
Zero transition voltage	V_{ZT}*1			–50	10	70	mV
Full-scale transition voltage	V_{FT}*2			4910	4970	5030	mV
Conversion time	t_{CONV}			160/f_{ADC}*3			µs
Sampling time	t_{SAMP}			12/f_{ADC}*3			µs
Reference input voltage	V_{REF}	AV_{REF}		V_{DD} – 0.5		V_{DD}	V
Analog input voltage	V_{IAN}	AN0 to AN7		0		AV_{REF}	V
AV_{REF} current	I_{REF}	AV_{REF}	Operation mode		0.6	1.0	mA
	I_{REFS}		SLEEP mode STOP mode 32kHz operation mode			10	µA

Fig. 6. Definition of A/D converter terms



*1) V_{ZT}: Value at which the digital transfer value changes from 00_H to 01_H and vice versa.

*2) V_{FT}: Value at which the digital transfer value changes from FE_H to FF_H and vice versa.

*3) f_{ADC} indicates the below values due to the contents of bit 6 (CKS) of the A/D control register (ADC: $00F9_H$) and bits 7 (PCK1) and 6 (PCK0) of the clock control register (CLC: $00FE_H$).

CKS / PCK1, PCK0	0 (ϕ/2 selection)	1 (ϕ selection)
00 (ϕ = f_{EX}/2)	f_{ADC} = f_C/2	f_{ADC} = f_C
01 (ϕ = f_{EX}/4)	f_{ADC} = f_C/4	f_{ADC} = f_C/2
11 (ϕ = f_{EX}/16)	f_{ADC} = f_C/16	f_{ADC} = f_C/8

(4) Interruption, reset input (Ta = –10 to +75°C, V_{DD} = 4.5 to 5.5V, Vss = 0V reference)

Item	Symbol	Pin	Condition	Min.	Max.	Unit
External interruption High, Low level width	t_{IH} t_{IL}	INT0 INT1 INT2 $\overline{NMI}$/INT3		1		µs
Reset input Low level width	t_{RSL}	$\overline{RST}$		32/fc		µs

Fig. 7. Interruption input timing

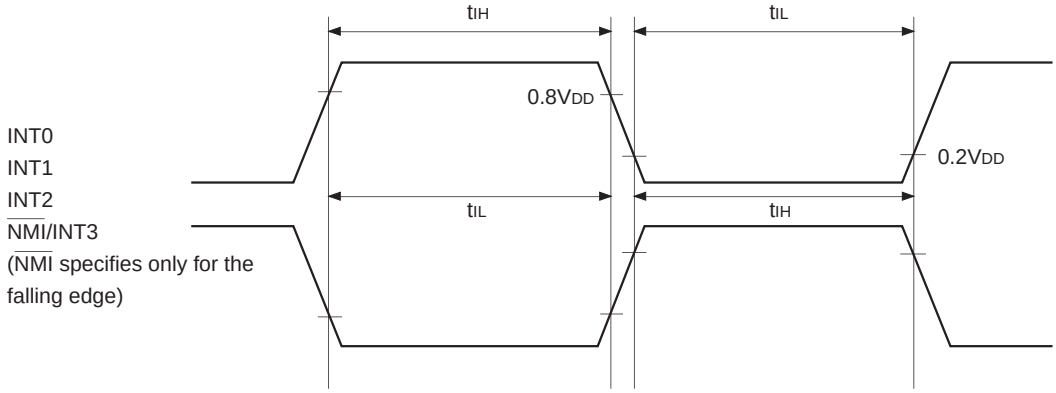
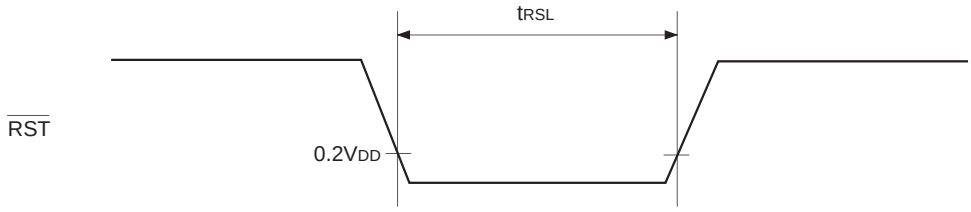


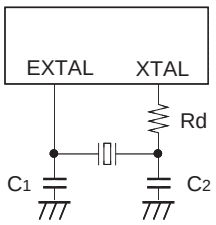
Fig. 8. $\overline{RST}$ input timing



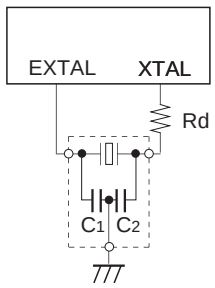
Appendix

Fig. 9. Recommended oscillation circuit

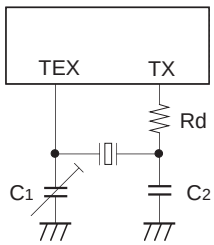
(i) Main clock



(ii) Main clock



(iii) Sub clock



Manufacturer	Model	fc (MHz)	C_1 (pF)	C_2 (pF)	Rd (Ω)	Circuit example
MURATA MFG CO., LTD.	CSA4.19MG	4.19	30	30	0	(i)
	CSA8.00MTZ	8.00				
	CSA10.0MTZ	10.00				
	CST4.19MGW*	4.19				(ii)
	CST8.00MTW*	8.00				
	CST10.0MTW*	10.00				
RIVER ELETEC CO., LTD	HC-49/U03	4.19	12	12	0	(i)
		8.00				
		10.00				
KINSEKI LTD.	HC-49/U (-S)	4.19	27	27	0	
		8.00				
		10.00	20	20		
	P3	32.768kHz	50	22	1M	(iii)

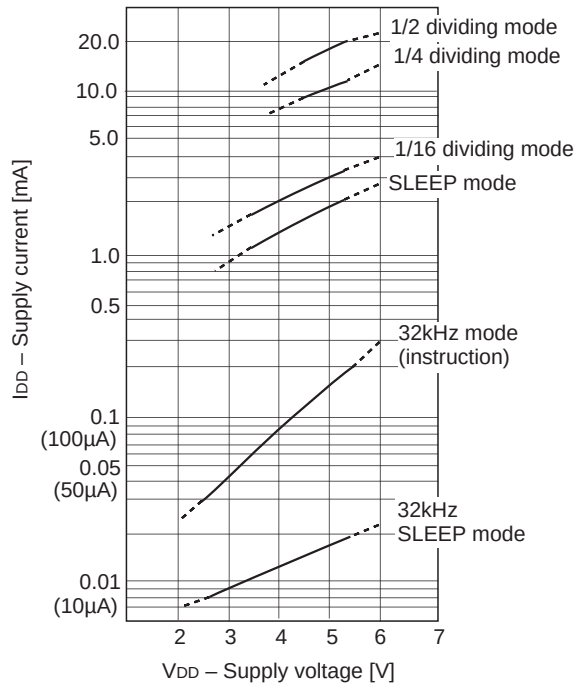
Models marked with an asterisk (*) have the built-in ground capacitance (C_1, C_2).

Mask option table

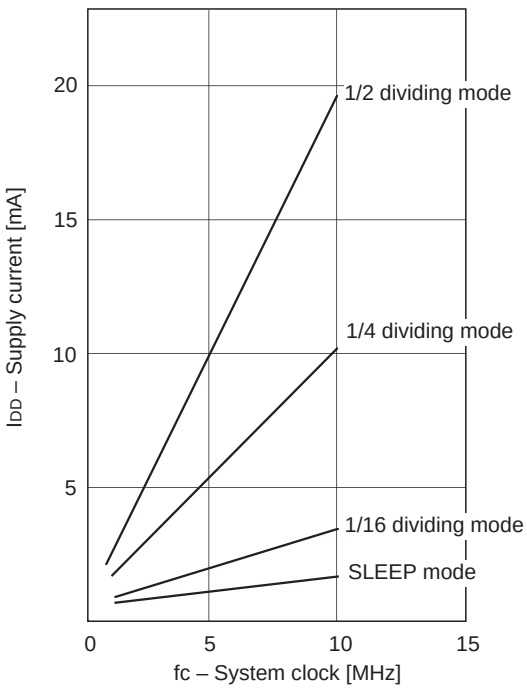
Option item	Product				
	Mask product				PROM version
	CXP82832	CXP82840	CXP82852	CXP82860	CXP828P60Q-1-□□□
Package	80-pin plasitc QFP				80-pin plasitc QFP
ROM capacitance	32K bytes	40K bytes	52K bytes	60K bytes	PROM 60K bytes
Reset pull-up resistance	Existent/Non-existent				Existent
High voltage drive pin pull-down resister	Existent/Non-existent				Non-existent (PD7/A24 to PD0/A55) Existent (G0/A0 to A23)

Characteristics Curve

IDD vs. VDD
(fc = 10MHz, Ta = 25°C, Typical)

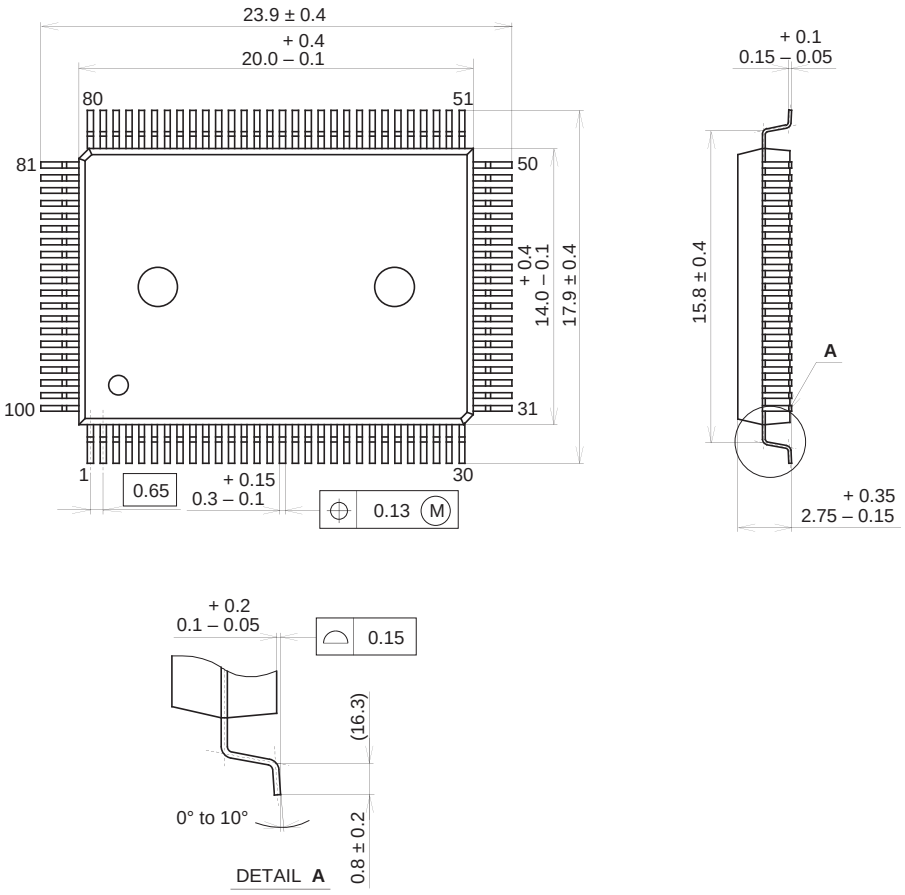


IDD vs. fc
(VDD = 5V, Ta = 25°C, Typical)



Package Outline Unit : mm

100PIN QFP (PLASTIC)



PACKAGE STRUCTURE

PACKAGE MATERIAL	EPOXY RESIN
LEAD TREATMENT	SOLDER PLATING
LEAD MATERIAL	42/COPPER ALLOY
PACKAGE MASS	1.7g

SONY CODE	QFP-100P-L01
EIAJ CODE	QFP100-P-1420
JEDEC CODE	