128K x 8 SRAM

High-Speed CMOS SRAM with 3.3V Revolutionary Pinout

FEATURES

- High-speed access times of 10, 12, 15 and 20 ns
- High-performance, low-power CMOS process
- Multiple center power and ground pins for greater noise immunity
- Easy memory expansion with CE\ and OE\ options
- CE\ power-down
- Fully static operation: no clock or refresh required
- TTL compatible inputs and outputs
- Single 3.3V power supply
- RoHS compliant options available

GENERAL DESCRIPTION

OPTIONS — MARKING

- Timing
  - 10ns access — -10
  - 12ns access — -12
  - 15ns access — -15
  - 20ns access — -20
- Package
  - Plastic SOJ (32-pin, 400-mil) — DJ — No. 906
- Operating Temperature Ranges
  - -Military (-55°C to +125°C) — /XT
  - -Industrial (-40°C to +85°C) — /IT
- 2V Data Retention / Low Power — L

The AS5LC1008 is a very high-speed, low power, 131,072-word by 8-bit CMOS static RAM in revolutionary pinout. The AS5LC1008 is fabricated using high-performance CMOS technology. This highly reliable process coupled with innovative circuit design techniques, yields higher performance and low power consumption devices.

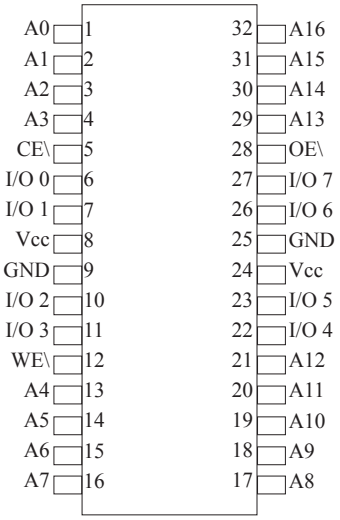
When CE\ is HIGH (deselected), the device assumes a standby mode at which the power dissipation can be reduced down to 250µW (typical) with CMOS input levels.

The AS5LC1008 operates from a single 3.3V power supply and all inputs are TTL-compatible.

PIN ASSIGNMENT

(Top View)

32-Pin, 400-mil
Plastic SOJ (DJ) & Plastic TSOPII (DGC & DGCR)



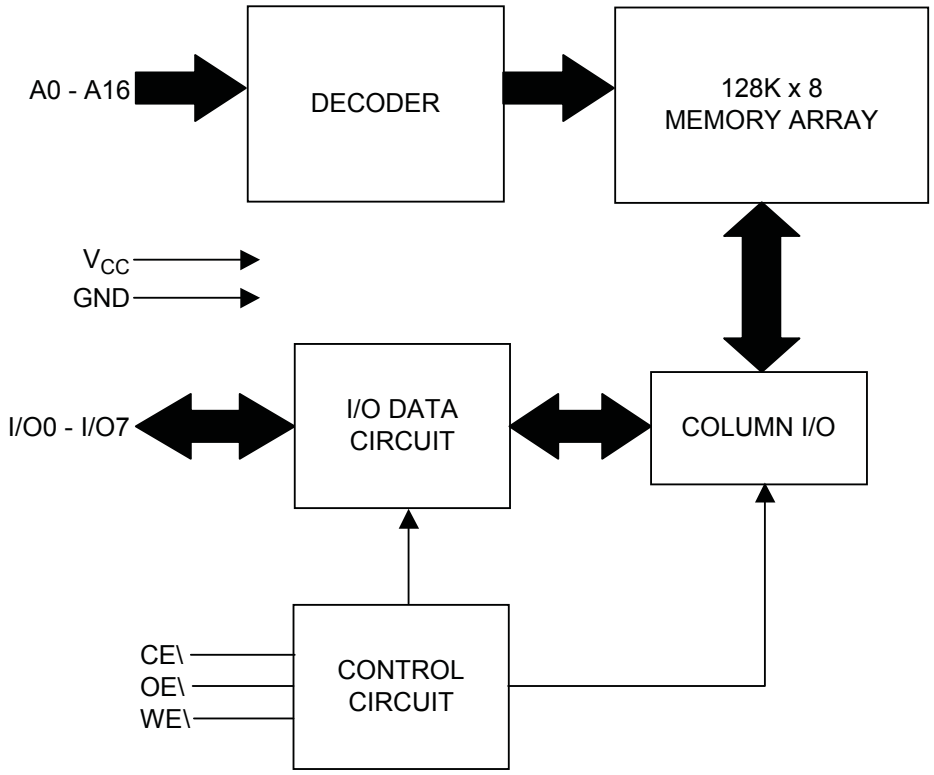
PIN FUNCTIONS

PIN	DESCRIPTION
A0 - A16	Address Inputs
CE\	Chip Enable Input
OE\	Output Enable Input
WE\	Write Enable Input
I/O0 - I/O7	Bidirectional Ports
V_{CC}	Power
GND	Ground

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FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS*

Terminal Voltage with Respect to GND (V_{TERM}).....-0.5V to V_{CC} + 0.5V
Temperature Under Bias (T_{BIAS}).....-55°C to +125°C
Storage Temperature (T_{STG}).....-65°C to +150°C
Power Dissipation (P_T).....1.0W

*Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operation section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

TRUTH TABLE

Mode	WE\	CE\	OE\	I/O Operation
Not Selected (Power-down)	X	H	X	High-Z
Output Disabled	H	L	H	High-Z
Read	H	L	L	D_{OUT}
Write	L	L	X	D_{IN}

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ELECTRICAL CHARACTERISTICS AND RECOMMENDED DC OPERATING CONDITIONS

($-55^oC \leq T_A \leq +125^oC$ or -40^oC to $+85^oC$; Vcc = 3.3V ±0.3V)

PARAMETER	SYMBOL	CONDITIONS	MIN	MAX	UNITS
Output HIGH Voltage	V_{OH}	V_{CC} = Min., I_{OH} = -4.0mA	2.4	---	V
Output LOW Voltage	V_{OL}	V_{CC} = Min., I_{OL} = 8.0mA	---	0.4	V
Input HIGH Voltage	V_{IH}		2.2	V_{CC} + 0.3	V
Input LOW Voltage[1]	V_{IL}		-0.3	0.8	V
Input Leakage	I_{LI}	GND ≤ V_{IN} ≤ V_{CC}	-5	5	µA
Output Leakage	I_{LO}	GND ≤ V_{OUT} ≤ V_{CC}; Outputs Disabled	-5	5	µA

NOTE: 1. V_{IL} = -3.0V for pulse width less than 10ns.

POWER SUPPLY CHARACTERISTICS[1]

($-55^oC \leq T_A \leq +125^oC$ or -40^oC to $+85^oC$; Vcc = 3.3V ±0.3V)

			-10		-12		-15		-20		
PARAMETER	SYM	CONDITIONS	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
V_{CC} Dynamic Operating Supply Current	I_{CC}	V_{CC} = Max, CE\ = V_{IL}, I_{OUT} = 0 mA, f = Max	---	105	---	100	---	95	---	90	mA
TTL Standby Current (TTL Inputs)	I_{SB}	V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} CE\ ≥ V_{IH}, f = Max	---	35	---	30	---	25	---	20	mA
	I_{SB1}	V_{CC} = Max, V_{IN} = V_{IH} or V_{IL} CE\ ≥ V_{IH}, f = 0	---	20	---	20	---	20	---	20	mA
CMOS Standby Current (CMOS Inputs)	I_{SB2}	V_{IN} ≥ V_{CC} - 0.2V, or V_{IN} ≤ 0.2V, f = 0	---	2	---	2	---	2	---	2	mA

NOTE: 1. At f = f_{MAX}, address and data inputs are cycling at the maximum frequency, f = 0 means no input lines change.

CAPACITANCE[1,2]

PARAMETER	SYMBOL	CONDITIONS	MAX	UNIT
Input Capacitance	C_{IN}	V_{IN} = 0V	6	pF
Input/Output Capacitance	$C_{I/O}$	V_{OUT} = 0V	8	pF

NOTE:
1. Tested initially and after any design or process changes that may affect these parameters.
2. Test conditions: T_A = 25°C, f = 1MHz, V_{CC} = 3.3V.

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READ CYCLE SWITCHING CHARACTERISTICS[1]

(-55°C ≤ T_A ≤ +125°C or -40°C to +85°C; Vcc = 3.3V ±0.3V)

		-10		-12		-15		-20		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNIT
Read Cycle Time	t_{RC}	10	---	12	---	15	---	20	---	ns
Address Access Time	t_{AA}	---	10	---	12	---	15	---	20	ns
Output Hold time	t_{OHA}	2	---	2	---	2	---	2	---	ns
CE\ Access Time	t_{ACE}	---	10	---	12	---	15	---	20	ns
OE\ Access Time	t_{DOE}	---	5	---	6	---	7	---	8	ns
OE\ to Low-Z Output	t_{LZOE}[2]	0	---	0	---	0	---	0	---	ns
OE\ to High-Z Output	t_{HZOE}[2]	0	5	0	6	0	7	0	8	ns
CE\ to Low-Z Output	t_{LZCE}[2]	2	---	2	---	2	---	2	---	ns
CE\ to High-Z Output	t_{HZCE}[2]	0	5	0	6	0	7	0	8	ns

NOTES:

1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and C1 output loading specified in Figure 1.
2. Tested with the C2 load in Figure 1. Transition is measured ±500 mV from steady-state voltage. Not 100% tested.

AC TEST CONDITIONS

PARAMETER	UNIT
Input Pulse Level	0V to 3.0V
Input Rise and Fall Times	3ns
Input and Output timing and Reference Levels	1.5V
Output Load	See Figures 1 and 2

AC TEST LOADS

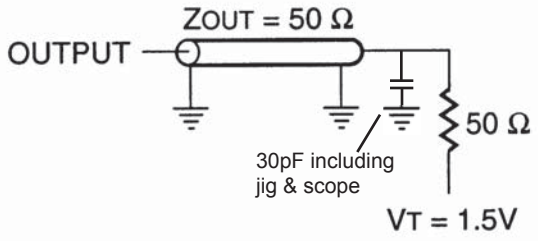


FIGURE 1

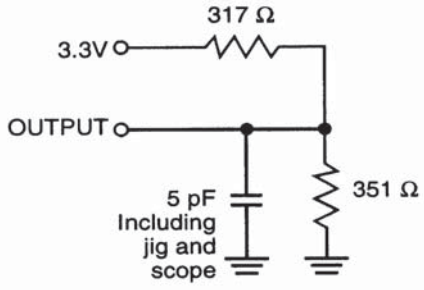


FIGURE 2

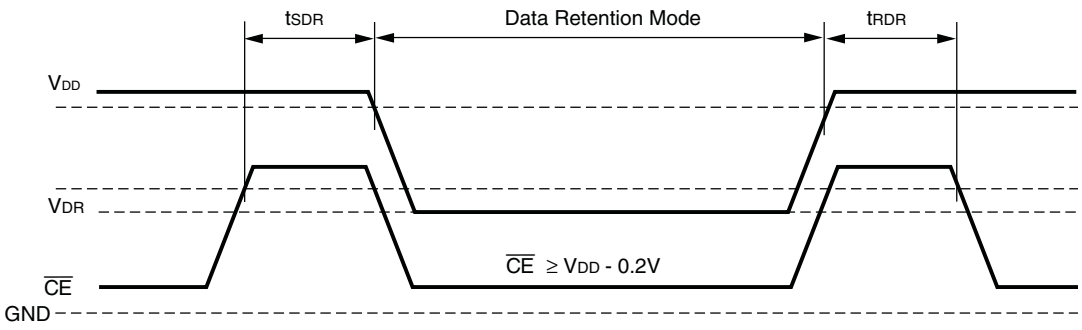
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DATA RETENTION SWITCHING CHARACTERISTICS (Low Power "L" Version)

Symbol	Parameter	Test Condition	Min.	Typ.	Max.	Unit
V_{DR}	V_{DD} for Data Retention	See Data Retention Waveform	2.0	-	3.6	V
I_{DR}	Data Retention Current	V_{DD} = 2.0V, CE\ ≥ V_{DD} - 0.2V	-	-	2	mA
I_{SDR}	Data Retention Setup Time	See Data Retention Waveform	0	-	-	ns
I_{RDR}	Recovery Time	See Data Retention Waveform	t_{RC}	-	-	ns

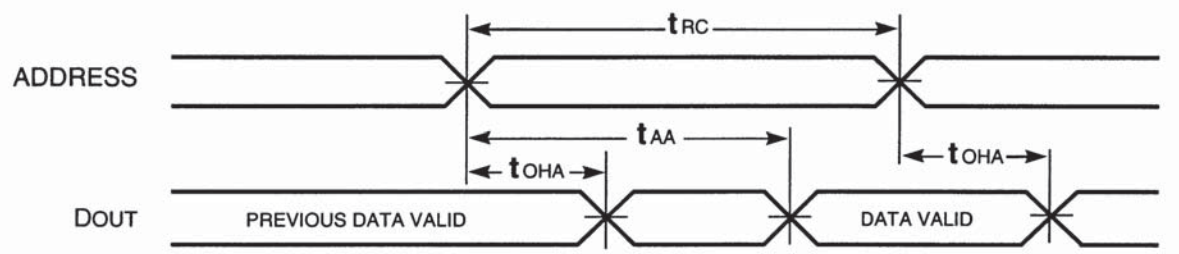
NOTES:
1. Typical values are measured at V_{DD}=3.0V, T_A=25ºC and not 100% tested.

DATA RETENTION SWITCHING WAVEFORM (CE\ Controlled)

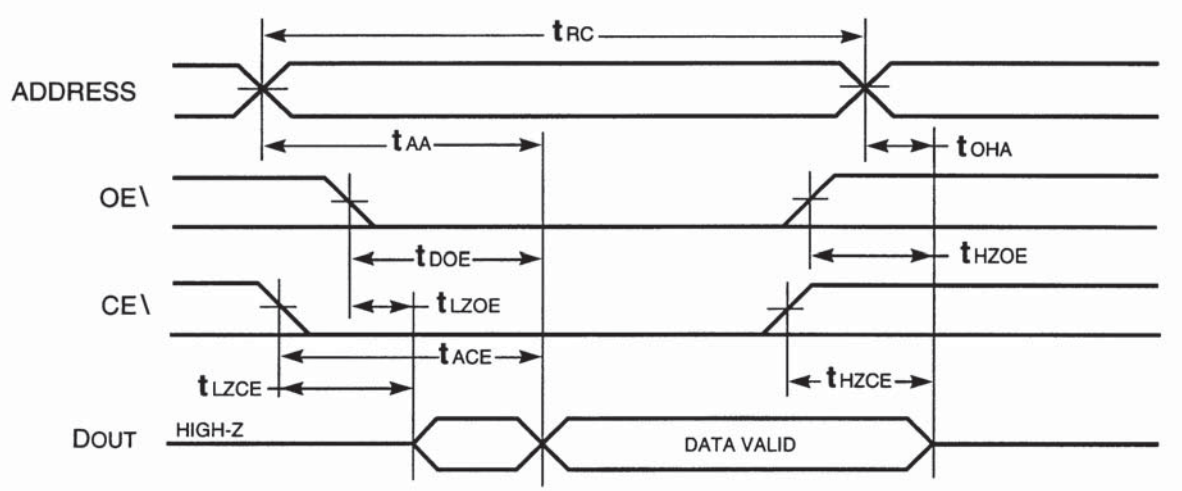


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READ CYCLE #1[1,2]



READ CYCLE #2[1,3]



NOTES:

1. WE\ is HIGH for a Read Cycle.
2. The device is continuously selected. OE\, CE\ = V_{IL}.
3. Address is valid prior to or coincident with CE\ LOW transitions.

WRITE CYCLE SWITCHING CHARACTERISTICS[1,3]

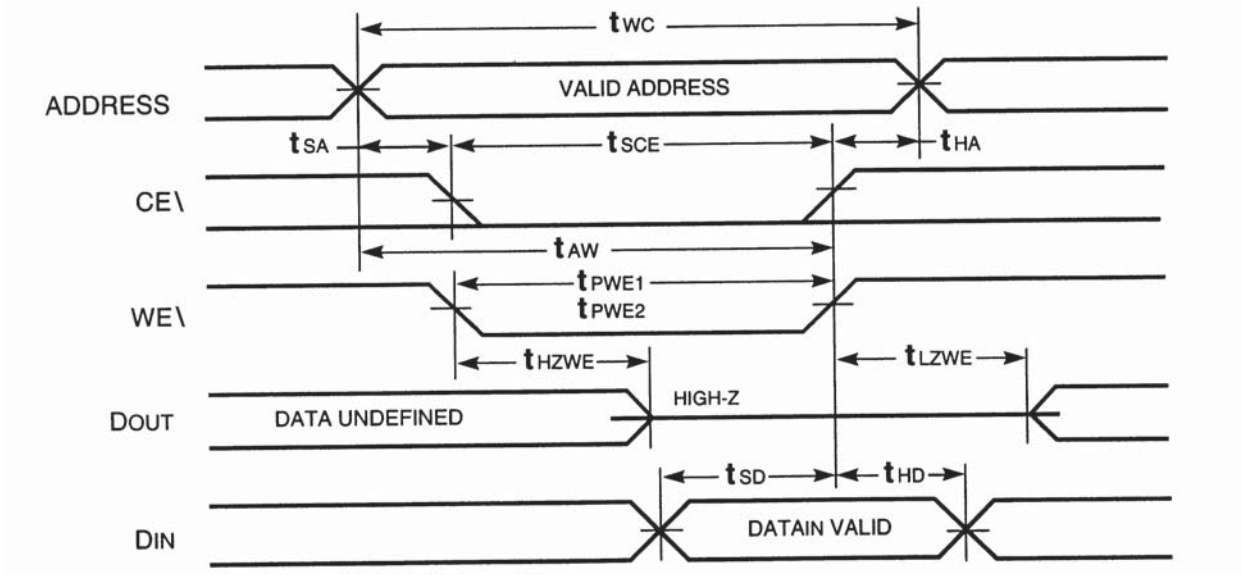
(-55°C ≤ T_A ≤ +125°C or -40°C to +85°C; Vcc = 3.3V ±0.3V)

		-10		-12		-15		-20		
PARAMETER	SYMBOL	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	UNITS
Write Cycle Time	t_{WC}	10	---	12	---	15	---	20	---	ns
CE\ to Write End	t_{SCE}	7	---	8	---	9	---	10	---	ns
Address Setup Time to Write End	t_{AW}	8	---	9	---	10	---	12	---	ns
Address Hold from Write End	t_{HA}	0	---	0	---	0	---	0	---	ns
Address Setup Time	t_{SA}	0	---	0	---	0	---	0	---	ns
WE\ Pulse Width (OE\ HIGH)	t_{PWE1}[1]	7	---	8	---	9	---	10	---	ns
WE\ Pulse Width (OE\ LOW)	t_{PWE2}[2]	10	---	12	---	12	---	15	---	ns
Data Setup to Write End	t_{SD}	5	---	6	---	7	---	8	---	ns
Data Hold to Write End	t_{HD}	0	---	0	---	0	---	0	---	ns
WE\ LOW to High-Z Output	t_{HZWE}[2]	---	5	---	6	---	7	---	8	ns
WE\ HIGH to Low-Z Output	t_{LZWE}[2]	2	---	2	---	2	---	2	---	ns

NOTES:

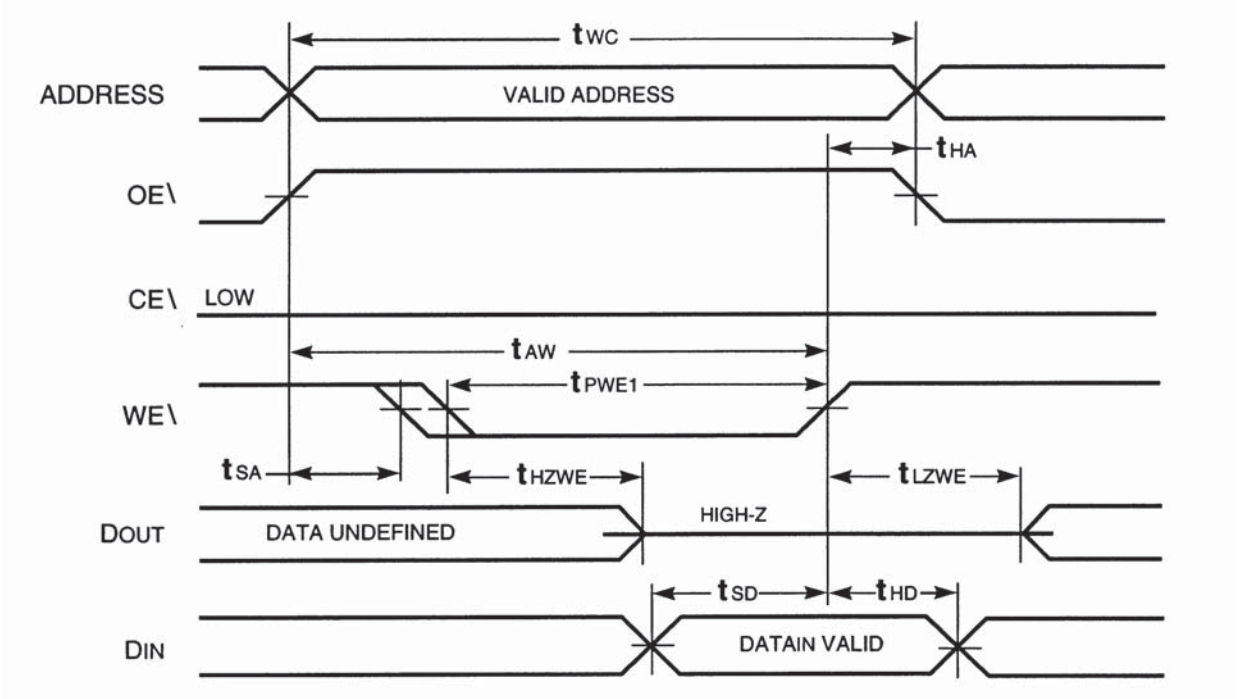
1. Test conditions assume signal transition times of 3ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V and output loading specified in Figure 1.
2. Tested with the load in Figure 2. Transition is measured ±200 mV from steady-state voltage. Not 100% tested.
3. The internal write time is defined by the overlap of CE\ LOW and WE\ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.

WRITE CYCLE #1[1,2] (CE\ Controlled, OE\ = HIGH or LOW)

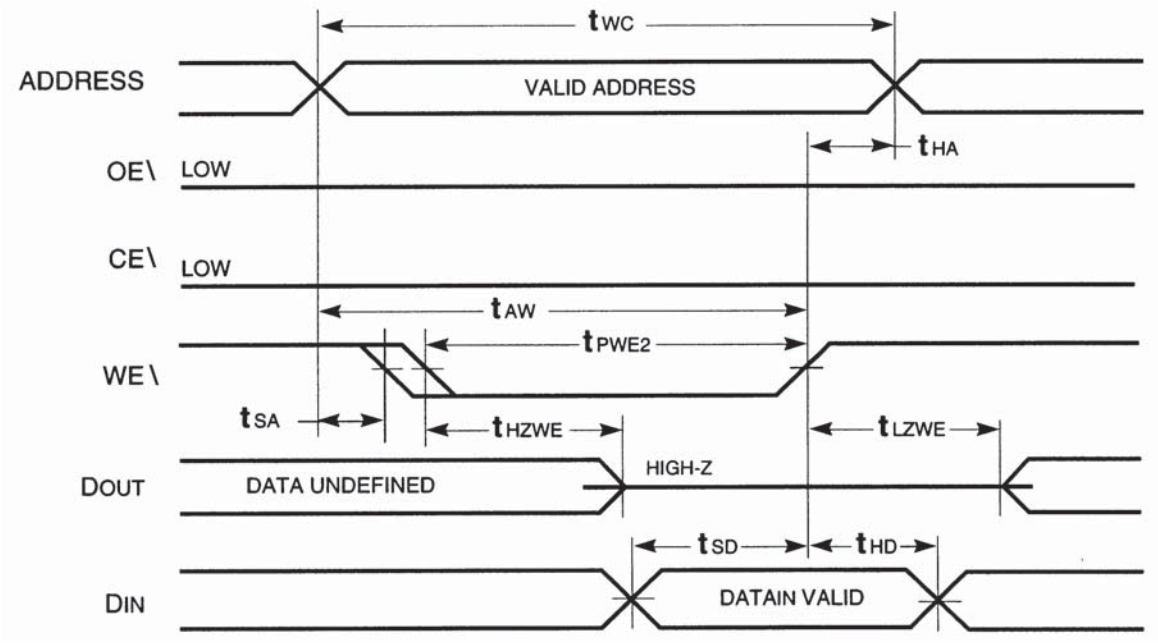


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WRITE CYCLE #2[1] (WE\ Controlled, OE\ = HIGH during Write Cycle)



WRITE CYCLE #3 (WE\ Controlled, OE\ = LOW during Write Cycle)



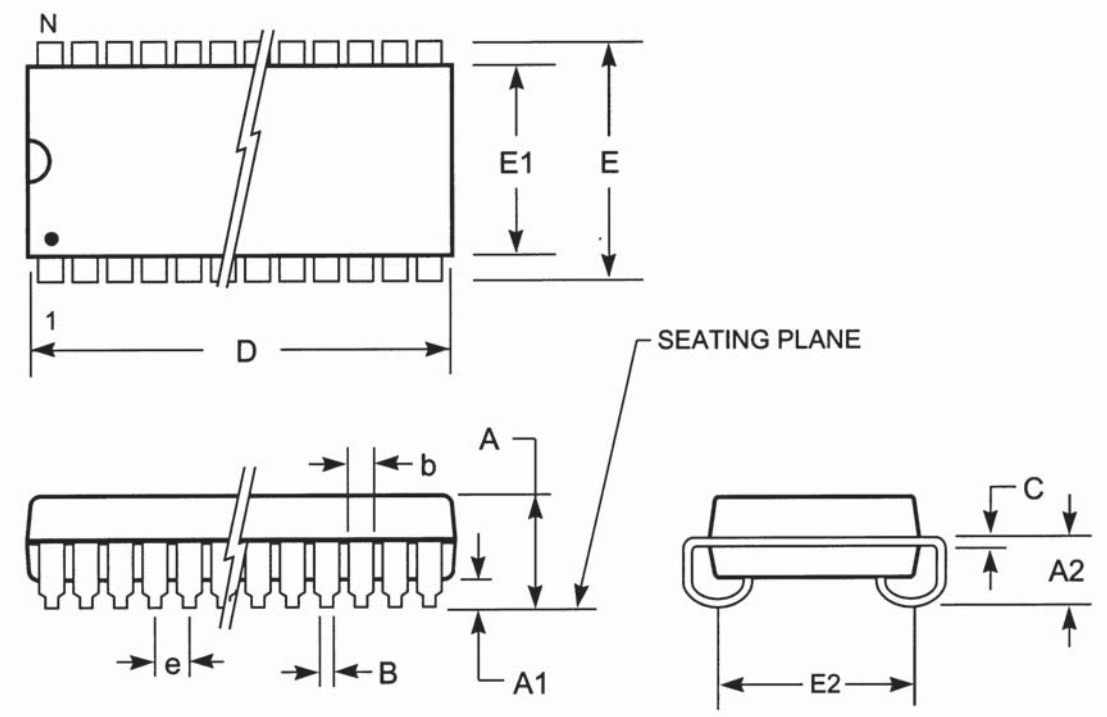
NOTES:

1. The internal write time is defined by the overlap of CE\ LOW and WE\ LOW. All signals must be in valid states to initiate a Write, but any one can go inactive to terminate the Write. The Data Input Setup and Hold timing are referenced to the rising or falling edge of the signal that terminates the Write.
2. I/O will assume the High-Z state if OE\ • V_{IH}.

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MECHANICAL DEFINITION*

Micross Case #906 (Package Designator DJ)



SYMBOL	MICROSS SPECIFICATIONS	
	MIN	MAX
A	0.128	0.148
A1	0.025	---
A2	0.082	---
B	0.015	0.020
b	0.026	0.032
C	0.007	0.013
D	0.820	0.830
E	0.435	0.445
E1	0.395	0.405
E2	0.370 BSC	
e	0.050 BSC	

**** All measurements are in inches.***

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ORDERING INFORMATION

Plastic SOJ

EXAMPLE: AS5LC1008DJ-12/XT

Device Number	Package Type	Speed ns	Options**	Process
AS5LC1008	DJ	-10	L	/*
AS5LC1008	DJ	-12	L	/*
AS5LC1008	DJ	-15	L	/*
AS5LC1008	DJ	-20	L	/*

***AVAILABLE PROCESSES**

IT = Industrial Temperature Range -40°C to +85°C
XT = Military Temperature Range -55°C to +125°C

****OPTION DEFINITIONS**

L = 2V Data Retention / Low Power

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DOCUMENT TITLE

128K x 8 SRAM High-Speed CMOS SRAM with 3.3V Revolutionary Pinout

Rev #	History	Release Date	Status
1.2	Added Micross Information	January 2010	Release
1.3	Added TSOPII Copper Lead Frame and RoHS compliant parts, pg 1 &10, Reduced Power Supply Currents:	March 2011	Release

Parameter	Speed	From (mA)	To (mA)
ICC	-10	160	105
ICC	-12	140	100
ICC	-15	130	95
ICC	-20	120	90
ISB	-10	45	35
ISB	-12	40	30
ISB	-15	35	25
ISB	-20	30	20
ISB1	-10	30	20
ISB1	-12	30	20
ISB1	-15	30	20
ISB1	-20	30	20
ISB2	-10	10	2
ISB2	-12	10	2
ISB2	-15	10	2
ISB2	-20	10	2

Added “L” Versions

1.4	Removed Cu-lead frame option	October 2013	Release

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