intersil

NOT RECOMMENDED FOR NEW DESIGNS

HI-5700/883

May 1997

8-Bit, 20 MSPS Flash A/D Converter

Features

- **This Circuit is Processed in Accordance to MIL-STD-883 and is Fully Conformant Under the Provisions of Paragraph 1.2.1.**
- **20 MSPS with No Missing Codes**
- **18MHz Full Power Input Bandwidth**
- **No Missing Codes Over Temperature**
- **Sample and Hold Not Required**
- **Single +5V Supply Voltage**
- **CMOS/TTL**
- **Overflow Bit**

Applications

- **Video Digitizing**
- **Radar Systems**
- **Medical Imaging**
- **Communication Systems**
- **High Speed Data Acquisition Systems**

Description

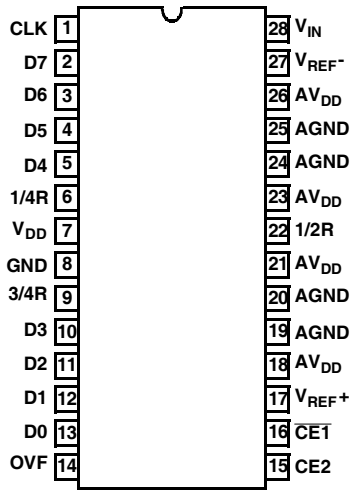
The HI-5700/883 is a monolithic, 8-bit, CMOS Flash Analog-to-Digital Converter. It is designed for high speed applications where wide bandwidth and low power consumption are essential. Its 20 MSPS speed is made possible by a parallel architecture which also eliminates the need for an external sample and hold circuit. The HI-5700/883 delivers ±0.5 LSB differential nonlinearity while consuming only 725mW (typical) at 20 MSPS. Microprocessor compatible data output latches are provided which present valid data to the output bus 1.5 clock cycles after the convert command is received. An overflow bit is provided to allow the series connection of two converters to achieve 9-bit resolution.

Ordering Information

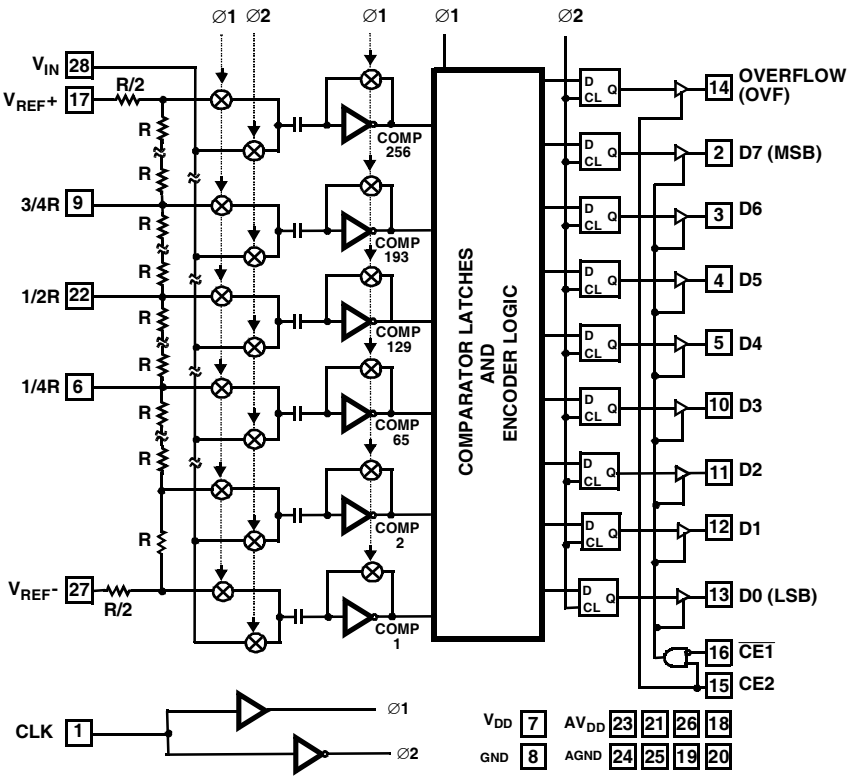
PART NUMBER	TEMPERATURE RANGE	PACKAGE
HI1-5700S/883	-55°C to +125°C	28 Lead CerDIP

Pinout

HI-5700/883
(28 LEAD CERDIP)
TOP VIEW



Functional Block Diagram



Spec Number **512023**
File Number **3286.1**

Pin Descriptions

PIN #	NAME	DESCRIPTION
1	CLK	Clock Input
2	D7	Bit 7, Output (MSB)
3	D6	Bit 6, Output
4	D5	Bit 5, Output
5	D4	Bit 4, Output
6	1/4R	1/4th Point of Reference Ladder
7	V_{DD}	Digital Power Supply
8	GND	Digital Ground
9	3/4R	3/4th Point of Reference Ladder
10	D3	Bit 3, Output
11	D2	Bit 2, Output
12	D1	Bit 1, Output
13	D0	Bit 0, Output (LSB)
14	OVF	Overflow, Output
15	CE2	Three-State Output Enable Input, Active High. (See Truth Table)
16	CE1	Three-State Output Enable Input, Active Low. (See Truth Table))
17	$V_{REF}+$	Reference Voltage Positive Input
18	AV_{DD}	Analog Power Supply, +5V
19	AGND	Analog Ground
20	AGND	Analog Ground
21	AV_{DD}	Analog Power Supply, +5V
22	1/2R	1/2 Point of Reference Ladder
23	AV_{DD}	Analog Power Supply, +5V
24	AGND	Analog Ground
25	AGND	Analog Ground
26	AV_{DD}	Analog Power Supply, +5V
27	$V_{REF}-$	Reference Voltage Negative Input
28	V_{IN}	Analog Input

Chip Enable Truth Table

CE1	CE2	D0 - D7	OVF
0	1	Valid	Valid
1	1	Three-State	Valid
X	0	Three-State	Three-State

X = Don't Care.

Absolute Maximum Ratings

Supply Voltage, V_{DD} to GND . . . . . (GND - 0.5) < V_{DD} < +7.0V
Analog and Reference Input Pins. .(V_{SS} - 0.5) < V_{INA} < (V_{DD} +0.5V)
Digital I/O Pins . . . . . (GND - 0.5) < $V_{I/O}$ < (V_{DD} +0.5V)
Operating Temperature Range
HI1-5700S/883 . . . . . -55°C to +125°C
Junction Temperature. . . . . +175°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (Soldering, 10s) . . . . . 300°C
ESD Clasification . . . . . Class 1

Thermal Information

Thermal Resistance	θ_{JA}	θ_{JC}
HI1-5700S/883	47°C/W	28°C/W

Power Dissipation at +75°C (Note 1)
HI1-5700S/883 . . . . . 2100mW
Power Dissipation Derating Factor Above +75°C
HI1-5700S/883 . . . . . 21mW/°C
Reliabiliy Information
Transistor Count 14677
Worst Case Density . . . . . 3.05 x 10^4A/cm^2

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $AV_{DD} = V_{DD} = +5.0V$; $V_{REF}+ = +4.0V$; $V_{REF}- = GND = AGND = 0V$; F_S = Specified Clock Frequency at 50% Duty Cycle; $C_L = 30pF$; Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT
ACCURACY							
Integral Linearity Error (Best Fit Method)	INL	F_S = 15MHz, f_{IN} = DC	1	+25°C	-	±2.0	LSB
			2, 3	+125°C, -55°C	-	±2.65	LSB
		F_S = 20MHz, f_{IN} = DC	1	+25°C	-	±2.25	LSB
			2, 3	+125°C, -55°C	-	±4.1	LSB
Differential Linearity Error (Guaranteed No Missing Codes)	DNL	F_S = 15MHz, f_{IN} = DC	1	+25°C	-	±0.9	LSB
			2, 3	+125°C, -55°C	-	±1.0	LSB
		F_S = 20MHz, f_{IN} = DC	1	+25°C	-	±0.9	LSB
			2, 3	+125°C, -55°C	-	±1.0	LSB
Offset Error (Adjustable to Zero)	VOS	F_S = 15MHz, f_{IN} = DC	1	+25°C	-	±8.0	LSB
			2, 3	+125°C, -55°C	-	±9.5	LSB
		F_S = 20MHz, f_{IN} = DC	1	+25°C	-	±8.0	LSB
			2, 3	+125°C, -55°C	-	±9.5	LSB
Full Scale Error (Adjustable to Zero)	FSE	F_S = 15MHz, f_{IN} = DC	1	+25°C	-	±4.5	LSB
			2, 3	+125°C, -55°C	-	±8.0	LSB
		F_S = 20MHz, f_{IN} = DC	1	+25°C	-	±4.5	LSB
			2, 3	+125°C, -55°C	-	±8.0	LSB
ANALOG INPUT							
Analog Input Resistance	R_{IN}	V_{IN} = 4V	1	+25°C	4	-	MΩ
			2, 3	+125°C, -55°C	4	-	MΩ
Analog Input Bias Current	I_B	V_{IN} = 0V, 4V	1	+25°C		±1.0	µA
			2, 3	+125°C, -55°C		±1.0	µA
REFERENCE INPUT							
Total Reference Resistance	R_L		1	+25°C	250	-	Ω
			2, 3	+125°C, -55°C	235	-	Ω

TABLE 1. DC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $AV_{DD} = V_{DD} = +5.0V$; $V_{REF}+ = +4.0V$; $V_{REF}- = GND = AGND = 0V$; F_S = Specified Clock Frequency at 50% Duty Cycle; $C_L = 30pF$; Unless Otherwise Specified.

PARAMETERS	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT
DIGITAL INPUTS							
Input High Voltage	V_{IH}		1	+25°C	2.0	-	V
			2, 3	+125°C, -55°C	2.0	-	V
Input Low Voltage	V_{IL}		1	+25°C	-	0.8	V
			2, 3	+125°C, -55°C	-	0.8	V
Logic Input Current	I_{IN}	V_{IN} = 0V, +5V	1	+25°C	-	±1	µA
			2, 3	+125°C, -55°C	-	±1	µA
DIGITAL OUTPUTS							
Output Leakage	I_{OZ}	CE2 = 0V, V_O = 0V, 5V	1	+25°C	-	±1.0	µA
			2, 3	+125°C, -55°C	-	±1.0	µA
Output Logic Source Current	I_{OH}	V_O = 4.5V	1	+25°C	-3.2	-	mA
			2, 3	+125°C, -55°C	-3.2	-	mA
Output Logic Sink Current	I_{OL}	V_O = 0.4V	1	+25°C	3.2	-	mA
			2, 3	+125°C, -55°C	3.2	-	mA
POWER SUPPLY REJECTION							
Offset Error PSRR	ΔVOS	V_{DD} = 5V ±10%	1	+25°C	-	±2.75	LSB
			2, 3	+125°C, -55°C	-	±5.5	LSB
Gain Error PSRR	ΔFSE	V_{DD} = 5V ±10%	1	+25°C	-	±2.75	LSB
			2, 3	+125°C, -55°C	-	±5.5	LSB
POWER SUPPLY CURRENT							
Supply Current	I_{DD}	F_S = 20MHz	1	+25°C	-	180	mA
			2, 3	+125°C, -55°C	-	190	mA

NOTE:

1. Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS

Device Tested at: $AV_{DD} = V_{DD} = +5.0V$; $V_{REF}+ = +4.0V$; $V_{REF}- = GND = AGND = 0V$; F_S = Specified Clock Frequency at 50% Duty Cycle; $C_L = 30pF$; Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS MIN	LIMITS MAX	UNIT
Maximum Conversion Rate		No Missing Codes	9	+25°C	20	-	MSPS
			10, 11	+125°C, -55°C	20	-	MSPS
Data Output Enable Time	t_{EN}		9	+25°C	-	25	ns
			10, 11	+125°C, -55°C	-	30	ns

TABLE 2. AC ELECTRICAL PERFORMANCE CHARACTERISTICS (Continued)

Device Tested at: $AV_{DD} = V_{DD} = +5.0V$; $V_{REF}+ = +4.0V$; $V_{REF}- = GND = AGND = 0V$; F_S = Specified Clock Frequency at 50% Duty Cycle; $C_L = 30pF$; Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	GROUP A SUBGROUP	TEMPERATURE	LIMITS		UNIT
					MIN	MAX	
Data Output Disable Time	t_{DIS}		9	+25°C	-	20	ns
			10, 11	+125°C, -55°C	-	25	ns
Data Output Delay	t_{OD}		9	+25°C	-	25	ns
			10, 11	+125°C, -55°C	-	30	ns
Data Output Hold	t_H		9	+25°C	10	-	ns
			10, 11	+125°C, -55°C	5	-	ns

TABLE 3. ELECTRICAL PERFORMANCE CHARACTERISTICS (NOTE 1)

Device Characterized at: $AV_{DD} = V_{DD} = +5.0V$; $V_{REF}+ = +4.0V$; $V_{REF}- = GND = AGND = 0V$; F_S = Specified Clock Frequency at 50% Duty Cycle; $C_L = 30pF$; Unless Otherwise Specified.

PARAMETER	SYMBOL	CONDITIONS	TEMPERATURE	LIMITS		UNIT
				MIN	MAX	
Minimum Conversion Rate		No Missing Codes	+25°C, +125°C, -55°C	-	0.125	MSPS

NOTE:

1. Parameters listed in Table 3 are controlled via design or process parameters and are not directly tested at final production. These parameters are lab characterized upon initial design release, or upon design changes. These parameters are guaranteed by characterization based upon data from multiple production runs which reflect lot to lot and within lot variation.

TABLE 4. ELECTRICAL TEST REQUIREMENTS

MIL-STD-883 TEST REQUIREMENTS	SUBGROUPS (SEE TABLES 1 AND 2)
Interim Electrical Parameters (Pre Burn-In)	1
Final Electrical Test Parameters	1 (Note 1), 2, 3, 9, 10, 11
Group A Test Requirements	1, 2, 3, 9, 10, 11
Groups C & D Endpoints	1

NOTE:

1. PDA applies to Subgroup 1 only. No other subgroups are included in PDA.

Die Characteristics

DIE DIMENSIONS:
154.3 x 173.2 x 19 ± 1mils

METALLIZATION:
Type: Si - Al
Thickness: 11kÅ ± 1kÅ

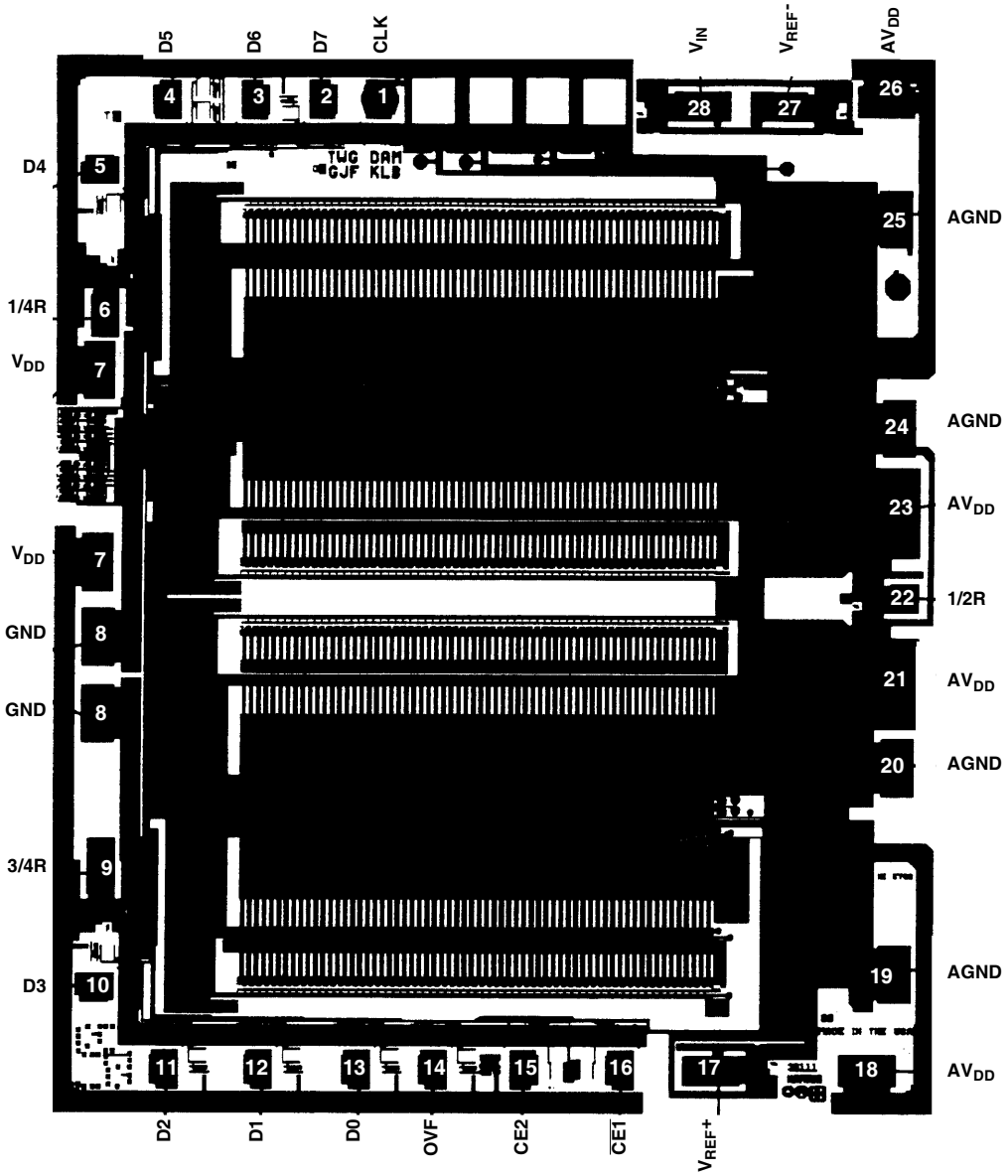
GLASSIVATION:
Type: SiO_2
Thickness: 8kÅ ± 1kÅ

DIE ATTACH:
Material: Gold Silicon Eutectic Alloy
Temperature: Ceramic DIP - 460°C (Max)

WORST CASE CURRENT DENSITY:
3.05×10^4 A/cm^2

Metallization Mask Layout

HI-5700/883



Timing Waveforms

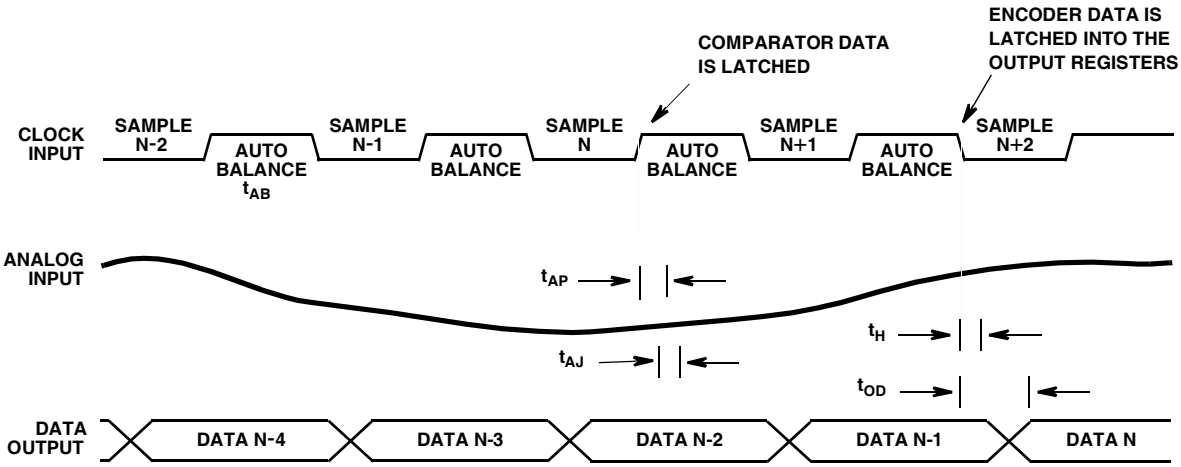


FIGURE 1. INPUT-TO-OUTPUT TIMING

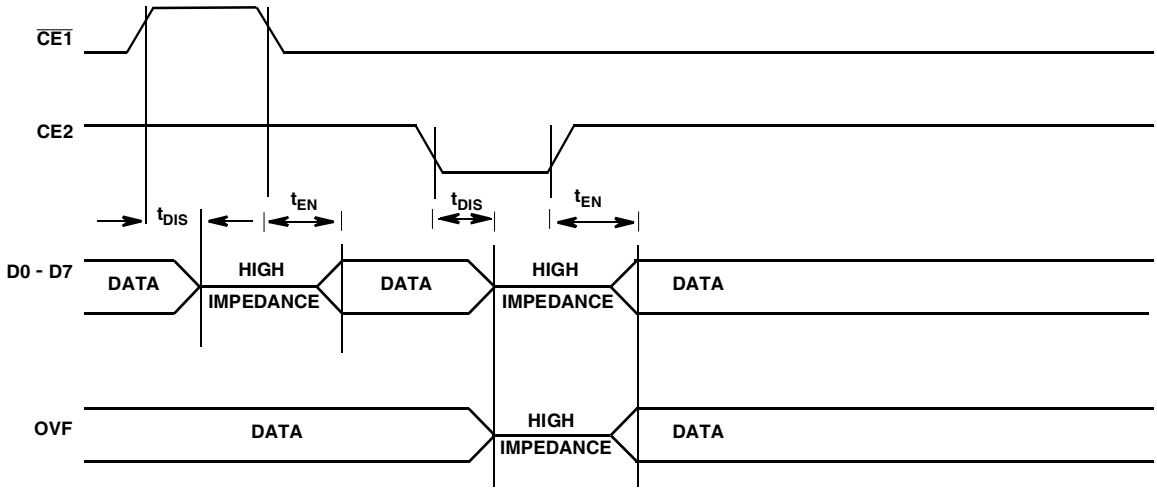


FIGURE 2. OUTPUT ENABLE TIMING

Burn-In Circuit

HI-5700/883 CERAMIC DIP