

SN5450, SN7450

DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

SDLS112 - DECEMBER 1983 - REVISED MARCH 1988

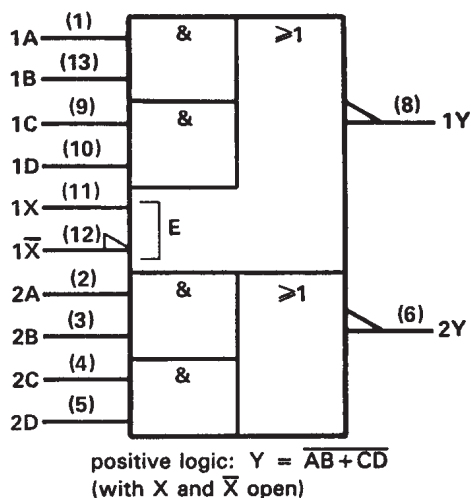
- Package Options Include Plastic and Ceramic DIPs and Ceramic Flat Packages
- Dependable Texas Instruments Quality and Reliability

description

These devices contain two independent 2-wide 2-input AND-OR-INVERT gates with one gate expandable. They perform the Boolean function $Y = \overline{AB + CD}$ with X and $\overline{X}$ left open.

The SN5450 is characterized for operation over the full military temperature range of -55°C to 125°C . The SN7450 is characterized for operation from 0°C to 70°C .

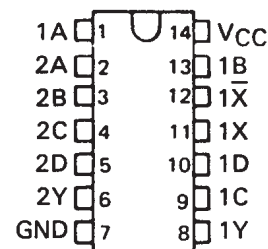
logic symbol†



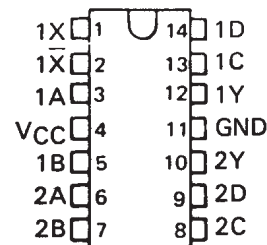
† This symbol is in accordance with ANSI/IEEE Std 91-1984 and IEC Publication 617-12.

Pin numbers shown are for J and N packages.

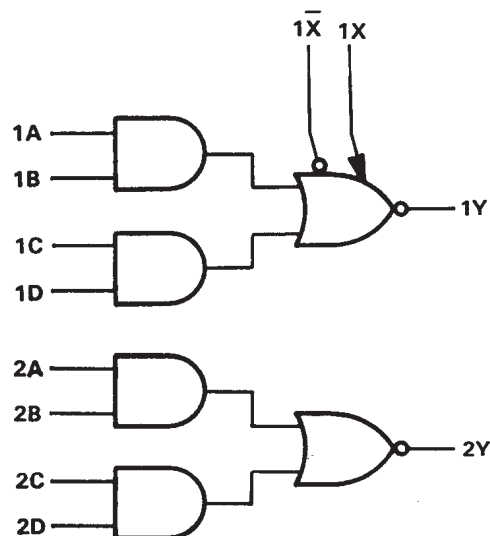
SN5450 . . . J PACKAGE
SN7450 . . . N PACKAGE
(TOP VIEW)



SN5450 . . . W PACKAGE
(TOP VIEW)



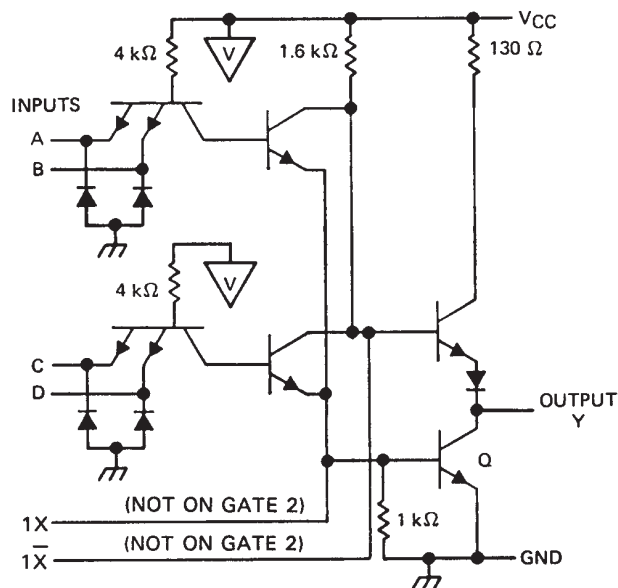
logic diagram (positive logic)



SN5450, SN7450 DUAL 2-WIDE 2-INPUT AND-OR-INVERT GATES (ONE GATE EXPANDABLE)

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schematic (each AND-OR-INVERT gate)



Resistor values shown are nominal.
 If expander is not used, leave X and $\bar{X}$ open.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	5.5 V
Operating free-air temperature range: SN5450	−55 °C to 125 °C
SN7450	0 °C to 70 °C
Storage temperature range	−65 °C to 150 °C

NOTE 1: Voltage values are with respect to network ground terminal.

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recommended operating conditions

		SN5450			SN7450			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage			0.8			0.8	V
I_{OH}	High-level output current			– 0.4			– 0.4	mA
I_{OL}	Low-level output current			16			16	mA
T_A	Operating free-air temperature	– 55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS†	SN5450			SN7450			UNIT
		MIN	TYP‡	MAX	MIN	TYP‡	MAX	
V_{IK}	$V_{CC} = \text{MIN}, I_I = -12 \text{ mA}$			– 1.5			– 1.5	V
V_{OH}	$V_{CC} = \text{MIN}, V_{IL} = 0.8 \text{ V}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4		2.4	3.4		V
V_{OL}	$V_{CC} = \text{MIN}, V_{IH} = 2 \text{ V}, I_{OL} = 16 \text{ mA}$		0.2	0.4		0.2	0.4	V
I_I	$V_{CC} = \text{MAX}, V_I = 5.5 \text{ V}$			1			1	mA
I_{IH}	$V_{CC} = \text{MAX}, V_{IH} = 2.4 \text{ V}$			40			40	µA
I_{IL}	$V_{CC} = \text{MAX}, V_{IL} = 0.4 \text{ V}$			– 1.6			– 1.6	mA
$I_{OS}§$	$V_{CC} = \text{MAX}$	– 20		– 55	– 18		– 55	mA
I_{CCH}	$V_{CC} = \text{MAX}, V_I = 0 \text{ V}$		4	8		4	8	mA
I_{CCL}	$V_{CC} = \text{MAX}, \text{See Note 2}$		7.4	14		7.4	14	mA
$I_{\bar{X}}¶$	$V_{\bar{X}X} = 0.4 \text{ V}, I_{OL} = 16 \text{ mA}$			– 2.9			– 3.1	mA
$V_{BE(Q)}¶$	$I_X + I_{\bar{X}} = 0.41 \text{ mA}, R_{\bar{X}X} = 0, I_{OL} = 16 \text{ mA}$			1.1				V
	$I_X + I_{\bar{X}} = 0.62 \text{ mA}, R_{\bar{X}X} = 0, I_{OL} = 16 \text{ mA}$						1	
$V_{OH}¶$	$I_X = 0.15 \text{ mA}, I_{\bar{X}} = -0.15 \text{ mA}, I_{OH} = -0.4 \text{ mA}$	2.4	3.4					V
	$I_X = 0.27 \text{ mA}, I_{\bar{X}} = -0.27 \text{ mA}, I_{OH} = -0.4 \text{ mA}$				2.4	3.4		
$V_{OL}¶$	$I_X + I_{\bar{X}} = 0.3 \text{ mA}, R_{\bar{X}X} = 138 \Omega, I_{OL} = 16 \text{ mA}$		0.2	0.4				V
	$I_X + I_{\bar{X}} = 0.43 \text{ mA}, R_{\bar{X}X} = 130 \Omega, I_{OL} = 16 \text{ mA}$					0.2	0.4	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$.

§ Not more than one output should be shorted at a time.

¶ Using expander inputs, $V_{CC} = \text{MIN}, T_A = \text{MIN}$, except typical values.

NOTE 2: All inputs of one AND gate at 4.5 V, all others at GND.

switching characteristics, $V_{CC} = 5 \text{ V}, T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Any	Y	$R_L = 400 \Omega, C_L = 15 \text{ pF}$ Expander pins open		13	22	ns
t_{PHL}					8	15	ns

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)	Op Temp (°C)	Top-Side Markings (4)	Samples
JM38510/00501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00501BCA	Samples
M38510/00501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00501BCA	Samples
M38510/00501BCA	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	JM38510/ 00501BCA	Samples
SN5450J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN5450J	Samples
SN5450J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SN5450J	Samples
SN7450N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SN7450N	OBSOLETE	PDIP	N	14		TBD	Call TI	Call TI	0 to 70		
SNJ5450J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5450J	Samples
SNJ5450J	ACTIVE	CDIP	J	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5450J	Samples
SNJ5450W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5450W	Samples
SNJ5450W	ACTIVE	CFP	W	14	1	TBD	A42	N / A for Pkg Type	-55 to 125	SNJ5450W	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

⁽⁴⁾ Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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OTHER QUALIFIED VERSIONS OF SN5450, SN7450 :

- Catalog: [SN7450](#)
- Military: [SN5450](#)

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



PINS ** DIM	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)

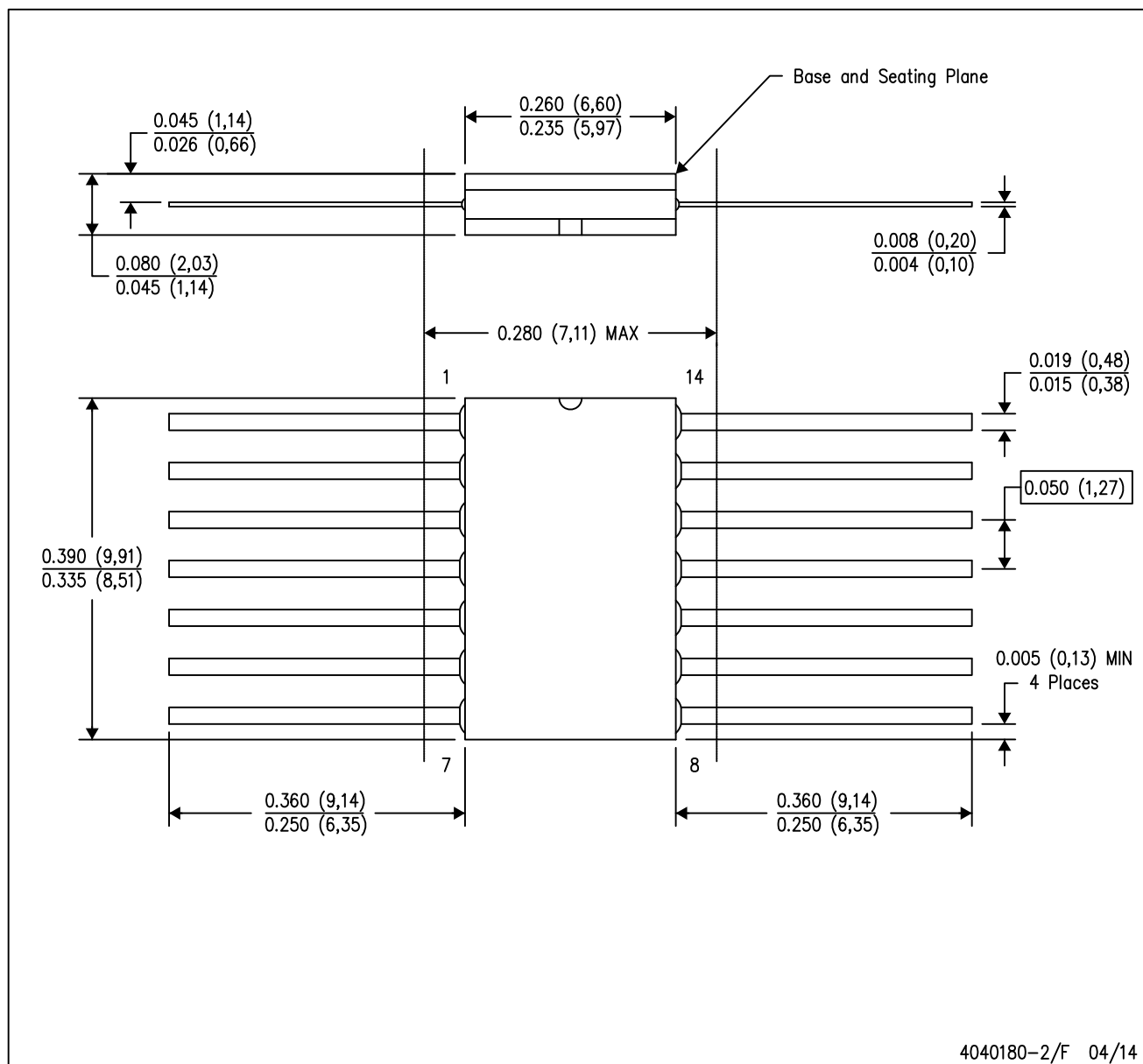


4040083/F 03/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package is hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - E. Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F14)

CERAMIC DUAL FLATPACK



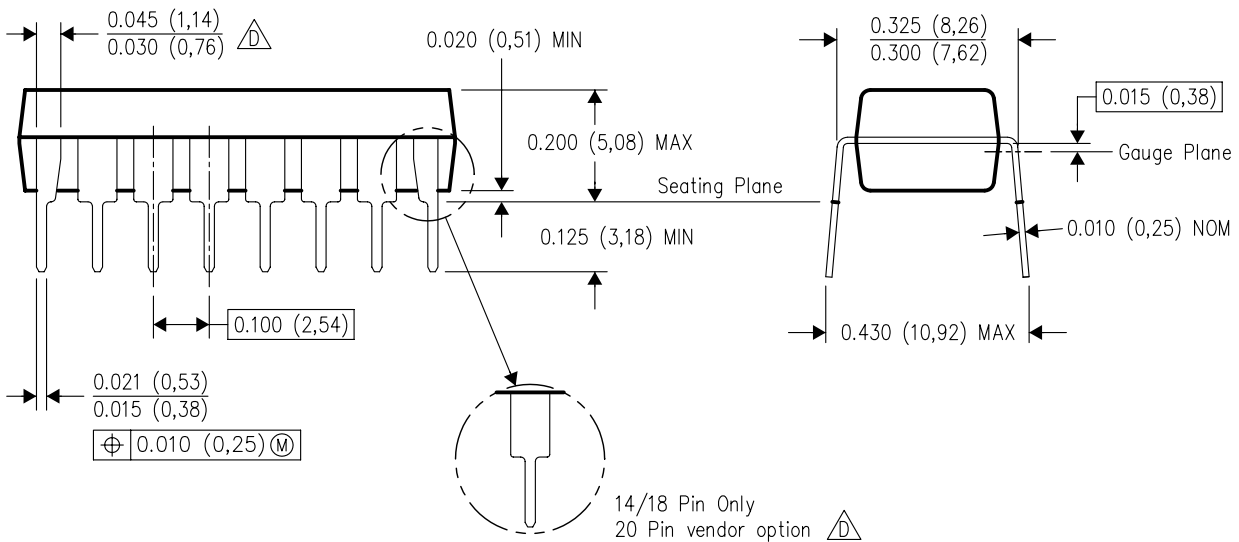
N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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