

SLUS530F − SEPTEMBER 2002 − REVISED AUGUST 2005

SINGLE-CHIP, LI-ION CHARGE MANAGEMENT IC FOR HANDHELD APPLICATIONS (bqTINY™)

FEATURES

- **Small 3 mm × 3 mm MLP (QFN) Package**
- **Ideal for Low-Dropout Designs for Single-Cell Li−Ion or Li−Pol Packs in Space Limited Applications**
- **Integrated Power FET and Current Sensor for Up to 1-A Charge Applications**
- **Reverse Leakage Protection Prevents Battery Drainage**
- **Integrated Current and Voltage Regulation**
- **± 0.5% Voltage Regulation Accuracy**
- **Charge Termination by Minimum Current and Time**
- **Precharge Conditioning With Safety Timer**
- **Status Outputs for LED or System Interface Indicates Charge and Fault Conditions**
- **Battery Insertion and Removal Detection**
- **Works With Regulated and Unregulated Supplies**
- **Short-Circuit Protection**

APPLICATIONS

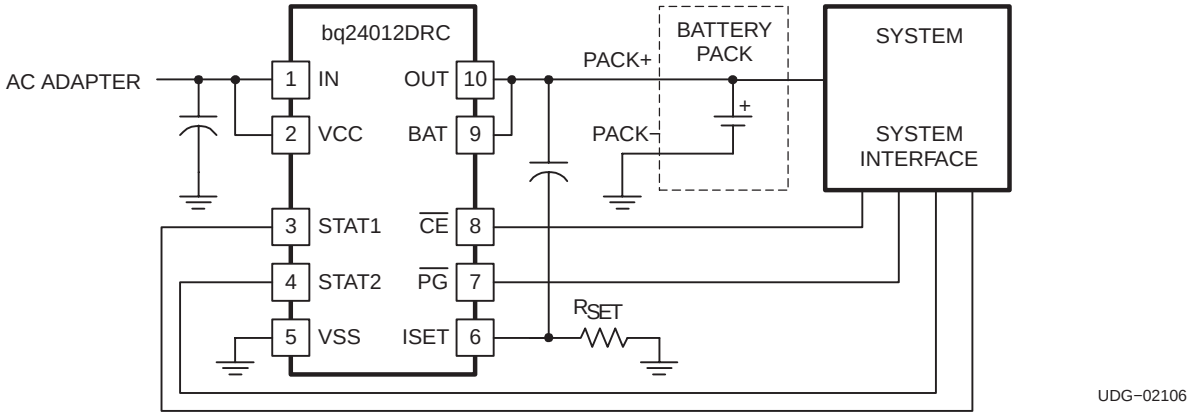
- **Cellular Phones**
- **PDAs, MP3 Players**
- **Digital Cameras**
- **Internet Appliances**

DESCRIPTION

The bqTINY™ series are highly integrated Li-Ion and Li-Pol linear charge management devices targeted at space limited portable applications. The bqTINY™ series offer integrated powerFET and current sensor, reverse blocking protection, high accuracy current and voltage regulation, charge status, and charge termination, in a small package.

The bqTINY™ charges the battery in three phases: conditioning, constant current, and constant voltage. Charge is terminated based on minimum current. An internal charge timer provides a backup safety feature for charge termination. The bqTINY™ automatically re-starts the charge if the battery voltage falls below an internal threshold. The bqTINY™ automatically enters sleep mode when V_{CC} supply is removed.

In addition to the standard features, different versions of the bqTINY™ offer a multitude of additional features. These include temperature sensing input for detecting hot or cold battery packs; power good ($\overline{PG}$) output indicating the presence of valid input power; a TTL−level charge-enable input ($\overline{CE}$) used to disable or enable the charge process; and a TTL-level timer and termination enable ($\overline{TTE}$) input used to disable or enable the fast-charge timer and charge termination.



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	CHARGE REGULATION VOLTAGE (V)(1)	OPTIONAL FUNCTIONS(1)	PART NUMBER(2)	MARKINGS
−40°C to 125°C	4.2	$\overline{PG}$ and TS	bq24010DRCR	AZN
	4.2	$\overline{PG}$ and $\overline{CE}$	bq24012DRCR	AZP
	4.2	$\overline{CE}$ and $\overline{TTE}$	bq24013DRCR	AZQ
	4.2	$\overline{CE}$ and TS	bq24014DRCR	AZR
			bq24014DRCT	

(1) Contact Texas Instruments for other options.
(2) The DRC package is available only taped and reeled. Quantities are 3,000 devices per reel (e.g. bq24010DRCR) and 250 devices per mini-reel (e.g. bq24014DRCT).

DISSIPATION RATINGS

PACKAGE	θ_{JA}	T_A < 40°C POWER RATING	DERATING FACTOR ABOVE T_A = 40°C
DRC(1)	47 °C/W	1.5 W	0.021 W/°C

(1) This data is based on using the JEDEC High-K board and the exposed die pad is connected to a copper pad on the board. This is connected to the ground plane by a 2x3 via matrix.

ABSOLUTE MAXIMUM RATINGS(1)

			UNIT
Supply voltage range, (V_{CC} all with respect to V_{SS})		−0.3 to 18	V
Input voltage range(2)	IN, STAT1, STAT2, TS, $\overline{PG}$, $\overline{CE}$, $\overline{TTE}$	−0.3 to VCC	
	BAT, OUT, ISET	−0.3 to 7	VDC
Voltage difference between V_{CC} and IN inputs $V_{CC} - V_{IN}$		± 0.5	V
Output sink/source current	STAT1, STAT2, $\overline{PG}$	15	mA
Output current	IN, OUT	1.5	A
Operating free−air temperature range, T_A		−40 to 125	°C
Junction temperature range, T_J			
Storage temperature, T_{stg}		−65 to 150	
Lead temperature 1,6 mm (1/16 inch) from case for 10 seconds		300	

(1) Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltages are DC and with respect to V_{SS}.

RECOMMENDED OPERATING CONDITIONS(1)

	MIN	NOM	MAX	UNIT
Supply voltage(1), V_{CC}	3.0		16.5	V
Input voltage(1), V_{IN}	3.0		16.5	
Operating junction temperature range, T_J	−40		125	°C

(1) Pins VCC and IN must be tied together.

ELECTRICAL CHARACTERISTICS

over $0°C \le T_J \le 125°C$ and recommended supply voltage, unless otherwise noted

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
INPUT CURRENT					
VCC current, $I_{CC(VCC)}$	$V_{CC} > V_{CC(min)}$, STATx pins in OFF state	0	3.5	5	mA
Sleep current, $I_{CC(SLP)}$	Sum of currents into OUT and BAT pins, $V_{CC} < V_{(SLP)}$			5	µA
Input bias current on BAT pin, $I_{IB(BAT)}$				500	nA
Input current on TS pin, $I_{IB(TS)}$	$V_{I(TS)} \le 10$ V			1	µA
Input current on $\overline{CE}$ pin, $I_{IB(CE)}$				1	
Input bias current on $\overline{TTE}$ pin, $I_{IB(TTE)}$				1	
VOLTAGE REGULATION $V_{O(REG)} + V_{(DO-MAX)} \le V_{CC}$, $I_{(TERM)} < I_{O(OUT)} \le 1$ A					
Output voltage, $V_{O(REG)}$			4.20		V
Voltage regulation accuracy	$T_A = 25°C$	−0.5%		0.5%	
		−1%		1%	
Dropout voltage ($V_{(IN)} - V_{(OUT)}$), $V_{(DO)}$	$V_{O(REG)} + V_{(DO-MAX)}) \le V_{CC}$, $I_{O(OUT)} = 1$A		650	790	mV
CURRENT REGULATION					
Output current range, $I_{O(OUT)}$ (1)	$V_{CC} \ge 4.5$ V, $V_{IN} \ge 4.5$ V, $V_{I(BAT)} > V_{(LOWV)}$, $V_{IN} - V_{I(BAT)} > V_{(DO-MAX)}$	100		1000	mA
Output current set voltage, $V_{(SET)}$	Voltage on ISET pin, $V_{CC} \ge 4.5$ V, $V_{IN} \ge 4.5$ V, $V_{I(BAT)} > V_{(LOWV)}$, $V_{IN} - V_{I(BAT)} > V_{(DO-MAX)}$ $V_{O(REG)} = 4.2$ V	2.45	2.50	2.55	V
Output current set factor, $K_{(SET)}$	50 mA ≤ $I_{O(OUT)}$ ≤ 1000 mA, $V_{I(ISET)} \ge V_{(TAPER)}$	315	335	355	
	10 mA ≤ $I_{O(OUT)}$ < 50 mA, $V_{I(ISET)} \ge V_{(TAPER)}$	315	372	430	
	10 mA ≤ $I_{O(OUT)}$ < 50 mA, $V_{I(ISET)} < V_{(TAPER)}$	350		1000	
PRECHARGE AND SHORT-CIRCUIT CURRENT REGULATION					
Precharge to fast-charge transition threshold, $V_{(LOWV)}$	Voltage on BAT pin	2.80	2.95	3.10	V
Precharge to short-circuit transition threshold, $V_{(SC)}$	Voltage on BAT pin	1.0	1.4	1.8	
Precharge range, $I_{O(PRECHG)}$ (2)	$V_{(SC)} < V_{I(BAT)} < V_{(LOWV)}$, $t < t_{(PRECHG)}$	10		100	mV
Precharge set voltage, $V_{(PRECHG)}$	Voltage on ISET pin, $V_{(SC)} < V_{I(BAT)} < V_{(LOWV)}$	225	250	280	
Short circuit current, I_{SC}	$V_{(SC)} > V_{I(BAT)}$	660	900	1200	µA
CHARGE TAPER AND TERMINATION DETECTION					
Charge taper detection range, $I_{(TAPER)}$ (3)	$V_{I(BAT)} > V_{(RCH)}$, $t < t_{(TAPER)}$	10		100	mA
Charge taper detection set voltage, $V_{(TAPER)}$	Voltage on ISET pin, $V_{I(BAT)} > V_{(RCH)}$, $t < t_{(TAPER)}$, $V_{I(BAT)} = V_{O(REG)}$	225	250	275	mV
Charge termination detection set voltage, $V_{(TERM)}$	Voltage on ISET pin, $V_{I(BAT)} = V_{O(REG)}$, $V_{I(BAT)} > V_{(RCH)}$, $I_{(TERM)} = K_{(SET)} \times V_{(TERM)} / R_{(SET)}$	5.0	17.5	50.0	
TEMPERATURE COMPARATOR					
Lower threshold, $V_{(TS1)}$	Voltage on TS pin	29	30	31	%VCC
Upper threshold, $V_{(TS2)}$	Voltage on TS pin	60	61	62	
Hysteresis			1		

(1)
$$I_{O(OUT)} = \frac{\left(K_{(SET)} \times V_{(SET)}\right)}{R_{SET}}$$

(2)
$$I_{O(PRECHG)} = \frac{\left(K_{(SET)} \times V_{(PRECHG)}\right)}{R_{SET}}$$

(3)
$$I_{O(TAPER)} = \frac{\left(K_{(SET)} \times V_{(TAPER)}\right)}{R_{SET}}$$

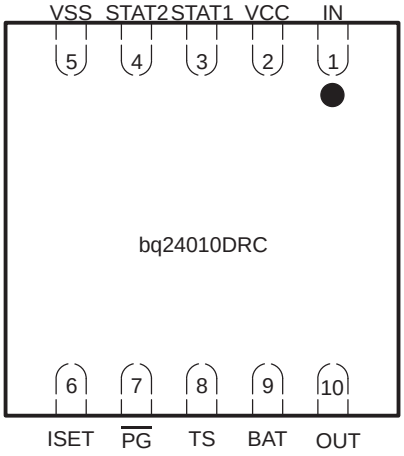
ELECTRICAL CHARACTERISTICS (continued)

over $0°C \le T_J \le 125°C$ and recommended supply voltage, unless otherwise noted

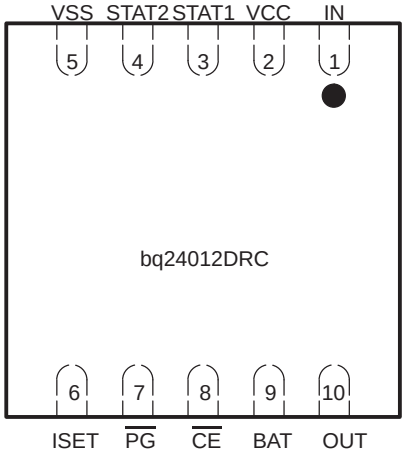
PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
BATTERY RECHARGE THRESHOLD					
Recharge threshold, $V_{(RCH)}$		$V_{O(REG)}$ −0.135	$V_{O(REG)}$ −0.1	$V_{O(REG)}$ −0.075	V
STAT1, STAT2, and $\overline{PG}$ OUTPUTS					
Output (low) saturation voltage, V_{OL}	I_O = 10 mA			0.5	V
CHARGE ENABLE ($\overline{CE}$) AND TIMER AND TERMINATION ENABLE ($\overline{TTE}$) INPUTS					
Low-level input voltage, V_{IL}	I_{IL} = 1 µA	0		0.8	V
High-level input voltage, V_{IH}	I_{IH} = 1 µA	2.0			
TIMERS					
Precharge time, $t_{(PRECHG)}$		1,548	2,065	2,581	s
Taper time, $t_{(TAPER)}$		1,548	2,065	2,581	
Charge time, $t_{(CHG)}$		15,480	20,650	25,810	
SLEEP COMPARATOR					
Sleep mode entry threshold voltage, V_{SLP}	$V_{POR} \le V_{(IBAT)} \le V_{O(REG)}$			$V_{CC} \le V_{I(BAT)}$ +30 mV	V
Sleep mode exit threshold voltage	$V_{POR} \le V_{(IBAT)} \le V_{O(REG)}$	$V_{CC} \ge V_{I(BAT)}$ +22 mV			
Sleep mode deglitch time	VCC decreasing below threshold, 100 ns fall time, 10 mV overdrive	250		650	ms
BATTERY DETECTION THRESHOLDS					
Battery detection current, $I_{(DETECT)}$	$2 V \le V_{(IBAT)} \le V_{(RCH)}$	−3.1	−4.6	−6.1	mA
Battery detection time, $t_{(DETECT)}$	$2 V \le V_{(IBAT)} \le V_{(RCH)}$	100	125	150	ms
Fault current, $I_{(FAULT)}$	$V_{(IBAT)} < V_{(RCH)}$ and/or $t > t_{(PRECHG)}$	660	900	1200	µA
POWER−ON RESET AND INPUT VOLTAGE RAMP RATE					
Power−on reset threshold voltage, V_{POR}(4)		2.25	2.5	2.75	V

(4) Ensured by design. Not production tested.

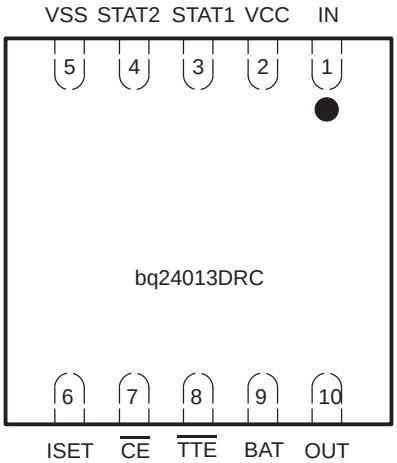
DRC PACKAGE
(TOP VIEW)



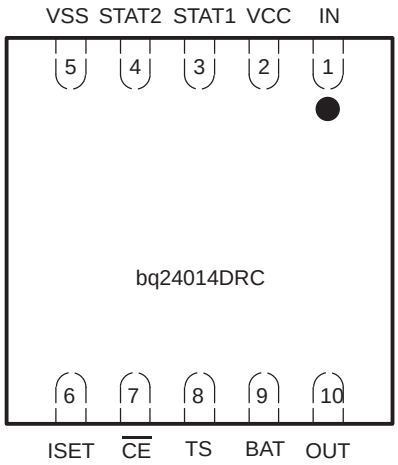
DRC PACKAGE
(TOP VIEW)



DRC PACKAGE
(TOP VIEW)



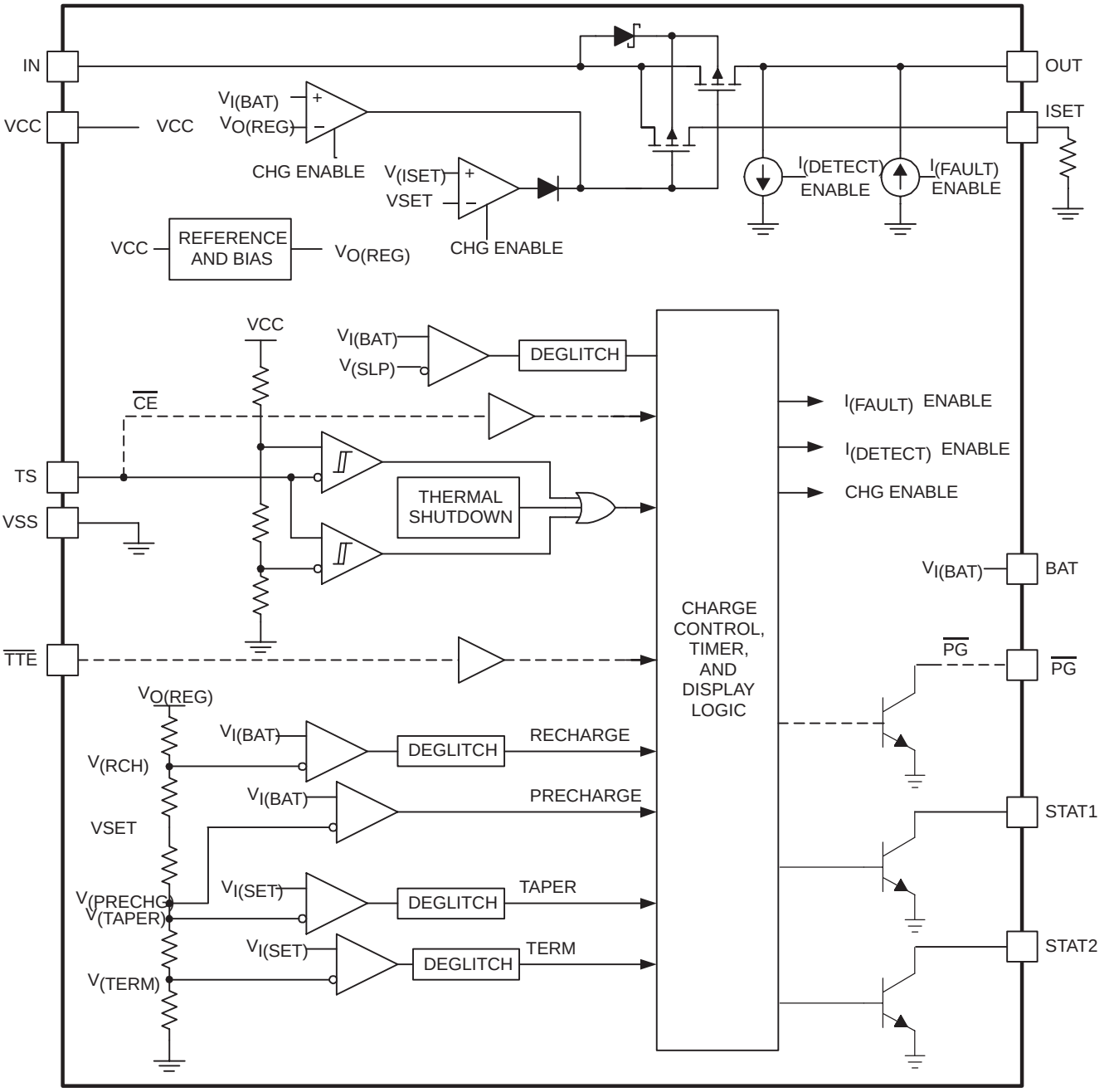
DRC PACKAGE
(TOP VIEW)



TERMINAL FUNCTIONS

NAME	TERMINAL				I/O	DESCRIPTION
	bq24010	bq24012	bq24013	bq24014		
BAT	9	9	9	9	I	Battery voltage sense input
$\overline{CE}$	−	8	7	7	I	Charge enable input (active low)
IN	1	1	1	1	I	Charge input voltage. This input must be tied to the VCC pin.
ISET	6	6	6	6	O	Charge current set point
OUT	10	10	10	10	O	Charge current output
$\overline{PG}$	7	7	−	−	O	Power good status output (open collector)
STAT1	3	3	3	3	O	Charge status output 1 (open collector)
STAT2	4	4	4	4	O	Charge status output 2 (open collector)
$\overline{TTE}$	−	−	8	−	I	Timer and termination enable input (active low)
TS	8	−	−	8	I	Temperature sense input
VCC	2	2	2	2	I	VCC supply input
VSS	5	5	5	5	−	Ground input
Exposed Thermal PAD	pad	pad	pad	pad	−	There is an internal electrical connection between the exposed thermal pad and V_{SS} pin of the device. The exposed thermal pad must be connected to the same potential as the Vss pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. V_{SS} pin must be connected to ground at all times.

FUNCTIONAL BLOCK DIAGRAM



Dotted lines represent optional features

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TYPICAL CHARACTERISTICS

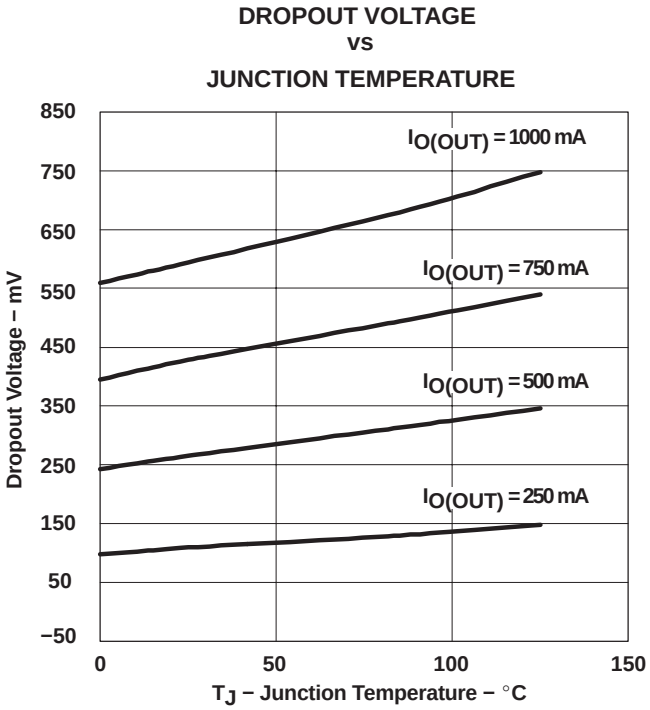


Figure 1

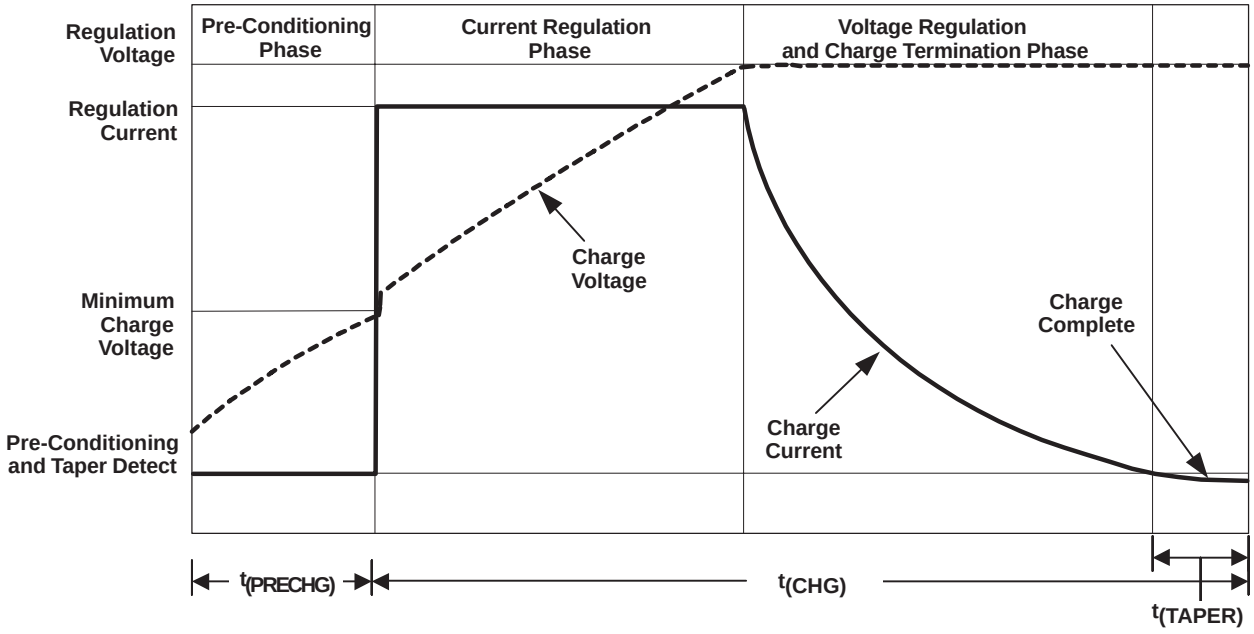


Figure 2. Typical Charging Profile

FUNCTIONAL DESCRIPTION

The bqTINY™ supports a precision Li-Ion, Li-Pol charging system suitable for single-cells . Figure 2 shows a typical charge profile, application circuit and Figure 5 shows an operational flow chart.

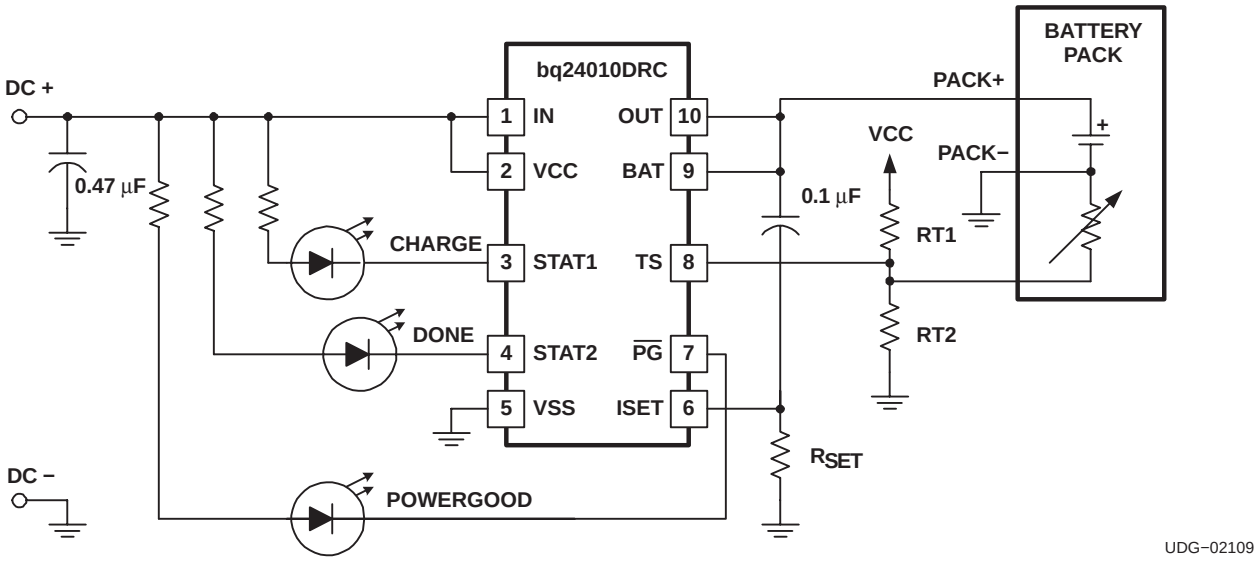


Figure 3. Typical Application Circuit

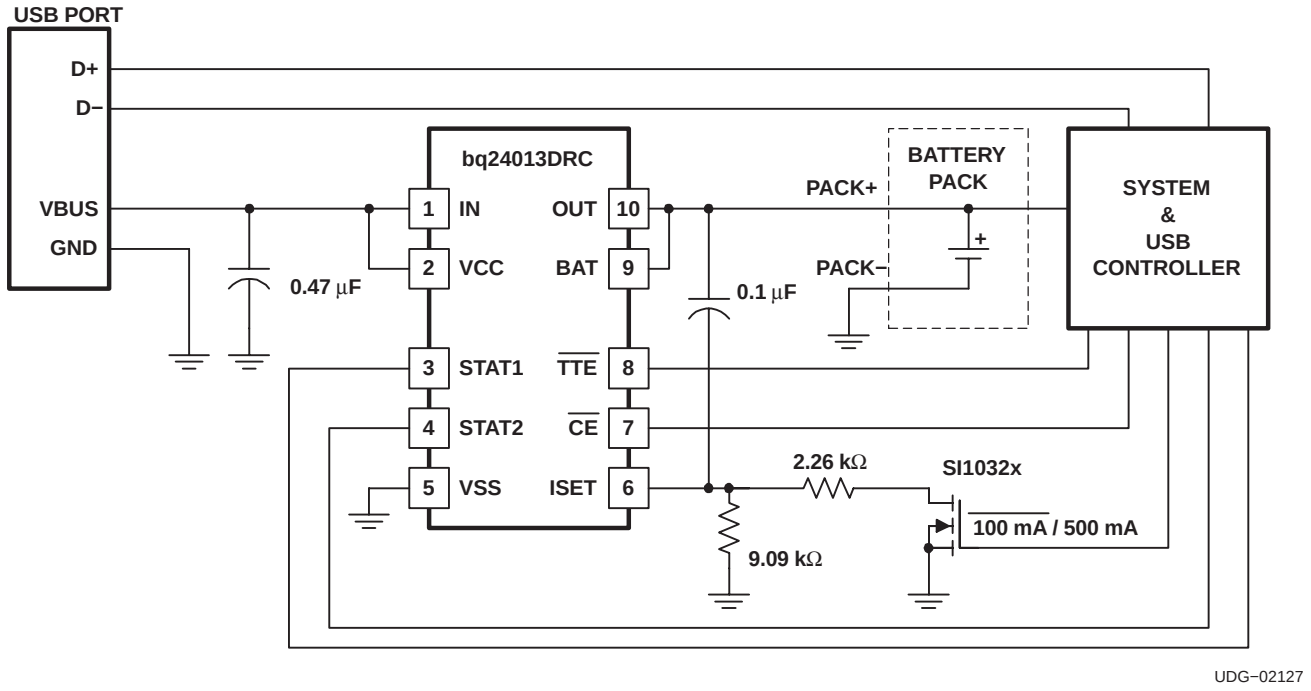


Figure 4. USB Charger Circuit

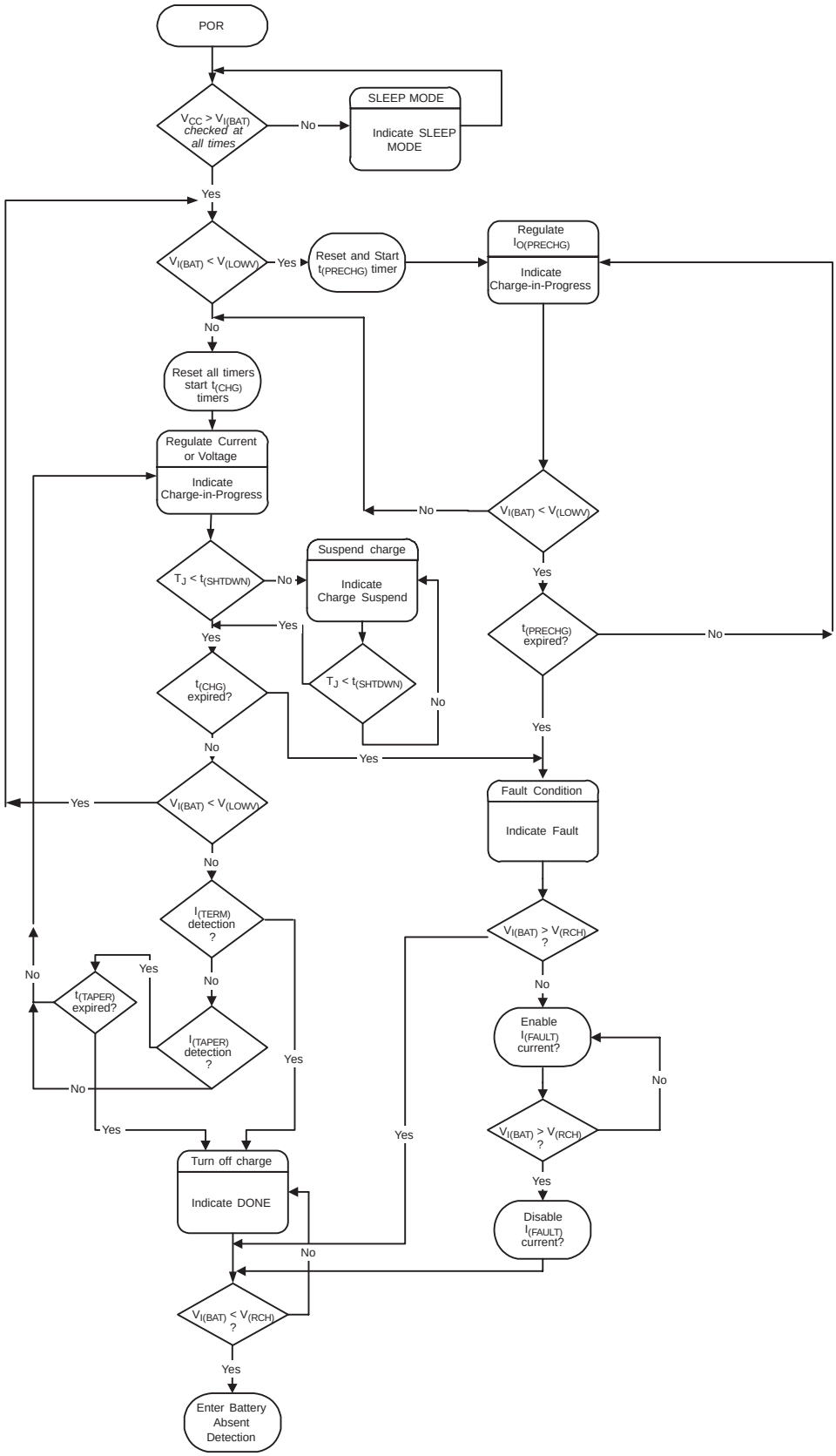


Figure 5. Operational Flow Chart

FUNCTIONAL DESCRIPTION

TEMPERATURE QUALIFICATION

NOTE: The temperature qualifications apply only to versions with temperature sense input (TS) pin option (bq24010 and bq24014).

Versions of the bqTINY with the TS pin option, continuously monitor battery temperature by measuring the voltage between the TS and VSS pins. A negative temperature coefficient thermistor (NTC) and an external voltage divider typically develops this voltage (see Figure 3). The bqTINY compare this voltage against the internal $V_{(TS1)}$ and $V_{(TS2)}$ thresholds to determine if charging is allowed (see Figure 6). The temperature sensing circuit is immune to any fluctuation in V_{CC} since both the external voltage divider and the internal thresholds are ratiometric to V_{CC}.

Once a temperature outside the $V_{(TS1)}$ and $V_{(TS2)}$ thresholds is detected the bqTINY immediately suspend the charge. The bqTINY suspends charge by turning off the powerFET and holding the timer value (i.e. timers are NOT reset). Charge is resumed when the temperature returns to the normal range.

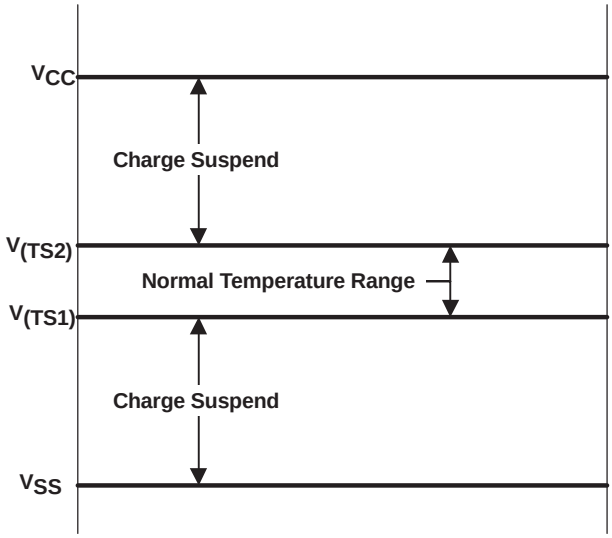


Figure 6. TS Pin Thresholds

The resistor values of R_{T1} and R_{T2} are calculated by equations (1) and (2) (for NTC Thermistors)

$$R_{T1} = \frac{\left(5 \times R_{TH} \times R_{TC}\right)}{\left(3 \times \left(R_{TC} - R_{TH}\right)\right)} \quad (9)$$

$$R_{T2} = \frac{\left(5 \times R_{TH} \times R_{TC}\right)}{\left(2 \times R_{TC}\right) - \left(7 \times R_{TH}\right)} \quad (10)$$

Where R_{TC} is the cold temperature resistance and R_{TH} is the hot temperature resistance of thermistor, as specified by the thermistor manufacturer.

R_{T1} or R_{T2} can be omitted If only one temperature (hot or cold) setting is required. Applying a constant voltage between the V_{TS1} and V_{TS2} thresholds to pin TS disables the temperature-sensing feature.

FUNCTIONAL DESCRIPTION

BATTERY PRE-CONDITIONING

During a charge cycle if the battery voltage is below the $V_{(LOWV)}$ threshold, the bqTINY applies a precharge current, $I_{O(PRECHG)}$, to the battery. This feature revives deeply discharged cells. The resistor connected between the ISET and V_{SS}, R_{SET}, determines the precharge rate. The $V_{(PRECHG)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O\ (PRECHG)} = \frac{V_{(PRECHG)} \times K_{(SET)}}{R_{SET}} \quad (11)$$

The bqTINY activates a safety timer, $t_{(PRECHG)}$, during the conditioning phase. If $V_{(LOWV)}$ threshold is not reached within the timer period, the bqTINY turns off the charger and enunciates FAULT on the STAT1 and STAT2 pins. Refer to *Timer Fault Recovery* section for additional details.

BATTERY CHARGE CURRENT

The bqTINY offers on-chip current regulation with programmable set point. The resistor connected between the ISET and V_{SS}, R_{SET}, determines the charge rate. The $V_{(SET)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{O\ (OUT)} = \frac{V_{(SET)} \times K_{(SET)}}{R_{SET}} \quad (12)$$

BATTERY VOLTAGE REGULATION

Voltage regulation feedback is accomplished through the BAT pin. This input is tied directly and close to the positive side of the battery pack. The bqTINY monitors the battery-pack voltage between the BAT and VSS pins. When the battery voltage rises to $V_{O(REG)}$ threshold, the voltage regulation phase begins and the charging current begins to taper down.

As a safety backup, the bqTINY also monitors the charge time in the charge mode. If termination does not occur within this time period, $t_{(CHG)}$, the bqTINY turns off the charger and enunciates FAULT on the STAT1 and STAT1 pins. Refer to the *Timer Fault Recovery* section for additional details.

CHARGE TAPER DETECTION, TERMINATION AND RECHARGE

The bqTINY monitors the charging current during the voltage regulation phase. Once the taper threshold, $I_{(TAPER)}$, is detected the bqTINY initiates the taper timer, $t_{(TAPER)}$. Charge is terminated after the timer expires. The resistor connected between the ISET and V_{SS}, R_{SET}, determines the taper detection level. The $V_{(TAPER)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{(TAPER)} = \frac{V_{(TAPER)} \times K_{(SET)}}{R_{SET}} \quad (13)$$

The bqTINY resets the taper timer in the event that the charge current returns above the taper threshold, $I_{(TAPER)}$.

In addition to the taper current detection, the bqTINY terminates charge in the event that the charge current falls below the $I_{(TERM)}$ threshold. This feature allows for quick recognition of a battery removal condition or insertion of a fully charged battery. Note that taper timer is not used for $I_{(TERM)}$ detection. The resistor connected between the ISET and V_{SS}, R_{SET}, determines the taper detection level. The $V_{(TERM)}$ and $K_{(SET)}$ parameters are specified in the specifications table.

$$I_{(TERM)} = \frac{V_{(TERM)} \times K_{(SET)}}{R_{SET}} \quad (14)$$

FUNCTIONAL DESCRIPTION

After charge termination, the bqTINY restarts the charge once the voltage on the BAT pin falls below the $V_{(RCH)}$ threshold. This feature keeps the battery at full capacity at all times. Please see *Battery Absent Detection* section for additional details.

SLEEP MODE

The bqTINY enters the low-power sleep mode if the V_{CC} is removed from the circuit ($\overline{PG}$ pin is high impedance). This feature prevents draining the battery during the absence of V_{CC}. The status pins do not function when in sleep mode or when $V_{CC} < V_{POR}$ and default to the OFF state.

CHARGE STATUS OUTPUTS

The open-collector STAT1 and STAT2 outputs indicate various charger operations as shown in the following table. These status pins can be used to drive LEDs or communicate to the host processor. Note that OFF indicates the open-collector transistor is turned off. When $V_{CC} < V_{POR}$ or $V_{CC} < V_{BAT}$ (Sleep Mode − PG OFF) the STAT pins default to their OFF state. Note that this STAT1/STAT2 OFF/OFF state is shared by several operating conditions. Monitoring IN, BAT, $\overline{PG}$ and TS, it is possible to decode the actual fault condition.

Table 2. Status Pins Summary

CHARGE STATE	STAT1	STAT2
Charge-in-progress	ON	OFF
Charge done	OFF(†)	ON
Battery absent Charge suspend (temperature) Timer fault Sleep mode	OFF	OFF

(†) OFF means the open-collector output transistor on the STAT1 or STAT2 pins is in an off state.

$\overline{PG}$ OUTPUT

The open-collector $\overline{PG}$ (power good) indicates when the ac adapter (i.e. V_{CC}) is present. The $\overline{PG}$ bipolar transistor turns ON when a valid V_{CC} is detected. This output is turned off in the sleep mode. The $\overline{PG}$ pin can be used to drive an LED or communicate to the host processor.

$\overline{CE}$ INPUT (CHARGE ENABLE)

The $\overline{CE}$ digital input is used to disable or enable the charge process. A low-level signal on this pin enables the charge and a high-level signal disables the charge. A high-to-low transition on this pin also resets all timers and fault conditions and starts a new charge cycle.

$\overline{TTE}$ INPUT (TIMER AND TERMINATION ENABLE)

The $\overline{TTE}$ digital input is used to disable or enable the fast-charge timer and charge termination. A low-level signal on this pin enables the fast-charge timer and termination and a high-level signal disables this feature. A high-to-low transition on this pin also resets all timers.

THERMAL SHUTDOWN AND PROTECTION

The bqTINY monitors the junction temperature, T_J, of the die and suspends charging if T_J exceeds 155°C. Charging resumes when T_J falls below approximately 130°C.

FUNCTIONAL DESCRIPTION

BATTERY ABSENT DETECTION

For applications with removable battery packs, bqTINY provides a battery absent detection scheme to reliably detect insertion and/or removal of battery packs.

The voltage at the BAT pin is held above the battery recharge threshold, $V_{(RCH)}$, by the charged battery following fast charging. When the voltage at the BAT pin falls to the recharge threshold, either by a load on the battery or due to battery removal, the bqTINY begins a battery absent detection test. This test involves enabling a detection current, $I_{(DETECT)}$, for a period of $t_{(DETECT)}$ and checking to see if the battery voltage is below the pre-charge threshold, $V_{(LOWV)}$. Following this, the precharge current, $I_{O(PRECHG)}$ is applied for a period of $t_{(DETECT)}$ and the battery voltage checked again to be above the recharge threshold. The purpose is to attempt to *close* a battery pack with an open protector, if one is connected to the bqTINY. Passing both of the discharge and charging tests indicates a battery absent fault at the STAT pins. Failure of either test starts a new charge cycle. For the absent battery condition the voltage on the BAT pin rises and falls between the $V_{(LOWV)}$ and $V_{O(REG)}$ thresholds indefinitely. See Figure 7.

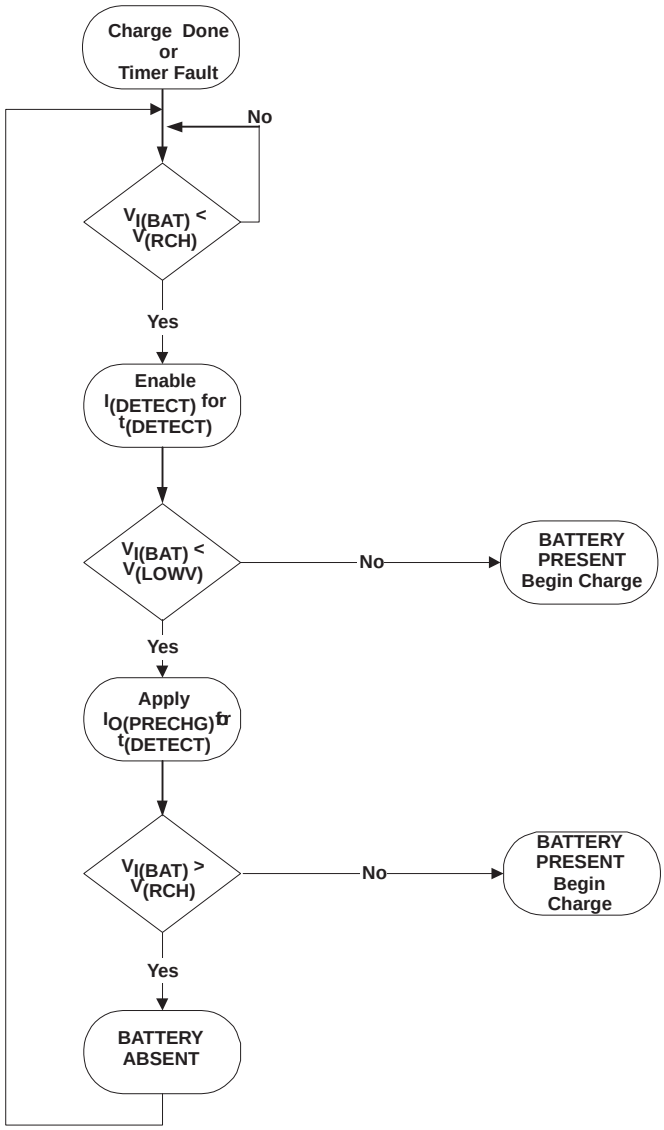


Figure 7. Battery Absent Detection

FUNCTIONAL DESCRIPTION

TIMER FAULT RECOVERY

As shown in Figure 5, bqTINY provides a recovery method to deal with timer fault conditions. The following conditions summarize this method.

Condition #1: Charge voltage above recharge threshold ($V_{(RCH)}$) and timeout fault occurs

Recovery method: bqTINY waits for the battery voltage to fall below the recharge threshold. This could happen as a result of a load on the battery, self-discharge or battery removal. Once the battery falls below the recharge threshold, the bqTINY clears the fault and enters the battery absent detection routine. A POR or $\overline{CE}$ toggle also clears the fault.

Condition #2: Charge voltage below recharge threshold ($V_{(RCH)}$) and timeout fault occurs

Recovery method: Under this scenario, the bqTINY applies the $I_{(FAULT)}$ current. This small current is used to detect a battery removal condition and remains on as long as the battery voltage stays below the recharge threshold. If the battery voltage goes above the recharge threshold, then the bqTINY disables the $I_{(FAULT)}$ current and executes the recovery method described for condition #1. Once the battery falls below the recharge threshold, the bqTINY clears the fault and enters the battery absent detection routine. A POR or $\overline{CE}$ toggle also clears the fault.

APPLICATION INFORMATION

SELECTING INPUT CAPACITOR

In most applications, all that is needed is a high-frequency decoupling capacitor. A 0.47-µF ceramic, placed in close proximity to V_{CC} and V_{SS} pins, works well. The bqTINY is designed to work with both regulated and unregulated external dc supplies. If a non-regulated supply is chosen, the supply unit should have enough capacitance to hold up the supply voltage to the minimum required input voltage at maximum load. If not, more capacitance has to be added to the input of the charger.

SELECTING OUTPUT CAPACITOR

The bqTINY requires only a small output capacitor for loop stability. A 0.1-µF ceramic capacitor placed between the BAT and ISET pins is typically sufficient for embedded applications (i.e. non-removable battery packs). For application with removable battery packs a 1-µF ceramic capacitor ensure proper operation of the battery detection circuitry. Note that the output capacitor can also be placed between BAT and VSS pins.

THERMAL CONSIDERATIONS

The bqTINY is packaged in a thermally enhanced MLP (also referred to as QFN) package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled, *QFN/SON PCB Attachment Application Note* (TI Literature No. SLUA271).

The most common measure of package thermal performance is thermal impedance (θ_{JA}) measured (or modeled) from the device junction to the air surrounding the package surface (ambient). The mathematical expression for θ_{JA} is:

$$\theta_{JA} = \frac{T_J - T_A}{P} \tag{15}$$

Where:

- T_J = device junction temperature
- T_A = ambient temperature
- P = device power dissipation

Factors that can greatly influence the measurement and calculation of θ_{JA} include:

- whether or not the device is board mounted
- trace size, composition, thickness, and geometry
- orientation of the device (horizontal or vertical)
- volume of the ambient air surrounding the device under test and airflow
- whether other surfaces are in close proximity to the device being tested

The device power dissipation, P, is a function of the charge rate and the voltage drop across the internal PowerFET. It can be calculated from the following equation:

$$P = V_{IN} - V_{I(BAT)} \times I_{O(OUT)} \tag{16}$$

Due to the charge profile of Li-xx batteries, the maximum power dissipation is typically seen at the beginning of the charge cycle when the battery voltage is at it's lowest. See Figure 2.

APPLICATION INFORMATION

PCB LAYOUT CONSIDERATIONS

It is important to pay special attention to the PCB layout. The following provides some guidelines:

- To obtain optimal performance, the decoupling capacitor from V_{CC} to V_{SS} and the output filter capacitors from BAT to ISET should be placed as close as possible to the bqTINY, with short trace runs to both signal and V_{SS} pins.
- All low-current V_{SS} connections should be kept separate from the high-current charge or discharge paths from the battery. Use a single-point ground technique incorporating both the small signal ground path and the power ground path.
- The BAT pin is the voltage feedback to the device and should be connected with its trace as close to the battery pack as possible.
- The high current charge paths into IN and from the OUT pins must be sized appropriately for the maximum charge current in order to avoid voltage drops in these traces.
- The bqTINY is packaged in a thermally enhanced MLP package. The package includes a thermal pad to provide an effective thermal contact between the device and the printed circuit board (PCB). Full PCB design guidelines for this package are provided in the application note entitled: *QFN/SON PCB Attachment Application Note* (TI Literature No. SLUA271).
- There is an internal electrical connection between the exposed thermal pad and V_{SS} pin of the device. The exposed thermal pad must be connected to the same potential as the V_{SS} pin on the printed circuit board. Do not use the thermal pad as the primary ground input for the device. V_{SS} pin must be connected to ground at all times.

THERMAL PAD MECHANICAL DATA

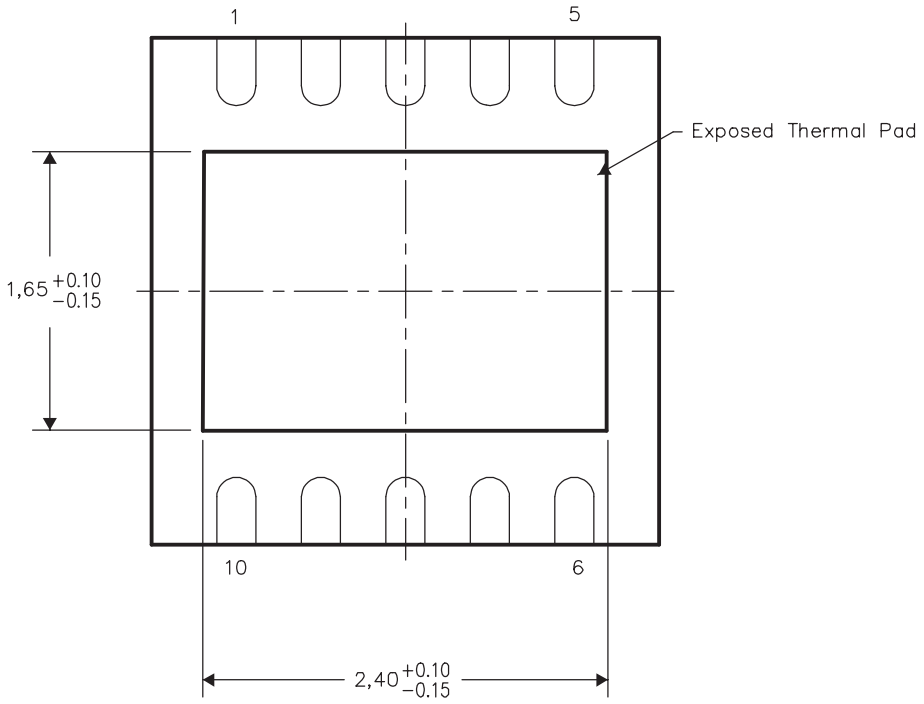
DRC (S–PDSO–N10)

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB), the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to a ground plane or special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No–Lead (QFN) package and its advantages, refer to Application Report, Quad Flatpack No–Lead Logic Packages, Texas Instruments Literature No. SCBA017. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

NOTE: All linear dimensions are in millimeters

Exposed Thermal Pad Dimensions

4206565–5/A 12/04

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
BQ24010DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24010DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24012DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24012DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24013DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24013DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24014DRCR	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
BQ24014DRCRG4	ACTIVE	SON	DRC	10	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

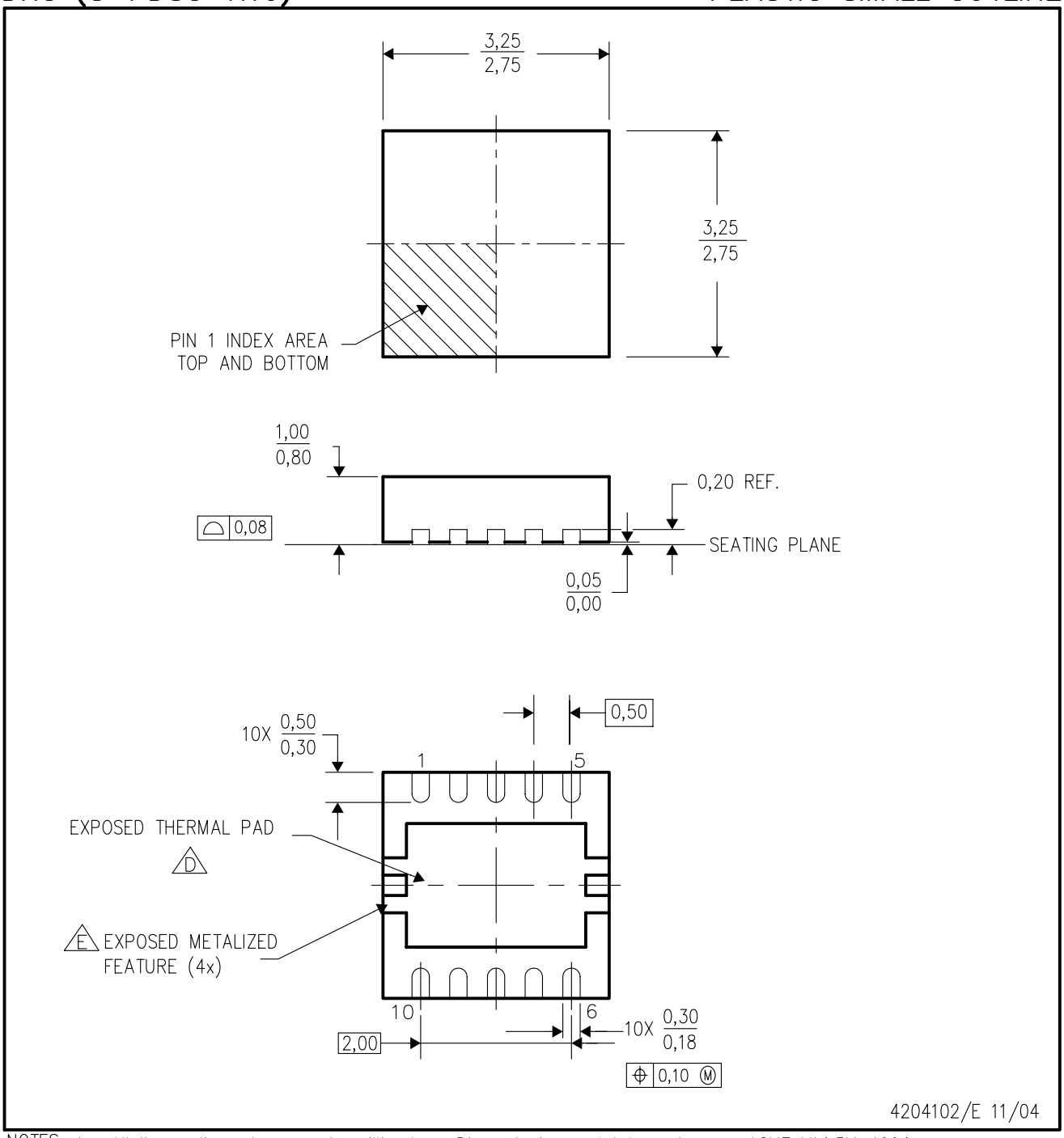
(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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DRC (S–PDSO–N10) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance. See the Product Data Sheet for details regarding the exposed thermal pad dimensions.
E. Metalized features are supplier options and may not be on the package.

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