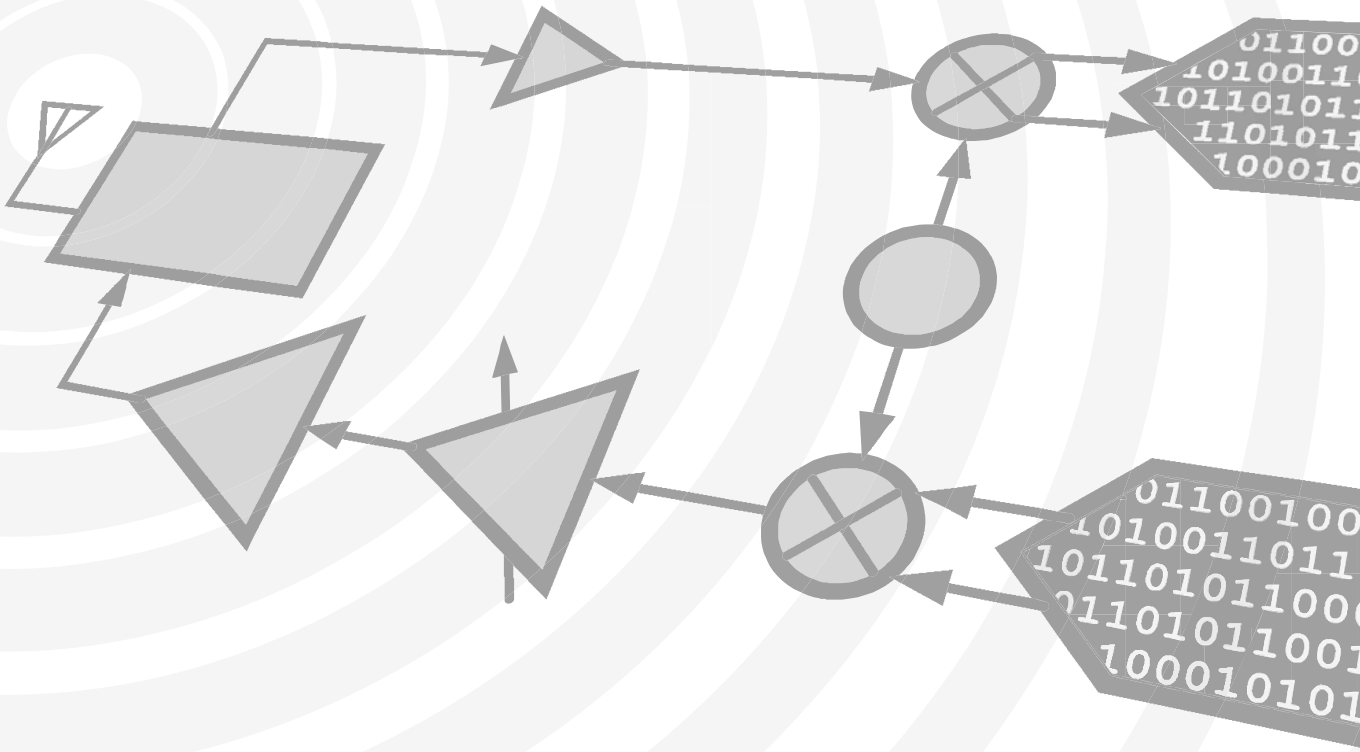
ANALOG DEVICES

Hittite MICROWAVE PRODUCTS FROM ANALOG DEVICES

Analog Devices Welcomes Hittite Microwave Corporation

NO CONTENT ON THE ATTACHED DOCUMENT HAS CHANGED



www.analog.com

www.hittite.com

THIS PAGE INTENTIONALLY LEFT BLANK

HMC1021LP4E

RMS POWER DETECTOR & ENVELOPE TRACKER, DC - 3.9 GHz

Typical Applications

The HMC1021LP4E is ideal for:

- Log –> Root-Mean-Square (RMS) Conversion
- Tx/Rx Signal Strength Indication (TSSI/RSSI)
- RF Power Amplifier Efficiency Control
- Receiver Automatic Gain Control
- Transmitter Power Control
- Envelope Tracking
- PA Linearization

Features

Broadband Single-Ended RF Input

RMS Detector with ±1 dB Detection Accuracy to 3.9 GHz

Input Dynamic Range: -62 dBm to +8 dBm

±1 dB Envelope Detection Accuracy over 20 dB Input Range

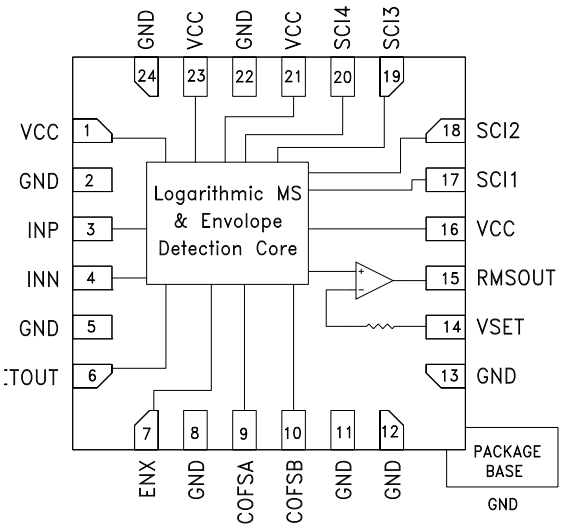
Envelope Detection Bandwidth > 150MHz

Digitally Programmable Integration Bandwidth

Power-Down Mode

24 Lead 4x4mm SMT Package: 16mm²

Functional Diagram



General Descriptions

The HMC1021LP4E is an RMS power detector with an integrated high bandwidth envelope detector. The RMS output is a temperature compensated, monotonic, linear-in-dB representation of real RF signal power, measured over an input sensing range of 70 dB. The envelope detector provides an accurate voltage output which is linearly proportional to the envelope amplitude of the RF input signal for modulation bandwidths up to 150 MHz. The high bandwidth envelope detection of the HMC1021LP4E makes it ideal for detecting broadband and high crest factor RF signals commonly used in CDMA2000, WCDMA, and LTE systems. Additionally, the instantaneous envelope output can be used to create fast, excessive RF power protection, PA linearization, and efficiency enhancing envelope-tracking PA implementations.

The HMC1021LP4E's RMS detector integration bandwidth is digitally programmable via input pins SCI1-4 over a range of more than 4 decades. This allows the user to dynamically set the operation bandwidth and also permits the detection of different types of modulations on the same platform.

The HMC1021LP4E features an internal op-amp at the RMS output stage, which accommodates slope and intercept adjustments and supports a wide range of applications.

Electrical Specifications I

T_A = +25 °C, Vcc = 5V, Sci4 = Sci1 = 0V, Sci3 = Sci2 = 5V, Unless Otherwise Noted

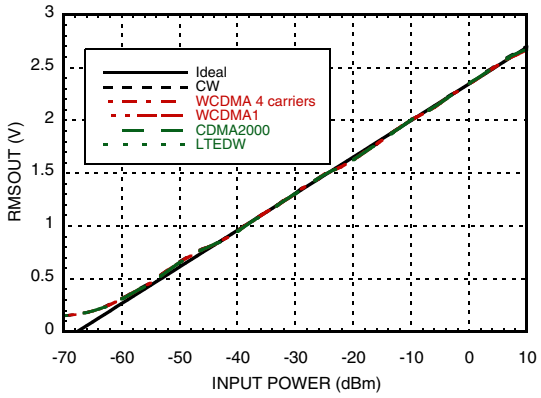
Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Dynamic Range (±1dB Error) [1]								
Input Frequency	100	900	1900	2200	2700	3500	3900	MHz
RMSOUT Output	71	71	70	69	68	64	60	dB
ETOUT Output	18	19	20	19	20	19	19	dB
Deviation vs Temperature: (Over full temperature range -40 °C to 85 °C). Deviation is measured from reference, which is the same WCDMA input at 25 °C.						1		dB
[1] With WCDMA 4 Carrier (TM1-64 DPCH)								

Electrical Specifications II

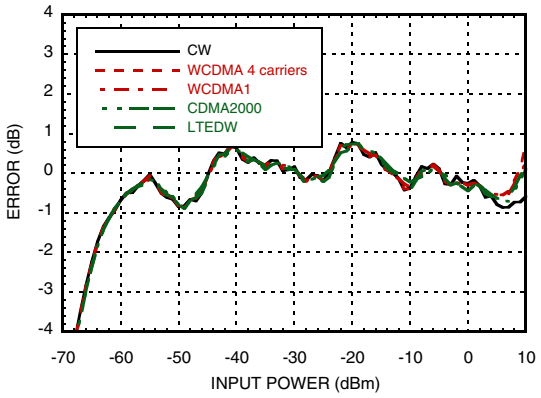
T_A = +25 °C, Vcc = 5V, Sci4 = Sci1 = 0V, Sci3 = Sci2 = 5V, Unless Otherwise Noted

Parameter	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Typ.	Units
Input Frequency	100	900	1900	2200	2700	3500	3900	MHz
Modulation Deviation (Output deviation from reference, which is measured with CW input at equivalent input signal power)								
WCDMA 4 Carrier (TM1-64 DPCH) at +25 °C	0.1	0.1	0.1	0.1	0.1	0.1	0.1	dB
WCDMA 4 Carrier (TM1-64 DPCH) at +85 °C	0.1	0.1	0.1	0.1	0.1	0.1	0.1	dB
WCDMA 4 Carrier (TM1-64 DPCH) at -40 °C	0.1	0.1	0.1	0.1	0.1	0.1	0.1	dB
RMSOUT Logarithmic Slope and Intercept [1]								
Logarithmic Slope	33.6	33.7	34.1	34.5	35.4	37.8	39.7	mV/dB
Logarithmic Intercept	-69.4	-69.2	-68.4	-67.8	-66.2	-62.2	-59.3	dBm
Max. Input Power at ±1dB Error	8	8	8	8	8	7	5	dBm
Min. Input Power at ±1dB Error	-63	-63	-62	-61	-60	-57	-55	dBm
ETOUT Linear Slope and Intercept								
Linear Slope	16.6	16.0	14.8	14.5	13.6	12.3	11.3	V/V
Linear Intercept	-56.0	-58.2	-63.0	-64.0	-68.0	-75.3	-81.8	mV
Max. Input Power at ±1dB Error	-14	-13	-11	-11	-10	-10	-9	dBm
Min. Input Power at ±1dB Error	-32	-32	-31	-30	-30	-29	-28	dBm
[1] With WCDMA 4 Carrier (TM1-64 DPCH)								

RMSOUT vs. Pin with Different Modulations @ 1900 MHz [1]



RMSOUT Error vs. Pin with Different Modulations @ 1900 MHz [1]



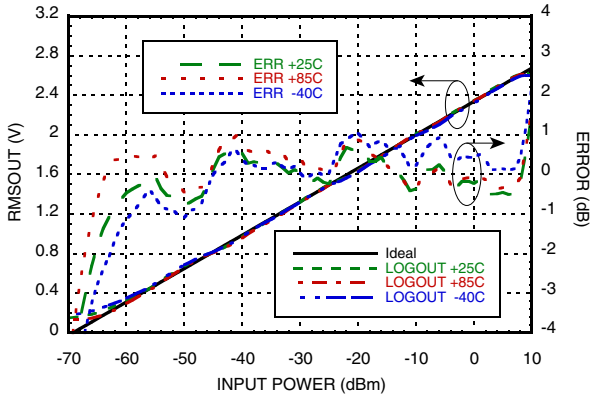
[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

Electrical Specifications III

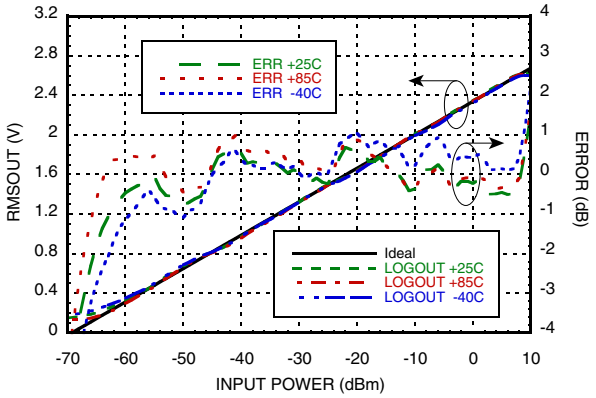
T_A = +25 °C, Vcc = 5V, Sci4 = Sci1 = 0V, Sci3 = Sci2 = 5V, Unless Otherwise Noted

Parameter	Conditions	Min	Typ.	Max	Units
Single-Ended Input Configuration					
Input Network Return Loss	up to 3.9 GHz		> 15		dB
Input Resistance between INP and INN	Between pins 3 and 4		100		Ω
Input Voltage Range	AC Coupled Peak Voltage at INP_			0.85	V
RMSOUT Output					
Output Voltage Range			0.13 to 2.7		V
Source/Sink Current Compliance	RMSOUT held at VCC/2		8 / -0.55		mA
Output Slew Rate (rise / fall)	Sci4=Sci3=Sci2=Sci1=0V, Cofs=1nF		24 / 1.9		10^6 V/s
ETOUT Output					
Modulation Bandwidth			150		MHz
Output Voltage Range			1.2 to 2.2		V
Source/Sink Current Compliance			8 / -3.7		mA
Output Slew Rate (rise / fall)			28 / 27		10^6 V/s
VSET Input (Negative Feedback Terminal)					
Input Voltage Range	For control applications with nominal slope/intercept settings		0.13 to 2.7		V
Input Resistance			5		MΩ
SCI1-4 Inputs, ENX Logic Input (Power Down Control)					
Input High Voltage		0.7xVCC			V
Input Low Voltage				0.3xVCC	V
Input High Current				1	µA
Input Low Current				1	µA
Input Capacitance			0.5		pf
Power Supply					
Supply Voltage		4.5	5	5.5	V
Supply Current with no input power			75		mA
Supply Current with -20 dBm			78		mA
Standby Mode Supply Current			5		mA

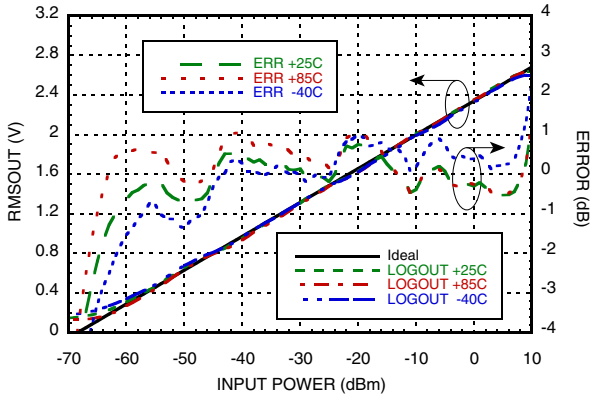
RMSOUT & Error vs. Pin @ 100 MHz [1][2]



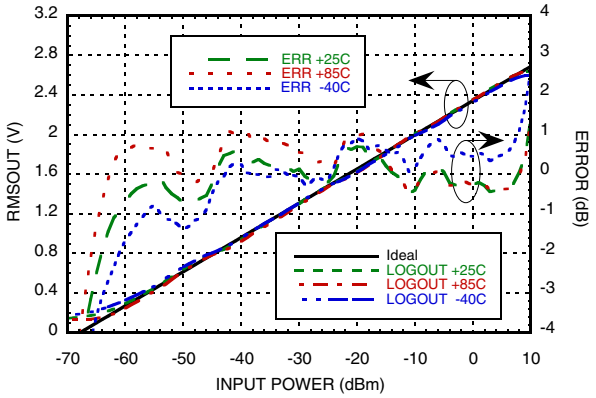
RMSOUT & Error vs. Pin @ 900 MHz [1][2]



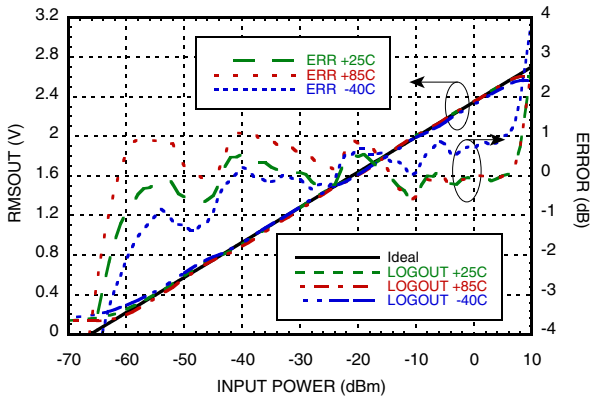
RMSOUT & Error vs. Pin @ 1900 MHz [1][2]



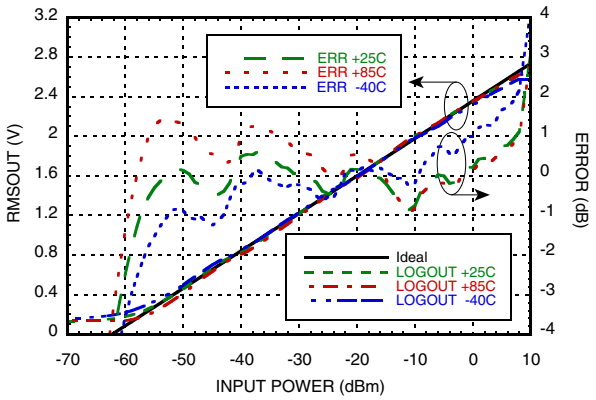
RMSOUT & Error vs. Pin @ 2200 MHz [1][2]



RMSOUT & Error vs. Pin @ 2700 MHz [1][2]



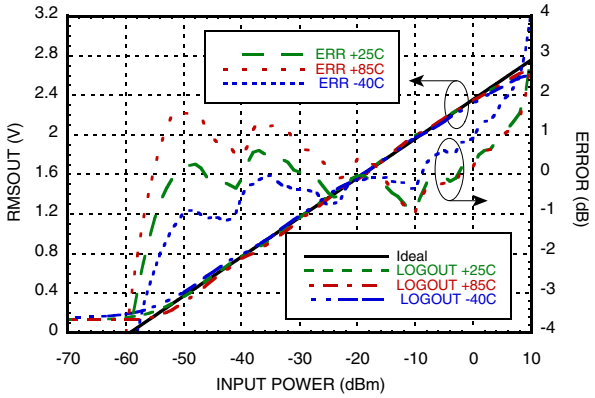
RMSOUT & Error vs. Pin @ 3500 MHz [1][2]



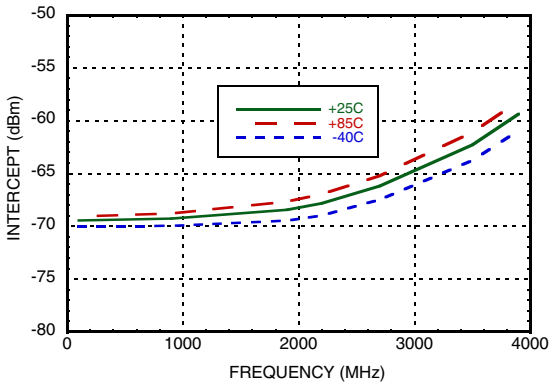
[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

[2] WCDMA 4 carriers input waveform

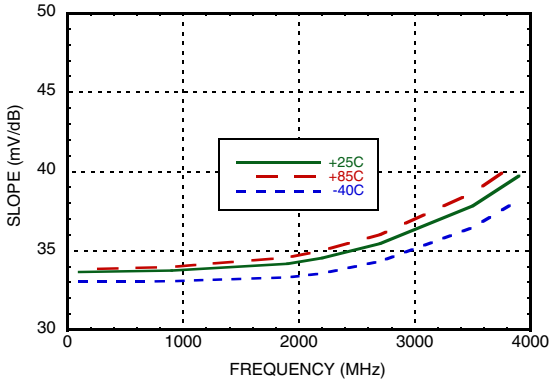
RMSOUT & Error vs. Pin @ 3900 MHz [1][2]



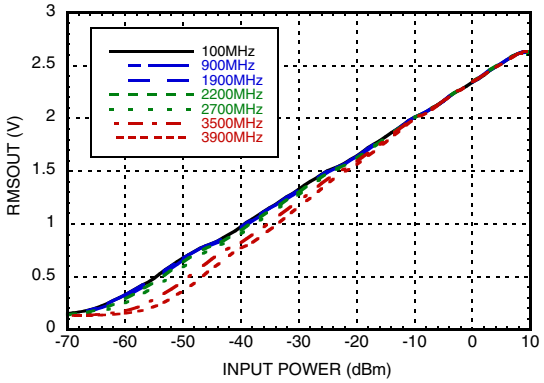
RMSOUT Intercept vs. Frequency [1][2]



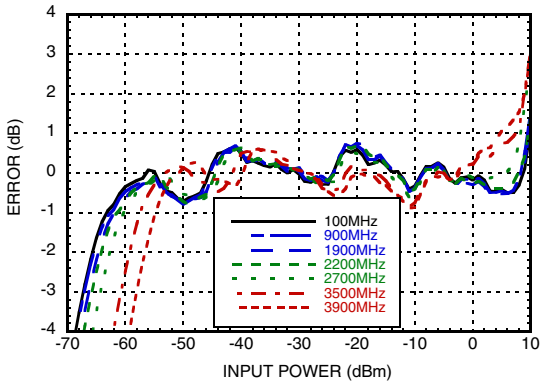
RMSOUT Slope vs. Frequency [1][2]



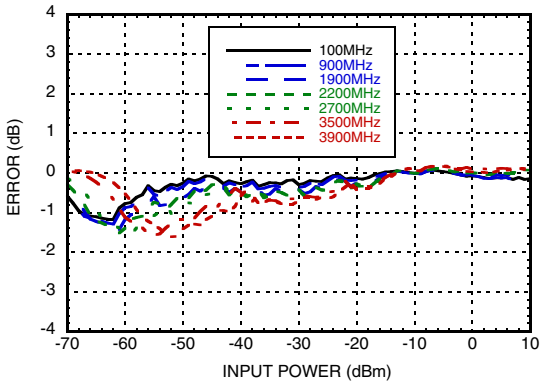
RMSOUT vs. Pin with WCDMA 4 Carrier @ +25 °C [1]



RMSOUT Error vs. Pin with WCDMA 4 Carrier @ +25 °C [1]



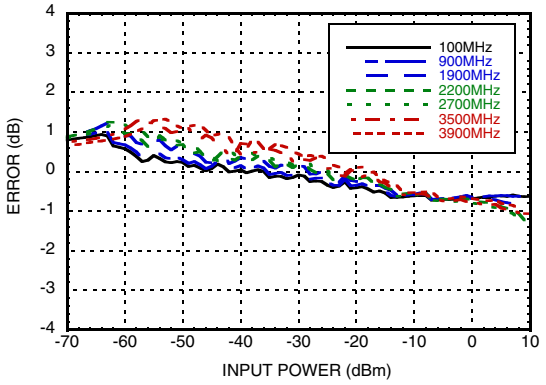
RMSOUT Error vs. Pin with WCDMA 4 Carrier @ +85 °C wrt +25 °C Response [1]



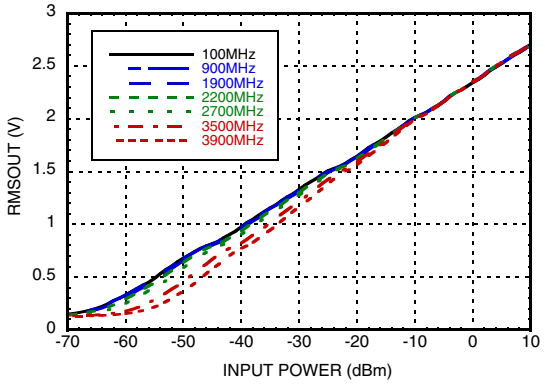
[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

[2] WCDMA 4 carriers input waveform

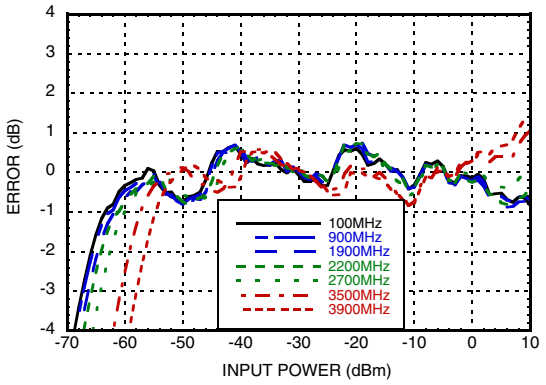
RMSOUT Error vs. Pin with WCDMA 4 Carrier @ -40 °C wrt +25 °C Response [1]



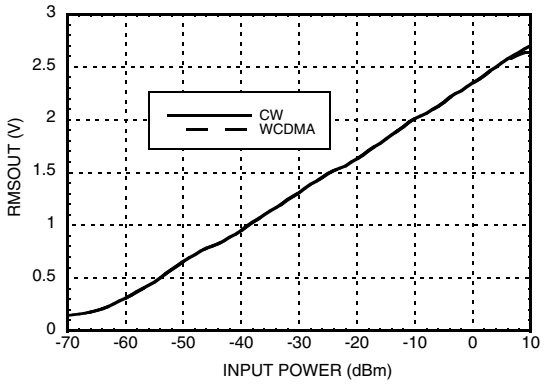
RMSOUT vs. Pin with CW @ +25 °C [1]



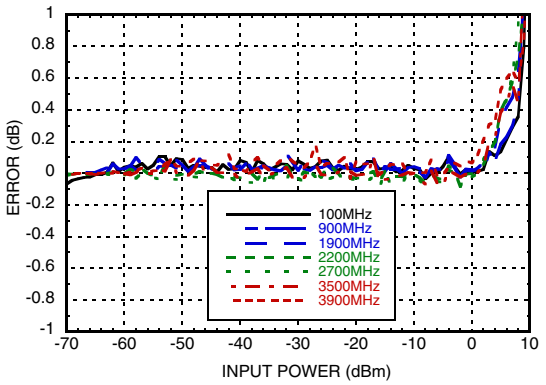
RMSOUT Error vs. Pin with CW @ +25 °C [1]



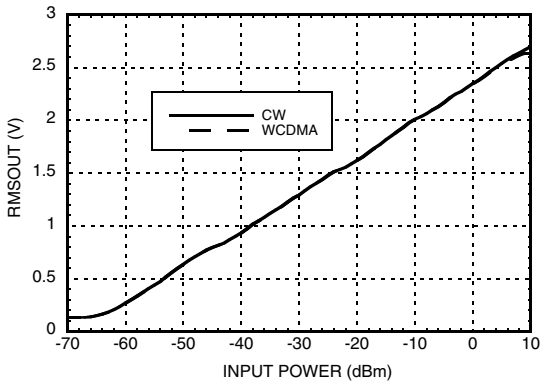
RMSOUT vs. Pin w/ CW & WCDMA 4 Carrier @ 1900 MHz & +25 °C [1]



Reading Error for WCDMA 4 Carrier wrt CW Response @ +25 °C [1]

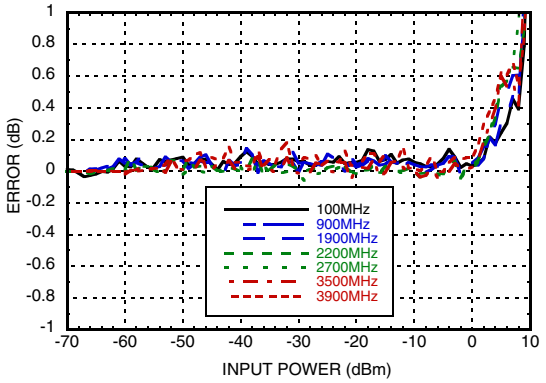


RMSOUT vs. Pin w/ CW & WCDMA 4 Carrier @ 1900 MHz & +85 °C [1]

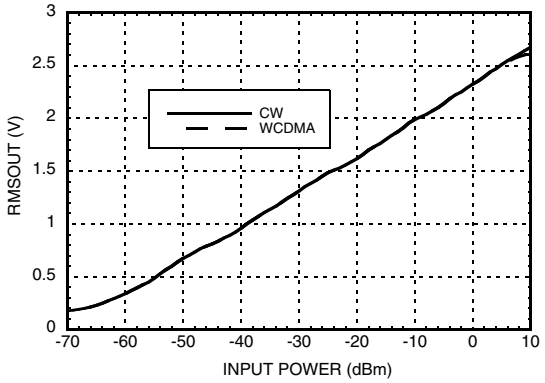


[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

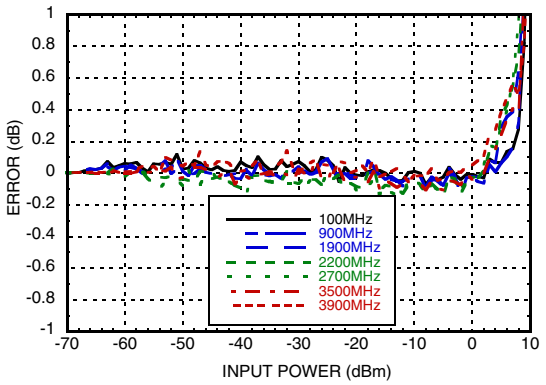
Reading Error for WCDMA 4 Carrier wrt CW Response @ +85 °C [1]



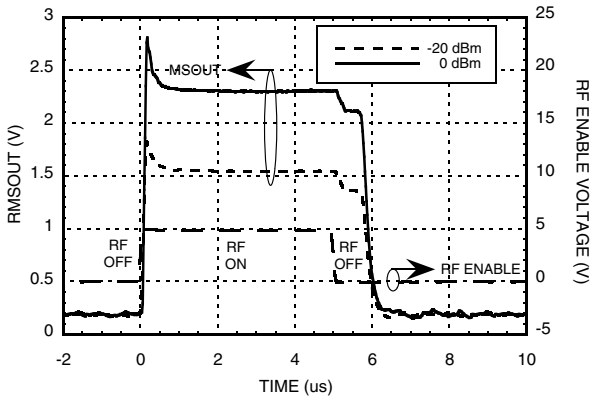
RMSOUT vs. Pin w/ CW & WCDMA 4 Carrier @ 1900 MHz & -40 °C [1]



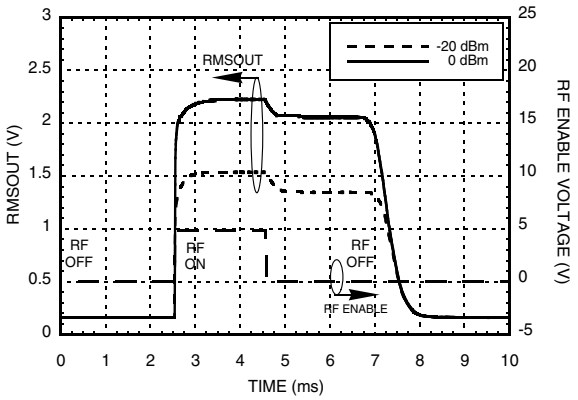
Reading Error for WCDMA 4 Carrier wrt CW Response @ -40 °C [1]



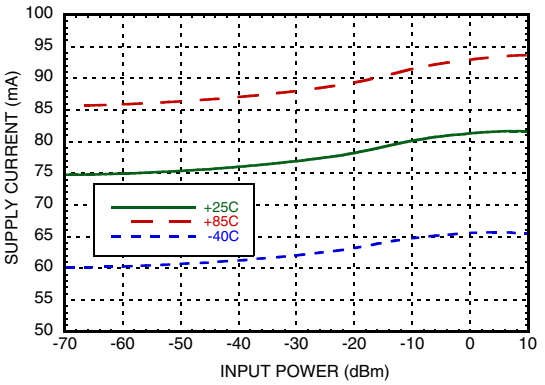
RMSOUT Output Response with SCI = 0000 @ 1900 MHz



RMSOUT Output Response with SCI = 1100 @ 1900 MHz

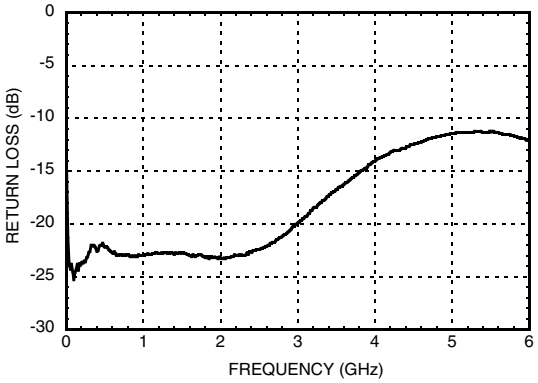


Typical Supply Current vs. Pin, Vcc = 5V

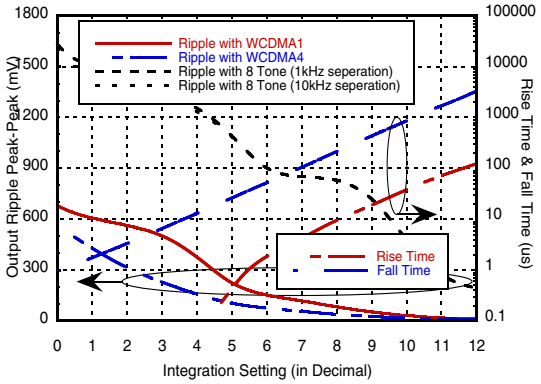


[1] Data was taken at Sci4=Sci1=0V, Sci3=Sci2=5V, shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100

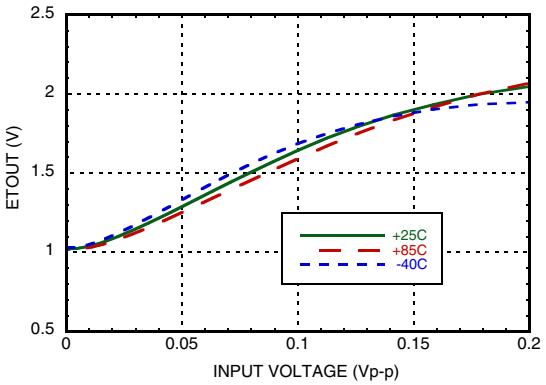
Input Return Loss vs. Frequency



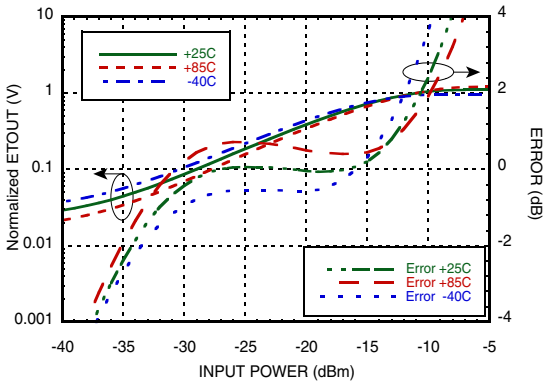
Output Ripple & Rise/Fall Time vs. Integration Setting [Sci4,Sci3,Sci2,Sci1] in Decimal



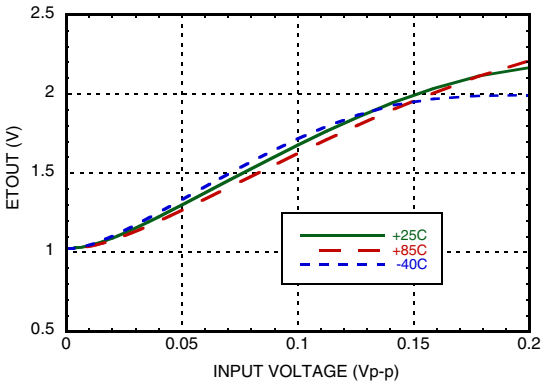
ETOUT vs. Pin with CW @ 900 MHz



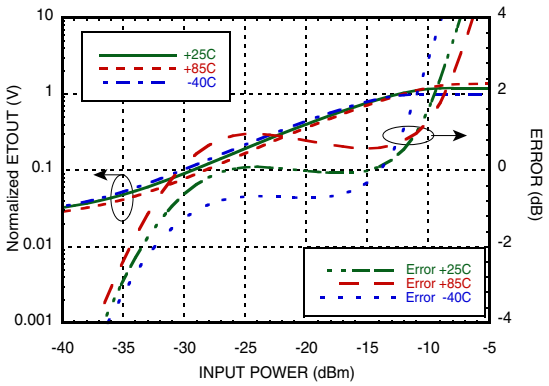
ETOUT & ETOUT Error vs. Pin with CW @ 900 MHz



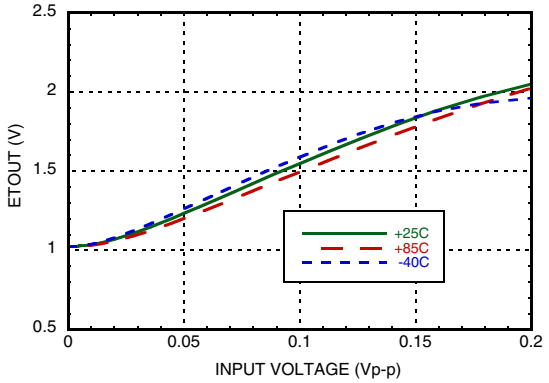
ETOUT vs. Pin with CW @ 1900 MHz



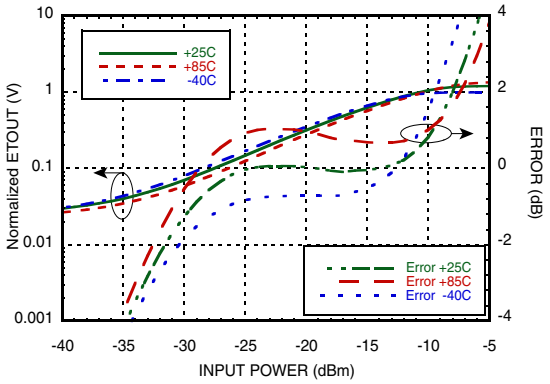
ETOUT & ETOUT Error vs. Pin with CW @ 1900 MHz



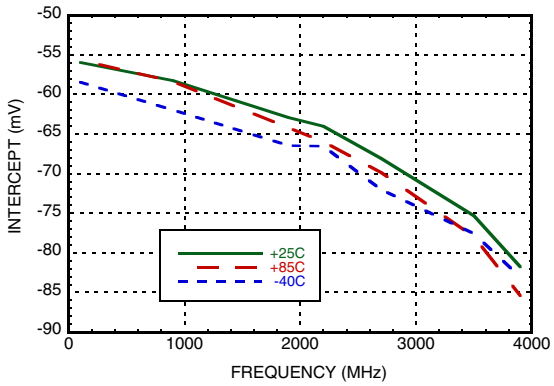
ETOUT vs. Pin with CW @ 3500 MHz



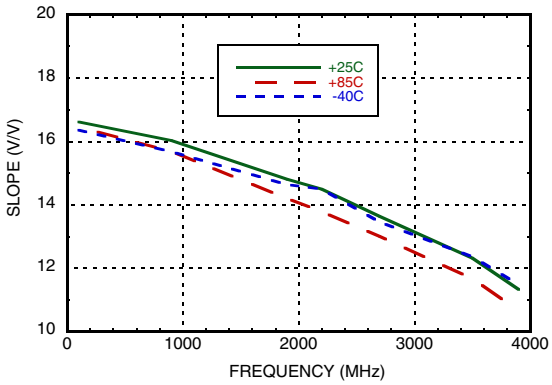
ETOUT & ETOUT Error vs. Pin with CW @ 3500 MHz



ETOUT Intercept vs. Frequency with CW



ETOUT Slope vs. Frequency with CW

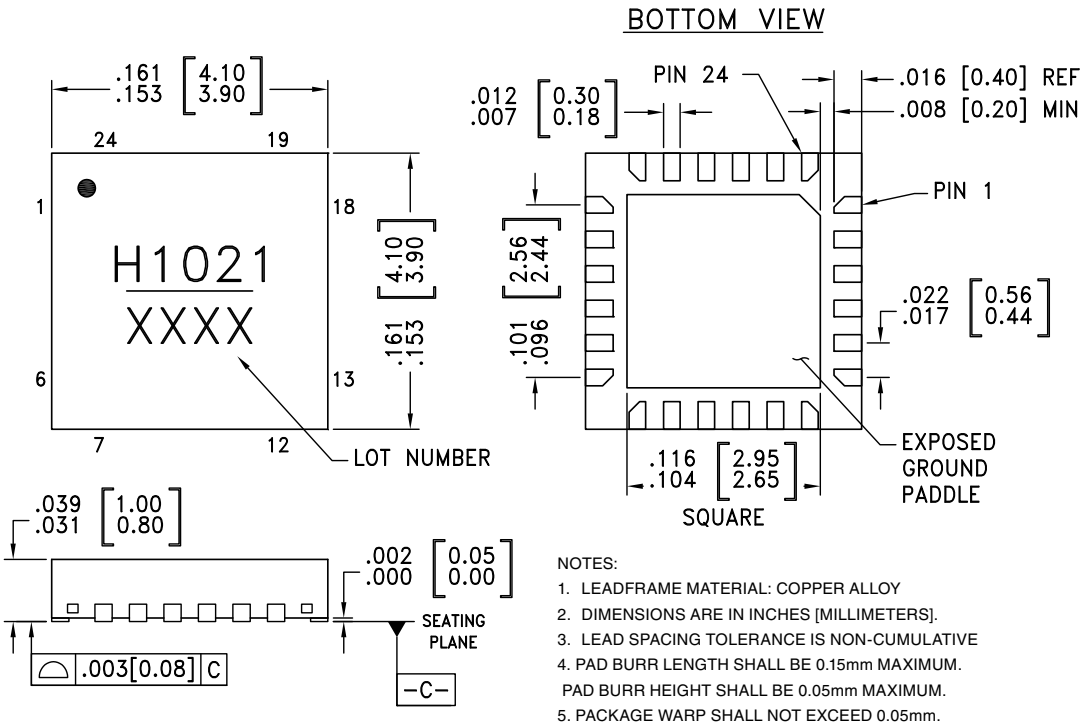


Absolute Maximum Ratings

Power Supply Voltage (Vcc)	5.6V
RF Input Power	10 dBm
Input Voltage	VCC ± 0.6V
Junction Temperature	125 °C
Continuous Pdiss (T = 85°C) (Derate 32.45 mW/°C above 85°C)	1.39 W
Thermal Resistance (R_{th}) (junction to ground paddle)	28.68 °C/W
Storage Temperature	-65 to +150 °C
Operating Temperature	-40 to +85 °C
ESD Sensitivity (HBM)	Class 1B

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Outline Drawing



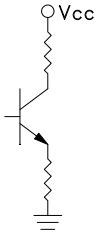
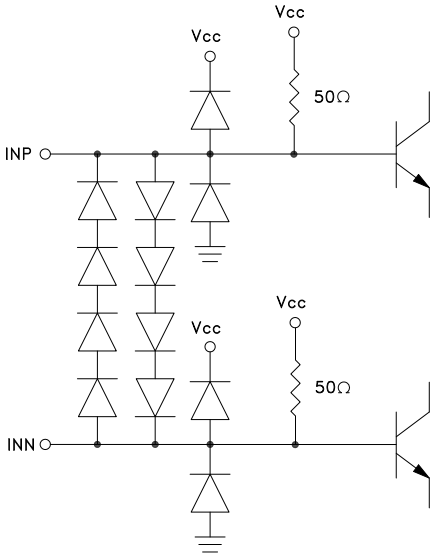
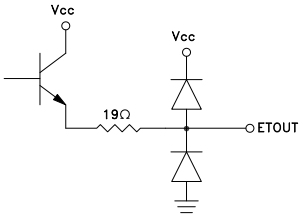
NOTES:
1. LEADFRAME MATERIAL: COPPER ALLOY
2. DIMENSIONS ARE IN INCHES [MILLIMETERS].
3. LEAD SPACING TOLERANCE IS NON-CUMULATIVE
4. PAD BURR LENGTH SHALL BE 0.15mm MAXIMUM. PAD BURR HEIGHT SHALL BE 0.05mm MAXIMUM.
5. PACKAGE WARP SHALL NOT EXCEED 0.05mm.
6. ALL GROUND LEADS AND GROUND PADDLE MUST BE SOLDERED TO PCB RF GROUND.
7. REFER TO HMC APPLICATION NOTE FOR SUGGESTED PCB LAND PATTERN.

Package Information

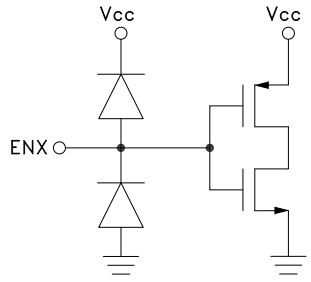
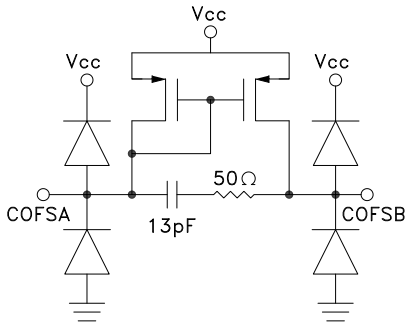
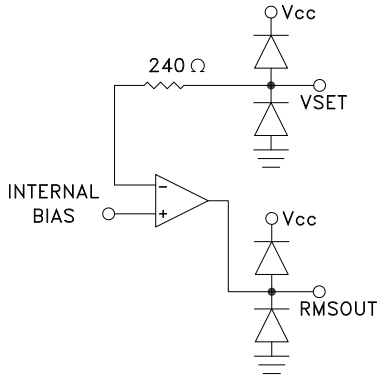
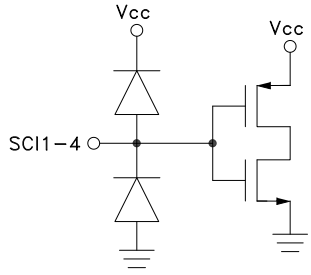
Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [1]
HMC1021LP4E	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL1 [2]	H1021 XXXX

[1] 4-Digit lot number XXXX
[2] Max peak reflow temperature of 260 °C

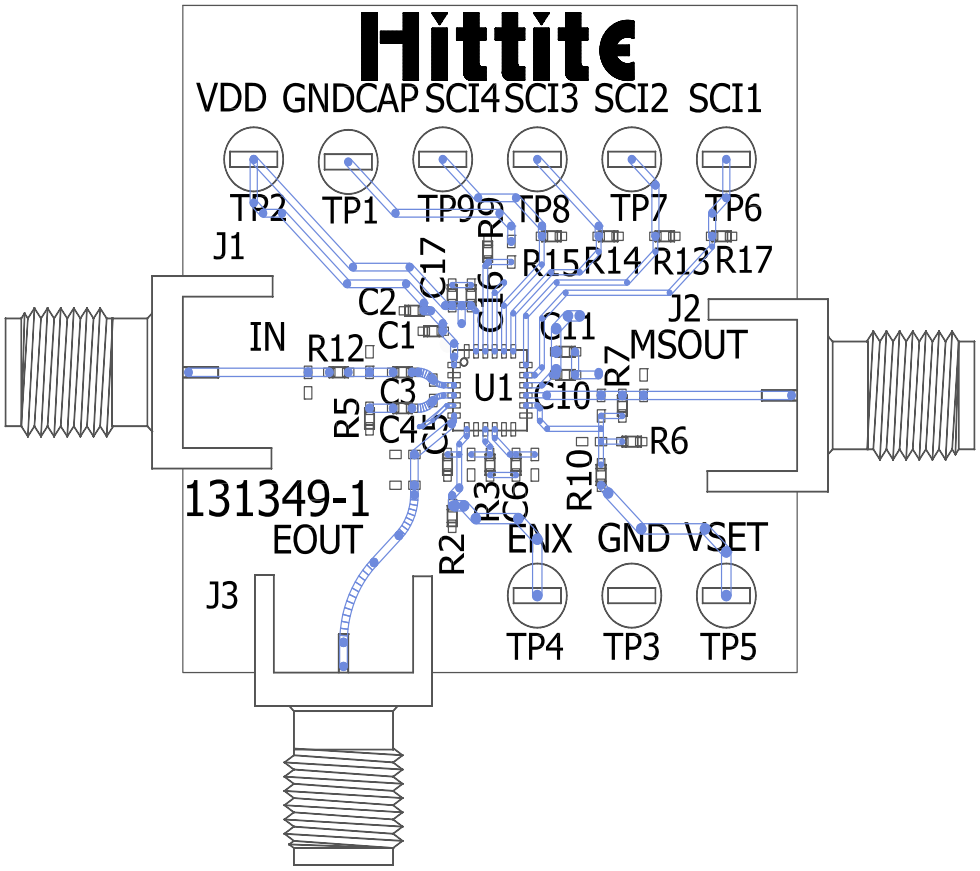
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 16, 21, 23	Vcc	Bias Supply. Connect supply voltage to these pins with appropriate filtering.	
2, 5, 8, 11, 12, 13, 22, 24	GND	Package bottom has an exposed metal paddle that must be connected to RF/DC ground.	
3 ,4	INP, INN	RF input pins	
6	ETOUT	Linear output that provides an indication of envelope of the input signal.	

Pin Descriptions (Continued)

Pin Number	Function	Description	Interface Schematic
7	ENX	Disable pin. Connect to GND for normal operation. Applying voltage V>0.8xVcc will initiate power saving mode.	
9, 10	COFSA, COFSB	Input high pass filter capacitor. Connect a capacitor between COFSA and COFSB to determine 3 dB point of input signal high-pass filter.	
14	VSET	Set input point for controller mode.	
15	RMSOUT	Logarithmic output that provides an indication of mean square input power.	
17, 18, 19, 20	SCI1, SCI2, SCI3, SCI4	Digital input pins that control the internal integration time constant for mean square calculation. SCI4 is the most significant bit. Set V>0.2xVcc to disable. Shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100 (1101, 1110 and 1111 SCI settings are forbidden states). Each step changes the integration time by 1 octave.	

Evaluation PCB



List of Materials for Evaluation PCB 131352 [1]

Item	Description
J1, J2	SMA Connector
TP1 - TP9	DC Pin
C1, C10, C16	100 pF Capacitor, 0402 Pkg.
C2, C5, C11, C17	100 nF Capacitor, 0402 Pkg.
C3, C4, C6	1000 pF Capacitor, 0402 Pkg.
R2, R13 - R15, R17	10K Ohm Resistor, 0402 Pkg.
R3, R9, R10, R12	0 Ohm Resistor, 0402 Pkg.
R5	49.9 Ohm Resistor, 0402 Pkg.
R6, R7	4.7K Ohm Resistor, 0402 Pkg.
U1	HMC1021LP4E RMS Power Detector
PCB [2]	131349-1 Evaluation PCB

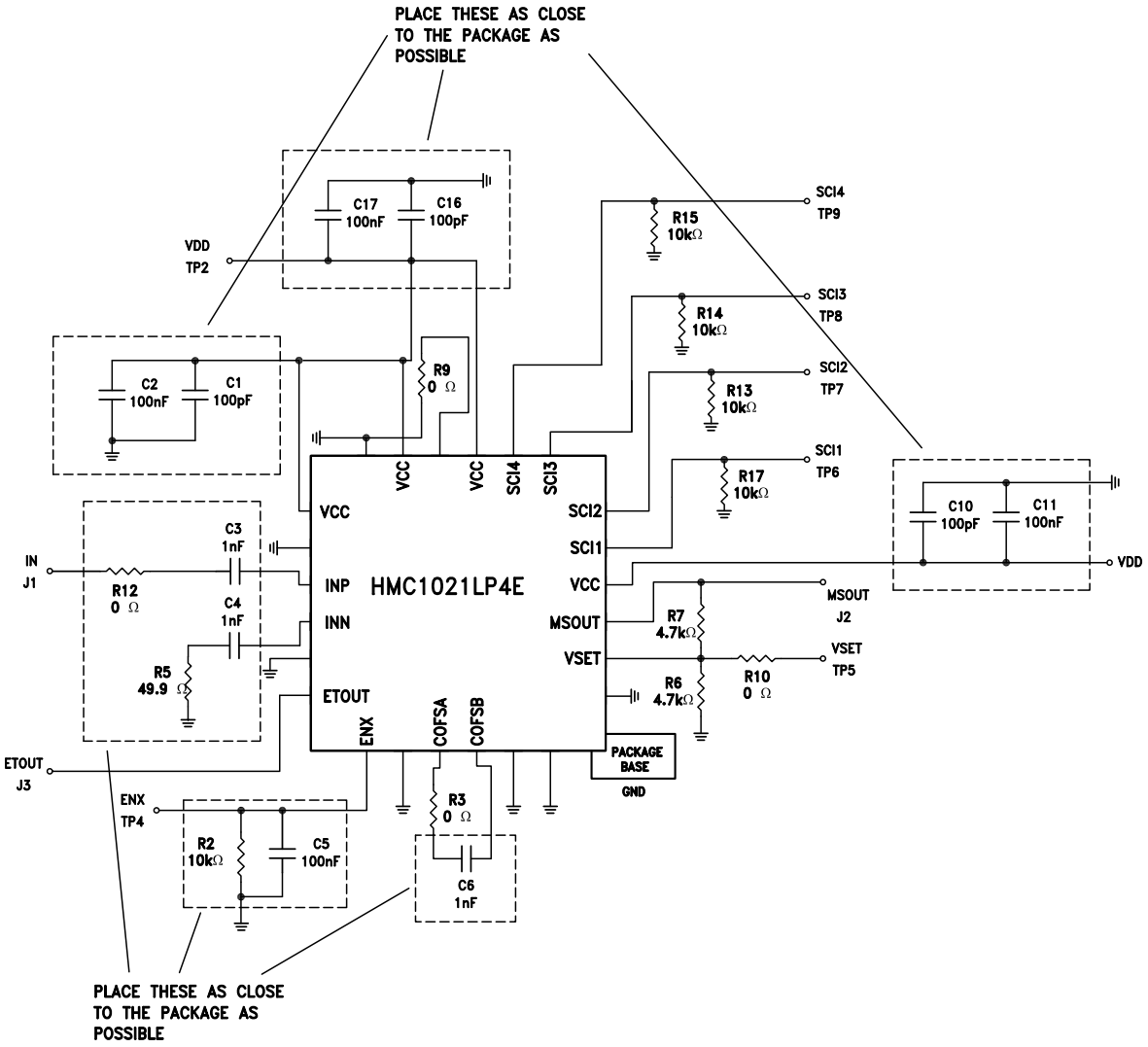
[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Rogers 4350 or Arlon 25FR

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 ohm impedance while the package ground leads and exposed paddle should be connected directly to the ground plane similar to that shown. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Hittite upon request.

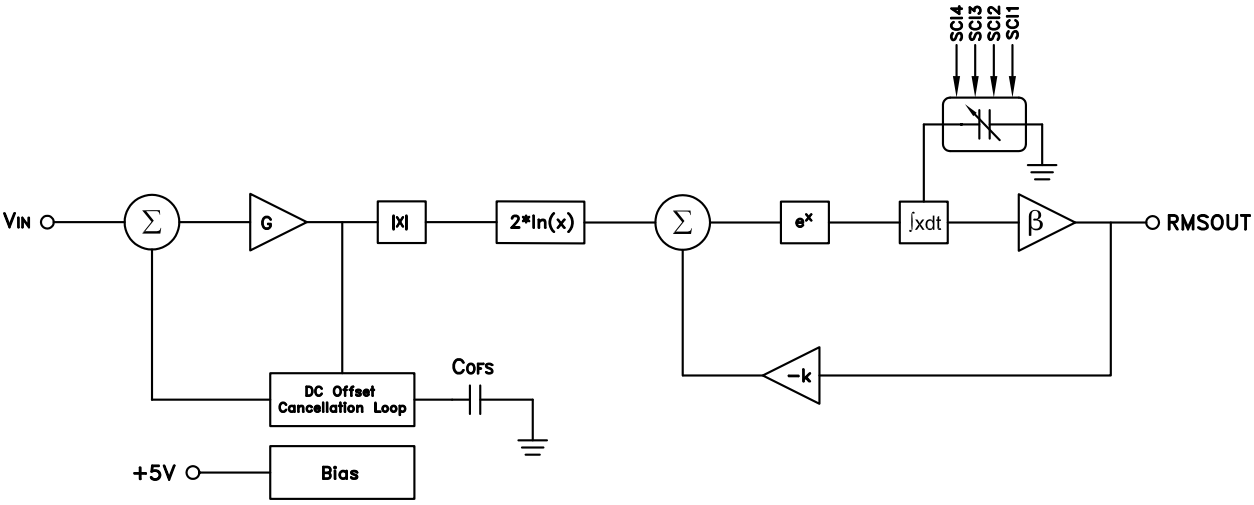
Board is configured with wideband single-ended input interface suitable for input signal frequencies above 100 MHz. Refer to wideband single-ended input interface section in application information for operating with signals below 100 MHz.

Application Circuit



Application Information

Principle of Operation



The HMC1021LP4E combines an RMS detector core with an Envelope Detector in a single package which is capable of extracting envelope information of the modulated RF signal with modulation bandwidths in excess of 100 MHz. The extracted envelope information is independent of the average power and the crest factor of the RF signal. The RMS detector core provides a linear-in-dB output of the average RF power, whereas the envelope detector core provides a linear representation of the instantaneous envelope waveform. The instantaneous envelope output ETOUT may be used in ultra-fast excessive RF power protection systems, PA linearization techniques and in efficiency enhancing Envelope-Tracking PA implementations.

The HMC1021LP4E's RMS detector core is designed to measure the actual RMS power of the input signal, independent of the modulated signal waveform complexity or modulation scheme. The RMS detector core architecture of HMC1021LP4E is composed of a full-wave rectifier, log/antilog circuit, and an integrator as shown above. The RMSOUT signal is directly proportional to the logarithm of the time-average of V_{IN}^2. The bias block also contains temperature compensation circuits which stabilize output accuracy over the entire operating temperature range. The DC offset cancellation circuit actively cancels internal offsets so that even very small input signal levels can be measured accurately.

The HMC1021LP4E achieves exceptional RF power measurement accuracy independent of the modulation of the carrier with the system architecture shown in the block diagram figure. The relation between the HMC1021LP4E's RMSOUT output and the RF input power is given below:

$$RMSOUT = \frac{1}{k}\ln\left(\beta k G^2 \int V_{IN}^2 dt\right)$$

P_{IN} = RMSOUT / [log-slope] + [log-intercept], dBm

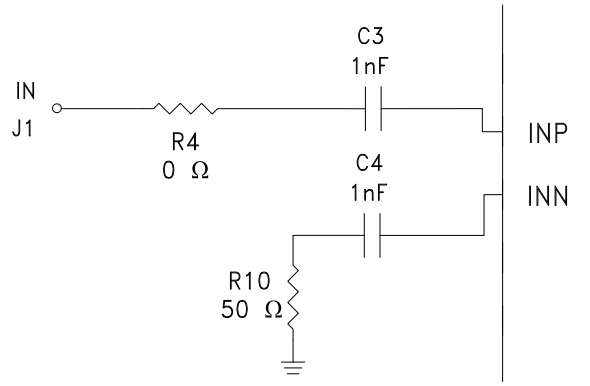
Configuration For The Typical Application

The HMC1021LP4E is a logarithmic RMS detector that can be directly driven with a single-ended 50-Ohm RF source. The integrated broadband single-ended input interface of HMC1021LP4E eliminates the requirement for an external balun transformer or matching network. The HMC1021LP4E can be operated from DC to 3.9 GHz by using only standard DC blocking capacitors. This simple input interface provides cost and PCB area reductions and increases measurement repeatability.

The RMS output signal is typically connected to VSET through a resistive network providing a Pin -> RMSOUT transfer characteristic slope of 33.7 mV/dBm (at 900 MHz). However the RMS output can be re-scaled to “magnify” a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS output. Refer to the section under the “Log-Slope and Intercept” section for details.

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements; refer to the “System Calibration” section for more details.

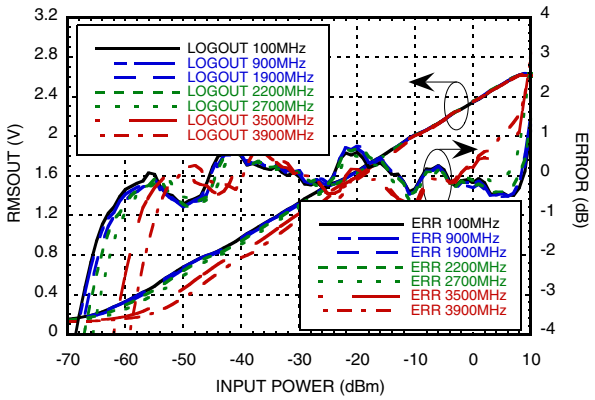
Broadband Single-Ended Input Interface



The HMC1021LP4E operates with a single-ended input interface and requires only two external DC blocking capacitors and an external 50Ohm resistor. The HMC1021LP4E input interface shown below provides a compact, broadband solution.

Note that the provided single-ended input interface covers the whole operating spectrum of the HMC1021LP4E and does not require matching/tuning for different frequencies. The performance of the HMC1021LP4E at different frequencies is shown below:

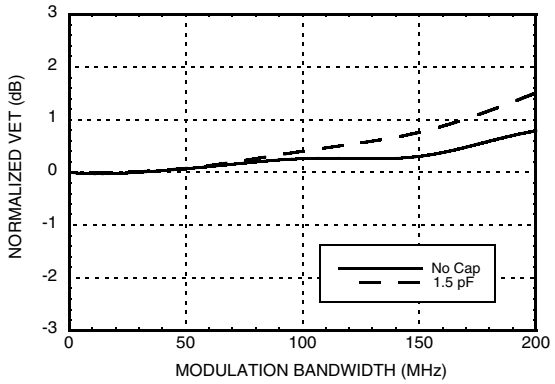
RMSOUT & Error vs. Pin



Envelope Detector Output

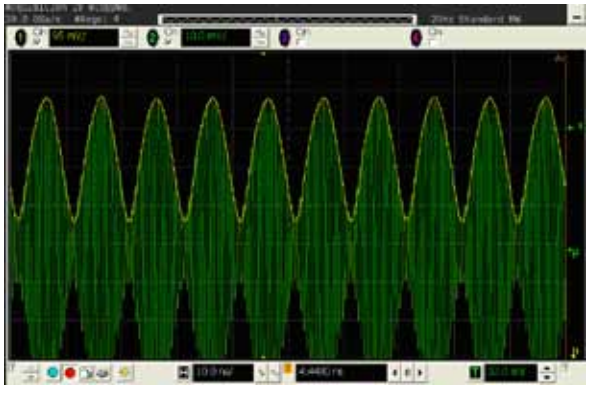
The HMC1021LP4E's ETOUT output provides a linearly scaled replica of the instantaneous envelope of the modulated RF signal for modulation bandwidths up to 150 MHz. For optimum performance, the ETOUT pin of the HMC1021LP4E should be terminated with a 560 Ω load resistor to GND. Note that any capacitive loading on the ETOUT pin would reduce the modulation bandwidth of the envelope detection. The envelope output has a conversion gain of 11.5V/V with an output voltage ranging from 1.2V to 2.2V.

ETOUT Bandwidth



The waveform below shows the HMC1021LP4E's envelope detector response to an RF input signal with a 100 MHz modulation bandwidth.

ETOUT Response to an RF Input Signal with a 100 MHz Modulation Bandwidth



RMS Output Interface and Transient Response

The HMC1021LP4E features digital input pins (SCI1-SCI4) that control the internal integration time constant. Output transient response is determined by the digital integration controls, and output load conditions.

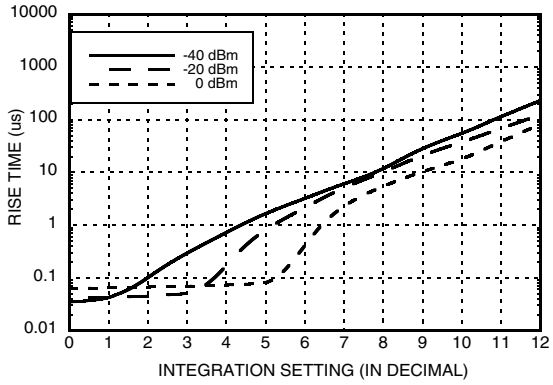
Shortest integration time is for SCI=0000, allowed longest integration time is for SCI=1100 (1101, 1110 and 1111 SCI settings are forbidden states).

Using larger values of SCI will narrow the operating bandwidth of the integrator, resulting in a longer averaging time interval and a more filtered output signal. It will also slow the power detector's transient response. A larger SCI value favors output accuracy over speed. For the fastest possible transient settling times set SCI to 0000. This configuration will operate the integrator at its widest possible bandwidth, resulting in short averaging time-interval and an output signal with little filtering. For most applications an SCI setting may be selected to maintain a balance between speed and accuracy. Furthermore, error performance over modulation bandwidth is dependent on the SCI setting. For example modulations with relatively low frequency components and high crest factors may require higher SCI (integration) settings.

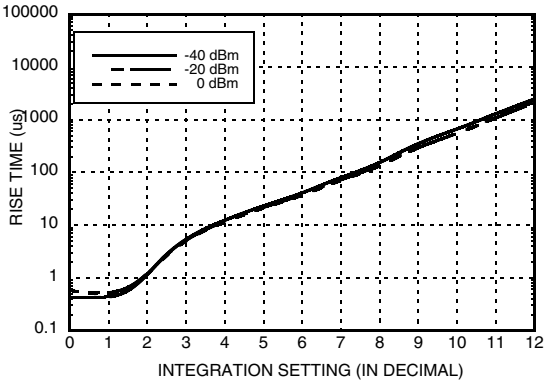
Table 1: Transient Response vs. SCI Setting [1]:

	RMSOUT Rise-Time 10% -> 90% (µs) [3]			RMSOUT Rise Settling Time (µs) [2]			RMSOUT Fall-time 100% -> 10% (µs) [4]		
SCI4,3,2,1	Pin = 0 dBm	Pin = -20 dBm	Pin = -40 dBm	Pin = 0 dBm	Pin = -20 dBm	Pin = -40 dBm	Pin = 0 dBm	Pin = -20 dBm	Pin = -40 dBm
0000	0.0626	0.042	0.0346	0.425	0.529	0.5806	0.9484	0.9694	0.9008
0010	0.0668	0.0444	0.078	0.4736	0.5476	0.5348	2.9932	3.12	3.0216
0100	0.072	0.064	0.648	11.748	11.254	10.89	12.252	12.094	12.786
0110	0.096	1.848	2.976	36.904	34.448	33.552	48.176	49.112	51.96
1000	5.16	9.18	9.72	130.76	119.2	114.78	194.12	199.64	201.2
1010	16.4	35.8	51.2	628.4	515.1	515.8	780.1	800	833.6
1100	81.41	123.637	229.2	2469.2	2102.801	2214	3198.8	3301.6	3358.801

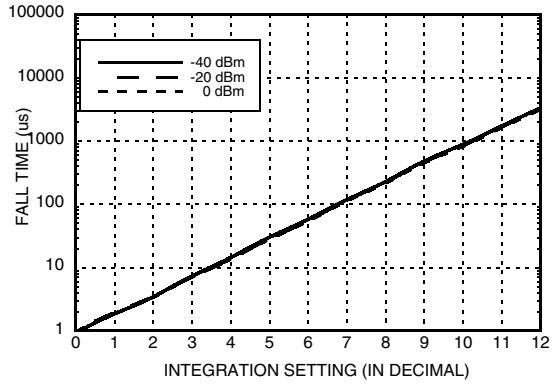
Rise Time[2] vs. SCI Setting over Input Power



Rise Settling Time [3] vs. SCI Setting over Input Power



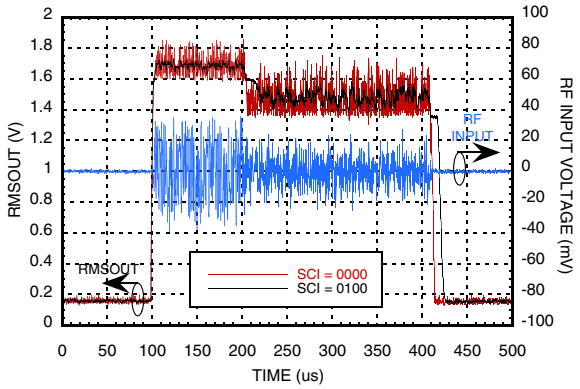
Fall Time [4] vs. SCI Setting over Input Power



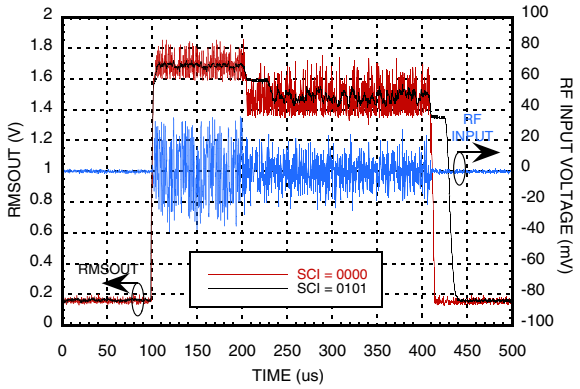
For increased load drive capability, consider a buffer amplifier on the RMS output. Using an integrating amplifier on the RMS output allows for an alternative treatment for faster settling times. An external amplifier optimized for transient settling can also provide additional RMS filtering, when operating HMC1021LP4E with a lower SCI value.

Following figures show how the peak-to-peak ripple decreases with higher SCI settings along with the RF pulse response over different modulations.

Residual Ripple for 900 MHz WiMAX @ SCI=0100



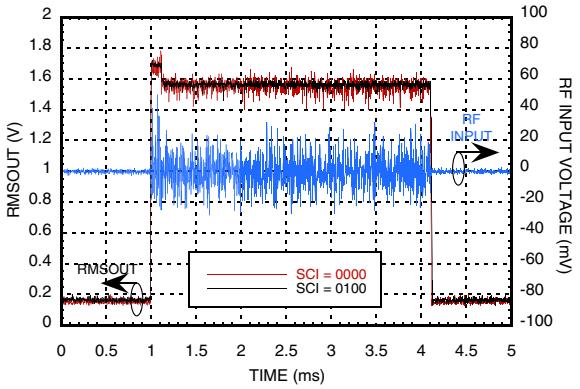
Residual Ripple for 900 MHz WiMAX @ SCI=0101



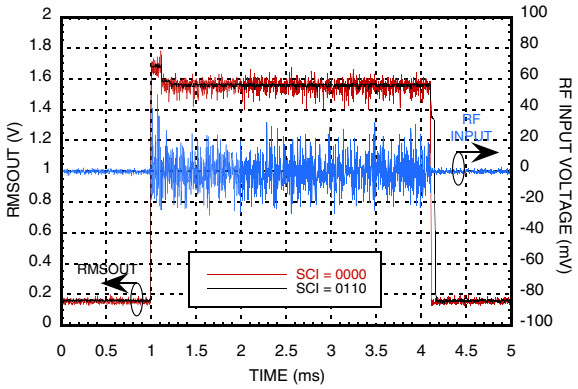
[1] Input signal is 1900 MHz CW -tone switched on and off
[2] Measured from 10% to 90%
[3] Measured from RF switching edge to 1dB (input referred) settling of RMSOUT.
[4] Measured from 100% to 10%

For price, delivery and to place orders: Hittite Microwave Corporation, 20 Alpha Road, Chelmsford, MA 01824
Phone: 978-250-3343 Fax: 978-250-3373 Order On-line at www.hittite.com
Application Support: Phone: 978-250-3343 or apps@hittite.com

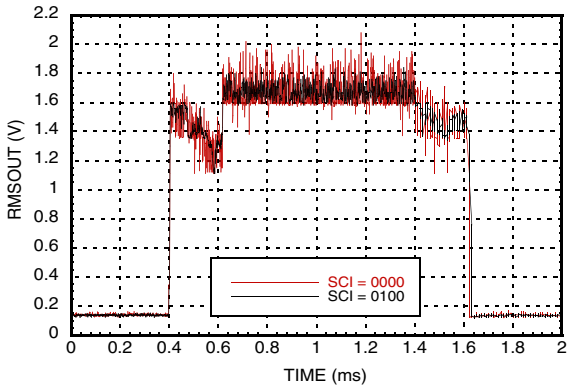
Residual Ripple for 900 MHz WiBRO @ SCI=0100



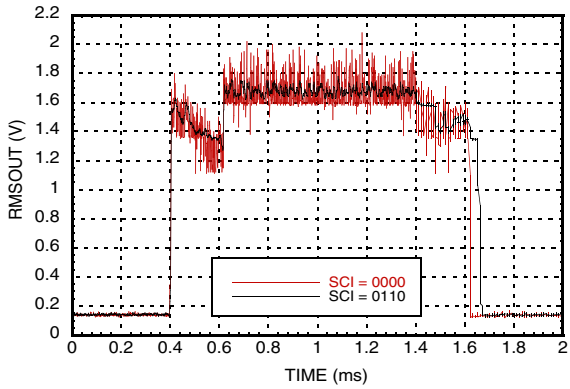
Residual Ripple for 900 MHz WiBRO@ SCI=0110



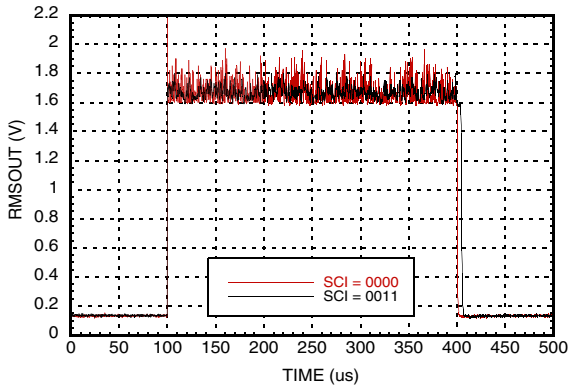
Residual Ripple for 900 MHz LTE Downlink @ SCI=0100



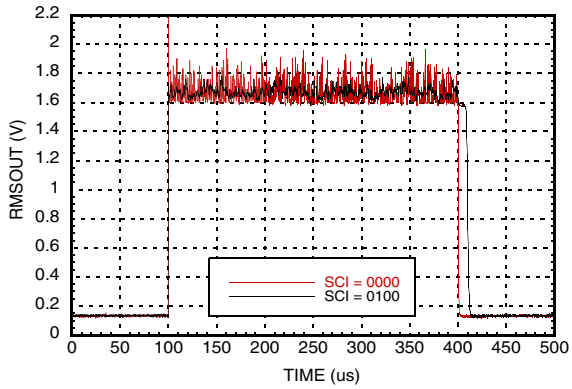
Residual Ripple for 900 MHz LTE Downlink @ SCI=0110



Residual Ripple for 900 MHz WCDMA4 @ SCI=0011



Residual Ripple for 900 MHz WCDMA4 @ SCI=0100

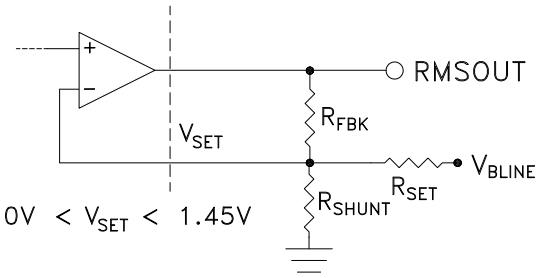


LOG-Slope and Intercept

The HMC1021LP4E provides for an adjustment of output scale with the use of an integrated operational amplifier. Logslope and intercept can be adjusted to "magnify" a specific portion of the input sensing range, and to fully utilize the dynamic range of the RMS output.

A log-slope of 37.3 mV/dB (@1900 MHz) is set by connecting RMS Output to VSET through a resistor network for ß=1 (see application schematic).

The log-slope is adjusted by applying the appropriate resistors on the RMS and VSET pins. Log-intercept is adjusted by applying a DC voltage to the VSET pin.



Optimized slope = ß * log-slope

Optimized intercept = log_intercept – (R_{FBK} /R_{SET}) * V_{BLINE}

$$ß = \frac{1}{2} \frac{R_{FBK}}{R_{FBK} // R_{SHUNT} // R_{SET}}$$

When R_{FBK}=0 to set RMSOUT=V_{SET}, then ß=1/2

If R_{SET} is not populated, then ß = ½ * (R_{FBK}/ (R_{FBK} // R_{SHUNT})) and intercept is at nominal value.

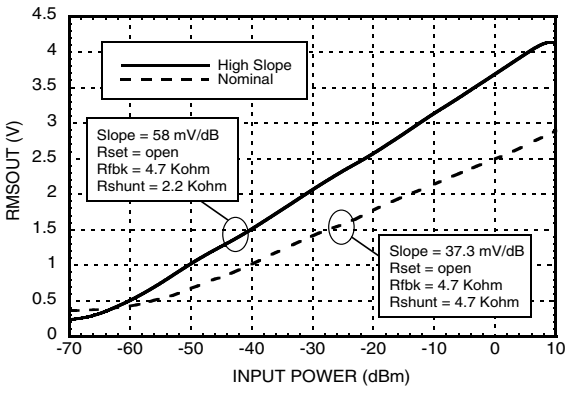
Example: The logarithmic slope can be simply increased by choosing appropriate R_{FBK} and R_{SHUNT} values while not populating the RSET resistor on the evaluation board to keep the intercept at nominal value.

Setting R_{FBK}=4.7KΩ and R_{SHUNT} = 2.2KΩ results in an optimized slope of:

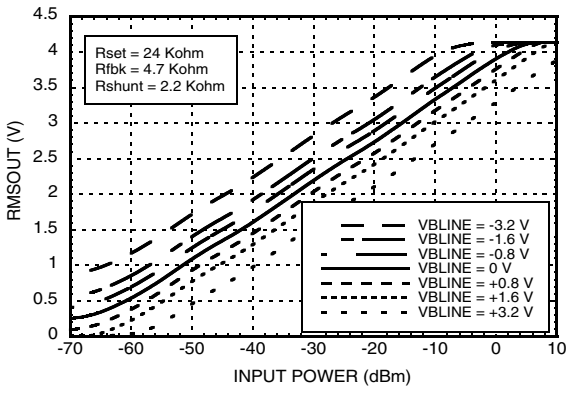
Optimized Slope = ß * log_slope = 1.57* 37.3mV / dB

Optimized Slope = 58 mV / dB

Slope Adjustment



Intercept Adjustment



DC Offset Compensation Loop

Internal DC offsets, which are input signal dependant, require continuous cancellation. Offset cancellation is a critical function needed for maintenance of measurement accuracy and sensitivity. The DC offset cancellation loop performs this function, and its response is largely defined by the capacitance (COFS) connected between COFSA, COFS pins.

COFS capacitor sets the loop bandwidth of the DC offset compensations. Higher COFS values are required for measuring lower RF frequencies. The optimal loop bandwidth setting will allow internal offsets to be cancelled at a minimally acceptable speed.

DC Offset Cancellation Loop ≈ $\frac{1}{\pi(5000)(C_{OFS}+20\times10^{12})}$ Bandwidth , Hz

For example: loop bandwidth for DC cancellation with COFS = 1nF, bandwidth is ~62 kHz

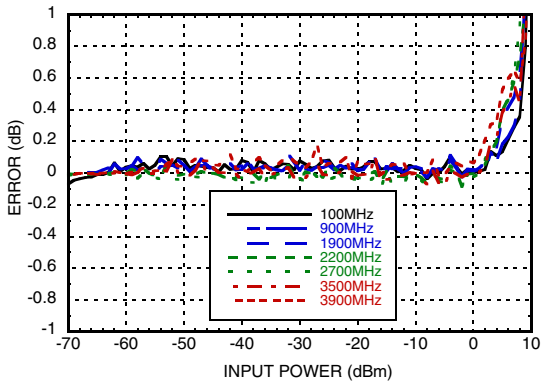
Standby Mode

The ENX pin can be used to force the power detector into a low-power standby mode. As ENX is deactivated, power is restored to all of the circuits. There is no memory of previous conditions. Coming out of stand by mode, internal integration and COFS capacitors will require recharging, so if large SCI values have been chosen, the wake-up time will be lengthened.

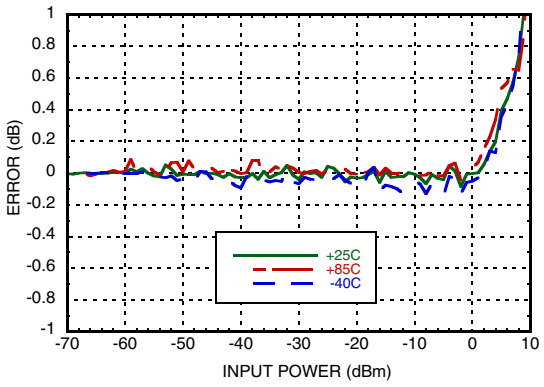
Modulation Performance – Crest factor performance

The HMC1021LP4E is able to detect the average power of RF signals with complex modulation schemes with exceptional accuracy. The proprietary RMS detection core is optimized to accurately detect the RMS power of the modulated RF signals with very high crest factors. This crest factor immune detection architecture of HMC1021LP4E results in detection accuracy of better than 0.2 dB over the entire operating frequency and temperature range, compared with the CW response under actual WCDMA4TM test signals shown below:

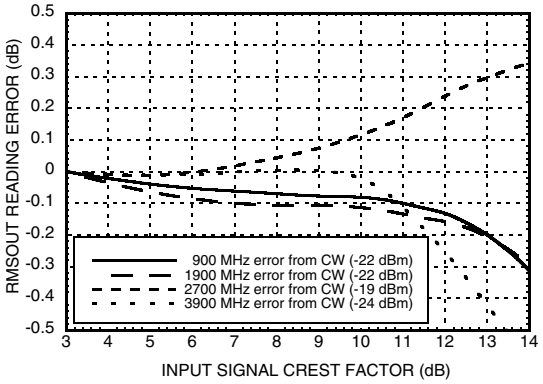
Reading Error for WCDMA 4 Carrier wrt CW Response @ +25 °C



Reading Error for WCDMA 4 Carrier wrt CW Response @ 2200 MHz



RMSOUT Error vs. Crest Factor over Frequency



System Calibration

Due to part-to-part variations in log-slope and log-intercept, a system-level calibration is recommended to satisfy absolute accuracy requirements. When performing this calibration, two test points near the top end and bottom-end of the desired detection dynamic range should be chosen. It is best to measure the calibration points in the regions (of frequency and amplitude) where accuracy is most important. The log-slope and log-intercept parameters should be derived and then stored in nonvolatile memory. These parameters relate the RMSOUT output voltage reading of HMC1021LP4 to the actual RMS power level as shown below:

P_{IN} = RMSOUT / [log-slope] + [log-intercept], dBm

The derivation procedure of the log-slope and log-intercept parameters is elaborated below:

For example if the following two calibration points were measured at 2.2 GHz:

With RMSOUT = 2.0338V at Pin = -10 dBm,
and RMSOUT = 0.5967V at Pin = -50 dBm
slope calibration constant = SCC
SCC = = (-50+10)/(0.5967-2.0338) =27.83 dB/V
intercept calibration constant = ICC
ICC = Pin – SCC *RMSO UT = -10 – 27.83 * 2.0338 = -66.60 dBm

Now performing a power measurement at -30 dBm:

RMSOUT measures 1.3089V
[Measured Pin] = [Measured RMSOUT]*SCC + ICC
[Measured Pin] = 1.3089*27.83 – 66.60 = -30.17 dBm
An error of only 0.17 dB

Factory system calibration measurements should be made using an input signal representative of the application. If the power detector is intended to operate over a wide range of frequencies, then a central frequency should be chosen for calibration.

Layout Considerations

• Mount RF input coupling capacitors close to the INP and INP pins.

• Solder the heat slug on the package underside to a grounded island which can draw heat away from the die with low thermal impedance. The grounded island should be at RF ground potential.

• Connect power detector ground to the RF ground plane, and mount the supply decoupling capacitors close to the supply pins.

Definitions

• Log-slope: slope of P_{IN} –> RMSOUT transfer characteristic. In units of mV/dB

• Log-intercept: x-axis intercept of P_{IN} –> RMSOUT transfer characteristic. In units of dBm.

• RMS Output Error: The difference between the measured P_{IN} and actual P_{IN} using a line of best fit.

[measured_P_{IN}] = [measured_ RMSOUT] / [best-fit-slope] + [best-fit-intercept], dBm

• Input Dynamic Range: the range of average input power for which there is a corresponding RMS output voltage with “RMS Output Error” falling within a specific error tolerance.

• Crest Factor: Peak power to average power ratio for time-varying signals.