DLPC900 Digital Controller for Advanced Light Control

1 Features

- One Scalable Controller Supports Both DLP6500 and DLP9000 DMDs for High Resolution Industrial and Display Applications
- Supports 1080p and WQXGA Capabilities of DLP6500 and DLP9500, Respectively
- Supports Multiple High-Speed Pattern Rates
  - 1-Bit Binary Patterns (Pre-Loaded) up to 9500 Hz
  - 1-Bit Binary Patterns (External Input) up to 9500 Hz
  - 8-Bit Gray Patterns (Pre-Loaded and External Input) up to 247 Hz
  - 1-to-1 Input Mapping to Micromirrors
  - Multiple Bit Depth and LEDs in Pattern Modes
  - 128 MB Internal DRAM Stores up to 400 1-Bit Binary Patterns
  - 48 MB External Flash Stores up to 250 1-Bit Binary or 30 8-Bit Gray Patterns
- Easy Synchronization With Cameras and Sensors
  - Two Configurable Input Triggers
  - Two Configurable Output Triggers
- Fully Programmable GPIO and PWM Signals
- Multiple Control Interfaces
  - One USB 1.1 Slave Port and Three I^2C Ports
  - LED Enable and PWM Generators
- Video Projection Mode
  - 24-Bit RGB Rates up to 120 Hz
  - YUV, YCrCb, or RGB Data Format
  - Two 24-Bit Input Pixel Ports
  - Standard Video from SVGA to 1080p
  - WQXGA up to 120 Hz With DLP9000 (requires 2× DLPC900)
- Integrated Clock and Micromirror Drivers

2 Applications

- Industrial
  - 3D Machine Vision and Quality Control
  - 3D Printing
  - Direct Imaging Lithography
  - Laser Marking and Repair
- Medical
  - Ophthalmology
  - 3D Scanners for Limb and Skin Measurement
  - Hyper-Spectral Scanning
- Displays
  - Intelligent and Adaptive Lighting
  - 3D Imaging Microscopes

3 Description

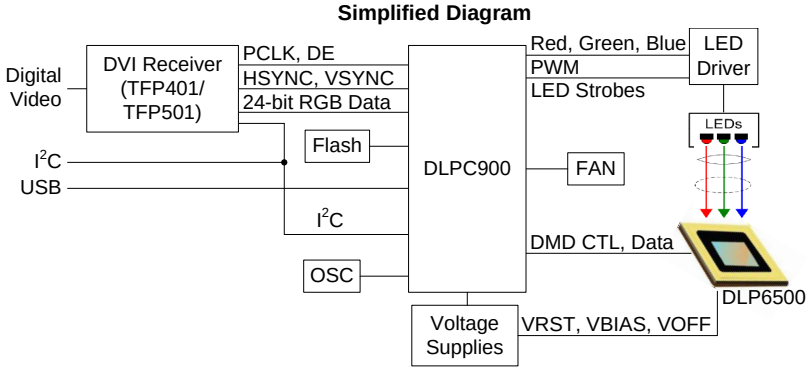
The DLPC900 is a single scalable DMD (digital micromirror device) controller that supports reliable operation of three high resolution DMD chips: DLP6500FLQ, DLP6500FYE, and DLP9000FLS. This high-performance DMD controller enables programmable, high-speed pattern rates for advanced light control, especially in industrial, medical, and scientific applications. DLPC900 pattern rates enable fast and accurate 3D scanning and 3D printing, as well as support high resolution and intelligent imaging applications. DLPC900 offers 128 MB of embedded DRAM for convenient storage of up to 400 1-bit patterns. Input and output triggers offer easy connection and synchronization with a variety of cameras, sensors, and other peripherals. Numerous ports and connectivity options offer system flexibility and simplify chip integration into a variety of end equipment.

Device Information (1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
DLPC900ZPC	BGA (516)	27.00 mm × 27.00 mm

(1) For all available packages, refer to the orderable addendum at the end of the data sheet.

Simplified Diagram



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4 Revision History

Changes from Original (October 2014) to Revision A **Page**

- Changed phrasing of pattern speed features 1
- Corrected the width of the input pixel ports to 24-bits 1
- Added I/O Type and Subscript Definition table 5
- Corrected maximum port width of Ports 1 and 2 in table note 10
- Updated *ESD Ratings* table title and value column 20
- ESD sensitivity machine model was removed 20
- Added note to clarify that Ports 1 and 2 are used as 24-bit buses 29
- Changed section title to correct bus size to 48-bits 30
- Removed references to 30-bit RGB video 36
- Corrected minor typos 38
- Corrected video pattern mode timing diagram and description 39
- Corrected pre-stored pattern mode timing diagram and description 39
- Corrected pre-stored pattern mode 3 pattern example diagram and description 39
- Removed Allowed Pattern Combinations table 40
- Added Minimum Exposure in Any Pattern Mode table 40
- Added Minimum Exposures for Number of Active DMD Blocks table 40
- Updated Boot Flash Memory Layout image to reflect firmware version 2.0 42
- Added note about firmware components. 43
- Corrected video data interface size to 24-bits 43
- Corrected video mode port maximum size to 24 bits 44
- Corrected P1 and P2 signal description regarding 24-bit bus width 44
- Corrected spacing and formatting 51
- Corrected minor typo 60
- Changed the number of P1 and P2 lines to reflect 24 bit-width 61

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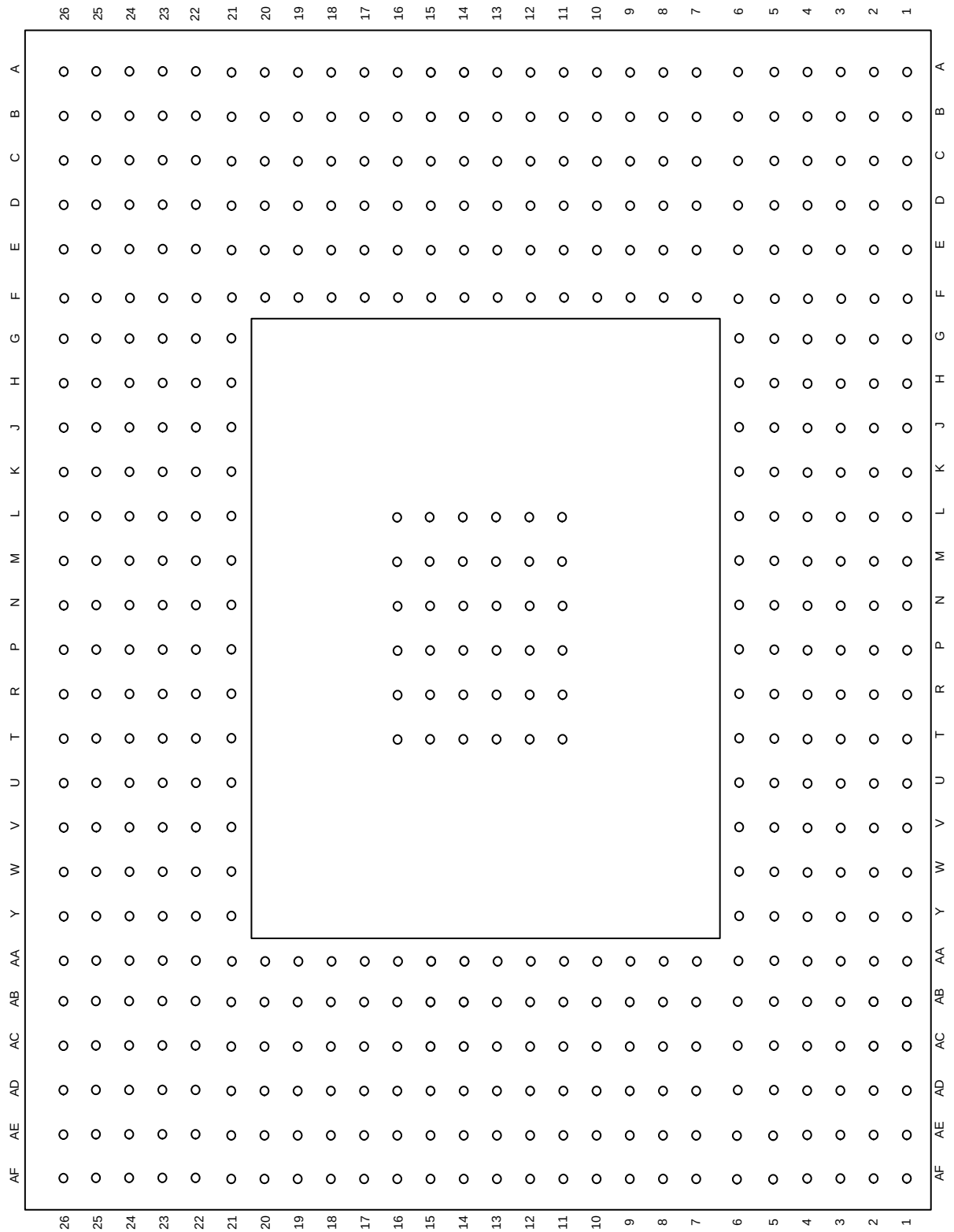
5 Pin Configuration and Functions

ZPC Package
516-Pin BGA
Bottom View



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Initialization Pin Functions

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
POSENSE	P22	VDD33	I_4 H	Async	Power-On Sense is an active high signal with hysteresis, that is generated from an external voltage monitor circuit. This signal should be driven active high when all the controller supply voltages have reached 90% of their specified minimum voltage. This signal should be driven inactive low after the falling edge of PWRGOOD as shown in Figure 2 Power Up and Power Down timing requirements. See also *System Power-Up Sequence*.
PWRGOOD	T26	VDD33	I_4 H	Async	Power Good is an active high signal with hysteresis that is provided from an external voltage monitor circuit. A high value indicates all power is within operating voltage specifications and the system is safe to exit its RESET state. A transition from high to low is used to indicate that the DLPC900 and DMD supply voltage will drop below their rated minimum level. This transition must occur prior to the supply voltage drop as specified. During this interval, POSENSE must remain active high. PWRGOOD serves as an early warning of an imminent power loss condition. A DMD park followed by a full controller reset is performed by the DLPC900 to protect the DMD. The minimum de-assertion time is used to protect the input from glitches. After the park sequence is complete, the DLPC900 will be held in its RESET state as long as PWRGOOD is low. PWRGOOD must be driven high for normal operation. The DLPC900 will acknowledge PWRGOOD as active once it's been driven high for its specified minimum time. See Figure 2 Power Up and Power Down timing requirements. See also *System Power-Up Sequence*.
EXT_ARSTZ	T24	VDD33	O_2	Async	General purpose active low reset output signal. This output is driver low immediately after POSENSE is externally driven low, placing the system in RESET and remains low while POSENSE remains low. EXT_ARSTZ will continue to be held low after POSENSE is driven high and released by the controller firmware. EXT_ARSTZ is also driven low approximately 5 µs after the detection of a PWRGOOD or any internally generated reset. In all cases, it will remain active for a minimum of 2 ms.
CTRL_ARSTZ	T25	VDD33	O_2	Async	Controller active low reset output signal. This output is driven low immediately after POSENSE is externally driven low and remains low while POSENSE remains low. CTRL_ARSTZ will continue to be held low after POSENSE is driven high and released by the controller firmware. CTRL_ARSTZ is also optionally asserted low approximately 5us after the detection of a PWRGOOD or any internally generated reset. In all cases it will remain active for a minimum of 2 ms.

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DMD Control Pin Functions

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION (1)
NAME	NUMBER				
DADOEZ	AE7	VDD33	O_5	Async	DMD output-enable (active low). This signal does not apply to the slave controller in a two-controller system configuration. On the slave controller, this pin is reserved and should be left unconnected.
DADADDR_3 DADADDR_2 DADADDR_1 DADADDR_0	AD6 AE5 AF4 AB8	VDD33	O_5	Async	DMD address. This signal does not apply to the slave controller in a two-controller system configuration. On the slave controller, this pin is reserved and should be left unconnected.
DADMODE_1 DADMODE_0	AD7 AE6	VDD33	O_5	Async	DMD mode. This signal does not apply to the slave controller in a two-controller system configuration. On the slave controller, this pin is reserved and should be left unconnected.
DADSEL_1 DADSEL_0	AE4 AC7	VDD33	O_5	Async	DMD select. This signal does not apply to the slave controller in a two-controller system configuration. On the slave controller, this pin is reserved and should be left unconnected.
DADSTRB	AF5	VDD33	O_5	Async	DMD strobe. This signal does not apply to the slave controller in a two-controller system configuration. On the slave controller, this pin is reserved and should be left unconnected.
DAD_INTZ	AC8	VDD33	I_4 H	Async	DMD interrupt (active low). Requires an external 1-kΩ pullup resistor.

(1) Refer to the *Typical Single Controller Chipset* and the *Typical Two Controller Chipset* for a description between a one controller and a two controller configuration.

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DMD LVDS Interface Pin Functions (1) (2)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
DCKA_P DCKA_N	V4 V3	VDD18	O_7	DCKA_P DCKA_N	DMD, LVDS interface channel A, differential clock
SCA_P SCA_N	V2 V1	VDD18	O_7	DCKA_P DCKA_N	DMD, LVDS interface channel A, differential serial control
DDA_P_15 DDA_N_15 DDA_P_14 DDA_N_14 DDA_P_13 DDA_N_13 DDA_P_12 DDA_N_12 DDA_P_11 DDA_N_11 DDA_P_10 DDA_N_10 DDA_P_9 DDA_N_9 DDA_P_8 DDA_N_8	P4 P3 P2 P1 R4 R3 R2 R1 T4 T3 T2 T1 U4 U3 U2 U1	VDD18	O_7	DCKA_P DCKA_N	DMD, LVDS interface channel A, differential serial data
DDA_P_7 DDA_N_7 DDA_P_6 DDA_N_6 DDA_P_5 DDA_N_5 DDA_P_4 DDA_N_4 DDA_P_3 DDA_N_3 DDA_P_2 DDA_N_2 DDA_P_1 DDA_N_1 DDA_P_0 DDA_N_0	W4 W3 W2 W1 Y2 Y1 Y4 Y3 AA2 AA1 AA4 AA3 AB2 AB1 AC2 AC1				
DCKB_P DCKB_N	J3 J4	VDD18	O_7	DCKB_P DCKB_N	DMD, LVDS interface channel B, differential clock
SCB_P SCB_N	J1 J2	VDD18	O_7	DCKB_P DCKB_N	DMD, LVDS interface channel B, differential serial control

(1) Several options allow reconfiguration of the DMD interface in order to better optimize board layout. The DLPC900 can swap channel A with channel B. The DLPC900 can also swap the data bit order within each channel independent of swapping the A and B channels.
(2) The DLPC900 is a full-bus DMD signaling interface. Figure 15 shows the controller connections for this configuration.

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DMD LVDS Interface Pin Functions (1) (2) (continued)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
DDB_P_15	N1	VDD18	O_7	DCKB_P DCKB_N	DMD, LVDS interface channel B, differential serial data
DDB_N_15	N2				
DDB_P_14	N3				
DDB_N_14	N4				
DDB_P_13	M2				
DDB_N_13	M1				
DDB_P_12	M3				
DDB_N_12	M4				
DDB_P_11	L1				
DDB_N_11	L2				
DDB_P_10	L3				
DDB_N_10	L4				
DDB_P_9	K1				
DDB_N_9	K2				
DDB_P_8	K3				
DDB_N_8	K4				
DDB_P_7	H1				
DDB_N_7	H2				
DDB_P_6	H3				
DDB_N_6	H4				
DDB_P_5	G1				
DDB_N_5	G2				
DDB_P_4	G3				
DDB_N_4	G4				
DDB_P_3	F1				
DDB_N_3	F2				
DDB_P_2	F3				
DDB_N_2	F4				
DDB_P_1	E1				
DDB_N_1	E2				
DDB_P_0	D1				
DDB_N_0	D2				

Program Memory Flash Interface Pin Functions (1)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION		
NAME	NUMBER				CHIP SELECT 0 (ADDITIONAL FLASH)	CHIP SELECT 1 (BOOT FLASH ONLY) (2)	CHIP SELECT 2 (ADDITIONAL FLASH)
PM_CSZ_0 (3)	D13	VDD33	O_5	Async	Chip select (active low)	N/A	N/A
PM_CSZ_1 (3)	E12	VDD33	O_5	Async	N/A	Boot flash chip select (active low)	N/A
PM_CSZ_2 (3)	A13	VDD33	O_5	Async	N/A	N/A	Chip select (active low)
PM_ADDR_22 (4)	A12	VDD33	B_5	Async	Address bit (MSB)	Address bit (MSB)	Address bit (MSB)
PM_ADDR_21 (4)	E11	VDD33	B_5	Async	Address bit	Address bit	Address bit
PM_ADDR_20	D12	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_19	C12	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_18	B11	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_17	A11	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_16	D11	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_15	C11	VDD33	O_5	Async	Address bit	Address bit	Address bit

(1) The default wait-state is set for a flash device of 120ns access time. Therefore, the slowest flash access time supported is 120ns. Refer to the *Program Memory Flash Interface* on how to program new wait-state values.
(2) Refer to the Figure 21 for the memory layout of the boot flash.
(3) Requires an external 10-kΩ pullup resistor.
(4) Requires an external 10-kΩ pulldown resistor.

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Program Memory Flash Interface Pin Functions (1) (continued)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION		
NAME	NUMBER				CHIP SELECT 0 (ADDITIONAL FLASH)	CHIP SELECT 1 (BOOT FLASH ONLY) (2)	CHIP SELECT 2 (ADDITIONAL FLASH)
PM_ADDR_14	E10	VDD33	O5	Async	Address bit	Address bit	Address bit
PM_ADDR_13	D10	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_12	C10	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_11	B9	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_10	A9	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_9	E9	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_8	D9	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_7	C9	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_6	B8	VDD33	O5	Async	Address bit	Address bit	Address bit
PM_ADDR_5	A8	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_4	D8	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_3	C8	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_2	B7	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_1	A7	VDD33	O_5	Async	Address bit	Address bit	Address bit
PM_ADDR_0	C7	VDD33	O_5	Async	Address bit (LSB)	Address bit (LSB)	Address bit (LSB)
PM_WEZ	B12	VDD33	O_5	Async	Write-enable (active low)	Write-enable (active low)	Write-enable (active low)
PM_OEZ	C13	VDD33	O_5	Async	Output-enable (active low)	Output-enable (active low)	Output-enable (active low)
PM_BLSZ_1	B6	VDD33	O_5	Async	UpperByte(15:8) enable (active low)	N/A	UpperByte(15:8) Enable (active low)
PM_BLSZ_0	A6	VDD33	O_5	Async	LowerByte(7:0) enable (active low)	N/A	LowerByte(7:0) Enable (active low)
PM_DATA_15	C17	VDD33	B_5	Async	Data bit (15)	Data bit (15)	Data bit (15)
PM_DATA_14	B16	VDD33	B_5	Async	Data bit (14)	Data bit (14)	Data bit (14)
PM_DATA_13	A16	VDD33	B_5	Async	Data bit (13)	Data bit (13)	Data bit (13)
PM_DATA_12	A15	VDD33	B_5	Async	Data bit (12)	Data bit (12)	Data bit (12)
PM_DATA_11	B15	VDD33	B_5	Async	Data bit (11)	Data bit (11)	Data bit (11)
PM_DATA_10	D16	VDD33	B_5	Async	Data bit (10)	Data bit (10)	Data bit (10)
PM_DATA_9	C16	VDD33	B_5	Async	Data bit (9)	Data bit (9)	Data bit (9)
PM_DATA_8	E14	VDD33	B_5	Async	Data bit (8)	Data bit (8)	Data bit (8)
PM_DATA_7	D15	VDD33	B_5	Async	Data bit (7)	Data bit (7)	Data bit (7)
PM_DATA_6	C15	VDD33	B_5	Async	Data bit (6)	Data bit (6)	Data bit (6)
PM_DATA_5	B14	VDD33	B_5	Async	Data bit (5)	Data bit (5)	Data bit (5)
PM_DATA_4	A14	VDD33	B_5	Async	Data bit (4)	Data bit (4)	Data bit (4)
PM_DATA_3	E13	VDD33	B_5	Async	Data bit (3)	Data bit (3)	Data bit (3)
PM_DATA_2	D14	VDD33	B_5	Async	Data bit (2)	Data bit (2)	Data bit (2)
PM_DATA_1	C14	VDD33	B_5	Async	Data bit (1)	Data bit (1)	Data bit (1)
PM_DATA_0	B13	VDD33	B_5	Async	Data bit (0)	Data bit (0)	Data bit (0)

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Port 1 and Port 2 Channel Data and Control Pin Functions

PIN (1) (2) (3)		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
P_CLK1	AE22	VDD33	I_4 D	N/A	Input port data pixel write clock (selectable as rising or falling edge triggered, and with which port it is associated (Port 1 or Port 2 or (Port 1 and Port 2))).
P_CLK2	W25	VDD33	I_4 D	N/A	Input port data pixel write clock (selectable as rising or falling edge triggered, and with which port it is associated (Port 1 or Port 2 or (Port 1 and Port 2))).
P_CLK3	AF23	VDD33	I_4 D	N/A	Input port data pixel write clock (selectable as rising or falling edge triggered, and with which port it is associated (Port 1 or Port 2 or (Port 1 and Port 2))).
P_DATEN1	AF22	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Active high data enable. Selectable as to which port it is associated with (Port 1 or Port 2 or (Port 1 and Port 2)).
P_DATEN2	W24	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Active high data enable. Selectable as to which port it is associated with (Port 1 or Port 2 or (Port 1 and Port 2)).
P1_A9 P1_A8 P1_A7 P1_A6 P1_A5 P1_A4 P1_A3 P1_A2 P1_A1 (1) P1_A0 (1)	AD15 AE15 AE14 AE13 AD13 AC13 AF14 AF13 AF12 AE12	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Port 1 A channel input pixel data (bit weight 128) Port 1 A channel input pixel data (bit weight 64) Port 1 A channel input pixel data (bit weight 32) Port 1 A channel input pixel data (bit weight 16) Port 1 A channel input pixel data (bit weight 8) Port 1 A channel input pixel data (bit weight 4) Port 1 A channel input pixel data (bit weight 2) Port 1 A channel input pixel data (bit weight 1) Unused, tie to 0 Unused, tie to 0
P1_B9 P1_B8 P1_B7 P1_B6 P1_B5 P1_B4 P1_B3 P1_B2 P1_B1 (1) P1_B0 (1)	AF18 AB18 AC15 AC16 AD16 AE16 AF16 AF15 AC14 AD14	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Port 1 B channel input pixel data (bit weight 128) Port 1 B channel input pixel data (bit weight 64) Port 1 B channel input pixel data (bit weight 32) Port 1 B channel input pixel data (bit weight 16) Port 1 B channel input pixel data (bit weight 8) Port 1 B channel input pixel data (bit weight 4) Port 1 B channel input pixel data (bit weight 2) Port 1 B channel input pixel data (bit weight 1) Unused, tie to 0 Unused, tie to 0
P1_C9 P1_C8 P1_C7 P1_C6 P1_C5 P1_C4 P1_C3 P1_C2 P1_C1 (1) P1_C0 (1)	AD20 AE20 AE21 AF21 AD19 AE19 AF19 AF20 AC19 AE18	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Port 1 C channel input pixel data (bit weight 128) Port 1 C channel input pixel data (bit weight 64) Port 1 C channel input pixel data (bit weight 32) Port 1 C channel input pixel data (bit weight 16) Port 1 C channel input pixel data (bit weight 8) Port 1 C channel input pixel data (bit weight 4) Port 1 C channel input pixel data (bit weight 2) Port 1 C channel input pixel data (bit weight 1) Unused, tie to 0 Unused, tie to 0
P1_VSYNC	AC20	VDD33	B_2 D	P_CLK1, P_CLK2, or P_CLK3	Port 1 vertical sync. While intended to be associated with port 1, it can be programmed for use with port 2.
P1_HSYNC	AD21	VDD33	B_2 D	P_CLK1, P_CLK2, or P_CLK3	Port 1 horizontal sync. While intended to be associated with port 1, it can be programmed for use with port 2.

(1) Port 1 and Port 2 are capable of 24-bits each. A maximum of 8-bits is available in each of the A, B, and C channels. The 8-bit color input should be connected to bits [9:2] of the corresponding A, B, C input channels. Sources feeding 8-bits or less per color component channel should be MSB justified when connected to the DLPC900, and the LSBs tied to ground along with the data lines 0 and 1 from every channel. Three port clocks options (1, 2, and 3) are provided to improve the signal integrity.
(2) Ports 1 and 2 can be used separately as two 24-bit ports, or can be combined into one 48-bit port (typically, for high data rate sources) for transmission of two pixels per clock.
(3) The A, B, C input data channels of ports 1 and 2 can be internally reconfigured or remapped for optimum board layout. Specifically each channel can individually remapped to the internal GBR/ YCbCr channels. For example, G data can be connected to channel A, B, or C and remapped to be appropriate channel internally. Port configuration and channel multiplexing is handled in the API software.

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Port 1 and Port 2 Channel Data and Control Pin Functions (continued)

PIN (1) (2) (3)		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
P2_A9	AD26	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Port 2 A channel input pixel data (bit weight 128)
P2_A8	AD25				Port 2 A channel input pixel data (bit weight 64)
P2_A7	AB21				Port 2 A channel input pixel data (bit weight 32)
P2_A6	AC22				Port 2 A channel input pixel data (bit weight 16)
P2_A5	AD23				Port 2 A channel input pixel data (bit weight 8)
P2_A4	AB20				Port 2 A channel input pixel data (bit weight 4)
P2_A3	AC21				Port 2 A channel input pixel data (bit weight 2)
P2_A2	AD22				Port 2 A channel input pixel data (bit weight 1)
P2_A1 (1)	AE23				Unused, tie to 0
P2_A0 (1)	AB19				Unused, tie to 0
P2_B9	Y22	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Port 2 B channel input pixel data (bit weight 128)
P2_B8	AB26				Port 2 B channel input pixel data (bit weight 64)
P2_B7	AA23				Port 2 B channel input pixel data (bit weight 32)
P2_B6	AB25				Port 2 B channel input pixel data (bit weight 16)
P2_B5	AA22				Port 2 B channel input pixel data (bit weight 8)
P2_B4	AB24				Port 2 B channel input pixel data (bit weight 4)
P2_B3	AC26				Port 2 B channel input pixel data (bit weight 2)
P2_B2	AB23				Port 2 B channel input pixel data (bit weight 1)
P2_B1 (1)	AC25				Unused, tie to 0
P2_B0 (1)	AC24				Unused, tie to 0
P2_C9	W23	VDD33	I_4 D	P_CLK1, P_CLK2, or P_CLK3	Port 2 C channel input pixel data (bit weight 128)
P2_C8	V22				Port 2 C channel input pixel data (bit weight 64)
P2_C7	Y26				Port 2 C channel input pixel data (bit weight 32)
P2_C6	Y25				Port 2 C channel input pixel data (bit weight 16)
P2_C5	Y24				Port 2 C channel input pixel data (bit weight 8)
P2_C4	Y23				Port 2 C channel input pixel data (bit weight 4)
P2_C3	W22				Port 2 C channel input pixel data (bit weight 2)
P2_C2	AA26				Port 2 C channel input pixel data (bit weight 1)
P2_C1 (1)	AA25				Unused, tie to 0
P2_C0 (1)	AA24				Unused, tie to 0
P2_VSYNC	U22	VDD33	B_2 D	P_CLK1, P_CLK2, or P_CLK3	Port 2 vertical sync. While intended to be associated with port 2, it can be programmed for use with port 1.
P2_HSYNC	W26	VDD33	B_2 D	P_CLK1, P_CLK2, or P_CLK3	Port 2 horizontal sync. While intended to be associated with port 2, it can be programmed for use with port 1.

Clock and PLL Support Pin Functions

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
MOSC	M26	VDD33	I_{10}	N/A	System clock oscillator input (3.3-V LVTTL). MOSC must be stable a maximum of 25 ms after POSENSE transitions from low to high.
MOSCN	N26	VDD33	O_{10}	N/A	MOSC crystal return.
OCLKA (1)	AF6	VDD33	O_5	Async	General-purpose output clock A. The frequency is software programmable. Power-up default is 787 kHz and the output frequency is maintained through all operations, except power loss and reset.

(1) This signal does not apply to the slave controller in a two controller system configuration. On the slave controller, this pin is reserved and should be left unconnected. Refer to the *Typical Single Controller Chipset* and the *Typical Two Controller Chipset* for a description between a one controller and a two controller configuration.

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Board Level Test and Debug Pin Functions (1)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
TDI	N25	VDD33	I_4 U	TCK	JTAG serial data in. Used in both Boundary Scan and ICE modes.
TCK	N24	VDD33	I_4 D	N/A	JTAG serial data clock. Used in both Boundary Scan and ICE modes.
TMS1	P25	VDD33	I_4 U	TCK	JTAG test mode select. Used in Boundary Scan mode.
TMS2	P26	VDD33	I_4 U	TCK	JTAG-ICE test mode select. Used in ICE mode.
TDO1	N23	VDD33	O_5	TCK	JTAG serial data out. Used in Boundary Scan mode.
TDO2	N22	VDD33	O_5	TCK	JTAG-ICE serial data out. Used in ICE mode.
TRSTZ	M23	VDD33	I_4 H U	Async	JTAG Reset. Used in both Boundary Scan and ICE modes. This pin should be pulled high (or left unconnected) when the JTAG interface is in use for boundary scan or debug. Connect this to ground otherwise. Failure to tie this pin low during normal operation will cause startup and initialization problems.
RTCK	E4	VDD33	O_2	N/A	JTAG return clock. Used in ICE mode.
ICTSEN	M24	VDD33	I_4 H D	Async	IC tri-state enable (active high). Asserting high will tri-state all outputs except the JTAG interface. Requires an external 4.7 kΩ pulldown resistor.

(1) All JTAG signals are LVTTL compatible.

Device Test Pin Functions

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
HW_TEST_EN	M25	VDD33	I_4 H D	N/A	Device manufacturing test enable. This signal must be connected to an external ground for normal operation.

Peripheral Interface Pin Functions

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
I2C0_SCL	A10	VDD33	B_8	N/A	I^2C bus 0, clock. This bus supports 400 kHz, fast mode operation. This input is not 5 V tolerant. This pin requires an external pullup resistor to 3.3 V. The minimum acceptable pullup value is 1 kΩ resistor.
I2C0_SDA	B10	VDD33	B_8	I2C0_SCL	I^2C bus 0, data. This bus supports 400 kHz, fast mode operation. This input is not 5 V tolerant. This pin requires an external pullup resistor to 3.3 V. The minimum acceptable pullup value is 1 kΩ resistor.
I2C1_SDA (1)	E19	VDD33	B_2	I2C1_SCL	I^2C bus 1, data. This bus supports 400 kHz, fast mode operation. This input is not 5 V tolerant. This pin requires an external pullup resistor to 3.3 V. The minimum acceptable pullup value is 1 kΩ resistor.
I2C1_SCL (1)	D20	VDD33	B_2	N/A	I^2C bus 1, clock. This bus supports 400 kHz, fast mode operation. This input is not 5 V tolerant. This pin requires an external pullup resistor to 3.3 V. The minimum acceptable pullup value is 1 kΩ resistor.
I2C2_SDA (1)	C21	VDD33	B_2	I2C2_SCL	I^2C bus 2, data. This bus supports 400 kHz, fast mode operation. This input is not 5 V tolerant. This pin requires an external pullup resistor to 3.3 V. The minimum acceptable pullup value is 1 kΩ resistor.

(1) This signal does not apply to the slave controller in a two controller system configuration. On the slave controller, this pin is reserved and should be left unconnected. Refer to *Typical Single Controller Chipset* and *Typical Two Controller Chipset* for a description between a one controller and a two controller configuration.

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Peripheral Interface Pin Functions (continued)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
I2C2_SCL (1)	B22	VDD33	B_2	N/A	I^2C bus 2, clock. This bus supports 400 kHz, fast mode operation. This input is not 5 V tolerant. This pin requires an external pullup resistor to 3.3 V. The minimum acceptable pullup value is 1 kΩ resistor.
SSP0_CLK	AD4	VDD33	B_5	N/A	Synchronous serial port 0, clock
SSP0_RXD	AD5	VDD33	I_4	SSP0_CLK	Synchronous serial port 0, receive data in
SSP0_TXD	AB7	VDD33	O_5	SSP0_CLK	Synchronous serial port 0, transmit data out
SSP0_CSZ_0 (1)	AC5	VDD33	B_5	SSP0_CLK	Synchronous serial port 0, chip select 0 (active low)
SSP0_CSZ_1 (1)	AB6	VDD33	B_5	SSP0_CLK	Synchronous serial port 0, chip select 1 (active low)
SSP0_CSZ_2 (1)	AC3	VDD33	B_5	SSP0_CLK	Synchronous serial port 0, chip select 2 (active low)
UART0_TXD	AB3	VDD33	O_5	Async	UART0, UART transmit data output. The firmware only outputs debug messages on this port.
UART0_RXD	AD1	VDD33	I_4	Async	UART0, UART receive data input. The firmware does not support receiving data on this port.
UART0_RTSZ	AD2	VDD33	O_5	Async	UART0, UART ready to send hardware flow control output (active low)
UART0_CTSZ	AE2	VDD33	I_4	Async	UART0, UART clear to send hardware flow control input (active low). This pin requires an external 10 kΩ pulldown resistor.
USB_DAT_N (1) USB_DAT_P	C5 D6	VDD33	B_9	Async	USB D– I/O USB D+ I/O
HOLD_BOOTZ	F24	VDD33	B_2	Async	Boot mode. When this pin is held low, the firmware boots-up in bootload mode. When pin is held high, the firmware boots-up in normal operating mode. This pin requires an external 1 kΩ pullup resistor.
USB_ENZ (1)	E25	VDD33	B_2	Async	The firmware will use this pin to enable an external buffer on the USB data lines after it has completed initialization.
FAULT_STATUS	AC11	VDD33	O_2	Async	This signal toggles or held high to indicate status faults.
HEARTBEAT	AB12	VDD33	O_2	Async	This signal toggles to indicate the system is operational. Period is ~1second.
SEQ_INT2	H26	VDD33	I_2	Async	This signal serves as an interrupt for pattern sequencing and must be connected to SEQ_AUX6.
SEQ_INT1	G26	VDD33	I_2	Async	This signal serves as an interrupt for pattern sequencing and must be connected to SEQ_AUX7.
SEQ_AUX7	F26	VDD33	O_2	Async	This signal serves as an interrupt for pattern sequencing and must be connected to SEQ_INT1.
SEQ_AUX6	E26	VDD33	O_2	Async	This signal serves as an interrupt for pattern sequencing and must be connected to SEQ_INT2.
TEST_FUNC_5 (1)	K22	VDD33	B_2	Async	On DLP® LightCrafter 9000 EVM, this pin connects to FPGA and could serve as a configuration pin. Otherwise can be left unconnected.
TEST_FUNC_4 (1)	J26	VDD33	B_2	Async	On DLP LightCrafter 9000 EVM, this pin connects to FPGA and could serve as a configuration pin. Otherwise can be left unconnected.
TEST_FUNC_3 (1)	J25	VDD33	B_2	Async	On DLP LightCrafter 9000 EVM, this pin connects to FPGA and serves as a configuration pin. This function configures the 24-bit parallel data output of the FPGA to be split between the master and the slave controllers. The firmware will set this pin high by default.
TEST_FUNC_2 (1)	J24	VDD33	B_2	Async	On DLP LightCrafter 9000 EVM, this pin connects to FPGA and could serve as a configuration pin. Otherwise can be left unconnected.
TEST_FUNC_1 (1)	J23	VDD33	B_2	Async	On DLP LightCrafter 9000 EVM, this pin connects to FPGA and could serve as a configuration pin. Otherwise can be left unconnected.

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Peripheral Interface Pin Functions (continued)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
GPIO_08 (1)	E21	VDD33	B_2	Async	This pin can be configured as GPIO 8. An external pullup resistor is required when this pin is configured as open-drain. (2)
GPIO_07 (1)	V23	VDD33	B_2	Async	This pin can be configured as GPIO 7. An external pullup resistor is required when this pin is configured as open-drain. (2)
GPIO_06 (1)	V24	VDD33	B_2	Async	This pin can be configured as GPIO 6. An external pullup resistor is required when this pin is configured as open-drain. (2)
GPIO_05 (1)	U24	VDD33	B_2	Async	This pin can be configured as GPIO 5. An external pullup resistor is required when this pin is configured as open-drain. (2)
GPIO_04 (1)	U25	VDD33	B_2	Async	This pin can be configured as GPIO 4. An external pullup resistor is required when this pin is configured as open-drain. (2)
GPIO_PWM_03 (1)	A23	VDD33	B_2	Async	This pin can be configured as GPIO 3 or PWM 3. An external pullup resistor is required when this pin is configured as open-drain. (2)
GPIO_PWM_02 (1)	A22	VDD33	B_2	Async	This pin can be configured as GPIO 2 or PWM 2. An external pullup resistor is required when this pin is configured as open-drain. (2)
GPIO_PWM_01 (1)	B21	VDD33	B_2	Async	This pin can be configured as GPIO 1 or PWM 1. An external pullup resistor is required when this pin is configured as open-drain. (2)
GPIO_PWM_00 (1)	A21	VDD33	B_2	Async	This pin can be configured as GPIO 0 or PWM 0. An external pullup resistor is required when this pin is configured as open-drain. (2)

(2) GPIO signals must be configured through software for input, output, bidirectional, or open-drain. Some GPIO have one or more alternative use modes, which are also software-configurable. The reset default for all GPIO signals is as an input signal. Refer to the *DLPC900 Programmer's Guide* (DLPU018).

Trigger Control Pin Functions

PIN (1)		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
TRIG_IN_1	AF7	VDD33	I_4	Async	In video pattern mode, this signal is used for advancing the pattern display.
TRIG_IN_2	H25	VDD33	I_2	Async	In video pattern mode, the rising edge of this signal is used for starting the pattern display and the falling edge is used for stopping the pattern display. It works along with the software start stop command.
TRIG_OUT_1	E20	VDD33	O_2	Async	Active high trigger output signal during pattern exposure.
TRIG_OUT_2	D22	VDD33	O_2	Async	Active high trigger output to indicate first pattern display.

(1) These signals do not apply to the slave controller in a two controller system configuration. On the slave controller, these pins are reserved and should be left unconnected. Refer to the *Typical Single Controller Chipset* and the *Typical Two Controller Chipset* for a description between a one controller and a two controller configuration.

LED Control Pin Functions

PIN (1)		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
BLU_LED_PWM	C20	VDD33	O_2	Async	Blue LED PWM current control signal
GRN_LED_PWM	B20	VDD33	O_2	Async	Green LED PWM current control signal
RED_LED_PWM	B19	VDD33	O_2	Async	Red LED PWM current control signal

(1) These signals do not apply to the slave controller in a two controller system configuration. On the slave controller, these pins are reserved and should be left unconnected. Refer to the *Typical Single Controller Chipset* and the *Typical Two Controller Chipset* for a description between a one controller and a two controller configuration.

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LED Control Pin Functions (continued)

PIN (1)		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
BLU_LED_EN	D24	VDD33	O_2	Async	Blue LED enable signal.
GRN_LED_EN	C25	VDD33	O_2	Async	Green LED enable signal.
RED_LED_EN	B26	VDD33	O_2	Async	Red LED enable signal.

Two Controller Support Pin Functions

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION (1)
NAME	NUMBER				
SEQ_SYNC	AB9	VDD33	B_3	Async	Sequence sync. This signal must be connected between the master and slave controller in a two controller configuration. Do not leave unconnected. This pin requires an external 10-kΩ pullup resistor.
SSP0_CSZ4_SLV	U26	VDD33	B_2	SSP0_CLK	This signal is used by the master controller to communicate with the slave controller over the SSP interface. This pin requires an external 4.7-kΩ pullup resistor
FSD12_OUTPUT	T23	VDD33	B_2	Async	This pin must be connected to DA_SYNC_INPUT (2)
DA_SYNC_INPUT	R22	VDD33	B_2	Async	This pin must be connected to FSD12_OUTPUT (3)
SLV_CTRL_PRST	V25	VDD33	B_2	Async	This signal must be connected between the master and slave controller in a two controller configuration. The slave controller will pull this signal high to inform the master controller that it is present and ready. This pin requires an external 10-kΩ pulldown resistor. Do not leave unconnected.
CTRL_MODE_CFG	V26	VDD33	B_2	Async	When this pin is high, the controller operates as the master controller. When this pin is low the controller operates as the slave controller. Use an external 4.7-kΩ pullup or pulldown resistor to identify the controller. Do not leave unconnected.

(1) Refer to the *Typical Single Controller Chipset* and the *Typical Two Controller Chipset* for a description between a one controller and a two controller configuration.
(2) The FSD12_OUTPUT of the slave controller must be left unconnected.
(3) The DA_SYNC_INPUT of the slave controller must be connected to the FSD12_OUTPUT of the master controller.

Reserved Pin Functions

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
AFE_ARSTZ	AC12	VDD33	O_2	Async	Reserved. This pin requires an external 4.7-kΩ pullup resistor.
RESERVED_AD12	AD12	VDD33	O_6	N/A	Reserved. Should be left unconnected.
AFE_IRQ	AB13	VDD33	I_4	Async	Reserved. Should be left unconnected.
RESERVED_AF11	AF11	VDD33	I_4	N/A	Reserved. Should be left unconnected.
RESERVED_AD11	AD11	VDD33	I_4	N/A	Reserved. Should be left unconnected.
RESERVED_AE11	AE11	VDD33	I_4	N/A	Reserved. Should be left unconnected.
RESERVED_AE8	AE8	VDD33	I_4	N/A	Reserved. This pin requires an external 10-kΩ pullup resistor.
RESERVED_AD8	AD8	VDD33	O_5	N/A	Reserved. Should be left unconnected.
RESERVED_AC9	AC9	VDD33	O_5	N/A	Reserved. Should be left unconnected.
RESERVED_AF8	AF8	VDD33	I_4	N/A	Reserved. This pin Requires an external 10-kΩ pulldown resistor.
RESERVED_E3	E3	VDD33	B_5	N/A	Reserved. Should be left unconnected.
RESERVED_AB10	AB10	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_AD9	AD9	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_AE9	AE9	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_AF9	AF9	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_AB11	AB11	VDD33	B_2	N/A	Reserved. Should be left unconnected.

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Reserved Pin Functions (continued)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
RESERVED_AC10	AC10	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_AD10	AD10	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_AE10	AE10	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_AF10	AF10	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_K24	K24	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_K23	K23	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_J22	J22	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_H24	H24	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_H23	H23	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_H22	H22	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_G25	G25	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_F25	F25	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_G24	G24	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_G23	G23	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_T22	T22	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_U23	U23	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_G22	G22	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_F23	F23	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_D26	D26	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_E24	E24	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_F22	F22	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_D25	D25	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_E23	E23	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_C26	C26	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_AB4	AB4	VDD33	B_5	N/A	Reserved. Should be left unconnected.
RESERVED_C23	C23	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_D21	D21	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_B24	B24	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_C22	C22	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_B23	B23	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_A20	A20	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_A19	A19	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_E18	E18	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_D19	D19	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_C19	C19	VDD33	B_2	N/A	Reserved. Should be left unconnected.
RESERVED_E8	E8	VDD33	B_2 D	N/A	Reserved. Should be left unconnected.
RESERVED_B4	B4	VDD33	B_2 D	N/A	Reserved. Should be left unconnected.
RESERVED_C4	C4	VDD33	B_2 D	N/A	Reserved. Should be left unconnected.
RESERVED_E7	E7	VDD33	B_2 D	N/A	Reserved. Should be left unconnected.
RESERVED_D5	D5	VDD33	B_2 D	N/A	Reserved. Should be left unconnected.
RESERVED_E6	E6	VDD33	B_2 D	N/A	Reserved. Should be left unconnected.

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Reserved Pin Functions (continued)

PIN		I/O POWER	I/O TYPE	CLK SYSTEM	DESCRIPTION
NAME	NUMBER				
RESERVED_D3	D3	VDD33	B_2 D	N/A	Reserved. Should be left unconnected.
RESERVED_C2	C2	VDD33	B_2 D	N/A	Reserved. Should be left unconnected.
RESERVED_A4	A4	VDD33	B_2 D	N/A	Reserved. Should be left unconnected.
RESERVED_B5	B5	VDD33	B_2 D	N/A	Reserved. Should be left unconnected.
RESERVED_C6	C6	VDD33	B_2 D	N/A	Reserved. Should be left unconnected.
RESERVED_A5	A5	VDD33	B_2 D	N/A	Reserved. Should be left unconnected.
RESERVED_D7	D7	VDD33	B_2 D	N/A	Reserved. Should be left unconnected.

Power and Ground Pin Functions

PIN		I/O TYPE	DESCRIPTION
NAME	NUMBER		
VDD33	F20, F17, F11, F8, L21, R21, Y21, AA19, AA16, AA10, AA7	PWR	3.3-V I/O power
VDD18	C1, F5, G6, K6, M5, P5, T5, W6, AA5, AE1, H5, N6, T6, AA13, U21, P21, H21, F14	PWR	1.8-V internal DRAMVDD and LVDSAVD I/O power (To shut this power down in a system low-power mode, see the *System Power-Up Sequence*.)
VDDC	F19, F16, F13, F10, F7, H6, L6, P6, U6, Y6, AA8, AA11, AA14, AA17, AA20, W21, T21, N21, K21, G21, L11, T11, T16, L16	PWR	1.15-V core power
PLLD_VDD	L22	PWR	1.15-V DMD clock generator PLL Digital power
PLLD_VSS	L23	GND	1.15-V DMD clock generator PLL Digital GND
PLLD_VAD	K25	PWR	1.8-V DMD clock generator PLL Analog power
PLLD_VAS	K26	GND	1.8-V DMD clock generator PLL Analog GND
PLLM1_VDD	L26	PWR	1.15-V master-LS clock generator PLL Digital power
PLLM1_VSS	M22	GND	1.15-V master-LS clock generator PLL Digital GND
PLLM1_VAD	L24	PWR	1.8-V master-LS clock generator PLL Analog power
PLLM1_VAS	L25	GND	1.8-V master-LS clock generator PLL Analog GND
PLLM2_VDD	P23	PWR	1.15-V master-HS clock generator PLL Digital power
PLLM2_VSS	P24	GND	1.15-V master-HS clock generator PLL Digital GND
PLLM2_VAD	R25	PWR	1.8-V master-HS clock generator PLL Analog power
PLLM2_VAS	R26	GND	1.8-V master-HS clock generator PLL Analog GND
PLLS_VAD	R23	PWR	1.15-V video-2X clock generator PLL Analog power

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Power and Ground Pin Functions (continued)

PIN		I/O TYPE	DESCRIPTION
NAME	NUMBER		
PLLS_VAS	R24	GND	1.15-V video-2X clock generator PLL Analog GND
L_VDQPAD_[7:0], R_VDQPAD_[7:0]	B18, D18, B17, E17, A18, C18, A17, D17, AE17, AC17, AF17, AC18, AB16, AD17, AB17, AD18	RES	DRAM direct test pins (for manufacturing use only). These pins should be tied directly to ground for normal operation.
CFO_VDD33	AE26	RES	DRAM direct test control pin (for manufacturing use only). This pin should be tied directly to 3.3 I/O power (VDD33) for normal operation.
VTEST1, VTEST2, VTEST3, VTEST4	AB14, AB15, E15, E16	RES	DRAM direct test control pins (for manufacturing use only). These pins should be tied directly to ground for normal operation.
LVDS_AVS1, LVDS_AVS2	V5, K5	PWR	Dedicated ground for LVDS bandgap reference. These pins should be tied directly to ground for normal operation.
VPGM	AC6	PWR	Fuse programming pin (for manufacturing use only). This pin should be tied directly to ground for normal operation.
GND	A26, A25, A24, B25, C24, D23, E22, F21, F18, F15, F12, F9, F6, E5, D4, C3, B3, A3, B2, A2, B1, A1, G5, J5, J6, L5, M6, N5, R5, R6, U5, V6, W5, Y5, AA6, AB5, AC4, AD3, AE3, AF3, AF2, AF1, AA9, AA12, AA15, AA18, AA21, AB22, AC23, AD24, AE24, AF24, AE25, AF25, AF26, V21, M21, J21, L15, L14, L13, L12, M16, M15, M14, M13, M12, M11, N16, N15, N14, N13, N12, N11, P16, P15, P14, P13, P12, P11, R16, R15, R14, R13, R12, R11, T15, T14, T13, T12	GND	Common ground

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Table 1. I/O Type and Subscript Definition (1)

I/O		ESD STRUCTURE
(SUBSCRIPT)	**DESCRIPTION**	
1	N/A	N/A
2	3.3 LVTTL I/O buffer, with 8-mA drive	ESD diode to V_{DD33} and GND
3	3.3 LVTTL I/O buffer, with 12-mA drive	
4	3.3 LVTTL receiver	
5	3.3 LVTTL I/O buffer, with 8-mA drive, with slew rate control	
6	3.3 LVTTL I/O buffer, with programmable 4-, 8-, or 12-mA drive	
7	1.8-V LVDS (DMD interface)	
8	3.3-V I^2C with 3-mA sink	
9	USB-compatible (3.3 V)	
10	OSC 3.3-V I/O compatible LVTTL	
(TYPE)		N/A
I	Input	
O	Output	
B	Bidirectional	
H	Hysteresis	
U	Includes an internal termination pullup resistor	
D	Includes an internal termination pulldown resistor	

(1) Refer to the *General Handling Guidelines for Unused CMOS-Type Pins* for instructions on handling unused pins

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature (unless otherwise noted) (see(1))

			MIN	MAX	UNIT
	Supply voltage (2) (3)	VDDC (core)	–0.3	1.6	V
		VDD18 (LVDSAVD I/O and internal DRAMVDD)	–0.3	2.5	
		VDD33 (I/O)	–0.3	3.9	
		PLLD_VDD (1.15 V DMD clock generator – digital)	–0.3	1.6	
		PLLM1_VDD (1.15 V master-LS clock generator – digital)	–0.3	1.6	
		PLLM2_VDD (1.15 V master-HS clock generator – digital)	–0.3	1.6	
		PLLD_VAD (1.8 V DMD clock generator – analog)	–0.3	2.5	
		PLLM1_VAD (1.8 V master-LS clock generator – analog)	–0.3	2.5	
		PLLM2_VAD (1.8 V master-HS clock generator – analog)	–0.3	2.5	
		PLLS_VAD (1.15 V video-2X – analog)	–0.5	1.4	
V_I	Input voltage (4)	USB	–1	5.25	V
		OSC	–0.3	VDD33 + 0.3 V	
		3.3 LVTTL	–0.3	3.6	
		3.3 I^2C	–0.5	3.8	
V_O	Output voltage	USB	–1	5.25	V
		1.8 LVDS	–0.3	2.2	
		3.3 LVTTL	–0.3	3.6	
		3.3 I^2C	–0.5	3.8	
T_J	Operating junction temperature		0	111	°C
T_{stg}	Storage temperature		–40	125	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) All voltage values are with respect to GND.
(3) All of the 3.3-, 1.8-, and 1.15-V power should be applied and removed per the procedure defined in *System Power-Up Sequence*. Overlap currents, if allowed to continue flowing unchecked not only increase total power dissipation in a circuit, but degrade the circuit reliability, thus shortening its usual operating life.
(4) Applies to external input and bidirectional buffers.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001, all pins (1)	±2000	V
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins (2)	±300	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

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6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted). The functional performance of the device specified in this data sheet is achieved when operating the device by the Recommended Operating Conditions. No level of performance is implied when operating the device above or below the Recommended Operating Conditions limits.

		I/O (1)	MIN	NOM	MAX	UNIT
$V_{DD}33$	3.3 V supply voltage, I/O		3.135	3.3	3.465	V
$V_{DD}18$	1.8 V supply voltage, LVDSAVD and DRAMVDD		1.71	1.8	1.89	
VDDC	1.15 V supply voltage, Core logic		1.100	1.15	1.200	
PLLD_V_{DD}	1.8 V supply voltage, PLL analog		1.71	1.8	1.89	
PLLM1_V_{DD}	1.8 V supply voltage, PLL analog		1.71	1.8	1.89	
PLLM2_V_{DD}	1.8 V supply voltage, PLL analog		1.71	1.8	1.89	
PLLS_V_{DD}	1.15 V supply voltage, PLL analog		1.090	1.15	1.200	
PLLD_V_{DD}	1.15 V supply voltage, PLL digital		1.090	1.15	1.200	
PLLM1_V_{DD}	1.15 V supply voltage, PLL digital		1.090	1.15	1.200	
PLLM2_V_{DD}	1.15 V supply voltage, PLL digital		1.090	1.15	1.200	
V_I	Input voltage	USB (9)	0		VDD33	V
		OSC (10)	0		VDD33	
		3.3 V LVTTL (1, 2, 3, 4)	0		VDD33	
		3.3 V I^2C (8)	0		VDD33	
V_O	Output voltage	USB (8)	0		VDD33	V
		3.3 V LVTTL (1, 2, 3, 4)	0		VDD33	
		3.3 V I^2C (8)	0		VDD33	
		1.8 V LVDS (7)	0		VDD18	
T_A	Operating ambient temperature range	See (2) and (3)	0		55	°C
T_C	Operating top-center case temperature	See (3) and (4)	0		109.16	°C
T_J	Operating junction temperature		0		111	°C

(1) The number inside the parentheses for the I/O refers to the I/O type defined in Table 1.
(2) Assumes minimum 1 m/s airflow.
(3) Maximum thermal values assume max power of 4.76 W (total for controller).
(4) Assume φ_{JT} equals 0.4°C/W.

6.4 Thermal Information

THERMAL METRIC		DLPC900 ZPC (BGA) 516 PINS	UNIT
$R_{\theta JC}$ (1)	Junction-to-air thermal resistance	4.4	°C/W
$R_{\theta JA}$ at 0 m/s of forced airflow (2)	Junction-to-air thermal resistance	14.4	°C/W
$R_{\theta JA}$ at 1 m/s of forced airflow (2)	Junction-to-air thermal resistance	9.5	°C/W
$R_{\theta JA}$ at 2 m/s of forced airflow (2)	Junction-to-air thermal resistance	9.0	°C/W
φ_{JT} (3)	Temperature variance from junction to package top center temperature, per unit power dissipation	0.4	°C/W

(1) $R_{\theta JC}$ analysis assumptions: The heat generated in the chip flows into overmold (top side) and also into the package laminate (bottom side) and then into PCB via package solder balls. Should be used for heat sink analysis only.
(2) Thermal coefficients abide by JEDEC Standard 51. $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC900 PCB and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance.
(3) Example: (3.2 W) × (0.4 C/W) ≈ 1.28°C temperature rise.

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6.5 Electrical Characteristics

over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)			TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
V_{IH}	High-level input threshold voltage	USB (9)		2			V
		OSC (10)		2			
		3.3-V LVTTL (1, 2, 3, 4)		2			
		3.3-V I^2C (8)		2.4		VDD33 + 0.5	
V_{IL}	Low-level input threshold voltage	USB (9)				0.8	V
		OSC (10)				0.8	
		3.3-V LVTTL (1, 2, 3, 4)				0.8	
		3.3-V I^2C (8)		–0.5		1	
V_{DIS}	Differential input sensitivity (Differential input voltage)	USB (9)		200			mV
V_{ICM}	Input common mode range (Differential cross point voltage)	USB (9)		0.8		2.5	V
V_{OH}	High-level output voltage	USB (9)		2.8			V
		1.8-V LVDS (7)		1.52			
		3.3-V LVTTL (1, 2, 3)	I_{OH} = Max rated	2.7			
V_{OL}	Low-level output voltage	USB (9)		0		0.3	V
		1.8-V LVDS (7)				0.88	
		3.3-V LVTTL (1, 2, 3)	I_{OL} = Max rated			0.4	
		3.3-V I^2C (8)	I_{OL} = 3-mA sink			0.4	
V_{OD}	Output differential voltage	1.8-V LVDS (7)		0.065		0.44	V
I_{IH}	High-level input current	USB (9)				200	µA
		OSC (10)		–10		10	
		3.3-V LVTTL (1 to 4) (without internal pulldown)	V_{IH} = VDD33	–10		10	
		3.3-V LVTTL (1 to 4) (with internal pulldown)	V_{IH} = VDD33	10		200	
		3.3-V I^2C (8)	V_{IH} = VDD33			10	
I_{IL}	Low-level input current	USB (9)		–10		10	µA
		OSC (10)		–10		10	
		3.3-V LVTTL (1-4) (without internal pullup)	V_{OH} = VDD33	–10		10	
		3.3-V LVTTL (1-4) (with internal pullup)	V_{OH} = VDD33	–10		–200	
		3.3-V I^2C (8)	V_{OH} = VDD33			–10	

(1) The number inside the parentheses for the I/O refers to the I/O type defined in Table 1.
(2) Normal mode refers to DLPC900 operation during full functionality. Typical values correspond to power dissipated on nominal process devices operating at nominal voltage and 70°C junction temperature (approximately 25°C ambient) displaying typical video-graphics content from a high-frequency source. Max values correspond to power dissipated on fast-process devices operating at high voltage and 105°C junction temperature (approximately 55°C ambient) displaying typical video-graphics content from a high-frequency source. The increased power dissipation observed on fast-process devices operated at max recommended temperature is primarily a result of increased leakage current.

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)			TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
I_{OH}	High-level output current (3)	USB (9)		–18.4			mA
		1.8-V LVDS (7) (V_{OD} = 300 mV)	VO = 1.4 V	–6.5			
		3.3-V LVTTL (1)	VO = 2.4 V	–4			
		3.3-V LVTTL (2)	VO = 2.4 V	–8			
		3.3-V LVTTL (3)	VO = 2.4 V	–12			
I_{OL}	Low-level output current (4)	USB (9)		19.1			mA
		1.8-V LVDS (7) (V_{OD} = 300 mV)	VO = 1 V	6.5			
		3.3-V LVTTL (1)	VO = 0.4 V	4			
		3.3-V LVTTL (2)	VO = 0.4 V	8			
		3.3-V LVTTL (3)	VO = 0.4 V	12			
		3.3-V I2C (8)		3			
I_{OZ}	High-impedance leakage current	USB (9)		–10		10	µA
		LVDS (7)		–10		10	
		3.3-V LVTTL (1, 2, 3)		–10		10	
		3.3-V I^2C (8)		–10		10	
C_I	Input capacitance (including package)	USB (9)		11.84		17.07	pF
		3.3-V LVTTL (1)		3.75		5.52	
		3.3-V LVTTL (2)		3.75		5.52	
		3.3-V LVTTL (4)		3.75		5.52	
		3.3-V I^2C (8)		5.26		6.54	

(3) VDDQ = 1.7 V; VOUT = 1420 mV. (VOUT – VDDQ) / I_{OH} must be < 21 Ω for values of VOUT between VDDQ and VDDQ – 280 mV.
(4) VDDQ = 1.7 V; VOUT = 280 mV. VOUT / I_{OL} must be < 21 Ω for values of VOUT between 0 V and 280 mV.

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Electrical Characteristics (continued)

over operating free-air temperature range (unless otherwise noted)

PARAMETER (1)		TEST CONDITIONS (2)	MIN	TYP	MAX	UNIT
I_{CC11}	Supply voltage, 1.15-V core power	Normal mode			2368	mA
I_{CC18}	Supply voltage, 1.8-V power (LVDS I/O and internal DRAM)	Normal mode			1005	mA
I_{CC33}	Supply voltage, 3.3-V I/O power	Normal mode			33	mA
I_{CC11_PLLD}	Supply voltage, DMD PLL digital power (1.15 V)	Normal mode		4.4	6.2	mA
I_{CC11_PLLM1}	Supply voltage, master-LS clock generator PLL digital power (1.15 V)	Normal mode		4.4	6.2	mA
I_{CC11_PLLM2}	Supply voltage, master-HS clock generator PLL digital power (1.15 V)	Normal mode		4.4	6.2	mA
I_{CC18_PLLD}	Supply voltage, DMD PLL analog power (1.8 V)	Normal mode		8	10.2	mA
I_{CC18_PLLM1}	Supply voltage, master-LS clock generator PLL analog power (1.8 V)	Normal mode		8	10.2	mA
I_{CC18_PLLM2}	Supply voltage, master-HS clock generator PLL analog power (1.8 V)	Normal mode		8	10.2	mA
I_{CC11_PLLS}	Supply voltage, video-2X PLL analog power (1.15 V)	Normal mode			2.9	mA
Total Power in Normal Mode					4.76	W

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6.6 System Oscillators Timing Requirements (1)

			MIN	MAX	UNIT
f_{clock}	Clock frequency, MOSC1 Stability and Tolerance. Crystal frequency 20MHz. (2)		19.998 100	20.002 100	MHz ppm
t_c	Cycle time, MOSC1		49.995	50.005	ns
$t_{w(H)}$	Pulse duration2, MOSC, high	50% to 50% reference points (signal)	20		ns
$t_{w(L)}$	Pulse duration2, MOSC, low	50% to 50% reference points (signal)	20		ns
t_t	Transition time2, MOSC, $t_t = t_f / t_r$	20% to 80% reference points (signal)		12	ns
t_{jp}	Period jitter2, MOSC (The deviation in period from ideal period due solely to high-frequency jitter – not spread spectrum clocking)			18	ps

(1) Applies only when driven through an external digital oscillator. The MOSC input cannot support spread spectrum clock spreading.
(2) Including impact to accuracy due to aging, temperature, and trim sensitivity.

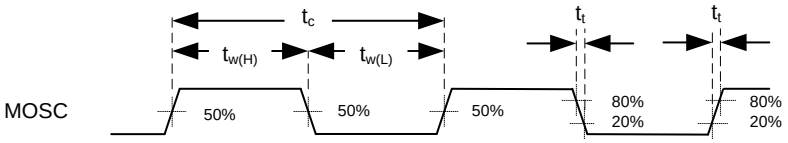
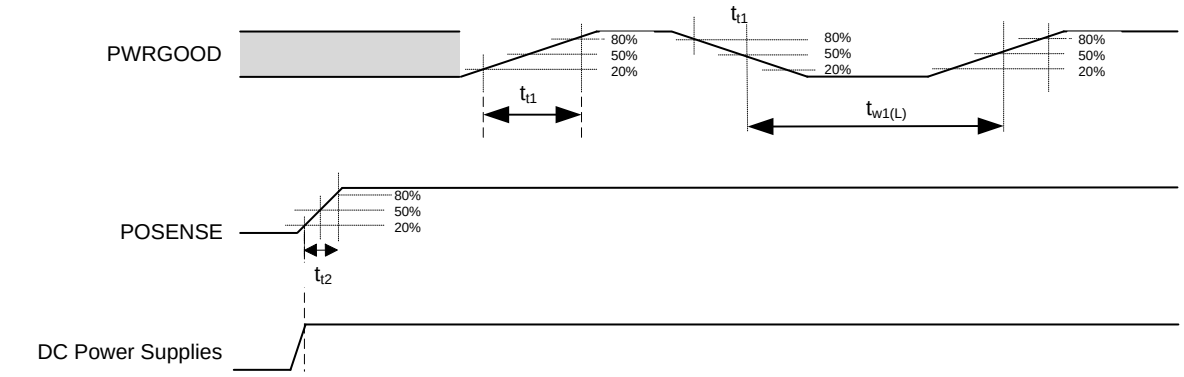


Figure 1. System Oscillators

6.7 Reset Timing Requirements

			MIN	MAX	UNIT
$t_{w1(L)}$	Pulse duration, inactive low, PWRGOOD	50% to 50% reference points (signal)	4		µs
$t_{w1(L)}$	Pulse duration, inactive low, PWRGOOD	50% to 50% reference points (signal)		1000	ms
t_{t1}	Transition time, PWRGOOD, $t_{t1} = t_f / t_r$	20% to 80% reference points (signal)		625	µs
$t_{w2(L)}$	Pulse duration, inactive low, POSENSE	50% to 50% reference points (signal)	500		µs
$t_{w2(L)}$	Pulse duration, inactive low, POSENSE	50% to 50% reference points (signal)		1000	ms
t_{t2}	Transition time, POSENSE, $t_{t2} = t_f / t_r$	20% to 80% reference points (signal)		25 (1)	µs
t_{PH}	Power hold time, POSENSE remains active after PWGOOD is deasserted.	20% to 80% reference points (signal)	500		µs
t_{EW}	Early warning time, PWRGOOD goes inactive low before any power supply voltage goes below its specification		500		µs
$t_{w1(L)} + t_{w2(L)}$	The sum of PWRGOOD and POSENSE inactive time			1050	ms

(1) As long as noise on this signal is below the hysteresis threshold.



A. PWRGOOD has no impact on operation for 60 ms after rising edge of POSENSE.

Figure 2. Power Up

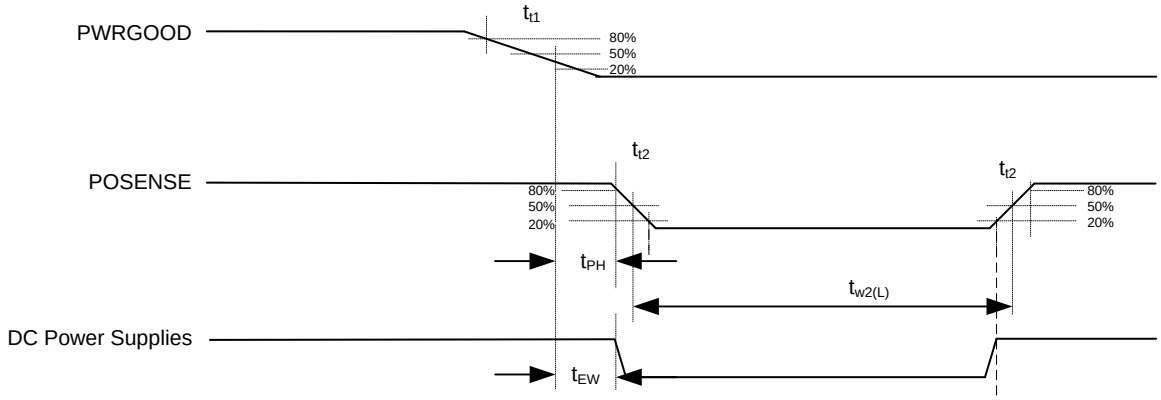


Figure 3. Power Down

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6.8 JTAG Interface: I/O Boundary Scan Application Timing Requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency, TCK			10	MHz
t_c	Cycle time, TCK		100		ns
$t_{w(H)}$	Pulse duration, high	50% to 50% reference points (signal)	40		ns
$t_{w(L)}$	Pulse duration, low	50% to 50% reference points (signal)	40		ns
t_t	Transition time, $t_t = t_f / t_r$	20% to 80% reference points (signal)		5	ns
t_{su}	Setup time, TDI valid before TCK↑		8		ns
t_h	Hold time, TDI valid after TCK↑		2		ns
t_{su}	Setup time, TMS1 valid before TCK↑		8		ns
t_h	Hold time, TMS1 valid after TCK↑		2		ns

6.9 JTAG Interface: I/O Boundary Scan Application Switching Characteristics

Switching characteristics over recommended operating conditions, C_L (min timing) = 5 pF, C_L (max timing) = 85 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
t_{pd}	Output propagation, clock to Q	TCK↑	TDO1	3	12	ns

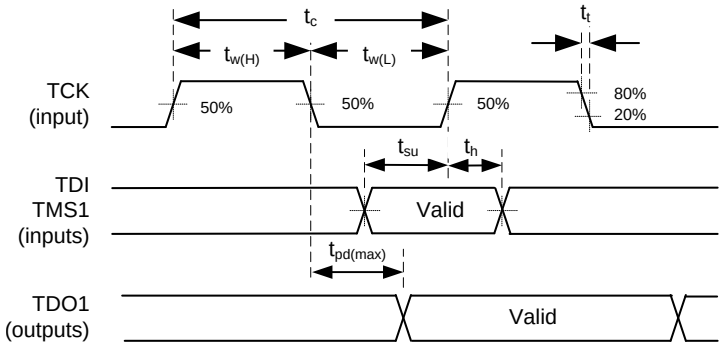

Figure 4. I/O Boundary Scan

6.10 Programmable Output Clocks Switching Characteristics

Switching characteristics over recommended operating conditions, C_L (min timing) = 5 pF, C_L (max timing) = 50 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock}	Clock frequency, OCLKA1 (1)	N/A	OCLKA	0.787	50.00	MHz
t_c	Cycle time, OCLKA	N/A	OCLKA	20.00	1270.6	ns
$t_w(H)$	Pulse duration, high2 (2) 50% to 50% reference points (signal)	N/A	OCLKA	$(t_c / 2) – 2$		ns
$t_w(L)$	Pulse duration, low2 50% to 50% reference points (signal)	N/A	OCLKA	$(t_c / 2) – 2$		ns
	Jitter	N/A	OCLKA		350	ps

(1) The frequency of OCLKA is programmable.
(2) The duty cycle of OCLKA will be within ±2 ns of 50%.

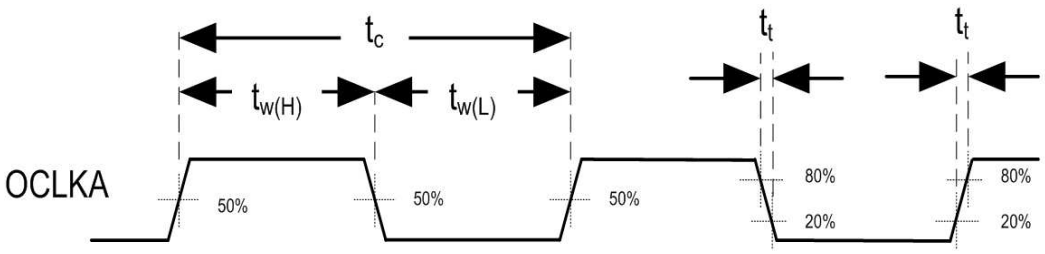

Figure 5. Programmable Output Clocks

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6.11 Port 1 and 2 Input Pixel Interface Timing Requirements

			MIN	MAX	UNIT
f_{clock}	Clock frequency, P_CLK1, P_CLK2, P_CLK3 (24-bit bus (1))		12	175	MHz
f_{clock}	Clock frequency, P_CLK1, P_CLK2, P_CLK3 (48-bit bus (1)) See *Two Pixels Per Clock (48-bit Bus) Timing Requirements* .		12	141	MHz
t_c	Cycle time, P_CLK1, P_CLK2, P_CLK3		5.714	83.33	ns
$t_{w(H)}$	Pulse duration, high	50% to 50% reference points (signal)	2.3		ns
$t_{w(L)}$	Pulse duration, low	50% to 50% reference points (signal)	2.3		ns
t_{jp}	Clock period jitter P_CLK1, P_CLK2, P_CLK3 (that is, the deviation in period from ideal period)	Max f_{clock}		See (2)	ps
t_t	Transition time, $t_t = t_f / t_r$, P_CLK1, P_CLK2, P_CLK3	20% to 80% reference points (signal)	0.6	2.0	ns
t_t	Transition time, $t_t = t_f / t_r$, P1_A(9:0), P1_B(9:0) , P1_C(9:0), P1_HSYNC, P1_VSYNC, P1_DATEN	20% to 80% reference points (signal)	0.6	3.0	ns
t_t	Transition time, $t_t = t_f / t_r$	20% to 80% reference points (signal)	0.6	3.0	ns
t_{su}	Setup time, P1_A(9:0), valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_h	Hold time, P1_A(9:0), valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_{su}	Setup time, P1_B(9:0), valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_h	Hold time, P1_B(9:0), valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_{su}	Setup time, P1_C(9:0), valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_h	Hold time, P1_C(9:0), valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_{su}	Setup time, P1_VSYNC, valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_h	Hold time, P1_VSYNC, valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_{su}	Setup time, P1_HSYNC, valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_h	Hold time, P1_HSYNC, valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_{su}	Setup time, P2_A(9:0), valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_h	Hold time, P2_A(9:0), valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_{su}	Setup time, P2_B(9:0), valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_h	Hold time, P2_B(9:0), valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_{su}	Setup time, P2_C(9:0), valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_h	Hold time, P2_C(9:0), valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_{su}	Setup time, P2_VSYNC, valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_h	Hold time, P2_VSYNC, valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_{su}	Setup time, P2_HSYNC, valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_h	Hold time, P2_HSYNC, valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_{su}	Setup time, P_DATEN1, valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_h	Hold time, P_DATEN1, valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_{su}	Setup time, P_DATEN2, valid before P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_h	Hold time, P_DATEN2, valid after P_CLK1, P_CLK2, or P_CLK3.		0.8		ns
t_w(A)	VSYNC active pulse duration		1		Video line
t_w(A)	HSYNC active pulse duration		16		Pixel clocks

(1) Ports 1 and 2 are both 30-bit buses, but only 24-bits are used
(2) For frequencies (f_{clock}) less than 175 MHz, use the following formula to obtain the jitter: Max clock jitter = ± [(1 / f_{clock}) – 5414 ps].

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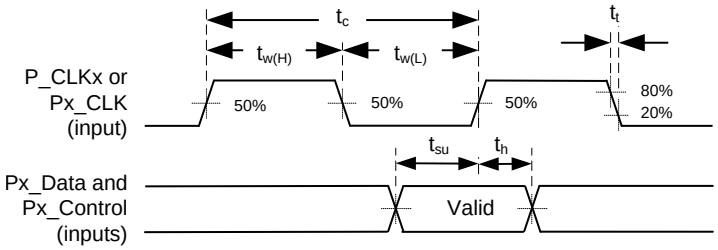

Figure 6. Input Port 1 and 2 Interface

6.12 Two Pixels Per Clock (48-bit Bus) Timing Requirements

When operating in two pixels per clock mode, the pixel clock must be maintained below 141MHz. A typical video source requiring two pixels per clock is shown in the following table and must have reduced blanking to stay below the maximum pixel clock.

SOURCE	RATE (Hz)	TOTAL PIXELS PER LINE (1)	TOTAL LINES PER FRAME (1)	PIXEL CLOCK ACHIEVED (MHz)
1080p	120	2060	1120	138.4

(1) Values chosen for front and back porches must meet the timing requirements in *Source Input Blanking Requirements* .

6.13 SSP Switching Characteristics

Switching characteristics over recommended operating conditions, C_L (min timing) = 5 pF, C_L (max timing) = 50 pF (unless otherwise noted)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock}	Clock frequency, SSPx_CLK	N/A	SSPx_CLK	73.00	25000	kHz
t_c	Cycle time, SSPx_CLK	N/A	SSPx_CLK	0.040	13.6	µs
$t_w(H)$	Pulse duration, high 50% to 50% reference points (signal)	N/A	SSPx_CLK	40%		
$t_w(L)$	Pulse duration, low 50% to 50% reference points (signal)	N/A	SSPx_CLK	40%		
SSP MASTER						
t_{pd}	Output propagation, clock to Q, SSPx_DO	SSPx_CLK↓ (1) (2)	SSPx_DO (1) (2)	–5	5	ns
		SSPx_CLK↑ (1) (3)	SSPx_DO (1) (3)	–5	5	ns
SSP SLAVE						
t_{pd}	Output propagation, clock to Q, SSPx_DO	SSPx_CLK↓ (1) (2)	SSPx_DO (1) (2)	0	34	ns
		SSPx_CLK↑ (1) (3)	SSPx_DO (1) (3)	0	34	ns

(1) The SSP is configured into four different modes of operation by the controller firmware. These modes are shown in Table 2, Figure 8, and Figure 9.
(2) Modes 0 and 3
(3) Modes 1 and 2

Table 2. SSP Clock Operational Modes

SPI CLOCKING MODE	SPI CLOCK POLARITY (CPOL)	SPI CLOCK PHASE (CPHA)
0	0	0
1	0	1
2	1	0
3	1	1

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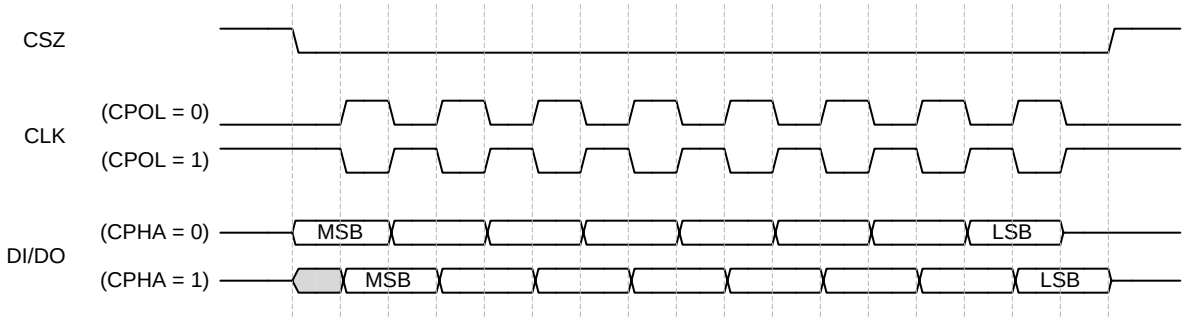

Figure 7. SSP Clock Mode Timing Diagram

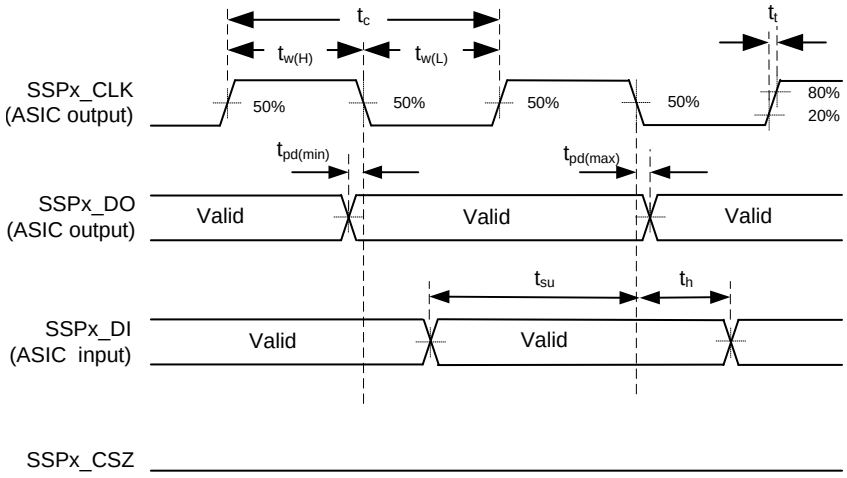

Figure 8. Synchronous Serial Port Interface – Master (Modes 0/3)

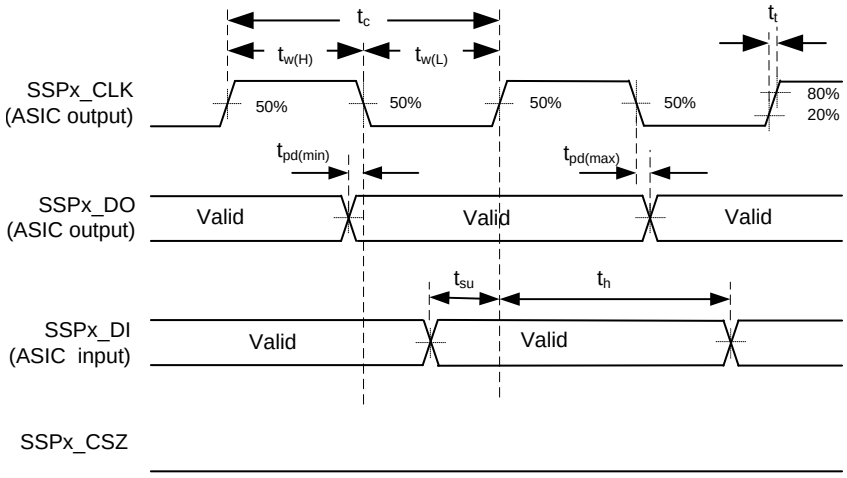

Figure 9. Synchronous Serial Port Interface – Slave (Modes 0/3)

6.14 DMD Interface Switching Characteristics (1)

over recommended operating conditions, C_L (min timing) = 5 pF, C_L (max timing) = 50 pF (unless otherwise noted)

PARAMETER		FROM	TO	MIN	MAX	UNIT
DMD TIMING MODE 0 (2)						
$t_{w(H)}$	DMD strobe high pulse duration	N/A	DADSTRB	29		ns
$t_{w(L)}$	DMD strobe low pulse duration	N/A	DADSTRB	29		ns
$T_{odv\text{-}min}$	Output data valid window, DADADDR_(3:0), DADMODE_(1:0), DADSEL_(1:0) with respect to DADSTRB	DADADDR_(3:0) DADMODE_(1:0) DADSEL_(1:0)	DADSTRB↑ (1)	–27		ns
$T_{odv\text{-}max}$	Output data valid window, DADADDR_(3:0), DADMODE_(1:0), DADSEL_(1:0) with respect to DADSTRB	DADADDR_(3:0) DADMODE_(1:0) DADSEL_(1:0)	DADSTRB↑ (1)	27		ns
DMD TIMING MODE 1 (2)						
t_w(H)	DMD strobe pulse duration	N/A	DADSTRB	14		ns
t_w(L)	DMD strobe low pulse duration	N/A	DADSTRB	14		ns
$T_{odv\text{-}min}$	Output data valid window, DADADDR_(3:0), DADMODE_(1:0), DADSEL_(1:0) with respect to DADSTRB	DADADDR_(3:0) DADMODE_(1:0) DADSEL_(1:0)	DADSTRB↑ (1)	–12		ns
$T_{odv\text{-}max}$	Output data valid window, DADADDR_(3:0), DADMODE_(1:0), DADSEL_(1:0) with respect to DADSTRB	DADADDR_(3:0) DADMODE_(1:0) DADSEL_(1:0)	DADSTRB↑ (1)	12		ns

(1) DMD control signals are captured on the rising edge of DADSTRB within the DMD.
(2) The DMD timing mode is controlled by the controller firmware.

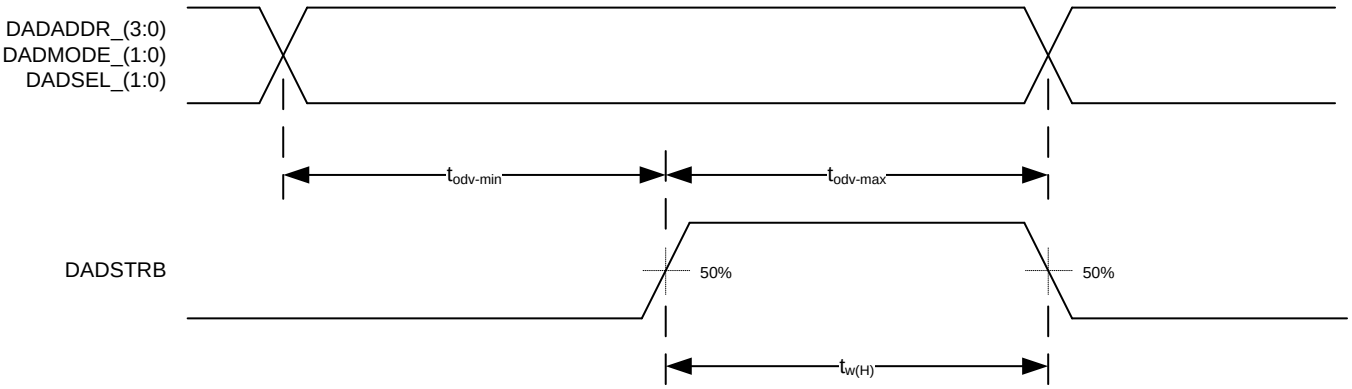

Figure 10. DMD Interface Timing

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6.15 DMD LVDS Interface Switching Characteristics

Switching characteristics over recommended operating conditions (1) (2) (3) (4) (5) (6)

PARAMETER		FROM (INPUT)	TO (OUTPUT)	MIN	MAX	UNIT
f_{clock}	Clock frequency, DCK_A	N/A	DCK_A	100	400	MHz
t_c	Cycle time, DCK_A1	N/A	DCK_A	2475.3		ps
$t_{w(H)}$	Pulse duration, high 5 (50% to 50% reference points)	N/A	DCK_A	1093		ps
$t_{w(L)}$	Pulse duration, low 5 (50% to 50% reference points)	N/A	DCK_A	1093		ps
t_t	Transition time, $t_t = t_f$ / t_r (20% to 80% reference points)	N/A	DCK_A	100	400	ps
t_{osu}	Output setup time at max clock rate3	DCK_A↑↓	SCA, DDA(15:0)	438		ps
t_{oh}	Output hold time at max clock rate3	DCK_A↑↓	SCA, DDA(15:0)	438		ps
f_{clock}	Clock frequency, DCK_B	N/A	DCK_B	100	400	MHz
t_c	Cycle time, DCK_B1	N/A	DCK_B	2475.3		ps
$t_{w(H)}$	Pulse duration, high 5 (50% to 50% reference points)	N/A	DCK_B	1093		ps
$t_{w(L)}$	Pulse duration, low 5 (50% to 50% reference points)	N/A	DCK_B	1093		ps
t_t	Transition time, $t_t = t_f$ / t_r (20% to 80% reference points)	N/A	DCK_B	100	400	ps
t_{osu}	Output setup time at max clock rate3	DCK_B↑↓	SCB, DDB(15:0)	438		ps
t_{oh}	Output hold time at max clock rate3	DCK_B↑↓	SCB, DDB(15:0)	438		ps
t_{sk}	Output skew, channel A to channel B	DCK_A↑	DCK_B↑		250	ps

(1) The minimum cycle time (t_c) for DCK_A and DCK_B includes 1.0% spread spectrum modulation.
(2) The DMD LVDS interface uses a double data rate (DDR) clock, thus both rising and falling edges of DCK_A and DCK_B are used to clock data into the DMD. As a result, the minimum $t_{w(H)}$ and $t_{w(L)}$ parameters determine the worse-case DDR clock cycle time.
(3) Output setup and hold times for DMD clock frequencies below the maximum can be calculated as follows: $t_{osu}(f_{clock}) = t_{osu}(f_{max}) + 250000 \times (1 / f_{clock} - 1 / 400)$ and $t_{oh}(f_{clock}) = t_{oh}(f_{max}) + 250000 \times (1 / f_{clock} - 1 / 400)$ where f_{clock} is in MHz.
(4) The DLPC900 is a Full-Bus DMD signaling interface. Figure 15 shows the controller connections for this configuration.
(5) The pulse duration minimum for any clock rate can be calculated using the following formulas.
  (a) Pulse duration minimum when using spread spectrum
    (a) Duty cycle % = 49.06 – [0.01335 × clock frequency (MHz)]
    (b) Minimum pulse duration = 1 / clock frequency × DC%
      (a) Example: At 400 MHz: DC% = 49.06 – [0.01335 × 400] = 43.72%
      (b) MPW = 1 / 400 MHz × 0.4372 = 1093.0 ps
  (b) Pulse duration minimum when not using spread spectrum
    (a) Duty cycle % = 49.00 – [0.01055 × clock frequency (MHz)]
    (b) Minimum pulse duration = 1 / clock frequency × DC%
      (a) Example: At 400 MHz: DC% = 49.00 – [0.01055 × 400] = 44.78%
      (b) MPW = 1 / 400 MHz × 0.448 = 1119.5 ps
(6) A duty cycle specification is not provided because the key limiting factor to clock frequency is the minimum pulse duration (that is, if the other half of the clock period is larger than the minimum, it is not limiting the clock frequency).

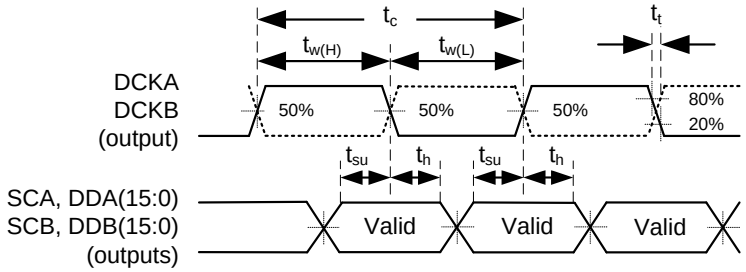

Figure 11. DMD LVDS Interface

6.16 Source Input Blanking Requirements

PORT	PARAMETER (1)	MINIMUM BLANKING
Port 1 Vertical Blanking	VBP	370 µs
	VFP	1 Line
	Total vertical blanking	370 µs + 2 lines
Port 2 Vertical Blanking	VBP	370 µs
	VFP	1 line
	Total vertical blanking	370 µs + 2 lines
Port 1 and 2 Horizontal Blanking	HBP	10 pixels
	HFP	0 pixels
	Total horizontal blanking	80 pixels

(1) Refer to *Video Timing Parameter Definitions*.

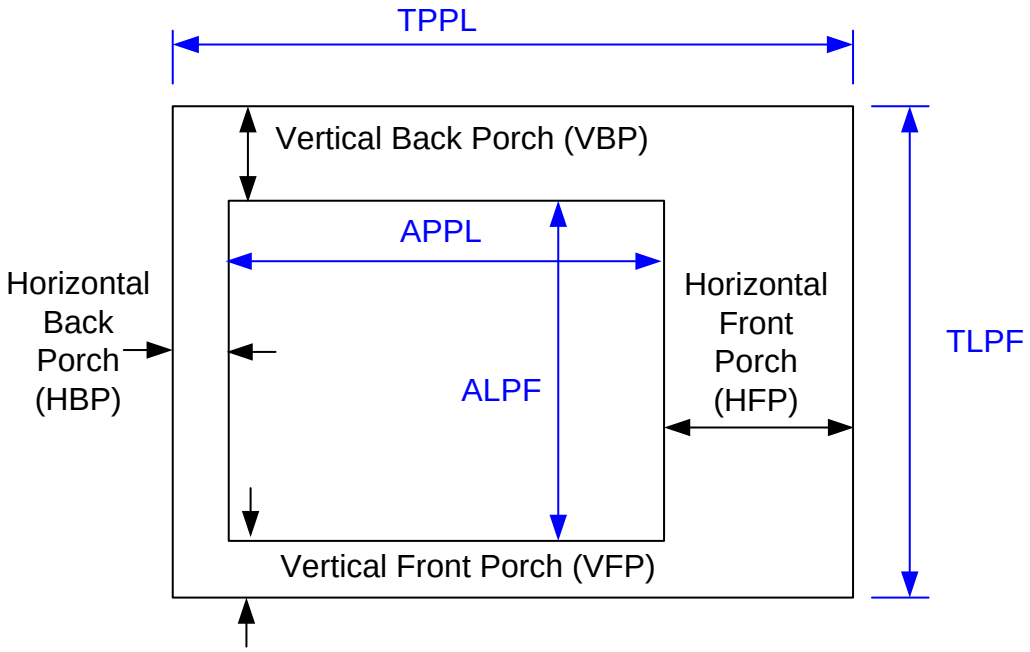

Figure 12. Video Timing Parameters

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7 Detailed Description

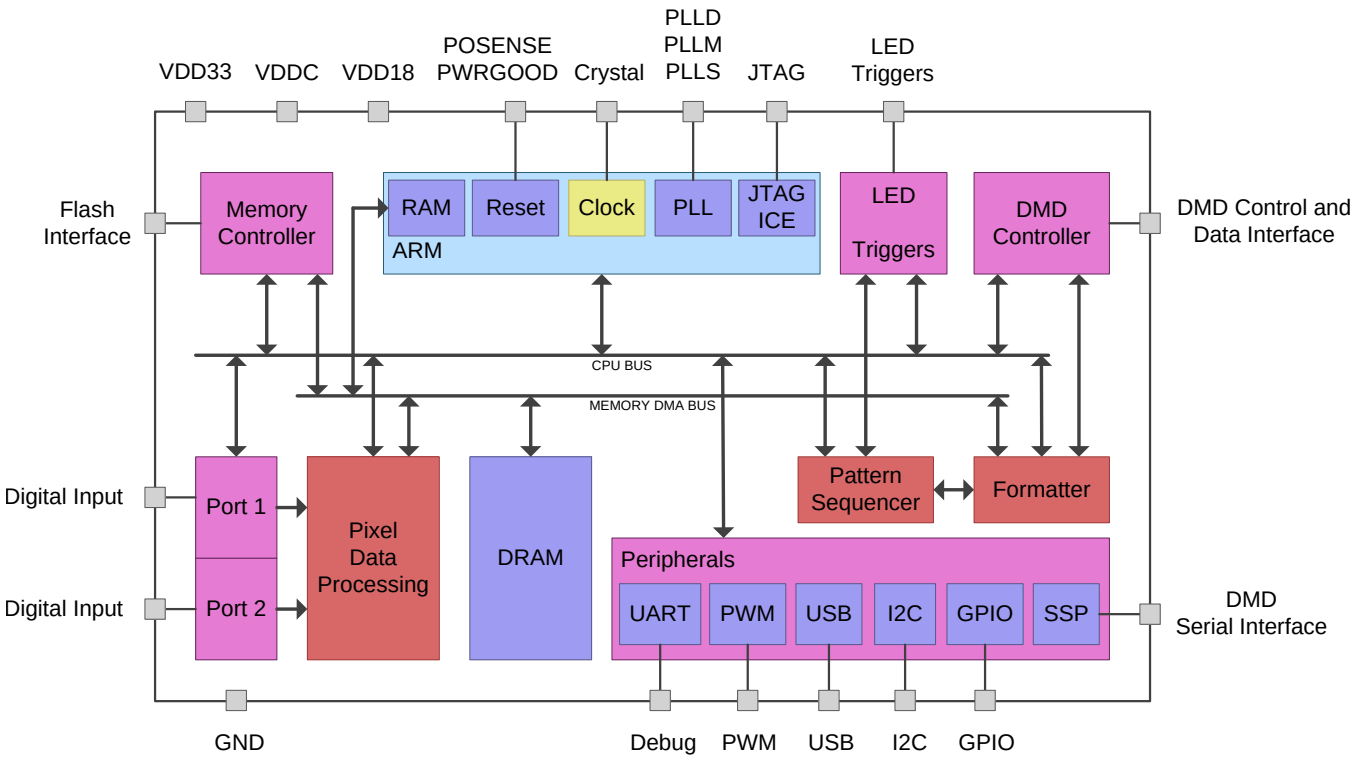
7.1 Overview

The DLPC900 controller processes the digital input image and converts the data into the digital format needed by the DLP9000 or the DLP6500. The DLP9000 and the DLP6500 reflect light by using binary pulse-width-modulation (PWM) for each micromirror. For further details, refer to the DLP9000 or the DLP6500 data sheets.

The DLPC900 combined with a DLP6500 supports a wide variety of resolutions from SVGA to 1080p. When accurate pattern display is needed, a native 1080p resolution source is used for a one-to-one association with the corresponding micromirror on the DLP6500.

The DLPC900 combined with a DLP9000 supports only native WQXGA resolution for a one-to-one association with the corresponding micromirror on the DLP9000. Both combinations are well-suited for structured light, additive manufacturing, or digital exposure applications.

7.2 Functional Block Diagram



7.3 Feature Description

The DLPC900 controller takes as input 16-, 20-, or 24-bit RGB data at up to 120-Hz frame rate. For example, a 120Hz 24-bit frame is composed of three colors (red, green, and blue) with each color equally divided in the 120-Hz frame rate. Thus, each color has a 2.78-ms time slot allocated. Because each color has an 8-bit depth, each color time slot is further divided into bit-planes. A bit-plane is the 2-dimensional arrangement of one-bit extracted from all the pixels in the full color 2D image to implement dynamic depth (see Figure 13).

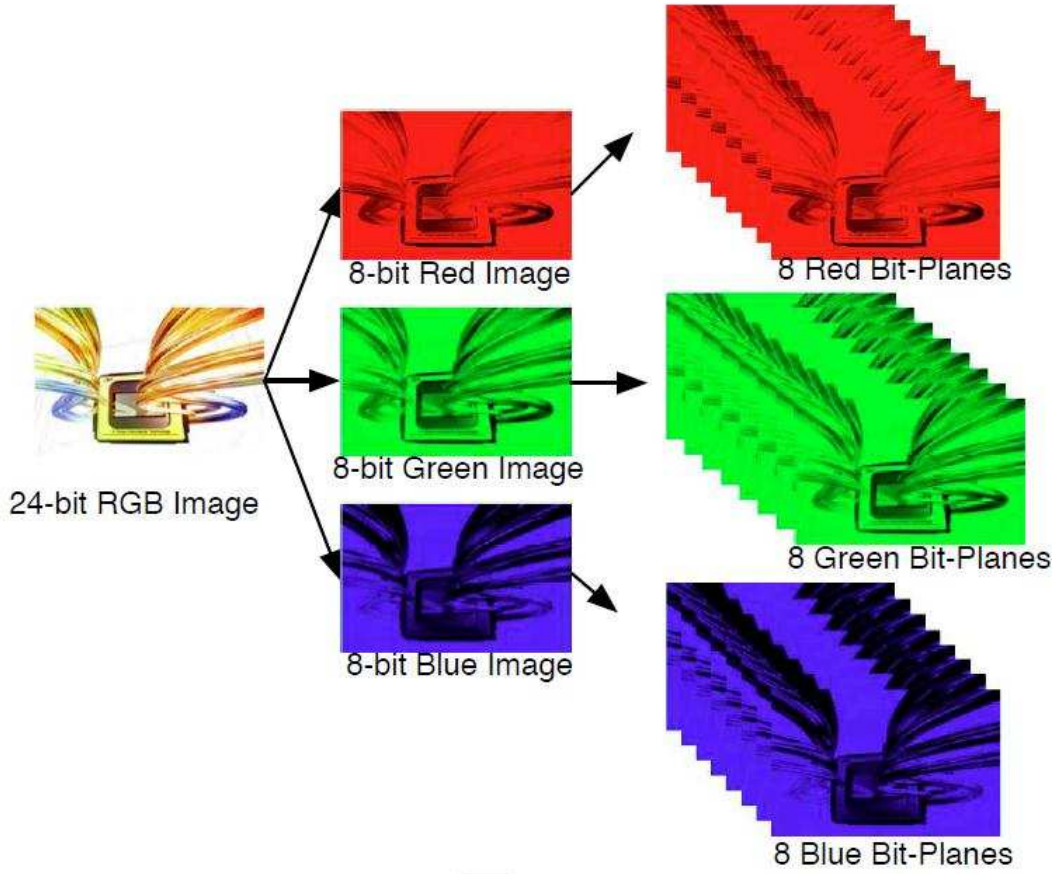


Figure 13. Bit Slices

The length of each bit-plane in the time slot is weighted by the corresponding power of two of its binary representation. This provides a binary pulse-width modulation of the image. For example, a 24-bit RGB input has three colors with 8-bit depth each. Each color time slot is divided into eight bit-planes, with the sum of the weight of all bit planes in the time slot equal to 256. See Figure 14 for an illustration of this partition of the bits in a frame.

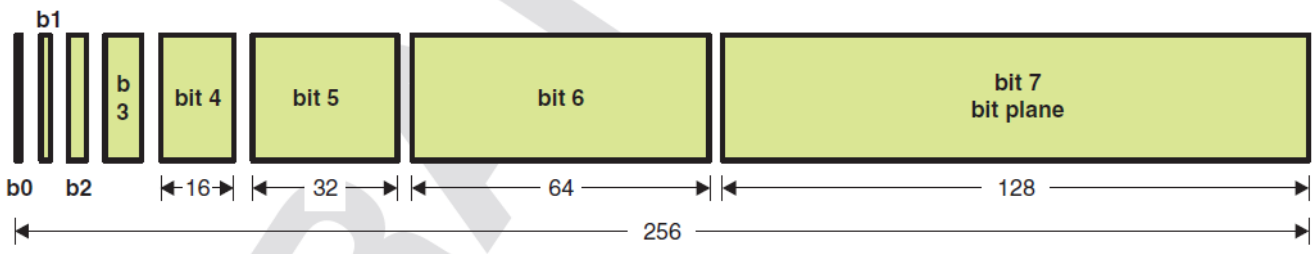


Figure 14. Bit Partition in a Frame for an 8-Bit Color

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Feature Description (continued)

Therefore, a single video frame is composed of a series of bit-planes. Because the DMD mirrors can be either on or off, an image is created by turning on the mirrors corresponding to the bit set in a bit-plane. With binary pulse-width modulation, the intensity level of the color is reproduced by controlling the amount of time the mirror is on. For a 24-bit RGB frame image inputted to the DLPC900 controller, the DLPC900 controller creates 24 bit-planes, stores them in internal embedded DRAM, and sends them to the DMD, one bitplane at a time. The bit weight controls the amount of time the mirror is on. To improve image quality in video frames, these bit-planes, time slots, and color frames are shuffled and interleaved within the pixel processing functions of the DLPC900 controller.

7.3.1 DMD Configurations

Figure 15 shows the controller connections for full-bus normal or swapped. Refer to the *DLPC900 Programmer's Guide* (DLPU018) for details on how to select the bus swap settings to match the board layout connections.

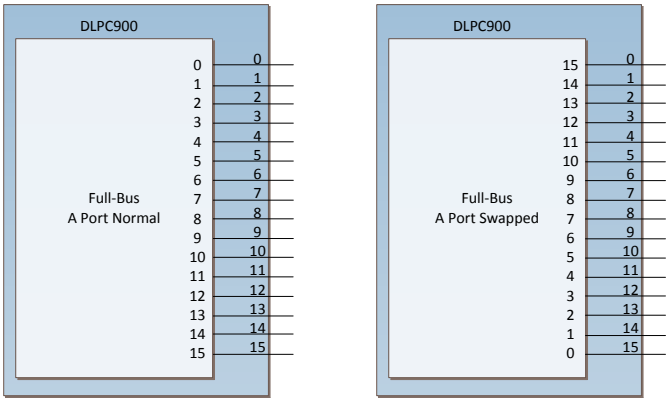

Figure 15. Controller to DMD Full-Bus Connections

7.3.2 Video Timing Input Blanking Specification

The DLPC900 controller requires a minimum horizontal and vertical blanking for both Port 1 and Port 2 as shown in *Source Input Blanking Requirements* . These parameters indicate the time allocated to retrace the signal at the end of each line and field of a display. Refer to *Video Timing Parameter Definitions*.

7.3.3 Board-Level Test Support

The In-Circuit Tri-State Enable signal (ICTSEN) is a board-level test control signal. By driving ICTSEN to a logic high state, all controller outputs (except TDO1 and TDO2) will be configured as tri-state outputs.

The DLPC900 also provides JTAG boundary scan support on all I/O except non-digital I/O and a few special signals. Table 3 lists these exceptions.

Table 3. DLPC900 – Signals Not Covered by JTAG (1)

SIGNAL NAME	PACKAGE BALL
HW_TEST_EN	M25
MOSC	M26
MOSCN	N26
USB_DAT_N	C5
USB_DAT_P	D6
TCK	N24
TDI	N25

(1) There is no JTAG connection to power or no-connect pins.

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Table 3. DLPC900 – Signals Not Covered by JTAG (1) (continued)

SIGNAL NAME	PACKAGE BALL
TRSTZ	M23
TDO1	N23
TDO2	N22
TMS1	P25
TMS2	P26

7.3.4 Two Controller Considerations

When two DLPC900 controllers drive a single high-resolution DLP9000 DMD, each controller is used to drive half of the DMD, as shown in Figure 16. Each controller must operate in two pixels per clock, and the pixel clock must be maintained below the maximum two pixel per clock frequency. Only WQXGA resolution is supported when two DLPC900 controllers are matched with a DLP9000 DMD.

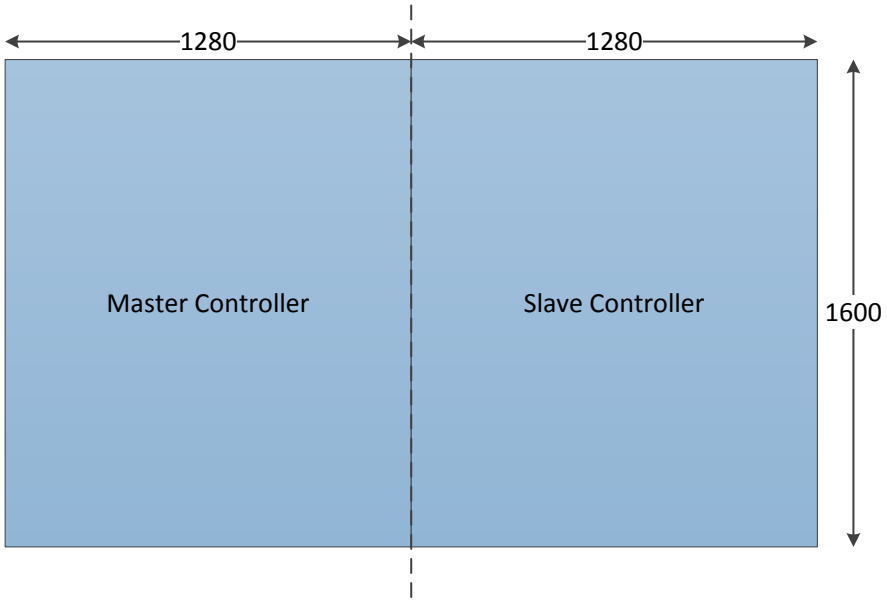

Figure 16. Two Controllers Connected to DLP9000 DMD

7.4 Device Functional Modes

7.4.1 Structured Light Application

For structured light applications, the DLPC900 can be commanded to enter high speed sequential pattern modes where a specific set of patterns are selected with a maximum of 24 bits per pixel. The bit-depth of the patterns are then allocated into the corresponding time slots. Furthermore, an output trigger signal is also synchronized with these time slots to indicate when the image is displayed.

This pattern mode provides the capability to display a set of patterns and signal a camera to capture these patterns overlaid on an object. The DLPC900 controller is capable of pre-loading up to 400 1-bit binary patterns into internal memory from the external flash memory. These pre-loaded binary patterns are then streamed to the DMD at high speed.

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Device Functional Modes (continued)

To synchronize a camera to the displayed patterns, the DLPC900 controller supports two pattern modes: Video pattern and Pre-stored pattern modes. In video pattern mode, the vertical sync is used as trigger input. In pre-stored pattern mode, an internal user configurable trigger or a TRIG_IN_1 pulse indicates to the DLPC900 controller to advance to the next pattern, while TRIG_IN_2 starts and stops the pattern sequence. In both pattern modes, TRIG_OUT_1 frames the exposure time of the pattern, while TRIG_OUT_2 indicates the start of the pattern sequence.

Figure 17 shows an example of a video pattern mode. The VSYNC starts the pattern sequence display. The pattern sequence consists of a series of four patterns followed by a series of three patterns and then repeats. The first pattern sequence consists of P1, P2, P3, and P4. The second pattern sequence consists of P5, P6, and P7. TRIG_OUT_1 frames each pattern exposed, while TRIG_OUT_2 indicates the start of each pattern in the sequence. If the pattern sequence is configured without dark time between patterns, then the TRIG_OUT_1 output would be high for the entire pattern sequence.

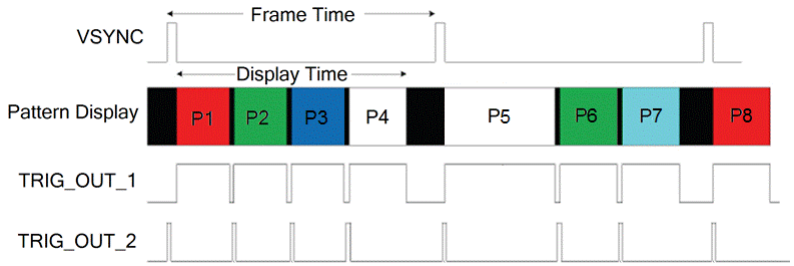

Figure 17. Video Pattern Mode Timing Diagram

Figure 18 shows an example of a pre-stored pattern mode. Pattern sequences of four are displayed. TRIG_OUT_1 frames each pattern exposed, while TRIG_OUT_2 indicates the start of each pattern in the sequence. If the pattern sequence is configured without dark time between patterns, then the TRIG_OUT_1 output would be high for the entire pattern sequence.

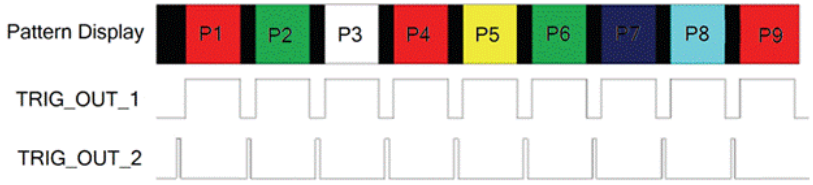

Figure 18. Pre-Stored Pattern Mode Timing Diagram

Another example of a pre-stored pattern mode is shown in Figure 19, where pattern sequences of three are displayed. TRIG_OUT_1 frames each pattern displayed, while TRIG_OUT_2 indicates the start of each pattern. TRIG_IN_2 serves as a start and stop signal. When high, the pattern sequence starts or continues. Note, in the middle of displaying the P4 pattern, TRIG_IN_2 is low, so the sequence stops displaying P4. When TRIG_IN_2 is raised, the pattern sequence continues where it stopped by re-displaying P4.

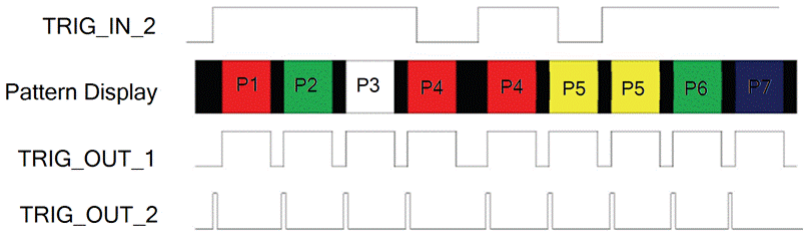

Figure 19. Pre-Stored Pattern Mode Timing Diagram for 3-Patterns

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Device Functional Modes (continued)

Table 4 shows the allowed pattern combinations in relation to the bit depth of the pattern. If the pattern sequence is configured without dark time between patterns, then the TRIG_OUT_1 output would be high for the entire pattern sequence.

Table 4. Minimum Exposure in Any Pattern Mode

BIT DEPTH	DLP6500 (µs)	DLP9000 (µs)
1	105	105
2	304	304
3	394	380
4	823	733
5	1215	1215
6	1487	1487
7	1998	1998
8	4046	4046

Table 5. Minimum Exposures for Number of Active DMD Blocks

ACTIVE BLOCKS	DLP6500 (µs)	DLP9000 (µs)
1	24	24
2	45	42
3	45	42
4	45	42
5	48	45
6	54	51
7	60	56
8	66	61
9	72	67
10	78	72
11	84	77
12	90	83
13	96	88
14	101	93
15	105	99
16	N/A	105

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The DLPC900 controller is required to be coupled with the DLP6500 or the DLP9000 DMDs to provide a reliable display solution for video display and structure light applications. The DLPC900 converts the digital input data into the digital format needed by the DLP6500 or the DLP9000 DMDs. The DMDs consist of an array of micromirrors which reflect incoming light to one of two directions by using binary pulse-width-modulation (PWM) for each micromirror, where the primary direction being into a projection or collection optics. Applications of interest include 3D machine vision, 3D printing, direct imaging lithography, and intelligent lighting.

8.2 Typical Applications

8.2.1 Typical Two Controller Chipset

A typical embedded system application using the DLPC900 controller and DLP9000 is shown in Figure 20. This configuration requires two DLPC900 controllers to drive a DLP9000 DMD and supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor. In this configuration, the 24-bit parallel RGB input data is split between the master and the slave controller as described in *Two Controller Considerations* using an FPGA or some other mechanism.

This system supports both still and motion video sources with the input resolution native to the DLP9000. However, the controller only supports sources with periodic synchronization pulses. This is ideal for motion video sources, but can also be used for still images by maintaining periodic syncs and only sending a new frame of data when needed. The still image must be fully contained within a single video frame and meet the frame timing constraints. The DLPC900 controller refreshes the displayed image at the source frame rate and repeats the last active frame for intervals in which no new frame has been received.

This configuration also supports high speed sequential pattern mode. The patterns are pre-stored in external flash and have a maximum of 24 bits per pixel. The patterns are pre-loaded into internal embedded DRAM and then streamed to the DLP9000 using the pattern modes mentioned in the *Structured Light Application* .

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Typical Applications (continued)

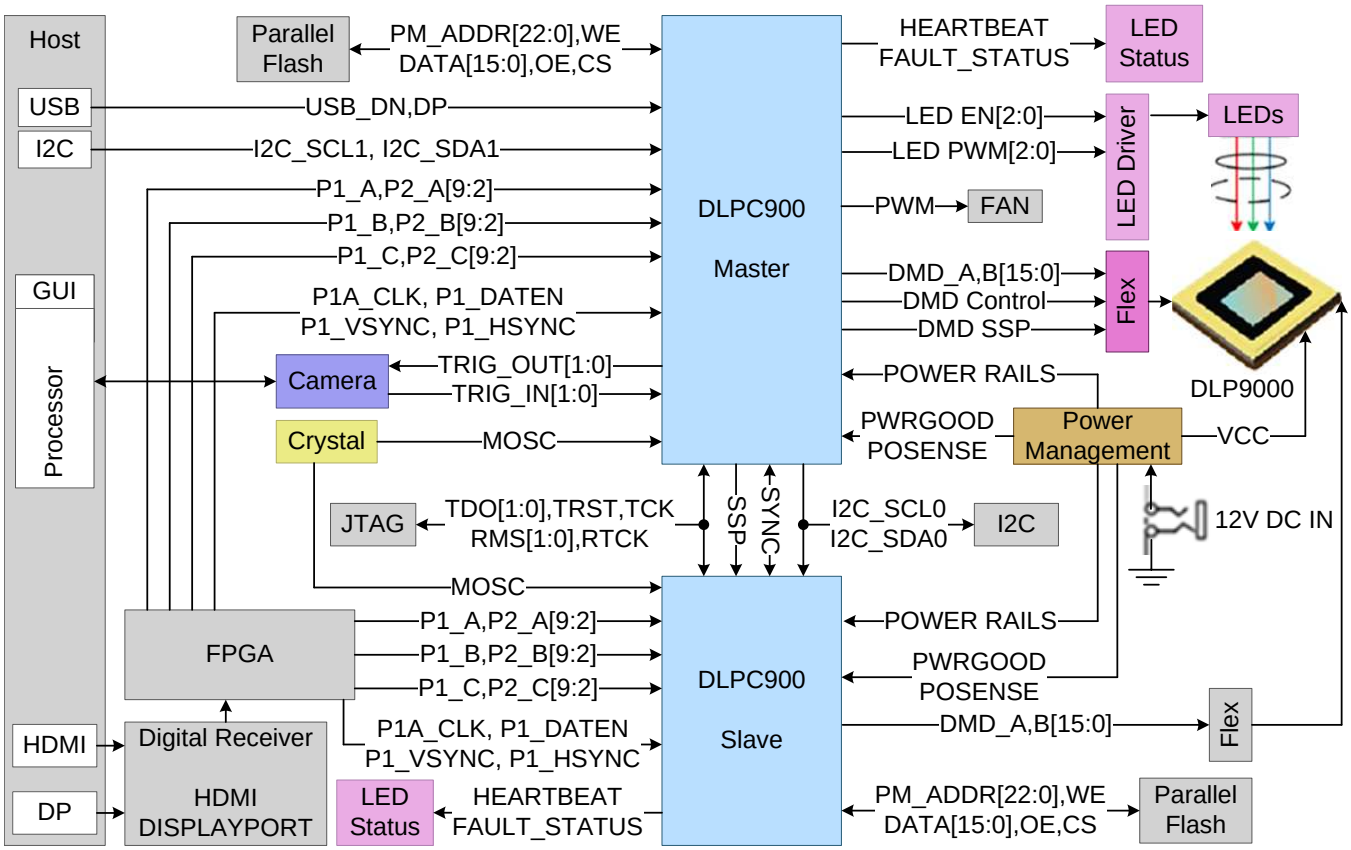

Figure 20. Typical Application Schematic for DLP9000

8.2.1.1 Design Requirements

All applications require both the controller and DMD components for reliable operation. The system uses an external parallel flash memory device loaded with the DLPC900 configuration and support firmware. The external boot flash must contain a minimum of 2 sectors, where the first sector starts at address 0xF9000000 which is the power-up reset start address. The first 128kB is reserved for the bootlloader image and must be in its own sector and can be made up of several smaller contiguous sectors that add up to 128kB as shown in Figure 21. The remaining sectors contains the rest of the firmware. The default wait-states is set for a flash device of 120-ns access time. For a faster flash access time, refer to the *Program Memory Flash Interface* on how to program new wait-state values.

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Typical Applications (continued)

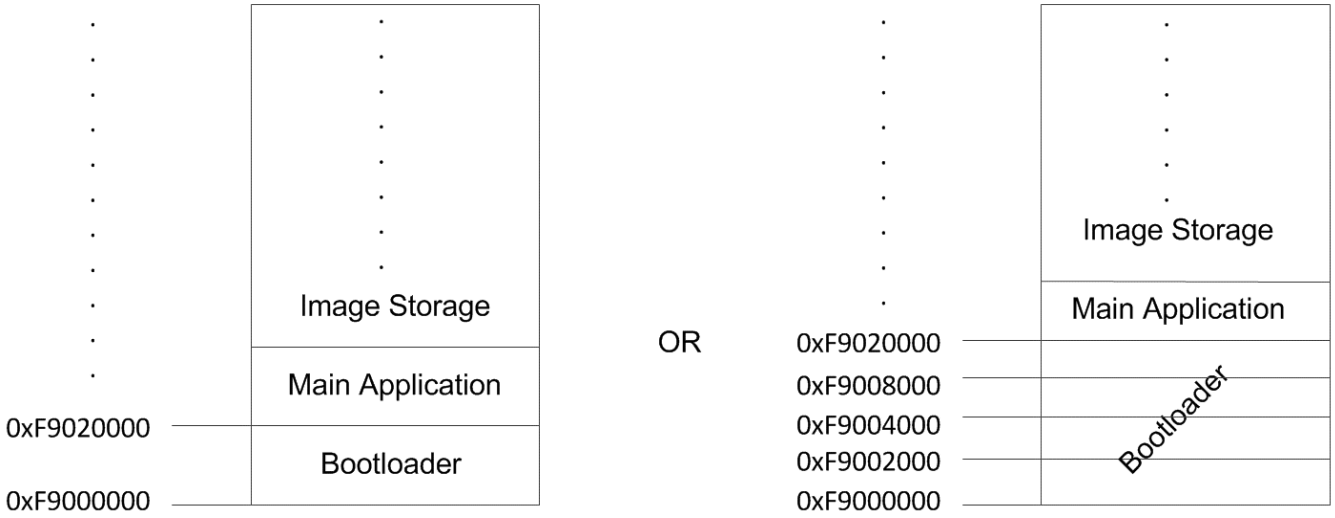

Figure 21. Boot Flash Memory Layout

NOTE

The Bootloader, the Main Application, and any images stored in flash (if present) are considered the firmware.

The chipset has the following interfaces and support circuitry:

- DLPC900 System Interfaces
  - Control Interfaces
  - Trigger Interface
  - Input Data Interfaces
  - Illumination Interface
- DLPC900 Support Circuitry and Interfaces
  - Reference Clock
  - PLL
  - Program Memory Flash Interface
- DMD Interface
  - DLPC900 to DLP6500/DLP9000 Digital Data
  - DLPC900 to DLP6500/DLP9000 Control and Clock Interface
  - DLPC900 to DLP6500/DLP9000 Serial Communication Interface

8.2.1.2 Detailed Design Procedure

8.2.1.2.1 DLPC900 System Interfaces

The DLPC900 chipset supports a 24-bit parallel RGB interface for image data transfers from another device and a 24-bit interface for video data transfers. The system input requires proper generation of the PWRGOOD and POSENSE inputs to ensure reliable operation. There are two primary output interfaces: illumination driver control interface and sync outputs.

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Typical Applications (continued)

8.2.1.2.1.1 Control Interface

The DLPC900 chipset supports I^2C or USB commands through the control interface. The control interface allows another master processor to send commands to the DLPC900 controller to query system status or perform real-time operations, such as, LED driver current settings. The DLPC900 allows the user to set a different I2C slave address for the host port. Refer to the *DLPC900 Programmer's Guide* to set a different I^2C master and slave addresses.

Table 6. Active Signals – I^2C Interfaces

SIGNAL NAME	DESCRIPTION
I2C2_SCL	I^2C clock. Bidirectional open-drain signal. I^2C master clock to external devices.
I2C2_SDA	I^2C data. Bidirectional open-drain signal. I^2C master to transfer data to external devices.
I2C1_SCL	I^2C clock. Bidirectional open-drain signal. I^2C master clock to external devices.
I2C1_SDA	I^2C data. Bidirectional open-drain signal. I^2C master to transfer data to external devices.
I2C0_SCL (1)	I^2C clock. Bidirectional open-drain signal. I^2C slave clock input from the external processor.
I2C0_SDA (1)	I^2C data. Bidirectional open-drain signal. I^2C slave to accept commands or transfer data to and from the external processor.

(1) This interface is the host port.

8.2.1.2.1.2 Input Data Interfaces

The data interface has a Parallel RGB input port and has a nominal I/O voltage of 3.3 V. Maximum and minimum input timing specifications for both components are provided in the Interface Timing Requirements. Each parallel RGB port can support up to 24 bits in video mode.

Table 7. Active Signals – Data Interface

SIGNAL NAME	DESCRIPTION
RGB Parallel Interface Port 1	
P1_(A, B, C)_[2:9] (1)	24-bit data inputs, 8 bits for each of the red, green, and blue channels. When interfacing to a system with 8-bits per color or less, connect the bus of the red, green, and blue channels to the upper bits of the DLPC900 10-bit bus.
P_CLK1	Pixel clock; all input signals on data interface are synchronized with this clock.
P1_VSYNC	Vertical sync
P1_HSYNC	Horizontal sync
P_DATAEN1	Input data valid
RGB Parallel Interface Port 2	
P2_(A, B, C)_[0:9] (1)	24-bit data inputs, 8 bits for each of the red, green, and blue channels. When interfacing to a system with 8-bits per color or less, connect the bus of the red, green, and blue channels to the upper bits of the DLPC900 10-bit bus.
P_CLK2	Pixel clock; all input signals on data interface are synchronized with this clock.
P2_VSYNC	Vertical sync
P2_HSYNC	Horizontal sync
P_DATAEN2	Input data valid
Optional Pixel Clock 3	
P_CLK3	Pixel clock; all input signals on data interface are synchronized with this clock.

(1) The A, B, and C input data channels of Port 1 and 2 can be internally swapped for optimum board layout. Refer to the DLPC900 Programmers Guide for details on how to configuring the port settings to match the board layout connections.

8.2.1.2.1.3 DLPC900 System Output Interfaces

8.2.1.2.1.3.1 Illumination Interface

An illumination interface is provided that supports up to a three (3) channel LED driver. The illumination interface provides signals that support: LED driver enable, LED enable, LED enable select, and PWM signals to control the LED current.

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Table 8. Active Signals - Illumination Interface

SIGNAL NAME	DESCRIPTION
HEARTBEAT	Signal toggles continuously to indicate system is running fine.
FAULT_STATUS	Signal toggles or held high indicating system faults
RED_LED_EN	Red LED enable
GRN_LED_EN	Green LED enable
BLU_LED_EN	Blue LED enable
RED_LED_PWM	Red LED PWM signal used to control the LED current
GRN_LED_PWM	Green LED PWM signal used to control the LED current
BLU_LED_PWM	Blue LED PWM signal used to control the LED current

8.2.1.2.1.3.2 Trigger and Sync Interface

The DLPC900 outputs a trigger signal for synchronizing displayed patterns with a camera, sensor, or other peripherals. The sync output supporting signals are: horizontal sync, vertical sync, two input triggers, and two output triggers. Depending on the application, these signals control how the pattern is displayed.

Table 9. Active Signals - Trigger and Sync Interface

SIGNAL NAME	DESCRIPTION
P1_HSYNC	Horizontal Sync
P1_VSYNC	Vertical Sync
TRIG_IN_1	Depending on the mode, advances the pattern display.
TRIG_IN_2	Depending on the mode, starts or stops the pattern display.
TRIG_OUT_1	Active high during pattern exposure
TRIG_OUT_2	Active high pulse to indicate first pattern display

8.2.1.2.1.4 DLPC900 System Support Interfaces

8.2.1.2.1.4.1 Reference Clock and PLL

The DLPC900 controller requires a 20-MHz 3.3-V external input from an oscillator. This signal serves as the DLPC900 chipset reference clock from which the majority of the interfaces derive their timing. This includes DMD interfaces and serial interfaces.

Refer to *PCB Layout Guidelines for Internal Controller PLL Power* on PLL guidelines.

8.2.1.2.1.4.2 Program Memory Flash Interface

The DLPC900 provides three external program memory chip selects for standard NOR-type flash:

- PM_CSZ_0 – flash device (≤ 128 Mb)
- PM_CSZ_1 – dedicated CS for boot flash device (≤ 128 Mb). Refer to the Figure 21 for the memory layout of the boot flash.
- PM_CSZ_2 – flash device (≤ 128 Mb)

Flash access timing is programmable up to 19 wait-states. Table 10 contains the formulas to calculate the required wait-states for each of the parameters shown in Figure 22 for a typical flash device. Refer to the DLPC900 Programmers Guide for details on how to set new wait-state values.

Table 10. Flash Wait-States

PARAMETER	FORMULA (1)	DEFAULT
T_{CS} (CSZ low to WEZ low)	= Roundup((T_{CS}+ 5 ns) / 6.7 ns)	2
T_{WP} (WEZ low to WEZ high)	= Roundup((T_{WP}+ 5 ns) / 6.7 ns)	11
T_{CH} (WEZ high to CSZ high)	= Roundup((T_{CH}+ 5 ns) / 6.7 ns)	2

(1) Assumes a maximum single direction trace length of 75 mm.

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Table 10. Flash Wait-States (continued)

PARAMETER	FORMULA (1)	DEFAULT
T_{ACC} (CSZ low to Output Valid) (2)	= Roundup((T_{ACC}+ 5 ns) / 6.7 ns)	19
Maximum supported wait-states	19 (120ns) (3)	

(2) In some flash device data sheets, the read access time may also be represented as T_{OE}, T_E, T_{RC}, or T_{CE}. Use the largest of these values to calculate the wait-states for the read access time.
(3) For each parameter.

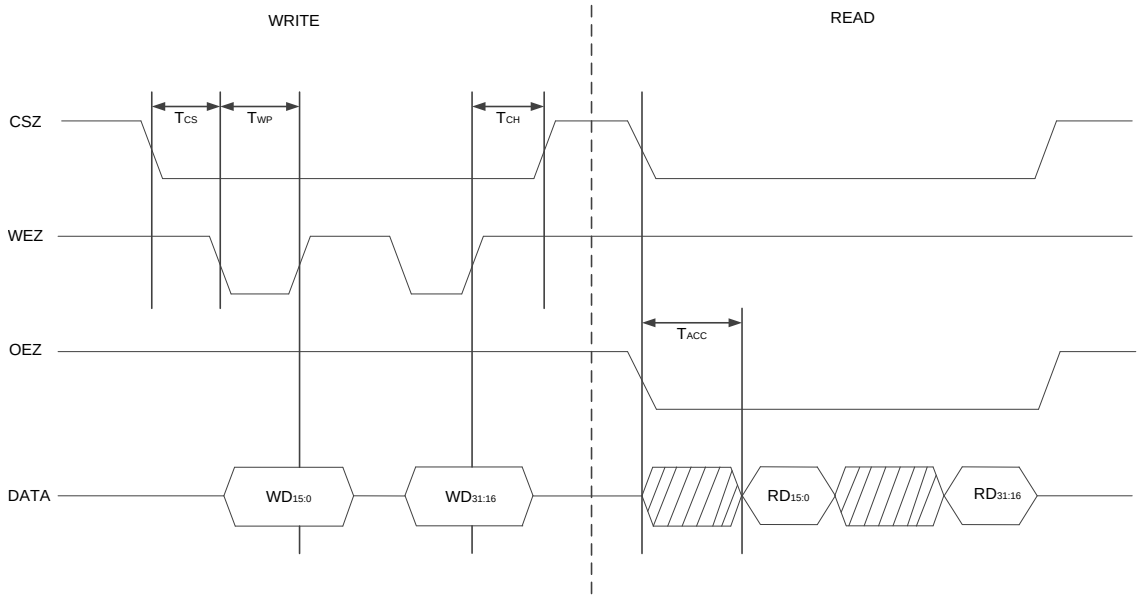

Figure 22. Flash Interface Timing Diagram

8.2.1.2.1.4.3 DMD Interface

The DLPC900 controller provides the pattern data to the DMD over a double data rate (DDR) interface. Table 11 describes the signals used for this interface.

Table 11. Active Signals - DLPC900 to DMD Digital Data Interface

SIGNAL NAME	DESCRIPTION
DDA(15:0)	DMD, LVDS interface channel A, differential serial data
DDB(15:0)	DMD, LVDS interface channel B, differential serial data
DCKA	DMD, LVDS interface channel A, differential clock
DCKB	DMD, LVDS interface channel B, differential clock
SCA	DMD, LVDS interface channel A, differential serial control
SCB	DMD, LVDS interface channel B, differential serial control

The DLPC900 controls the micromirror clock pulses in a manner to ensure proper and reliable operation of the DMD.

Table 12. Active Signals - DLPC900 to DMD Control Interface

SIGNAL NAME	DESCRIPTION
DADOEZ	DMD output-enable (active low)
DADADDR(3:0)	DMD address
DADMODE(1:0)	DMD mode
DADSEL(1:0)	DMD select
DADSTRB	DMD strobe
DAD_INTZ	DMD interrupt (active low). This signal requires an external 1-KΩ pullup and uses hysteresis.

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The DLPC900 controls the micromirror control interface signals in a manner to ensure proper and reliable operation of the DMD.

8.2.2 Typical Single Controller Chipset

A typical embedded system application using the DLPC900 controller and DLP6500 is shown in Figure 23. This configuration uses one DLPC900 controller to operate with a DLP6500 and supports a 24-bit parallel RGB input, typical of LCD interfaces, from an external source or processor.

This system supports both still and motion video sources. However, the controller only supports sources with periodic synchronization pulses. This is ideal for motion video sources, but can also be used for still images by maintaining periodic syncs and only sending a new frame of data when needed. The still image must be fully contained within a single video frame and meet the frame timing constraints. The DLPC900 controller refreshes the displayed image at the source frame rate and repeats the last active frame for intervals in which no new frame has been received.

This configuration also supports high speed sequential pattern mode. The patterns are pre-stored in external flash and have a maximum of 24 bits per pixel. The patterns are pre-loaded into internal embedded DRAM and then streamed to the DLP6500 using the pattern modes mentioned in the *Structured Light Application* .

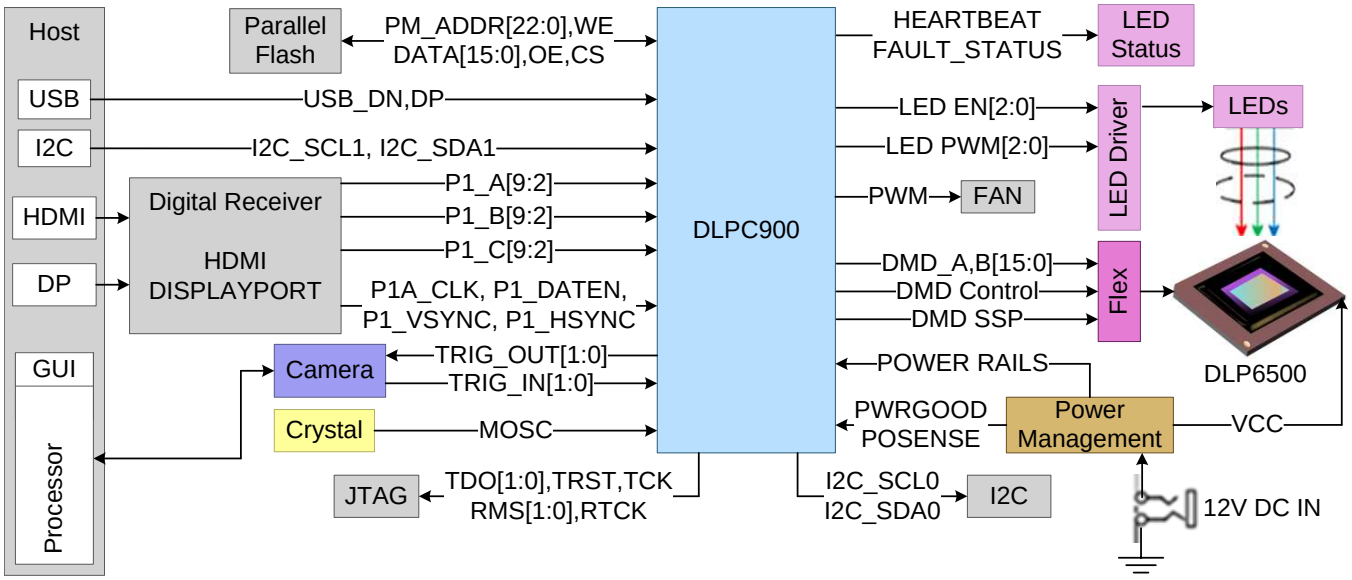

Figure 23. Typical Application Schematic for DLP6500

9 Power Supply Recommendations

9.1 System Power Regulation

The PLLD_VAD, PLLM1_VAD, and PLLM2_VAD power feeding internal PLLs must be derived from an isolated linear regulator with filter as recommended in *PCB Layout Guidelines for Internal Controller PLL Power* to minimize the AC noise component.

It is acceptable to derive PLLD_VDD, PLLM1_VDD, PLLM2_VDD, and PLLS_VAD from the same regulator as the core VDDC, but they should be filtered as recommended in the *PCB Layout Guidelines for Internal Controller PLL Power* .

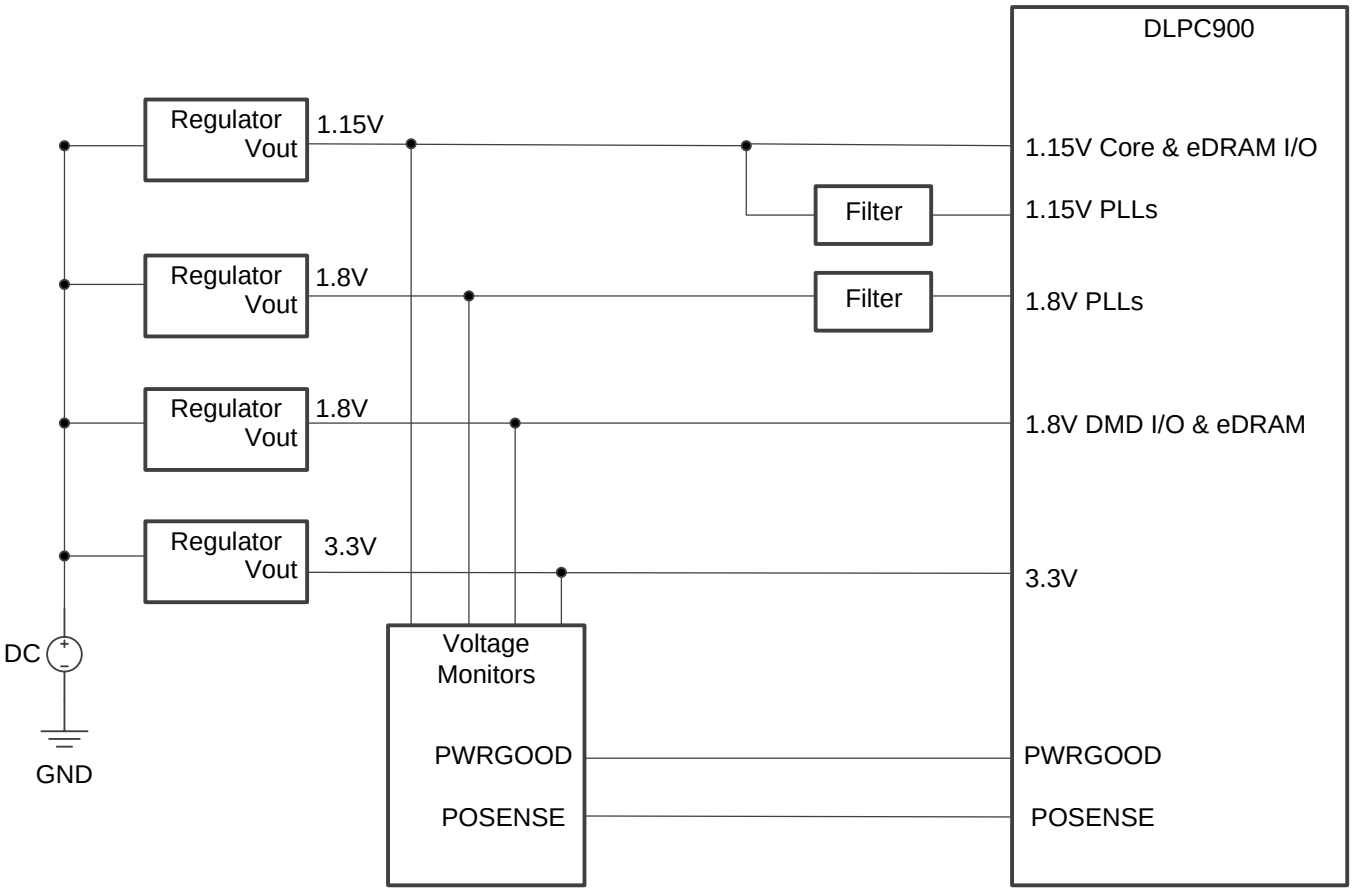

Figure 24. Power Regulation

9.1.1 Power Distribution System

9.1.1.1 1.15-V System Power

The DLPC900 can support a low-cost power delivery system with a single 1.15-V power source derived from a switching regulator. The main core should receive 1.15 V power directly from the regulator output, and the internal DLPC900 PLLs (PLLD_VDD, PLLM1_VDD, PLLM2_VDD, and PLLS_VAD) should receive individually filtered versions of this 1.15 V power. For specific filter recommendations, refer to the *PCB Layout Guidelines for Internal Controller PLL Power* .

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System Power Regulation (continued)

9.1.1.2 1.8-V System Power

The DLPC900 power delivery system provides two independent 1.8-V power sources. One of the 1.8-V power sources should be used to supply 1.8-V power to the DLPC900 LVDS I/O and internal DRAM. Power for these functions should always be fed from a common source, which is recommended as a linear regulator. The second 1.8-V power source should be used (along with appropriate filtering as discussed in the *PCB Layout Guidelines for Internal Controller PLL Power*) to supply all of the DLPC900 internal PLLs (PLLD_VAD, PLLM1_VAD, and PLLM2_VAD). To keep this power as clean as possible, a dedicated linear regulator is highly recommended for the 1.8-V power to the PLLs.

9.1.1.3 3.3-V System Power

The DLPC900 can support a low-cost power delivery system with a single 3.3-V power sources derived from a switching regulator. This 3.3-V power will supply all LVTTL I/O and the crystal oscillator cell. The 3.3-V power should remain active in all power modes for which 1.15-V core power is applied.

9.2 System Environment and Defaults

9.2.1 DLPC900 System Power-Up and Reset Default Conditions

Following system power-up, the DLPC900 will perform a power-up initialization routine that will default the controller to its normal power mode in which all blocks are powered, all processor clocks will be enabled at their full rate and associated resets will be released. Most other clocks will default disabled with associated resets asserted until released by the processor. These same defaults will also be applied as part of all system reset events that occur without removing or cycling power. The 1.8-V power should be applied prior to releasing the reset so that the LVDS I/O and the internal embedded DRAM are enabled before the DLPC900 begins executing its system initialization routines.

9.3 System Power-Up Sequence

Although the DLPC900 requires an array of power supply voltages, for example, 1.15 V, 1.8 V, and 3.3 V, there are no restrictions regarding the relative order of power supply sequencing to avoid damaging the DLPC900, as long as the system is held in reset during power supply sequencing. This is true for both power-up (reset controlled by POSENSE) and power-down (reset controlled by PWRGOOD) scenarios. Similarly, there is no minimum time between powering-up or powering-down the different supplies feeding the DLPC900. However, power-sequencing requirements are common for the devices that share the supplies with the DLPC900.

Power-sequencing recommendations to ensure proper operation are:

- 1.15-V core power should be applied whenever any I/O power is applied. This ensures the state of the associated I/O that are powered are set to a know state. Thus, applying core power first is recommended.
- All DLPC900 power should be applied before POSENSE is asserted to ensure proper power-up initialization is performed.

It is assumed that all DLPC900 power-up sequencing is handled by external hardware. It is also assumed that an external power monitor will hold the DLPC900 in system reset during power-up (that is, POSENSE = 0). During this time all controller I/O's will be tri-stated. The master PLL (PLLM1) will be released from reset upon the low-to-high transition of POSENSE, but the DLPC900 will be kept in for an additional 60 ms to allow the PLL to lock and stabilize its outputs. After this delay the DLPC900 internal resets will be deasserted, thus causing the processor to begin its boot-up routine.

Figure 25 shows the recommended DLPC900 system power-up sequence of the regulators:

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System Power-Up Sequence (continued)

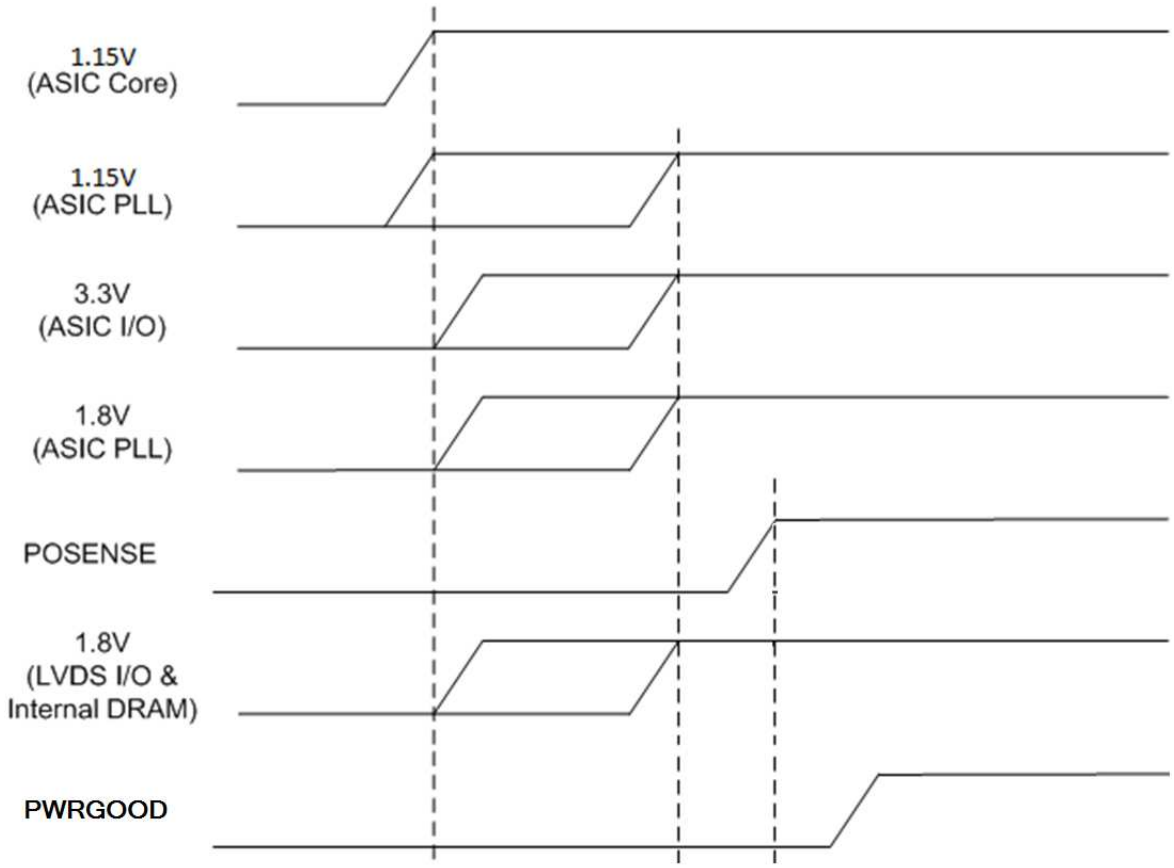

Figure 25. Power Sequencing

9.3.1 Power-On Sense (POSENSE) Support

It is difficult to set up a power monitor to trip exactly on the controller minimum supply voltage specification. Thus for practical reasons, the external power monitor generating POSENSE should target its threshold to 90% of the minimum supply voltage specifications and ensure that POSENSE remains low a sufficient amount of time for all supply voltages to reach minimum controller requirements and stabilize. The trip voltage for detecting the loss of power, as well as the reaction time to respond to a low voltage condition is not critical for POSENSE because PWRGOOD is used for this purpose. As such, PWRGOOD has critical requirements in these areas.

9.3.2 Power Good (PWRGOOD) Support

The PWRGOOD signal is defined as an early warning signal that alerts the controller a specified amount of time before the DC supply voltages drop below specifications. This warning lets the controller park the DMD mirrors and place the system into reset. See *Reset Timing Requirements* .

9.3.3 5-V Tolerant Support

With the exception of USB_DAT, the DLPC900 does not support any other 5-V tolerant I/O. However, I^2C typically have 5V requirements and special measures must be taken to support them. It is recommended that a 5-V to 3.3-V level shifter be used.

It is strongly recommended that a 0.5-W external series resistance (of 22 Ω) to limit the potential impact of a continuous short circuit between either USB D+ or USB D– to either Vbus, GND, the other data line, or the cable. For additional protection, also add an optional 200-mA Schottky diode from USB_DAT to VDD33.

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9.4 System Reset Operation

9.4.1 Power-Up Reset Operation

Immediately after a power-up event, DLPC900 hardware will automatically bring up the master PLL and place the controller in normal power mode. It will then follow the standard system reset procedure (see *System Reset Operation*).

9.4.2 System Reset Operation

Immediately after any type of system reset (power-up reset, PWRGOOD reset, watchdog timer time-out, and so forth), the DLPC900 automatically returns to normal power mode and returns to the following state:

- All GPIO will tri-state.
- The master PLL will remain active (it is only reset on a power-up reset) and most of the derived clocks will be active. However, only those resets associated with the DLPC900 processor and its peripherals will be released. (The DPLC900 firmware is responsible for releasing all other resets.)
- The DLPC900 associated clocks will default to their full clock rates (boot-up is at full speed).
- The PLL feeding the LVDS DMD interface (PLLD) will default to its power-down mode and all derived clocks will be inactive with corresponding resets asserted. (The DLPC900 firmware is responsible for enabling these clocks and releasing associated resets.)
- LVDS I/O will default to its power-down mode with tri-stated outputs.
- All resets output by the DLPC900 will remain asserted until released by the firmware (after boot-up).
- The DLPC900 processor will boot-up from external flash.

Once the DLPC900 processor boots-up, the DLPC900 firmware will:

- Configure the programmable DDR clock generator (DCG) clock rates (that is, the DMD LVDS interface rate)
- Enable the DCG PLL (PLLD) while holding divider logic in reset
- After the DCG PLL locks, the processor software will set DMD clock rates
- API software will then release DCG divider logic resets, which in turn, will enable all derived DCG clocks
- Release external resets

The LVDS I/O is reset by a system reset event and remains in reset until released by the DLPC900 firmware. Thus, the software is responsible for waiting until power is restored to these components before releasing reset.

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10 Layout

10.1 Layout Guidelines

10.1.1 General PCB Recommendations

Two-ounce copper planes are recommended in the PCB design in order to achieve needed thermal connectivity.

10.1.2 PCB Layout Guidelines for Internal Controller PLL Power

The following are guidelines to achieve desired controller performance relative to internal PLLs:

The DLPC900 contains four PLLs (PLLM1, PLLM2, PLLD, and PLLS), each of which have a dedicated 1.15 V digital supply; three of these PLLs (PLLM1, PLLM2, and PLLD) have a dedicated 1.8 V analog supply. It is important to have filtering on the supply pins that covers a broad frequency range. Each 1.15 V PLL supply pin should have individual high frequency filtering in the form of a ferrite bead and a 0.1 µF ceramic capacitor. These components should be located very close to the individual PLL supply balls. The impedance of the ferrite bead should far exceed that of the capacitor at frequencies above 10 MHz. The 1.15 V to the PLL supply pins should also have low frequency filtering in the form of an RC filter. This filter can be common to all the PLLs. The voltage drop across the resistor is limited by the 1.15 V regulator tolerance and the DLPC900 voltage tolerance. A resistance of 0.36 Ω and a 100 µF ceramic are recommended. Figure 26 shows the recommended filter topology.

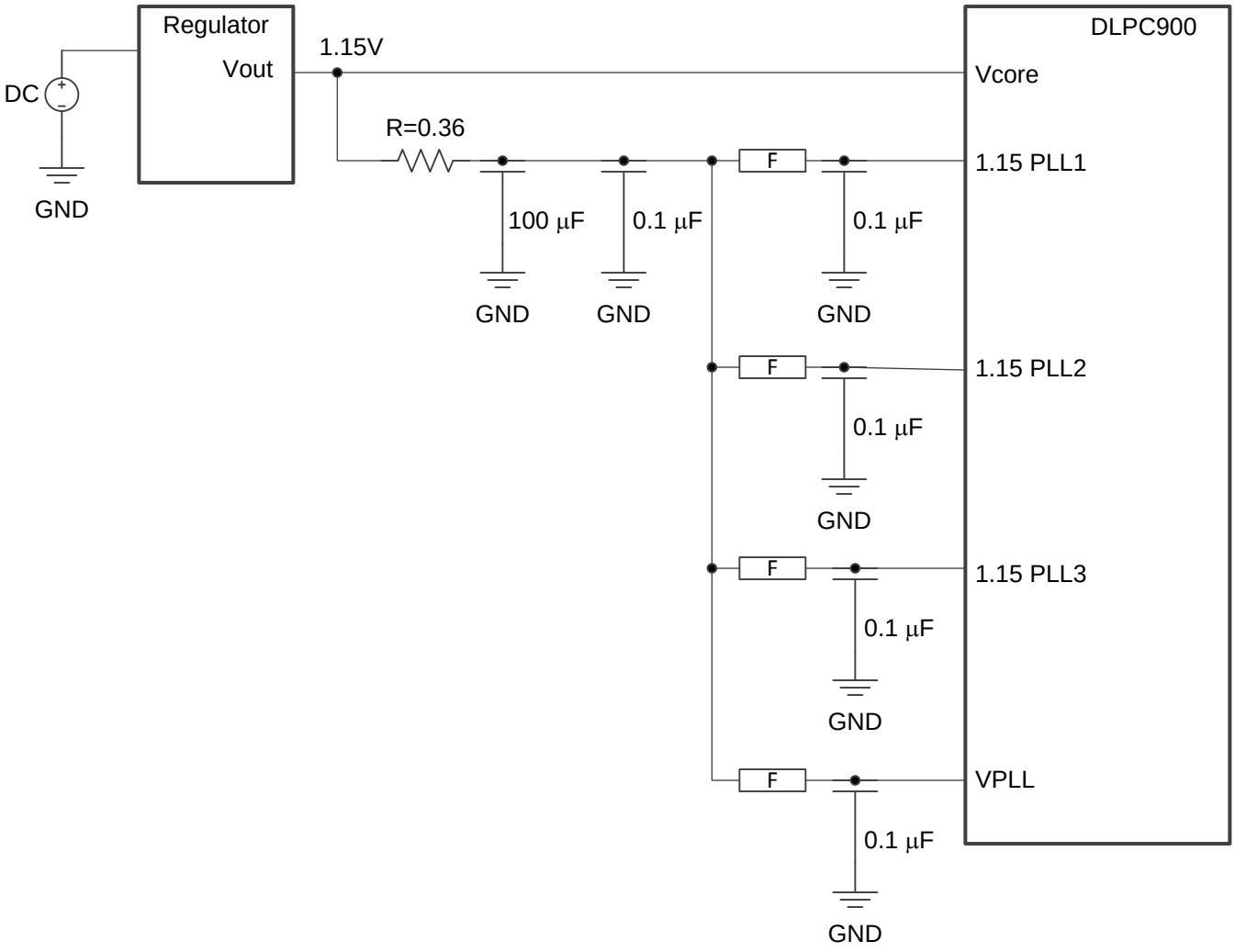

Figure 26. Recommended Filter Topology for PLL 1.15-V Supplies

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Layout Guidelines (continued)

The analog 1.8-V PLL power pins should have a similar filter topology as the 1.15 V. In addition, It is recommended that a dedicated linear regulator generates the 1.8 V. Figure 27 shows the recommended filtering topology.

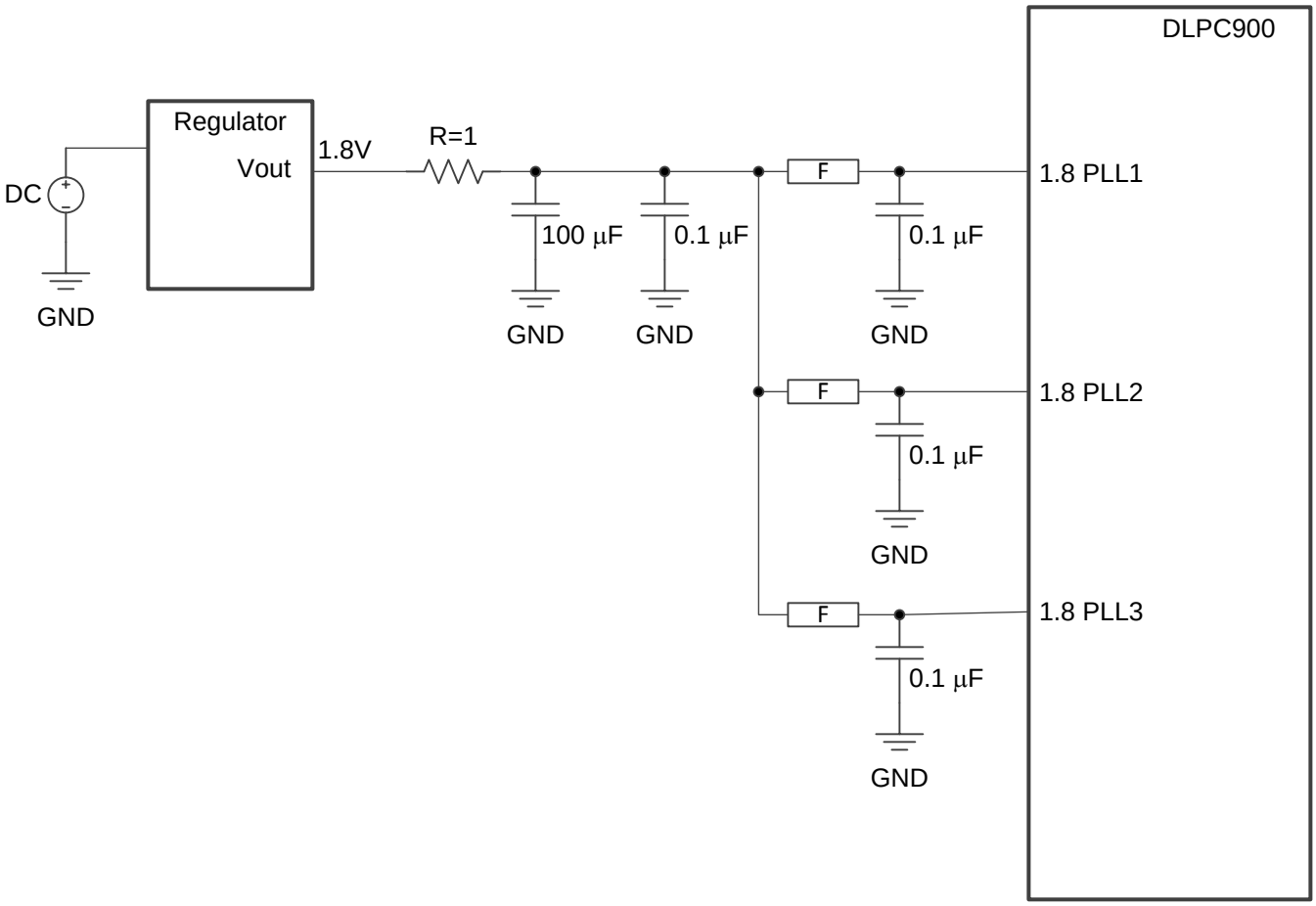

Figure 27. Recommended Filter Topology for PLL 1.8-V Supplies

When designing the overall supply filter network, care must be taken to ensure no resonance occurs. Specific care is required around the 1- to 2-MHz band, as this coincides with the PLL natural loop frequency.

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Layout Guidelines (continued)

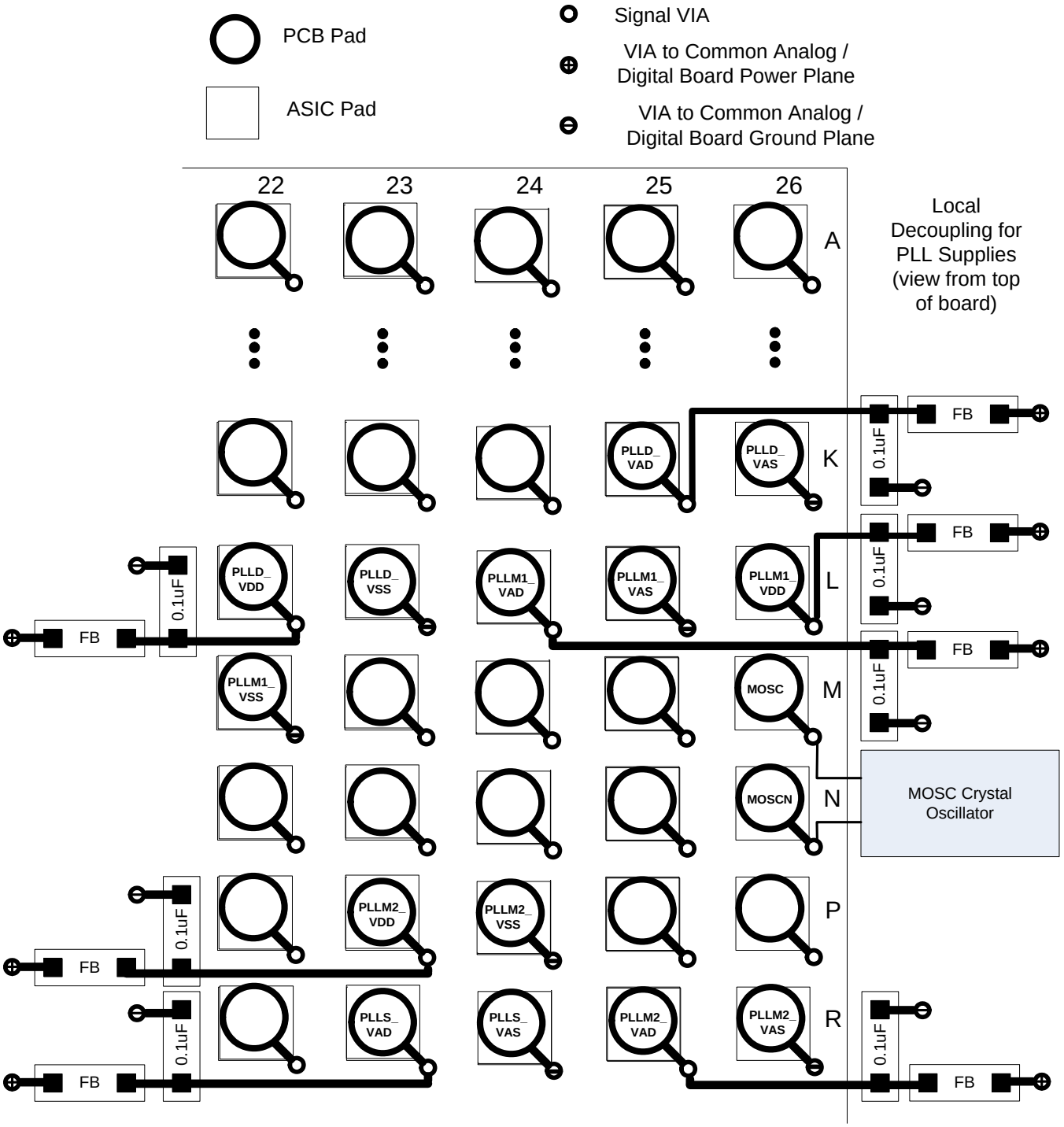

Figure 28. High Frequency Decoupling

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Layout Guidelines (continued)

High-frequency decoupling is required for 1.15-V and 1.8-V PLL supplies and should be provided as close as possible to each of the PLL supply package pins as shown in Figure 28. Placing decoupling capacitors under the package on the opposite side of the board is recommended. High-quality, low-ESR, monolithic, surface-mount capacitors should be used. Typically, 0.1 µF for each PLL supply should be sufficient. The length of a connecting trace increases the parasitic inductance of the mounting, and thus, where possible, there should be no trace, allowing the via to butt up against the land. Additionally, the connecting trace should be made as wide as possible. Further improvement can be made by placing vias to the side of the capacitor lands or doubling the number of vias.

The location of bulk decoupling depends on the system design.

10.1.3 PCB Layout Guidelines for Quality Video Performance

One of the most important factors to gain good performance is designing the PCB with the highest quality signal integrity possible. Here are a few recommendations:

1. Minimize the trace lengths between the video digital receiver and the DLPC900 port inputs.
2. Analog power should not be shared with the digital power directly.
3. Try to keep the trace lengths of the RGB as equal as possible.
4. Impedance matching between the digital receiver and the DLPC900 is important.

10.1.4 Recommended MOSC Crystal Oscillator Configuration

A recommended crystal oscillator configuration is shown in Figure 29.

It is assumed that the external crystal oscillator will stabilize within 50 ms after stable power is applied.

Table 13. Crystal Port Characteristics

PARAMETER	NOMINAL	UNIT
MOSC-to-GND capacitance	1.5	pF
MOSCZ-to-GND capacitance	1.5	pF

Table 14. Recommended Crystal Configuration (1)

PARAMETER	RECOMMENDED	UNIT
Crystal circuit configuration	Parallel resonant	
Crystal type	Fundamental (first harmonic)	
Crystal nominal frequency	20	MHz
Crystal temperature stability	± 30	PPM
Crystal frequency tolerance (including accuracy, temperature, aging, and trim sensitivity)	± 100	PPM
Crystal equivalent series resistance (ESR)	50 max	Ω
Crystal load	20	pF
Crystal shunt load	7 max	pF
R_S drive resistor (nominal)	100	Ω
R_{FB} feedback resistor (nominal)	1	MΩ
C_{L1} external crystal load capacitor (MOSC)	See Equation 1	pF
C_{L2} external crystal load capacitor (MOSCN)	See Equation 2	pF
PCB layout	A ground isolation ring around the crystal is recommended	

(1) Typical drive level with the XSA020000FK1H-OCX crystal (ESR_{max} = 40 Ω) = 50 µW

$$C_{L1} = 2 \times (C_L - C_{Stray\text{-}MOSC}) \quad (1)$$

$$C_{L2} = 2 \times (C_L - C_{Stray\text{-}MOSCN} \quad (2)$$

where

- C_L = Crystal load capacitance (Farads)
- $C_{Stray\text{-}MOSC}$ = Sum of package and PCB capacitance at the crystal pin associated with controller signal MOSC.

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- $C_{Stray\text{-}MOSCN}$ = Sum of package and PCB capacitance at the crystal pin associated with controller signal MOSCN. (3)

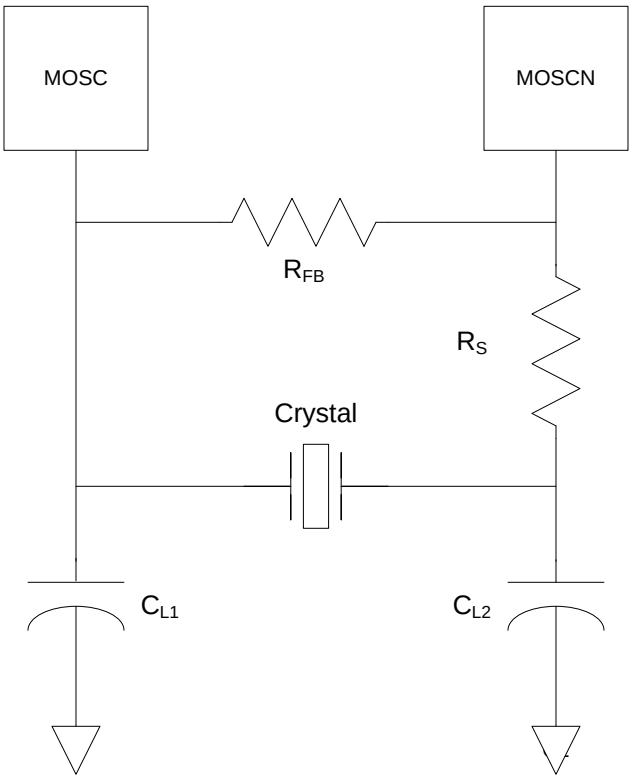

Figure 29. Crystal Oscillator Configuration

10.1.5 Spread Spectrum Clock Generator Support

DLPC900 supports limited, internally controlled, spread spectrum clock spreading on the DMD interface. The purpose is to frequency-spread all signals on this high-speed external interface to reduce EMI emissions. Clock spreading is limited to triangular waveforms. The DLPC900 provides modulation options of 0%, ±0.5%, and ±1.0% (center-spread modulation).

10.1.6 GPIO Interface

The DLPC900 provides 9 software-programmable, general-purpose I/O pins. Each GPIO pin is individually configurable as either input or output. In addition, each GPIO output can be either configured as push-pull or open-drain. Some GPIO have one or more alternative use modes, which are also software configurable. The reset default for all GPIO is as an input signal. However, any alternative function connected to these GPIO pins, with the exception of general-purpose clocks and PWM generation, will be reset. When configured as open-drain, the outputs must be externally pulled-up (to the 3.3-V supply). External pullup or pulldown resistors may be required to ensure stable operation before software can configure these ports.

10.1.7 General Handling Guidelines for Unused CMOS-Type Pins

To avoid potentially damaging current caused by floating CMOS input-only pins, it is recommended tying unused controller input pins through a pullup resistor to its associated power supply or through a pulldown to ground unless noted in the Pin Functions. For controller inputs with an internal pullup or pulldown resistor, it is unnecessary to add an external pullup or pulldown unless specifically recommended. Internal pullup and pulldown resistors are weak and should not be expected to drive the external line.

Unused output-only pins can be left open.

When possible, it is recommended to configure unused bidirectional I/O pins to their output state such that the pin can be left open. If this control is not available and the pins may become an input, then they should be pulled-up (or pulled-down) using an appropriate resistor unless noted in the Pin Functions.

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10.1.8 DMD Interface Considerations

High-speed interface waveform quality and timing on the DLPC900 controller (that is, the LVDS DMD interface) is dependent on the following factors:

- Total length of the interconnect system
- Spacing between traces
- Characteristic impedance
- Etch losses
- How well matched the lengths are across the interface

Thus, ensuring positive timing margin requires attention to many factors.

As an example, DMD interface system timing margin can be calculated as follows:

Setup Margin = (controller output setup) – (DMD input setup) – (PCB routing mismatch) – (PCB SI degradation) (4)

Hold-time Margin = (controller output hold) – (DMD input hold) – (PCB routing mismatch) – (PCB SI degradation) (5)

The PCB SI degradation is the signal integrity degradation due to PCB affects which includes such things as simultaneously switching output (SSO) noise, crosstalk, and intersymbol interference (ISI) noise.

DLPC900 I/O timing parameters, as well as DMD I/O timing parameters, can be easily found in their corresponding data sheets. Similarly, PCB routing mismatch can be easily budgeted and met via controlled PCB routing. However, PCB SI degradation is not as easy-to-determine.

In an attempt to minimize the signal integrity analysis that would otherwise be required, the following PCB design guidelines provide a reference of an interconnect system that satisfies both waveform quality and timing requirements (accounting for both PCB routing mismatch and PCB SI degradation). Deviation from these recommendations may work, but should be confirmed with PCB signal integrity analysis or lab measurements.

PCB design: Refer to the Figure 30.

Configuration:	Asymmetric dual stripline
Etch thickness (T):	1.0-oz copper (1.2 mil)
Flex etch thickness (T):	0.5-oz copper (0.6 mil)
Single-ended signal impedance:	50 Ω (±10%)
Differential signal impedance:	100 Ω (±10%)

PCB stackup: Refer to the Figure 30.

Reference plane 1 is assumed to be a ground plane for proper return path.

Reference plane 2 is assumed to be the I/O power plane or ground.

Dielectric FR4, (Er):	4.2 (nominal)
Signal trace distance to reference plane 1 (H1):	5.0 mil (nominal)
Signal trace distance to reference plane 2 (H2):	34.2 mil (nominal)

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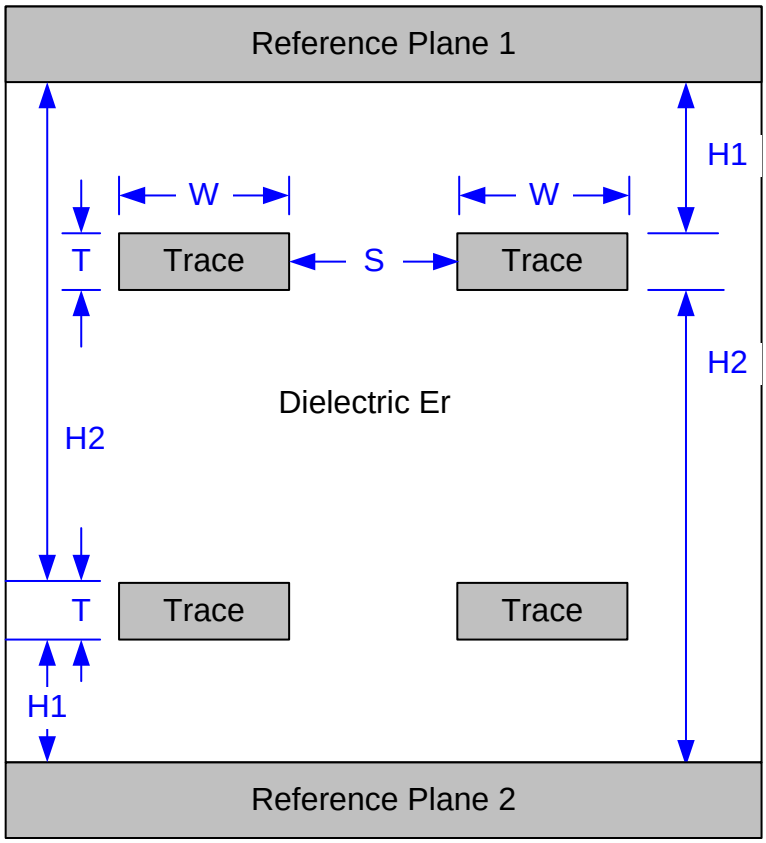

Figure 30. PCB Stackup Geometries

Table 15. General PCB Routing (Applies to All Corresponding PCB Signals refer to Figure 30)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	DIFFERENTIAL PAIRS	UNIT
Line width (W)	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
	PCB etch data or control	7 (0.18)	4.25 (0.11)	mil (mm)
	PCB etch clocks	7 (0.18)	4.25 (0.11)	mil (mm)
Differential signal pair spacing (S)	PCB etch data or control	N/A	5.75 (1) (0.15)	mil (mm)
	PCB etch clocks	N/A	5.75 (1) (0.15)	mil (mm)
Minimum differential pair-to-pair spacing (S)	PCB etch data or control	N/A	20 (0.51)	mil (mm)
	PCB etch clocks	N/A	20 (0.51)	mil (mm)
Minimum line spacing to other signals (S)	Escape routing in ball field	4 (0.1)	4 (0.1)	mil (mm)
	PCB etch data or control	10 (0.25)	20 (0.51)	mil (mm)
	PCB etch clocks	20 (0.51)	20 (0.51)	mil (mm)

(1) Spacing may vary to maintain differential impedance requirements.

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Table 15. General PCB Routing (Applies to All Corresponding PCB Signals refer to Figure 30) (continued)

PARAMETER	APPLICATION	SINGLE-ENDED SIGNALS	DIFFERENTIAL PAIRS	UNIT
Maximum differential pair P-to-N length mismatch	Total data	N/A	12 (0.3)	mil (mm)
	Total clock	N/A	12 (0.3)	mil (mm)

Table 16. DMD Interface Specific PCB Routing

SIGNAL GROUP LENGTH MATCHING				
INTERFACE	SIGNAL GROUP	REFERENCE SIGNAL	MAX MISMATCH	UNIT
DMD (LVDS)	SCA_P/ SCA_N DDA_P_(15:0)/ DDA_N_(15:0)	DCKA_P/ DCKA_N	± 150 (± 3.81)	mil (mm)
DMD (LVDS)	SCB_P/ SCB_N DDB_P_(15:0)/ DDB_N_(15:0)	DCKB_P/ DCKB_N	± 150 (± 3.81)	mil (mm)

When routing the DMD Interface signals it is recommended to:

- Minimize the number of layer changes for Single-ended signals.
- Individual differential pairs can be routed on different layers but the signals of a given pair should not change layers.

Table 17. DMD Signal Routing Length(1)

BUS	MIN	MAX	UNIT
DMD (LVDS)	50	375	mm

(1) Max signal routing length includes escape routing.

Stubs: Stubs should be avoided.

Termination Requirements: DMD interface: None – The DMD receiver is differentially terminated to 100 Ω internally.

Connector (DMD-LVDS interface bus only):

High-speed connectors that meet the following requirements should be used:

- Differential crosstalk: < 5%
- Differential impedance: 75 to 125 Ω

Routing requirements for right-angle connectors: When using right-angle connectors, P-N pairs should be routed in the same row to minimize delay mismatch. When using right-angle connectors, propagation delay difference for each row should be accounted for on associated PCB etch lengths.

These guidelines will produce a maximum PCB routing mismatch of 4.41 mm (0.174 inch) or approximately 30.4 ps, assuming 175 ps/inch FR4 propagation delay.

These PCB routing guidelines will result in approximately 25-ps system setup margin and 25-ps system hold margin for the DMD interface after accounting for signal integrity degradation as well as routing mismatch.

Both the DLPC900 output timing parameters and the DMD input timing parameters include timing budget to account for their respective internal package routing skew.

10.1.8.1 Flex Connector Plating

Plate all the pad area on top layer of flex connection with a minimum of 35 and maximum 50 micro-inches of electrolytic hard gold over a minimum of 100 micro-inches of electrolytic nickel.

10.1.9 PCB Design Standards

PCB designed and built in accordance with the following industry specifications:

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Table 18. Industry Design Specification

INDUSTRY SPECIFICATION	APPLICABLE TO
IPC-2221 and IPC2222, Type 3, Class X, at Level B producibility	Board Design
IPC-6011 and IPC-6012, Class 2	PWB Fabrication
IPC-SM-840, Class 3, Color Green	Finished PWB Solder mask
UL94V-0 Flammability Rating and Marking	Finished PWB
UL796 Rating and Marking	Finished PWB

10.1.10 Signal Layers

The PCB signal layers should follow typical good practice guidelines including:

- Layer changes should be minimized for single-ended signals.
- Individual differential pairs can be routed on different layers, but the signals of a given pair should not change layers.
- Stubs should be avoided.
- Only voltage or low-frequency signals should be routed on the outer layers, except as noted previously in this document.
- Double data rate signals should be routed first.
- Pin swapping on components is not allowed.

The PCB should have a solder mask on the top and bottom layers. The mask should not cover the vias.

- Except for fine pitch devices (pitch ≤ 0.032 inches), the copper pads and the solder mask cutout should be of the same size.
- Solder mask between pads of fine pitch devices should be removed.
- In the BGA package, the copper pads and the solder mask cutout should be of the same size.

10.1.11 Trace Widths and Minimum Spacing

BGA escape routing can be routed with 4-mils width and 4-mils spacing, as long as the escape nets are less than 1 inch long, to allow 2 traces fit between vias. After signals escape the BGA field, trace width should be widened to achieve the desired impedance and spacing.

All single-ended 50-Ω signal must have a minimum spacing of 10mils relative to other signals. Other special trace spacing requirements are listed in Table 19

Table 19. Traces Widths and Minimum Spacing

SIGNAL ON PIN	MINIMUM WIDTH	MINIMUM SPACE
VDDC, VDD18, VDD33	0.020	0.015
GND	0.015 (1)	0.005
PLLS_VAD, PLLM2_VDD, PLLD_VDD, PLLM1_VDD, PLLM1_VAD, PLLM2_VAD, PLLD_VAD	0.012 (keep length less than 260 mils)	0.015
MOSCP, OCLKA		0.020 (2)
SCA_(P,N), DDA_(P,N)_(15:00), SCB_(P,N), DDB_(P,N)_(15:00), DCKA_(P,N), DCKB_(P,N)		0.030 (2)
USB_DAT_(P,N)		0.030 (2)

(1) Make width of GND trace as wide as the pin it is connected to, when possible.
(2) Trace spacing of these signals/signal-pairs relative to other signals

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10.1.12 Trace Impedance and Routing Priority

For best performance, it is recommended that the trace impedance for differential signals as in Table 20.

All signals should be 50-Ω controlled impedance unless otherwise noted in Table 20.

Table 20. Trace Impedance

SIGNAL ON PIN	DIFFERENTIAL IMPEDANCE
DCKA_(P,N)	100 Ω ±10%
SCA_(P,N)	
DDA_(P,N)_(15:00)	
DCKB_(P,N)	100 Ω ±10%
SCB_(P,N)	
DDB_(P,N)_(15:00)	
USB_DAT_(P,N)	90 Ω ±10%
USB_(P,N)	
All other Differential Signals	100 Ω ±10%

Table 21 lists the signals' routing priority assignment.

Table 21. Routing Priority

SIGNAL ON PIN	PRIORITY
DCKA_(P,N) SCA_(P,N) DDA_(P,N)_(15:00) DCKB_(P,N) SCB_(P,N) DDB_(P,N)_(15:00)	1 (1) (2) (3)
USB_(P,N) USB_DAT_(P,N)	2 (1)
P1(A,B,C)(9:2),P2(A,B,C)(9:2), P_CLK1, P_CLK2, P_CLK3, P_DATEN1, P_DATEN2, P1_VSYNC, P2_VSYNC, P1_HSYNC, P2_HSYNC	3 (1) (2) (3)
OCLKA, MOSCP	4 (4)

(1) Refer to Table 8 for length matching requirement
(2) Switching layer should not be done except at the beginning and end of the trace
(3) Maximum routing length of 2 inches for each signal/pair, includes escape routing
(4) Keep routing length under 0.35 inches

10.1.13 Power and Ground Planes

For best performance, the following are recommendations:

- Solid ground planes between each signal routing layer
- Two solid power planes for voltages.
- Power and ground pins should be connected to these planes through a via for each pin
- All device pin and via connections to these planes should use a thermal relief with a minimum of four spokes
- Trace lengths for the component power and ground pins should be minimized to 0.03 inches or less
- Vias should be spaced out to avoid forming slots on the power planes
- High speed signals should not cross over a slot in the adjacent power planes
- Vias connecting all the digital layers should be placed around the edge of the rigid PCB regions 0.03 inches from the board edges with 0.1 inch spacing prior to routing
- Placing extra vias is not required if there are sufficient ground vias due to normal ground connections of devices
- All signal routing and signal vias should be inside the perimeter ring of ground vias

10.1.14 Power Vias

Power and Ground pins of each component shall be connected to the power and ground planes with a via for each pin. Avoid sharing vias to the power plane among multiple power pins, where possible. Trace lengths for component power and ground pins should be minimized (ideally, less than 0.100"). Unused or spare device pins that are connected to power or ground may be connected together with a single via to power or ground. The minimum spacing between vias shall be 0.050" to prevent slots from being developed on the ground plane.

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10.1.15 Decoupling

Decoupling capacitors must be located as near as possible to the DLPC900 voltage supply pins. Capacitors should not share vias. The DLPC900 power pins can be connected directly to the decoupling capacitor (no via) if the trace is less than 0.03”. Otherwise the component should be tied to the voltage or ground plane through a separate via. All capacitors should be connected to the power planes with trace lengths less than 0.05”. Try to mount decoupling capacitors connecting to power rail VDD11 (1.15 V) using “via on sides” geometry as shown below in Figure 31. If “via on the side” is not possible, 1.15 V decoupling capacitors can be mounted using “via at ends” method, providing traces between the vias and decoupling capacitors’ pads be as short and wide (at least 15mils wide) as possible.

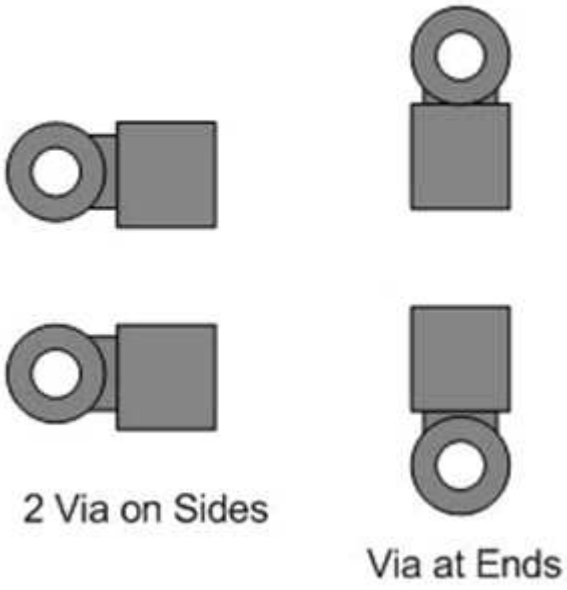

Figure 31. Decoupling Via Placement

10.1.16 Fiducials

Fiducials for automatic component insertion should be placed on the board according to the following guidelines or on recommendation from manufacturer:

- Fiducials for optical auto insertion alignment shall be placed on three corners of both sides of the PCB
- Fiducials should be 0.050” copper with 0.100” cutout (antipad).

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10.2 Layout Example

The DLP® LightCrafter™ 9000 EVM PCB is targeted at 14 layers with layer stack up shown in Figure 32. The PCB layer stack may vary depending on system design. However, careful attention is required to meet design considerations. Layers 1 and 14 should consist of the components layers. Layers 2, 4, 6, 9, 11,and 13 should consist of solid ground planes. Layers 7 and 8 should consist of solid power planes. Layers 1, 3, 5, 10, 12, and 14 should be used as the primary routing layers. Routing on external layers should be less than 0.25 inches for priority one and two signals. Refer to the Table 21 for signal priority groups. Board material should be FR-370HR or similar. PCB should be designed for lead-free assembly with the stackup geometry shown in Figure 32 and Figure 33.

Layer	Calc Thickness	Primary Stack	Description
	0.0005		Taiyo 4000-BN
Layer - 1	0.0020		**1/2oz Sig (Std Plt)**
	0.0046	2116	370H
Layer - 2	0.0006		**1/2oz P/G**
	0.0060	0.0060 (1-1652)	370H
Layer - 3	0.0006		**1/2oz Sig**
	0.0074	2113 2113	370H
Layer - 4	0.0006		**1/2oz P/G**
	0.0060	0.0060 (1-1652)	370H
Layer - 5	0.0006		**1/2oz Sig**
	0.0074	2113 2113	370H
Layer - 6	0.0006		**1/2oz P/G**
	0.0021	0.0020 (1-106)	370H
Layer - 7	0.0006		**1/2oz P/G**
	0.0115	2113 2113 2113	370H
Layer - 8	0.0006		**1/2oz P/G**
	0.0021	0.0020 (1-106)	370H
Layer - 9	0.0006		**1/2oz P/G**
	0.0074	2113 2113	370H
Layer - 10	0.0006		**1/2oz Sig**
	0.0060	0.0060 (1-1652)	370H
Layer - 11	0.0006		**1/2oz P/G**
	0.0074	2113 2113	370H
Layer - 12	0.0006		**1/2oz Sig**
	0.0060	0.0060 (1-1652)	370H
Layer - 13	0.0006		**1/2oz P/G**
	0.0046	2116	370H
Layer - 14	0.0020		**1/2oz Sig (Std Plt)**
	0.0005		Taiyo 4000-BN

Materials: Isola 370H High-Tg FR4

Requirement	Req. Thickness	Tol +	Tol -	Calc Thick
Incl. Plating & Mask	0.0900	0.0090	0.0090	0.0907
Incl. Mask over Laminate	0.0860	0.0086	0.0086	0.0867
Incl. Plating	0.0890	0.0089	0.0089	0.0897
After Lamination	0.0862	0.0043	0.0043	0.0869
Over Laminate	0.0850	0.0085	0.0085	0.0857

Figure 32. Board Layer Stack

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Layout Example (continued)

	Impedance Type	Layer	Design	Actual	Pitch	Plane	Target	Tol (ohms)	Predict
1	Surface MS	L1	-	0.0068	-	-	50	5.0	50.20
		-	-	-	-	L2			
2	EC Microstrip	L1	-	0.0055	0.0110	-	90	9.0	89.55
		-	-	0.0055	-	L2			
3	EC Microstrip	L1	0.00475	0.00475	0.0120	-	100	10.0	100.27
		-	0.00475	0.00475	-	L2			
4	Stripline	L3	-	0.0057	-	L2	50	5.0	49.34
		-	-	-	-	L4			
5	EC Stripline	L3	-	0.0054	0.0110	L2	90	9.0	89.75
		-	-	0.0054	-	L4			
6	EC Stripline	L3	0.00475	0.00475	0.0120	L2	100	10.0	99.03
		-	0.00475	0.00475	-	L4			
7	Stripline	L5	-	0.0057	-	L4	50	5.0	49.34
		-	-	-	-	L6			
8	EC Stripline	L5	-	0.0054	0.0110	L4	90	9.0	89.75
		-	-	0.0054	-	L6			
9	EC Stripline	L5	0.00475	0.00475	0.0120	L4	100	10.0	99.03
		-	0.00475	0.00475	-	L6			
10	Stripline	L10	-	0.0057	-	L9	50	5.0	49.34
		-	-	-	-	L11			
11	EC Stripline	L10	-	0.0054	0.0110	L9	90	9.0	89.75
		-	-	0.0054	-	L11			
12	EC Stripline	L10	0.00475	0.00475	0.0120	L9	100	10.0	99.03
		-	0.00475	0.00475	-	L11			
13	Stripline	L12	-	0.0057	-	L11	50	5.0	49.34
		-	-	-	-	L13			
14	EC Stripline	L12	-	0.0054	0.0110	L11	90	9.0	89.75
		-	-	0.0054	-	L13			
15	EC Stripline	L12	0.00475	0.00475	0.0120	L11	100	10.0	99.03
		-	0.00475	0.00475	-	L13			
16	Surface MS	L14	-	0.0068	-	L13	50	5.0	50.20
		-	-	-	-	-			

Figure 33. Board Trace Geometry

Refer to for a complete set of documentation for the DLP LightCrafter 9000 EVM reference design.

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10.3 Thermal Considerations

The thermal limitation for the DLPC900 is that the maximum operating junction temperature (T_J) must not be exceeded (this is defined in *Recommended Operating Conditions*). This temperature is dependent on operating ambient temperature, airflow, PCB design (including the component layout density and the amount of copper used), power dissipation of the DLPC900, and power dissipation of surrounding components. The DLPC900 device package is designed primarily to extract heat through the power and ground planes of the PCB, thus copper content and airflow over the PCB are important factors.

The recommended maximum operating ambient temperature (T_A) is provided primarily as a design target and is based on maximum DLPC900 power dissipation and $R_{\theta JA}$ at 1 m/s of forced airflow, where $R_{\theta JA}$ is the thermal resistance of the package as measured using a JEDEC-defined standard test PCB. This JEDEC test PCB is not necessarily representative of the DLPC900 PCB, and thus the reported thermal resistance may not be accurate in the actual product application. Although the actual thermal resistance may be different, it is the best information available during the design phase to estimate thermal performance. However after the PCB is designed and the product is built, it is highly recommended thermal performance be measured and validated.

To do this, the top-center case temperature should be measured under the worse case product scenario (max power dissipation, max voltage, max ambient temp) and validated not to exceed the maximum recommended case temperature (T_C). This specification is based on the measured φ_{JT} for the DLPC900 package and provides a relatively accurate correlation to junction temperature. Care must be taken when measuring this case temperature to prevent accidental cooling of the package surface. It is recommended to use a small (approximately 40 gauge) thermocouple. The bead and the thermocouple wire should be covered with a minimal amount of thermally conductive epoxy and contact the top of the package. The wires should be routed closely along the package and the board surface to avoid cooling the bead through the wires.

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11 Device and Documentation Support

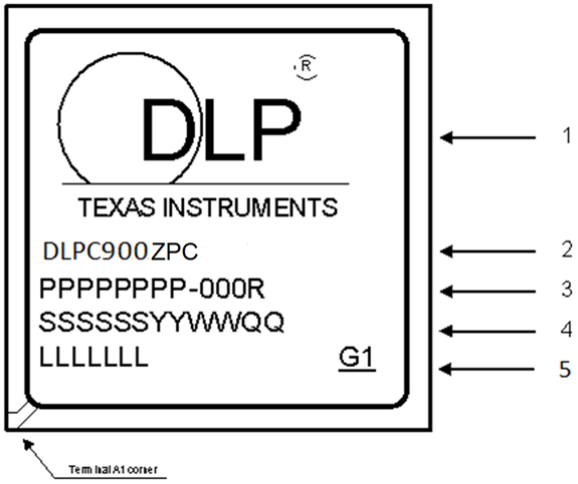
11.1 Device Support

11.1.1 Device Nomenclature

Table 22. Part Number Cross-Reference

TI PART NUMBER	DESCRIPTION	MANUFACTURER'S REFERENCE NAME	MANUFACTURER'S PROCESS CONTROL NUMBER
DLPC900ZPC	Production Units – DLPC900	DLPC900	T6WH0XBG-0001W2N

11.1.2 Device Markings



Marking Definitions:

Line 1: DLP logo

Line 2: DLP device name

Line 3: Foundry part number

Line 4: SSSSSSYYWW-QQ package assembly information
SSSSSS: Manufacturing site
YYWW: Date code (YY = Year :: WW = Week)
QQ: Qualification level option – Engineering samples are marked in this field with the suffix –ES.
For example, TAIWAN0324-ES would be engineering samples built in Taiwan the 24th week of 2003

Line 5: LLLLLLL G1 manufacturing lot code for semiconductor wafers and lead-free solder ball marking
LLLLLLL: Manufacturing lot code
G1: Lead-free solder balls consisting of SnAgCu

11.1.3 Video Timing Parameter Definitions

Active Lines Per Frame (ALPF) Defines the number of lines in a frame containing displayable data: ALPF is a subset of the TLPF.

Active Pixels Per Line (APPL) Defines the number of pixel clocks in a line containing displayable data: APPL is a subset of the TPPL.

Horizontal Back Porch (HBP) Blanking Number of blank pixel clocks after horizontal sync but before the first active pixel. Note: HBP times are reference to the leading (active) edge of the respective sync signal.

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Horizontal Front Porch (HFP) Blanking Number of blank pixel clocks after the last active pixel but before Horizontal Sync.

Horizontal Sync (HS) Timing reference point that defines the start of each horizontal interval (line). The absolute reference point is defined by the active edge of the HS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all horizontal blanking parameters are measured.

Total Lines Per Frame (TLPF) Defines the vertical period (or frame time) in lines: TLPF = Total number of lines per frame (active and inactive).

Total Pixel Per Line (TPPL) Defines the horizontal line period in pixel clocks: TPPL = Total number of pixel clocks per line (active and inactive).

Vertical Back Porch (VBP) Blanking Number of blank lines after vertical sync but before the first active line.

Vertical Front Porch (VFP) Blanking Number of blank lines after the last active line but before vertical sync.

Vertical Sync (VS) Timing reference point that defines the start of the vertical interval (frame). The absolute reference point is defined by the active edge of the VS signal. The active edge (either rising or falling edge as defined by the source) is the reference from which all vertical blanking parameters are measured.

11.2 Documentation Support

11.2.1 Related Documentation

The following documents contain additional information related to the use of the DLPC900 device.

Table 23. Related Documents

DOCUMENT	DOCUMENT LINK
DLP6500FLQ DMD Data Sheet	DLPS040
DLP6500FYE DMD Data Sheet	DLPS053
DLP9000 DMD Data Sheet	DLPS036
DLPC900 Programmer's Guide	DLPU018
DLP LightCrafter 6500 and 9000 EVM User's Guide	DLPU028
Reference Design Documentation	DLPLCR6500 DLPLCR9000

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

LightCrafter, E2E are trademarks of Texas Instruments.
DLP is a registered trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

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11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
DLPC900ZPC	ACTIVE	BGA	ZPC	516	1	Green (RoHS & no Sb/Br)	SNAGCU	Level-3-255C-168 HR			Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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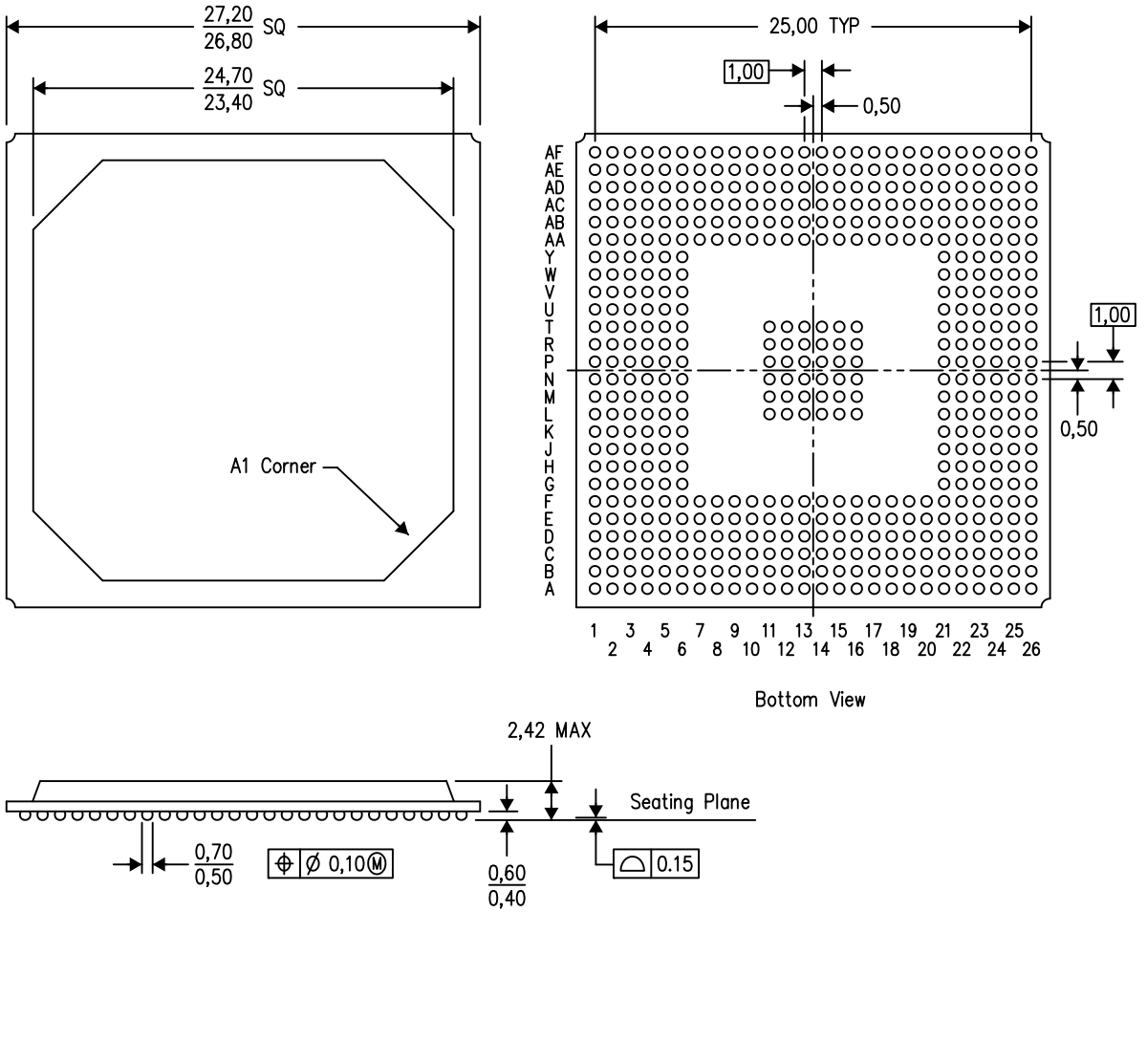
ZPC (S–PBGA–N516) PLASTIC BALL GRID ARRAY



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. This package is Pb–free.

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