Single Chip 12-Bit Data Acquisition System

FEATURES

- Built-In Sample-and-Hold
- Single Supply 5V Operation
- Power Shutdown
- Direct 3- or 4-Wire Interface to Most MPU Serial Ports and All MPU Parallel Ports
- Two-Channel Analog Multiplexer
- Analog Inputs Common Mode to Supply Rails
- 8-Pin DIP Package

KEY SPECIFICATIONS

- Resolution: 12 Bits
- Fast Conversion Time: 12µs Max Over Temp.
- Low Supply Current:
  6.0mA (Typ) Active Mode
  10µA (Max) Shutdown Mode

DESCRIPTION

The LTC®1291 is a data acquisition system that contains a serial I/O successive approximation A/D converter. It uses LTCMOS™ switched capacitor technology to perform a 12-bit unipolar A/D conversion. The input multiplexer can be configured for either single-ended or differential inputs. An on-chip sample-and-hold is included on the "+" input. When the LTC1291 is idle, it can be powered down in applications where low power consumption is desired. An external reference is not required because the LTC1291 takes its reference from the power supply (V_{CC}). All these features are packaged in an 8-pin DIP.

The serial I/O is designed to communicate without external hardware to most MPU serial ports and all MPU parallel I/O ports allowing data to be transmitted over three or four wires. Given the accuracy, ease of use and small package size, this device is well suited for digitizing analog signals in remote applications where minimum number of interconnects, small physical size, and low power consumption are important.

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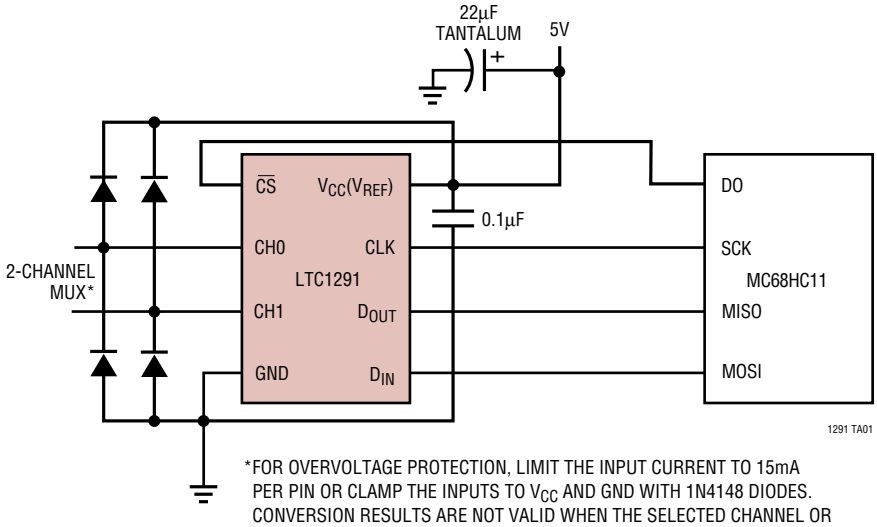
LTCMOS™ is a trademark of Linear Technology Corporation

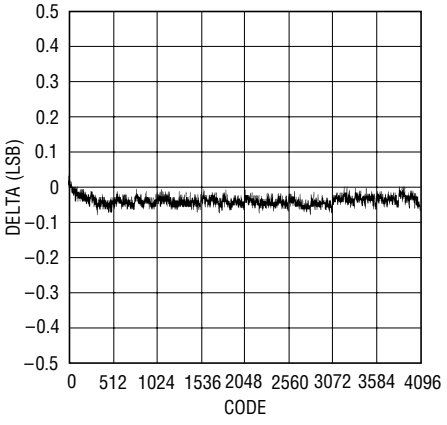
TYPICAL APPLICATION

2-Channel 12-Bit Data Acquisition System



*FOR OVERVOLTAGE PROTECTION, LIMIT THE INPUT CURRENT TO 15mA PER PIN OR CLAMP THE INPUTS TO V_{CC} AND GND WITH 1N4148 DIODES. CONVERSION RESULTS ARE NOT VALID WHEN THE SELECTED CHANNEL OR THE OTHER CHANNEL IS OVERVOLTAGED (V_{IN} < GND OR V_{IN} > V_{CC}). SEE SECTION ON OVERVOLTAGE PROTECTION IN THE APPLICATIONS INFORMATION.

Channel-to-Channel INL Matching

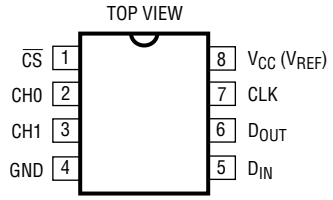


ABSOLUTE MAXIMUM RATINGS

(Notes 1 and 2)

Supply Voltage (V_{CC}) to GND 12V
Voltage
  Analog Inputs ..... −0.3V to V_{CC} + 0.3V
  Digital Inputs ..... −0.3V to 12V
  Digital Outputs ..... −0.3V to V_{CC} + 0.3V
Power Dissipation 500mW
Operating Temperature Range
  LTC1291BC, LTC1291CC,
  LTC1291DC ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

PACKAGE/ORDER INFORMATION



N8 PACKAGE
8-LEAD PLASTIC DIP
T_{JMAX} = 100°C, θ_{JA} = 130°C/W (N8)

J8 PACKAGE
8-LEAD CERAMIC DIP
T_{JMAX} = 150°C, θ_{JA} = 100°C/W (J8)

ORDER PART NUMBER
LTC1291BCN8 LTC1291CCN8 LTC1291DCN8
LTC1291BCJ8 LTC1291CCJ8 LTC1291DCJ8

OBSOLETE PACKAGE
Consider N8 Package for Alternate Source

Consult LTC Marketing for parts specified with wider operating temperature ranges.

CONVERTER AND MULTIPLEXER CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

PARAMETER	CONDITIONS		LTC1291B MIN	LTC1291B TYP	LTC1291B MAX	LTC1291C MIN	LTC1291C TYP	LTC1291C MAX	LTC1291D MIN	LTC1291D TYP	LTC1291D MAX	UNITS
Offset Error	(Note 4)	●			±3.0			±3.0			±3.0	LSB
Linearity Error (INL)	(Note 4 & 5)	●			±0.5			±0.5			±0.75	LSB
Gain Error	(Note 4)	●			±1.0			±2.0			±4.0	LSB
Minimum Resolution for which No Missing Codes are Guaranteed		●			12			12			12	Bits
Analog Input Range	(Note 7)			−0.05V to V_{CC} + 0.05V								V
On Channel Leakage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	µA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	µA
Off Channel Lekage Current (Note 8)	On Channel = 5V Off Channel = 0V	●			±1			±1			±1	µA
	On Channel = 0V Off Channel = 5V	●			±1			±1			±1	µA

AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1291B/LTC1291C/LTC1291D MIN	TYP	MAX	UNITS
f_{CLK}	Clock Frequency	V_{CC} = 5V (Note 6)		(Note 9)		1.0	MHz
t_{SMPL}	Analog Input Sample Time	See Operating Sequence			2.5		CLK Cycles
t_{CONV}	Conversion Time	See Operating Sequence			12		CLK Cycles
t_{CYC}	Total Cycle Time	See Operating Sequence (Note 6)		18 CLK + 500ns			Cycles
t_{dDO}	Delay Time, CLK↓ to D_{OUT} Data Valid	See Test Circuits	●		160	300	ns

AC CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1291B/LTC1291C/LTC1291D MIN	TYP	MAX	UNITS
t_{dis}	Delay Time, $\overline{CS}$↑ to D_{OUT} Hi-Z	See Test Circuits	●		80	150	ns
t_{en}	Delay Time, CLK↓ to D_{OUT} Enabled	See Test Circuits	●		80	200	ns
t_{hDI}	Hold Time, D_{IN} after CLK↑	V_{CC} = 5V (Note 6)		50			ns
t_{hDO}	Time Output Data Remains Valid after CLK↓				130		ns
t_{WHCLK}	CLK High Time	V_{CC} = 5V (Note 6)		300			ns
t_{WLCLK}	CLK Low Time	V_{CC} = 5V (Note 6)		400			ns
t_f	D_{OUT} Fall Time	See Test Circuits	●		65	130	ns
t_r	D_{OUT} Rise Time	See Test Circuits	●		25	50	ns
t_{suDI}	Setup Time, D_{IN} Stable before CLK↑	V_{CC} = 5V (Note 6)		50			ns
$t_{su\overline{CS}}$	Setup Time, $\overline{CS}$↓ before CLK↑	V_{CC} = 5V (Note 6)		50			ns
$t_{WH\overline{CS}}$	$\overline{CS}$ High Time During Conversion	V_{CC} = 5V (Note 6)		500			ns
$t_{WL\overline{CS}}$	$\overline{CS}$ Low Time During Data Transfer	V_{CC} = 5V (Note 6)		18			CLK Cycles
C_{IN}	Input Capacitance	Analog Inputs On Channel			100		pF
		Analog Inputs Off Channel			5		pF
		Digital Inputs			5		pF

DIGITAL AND DC ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the full operating temperature range, otherwise specifications are at T_A = 25°C. (Note 3)

SYMBOL	PARAMETER	CONDITIONS		LTC1291B/LTC1291C/LTC1291D MIN	TYP	MAX	UNITS
V_{IH}	High Level Input Voltage	V_{CC} = 5.25V	●	2.0			V
V_{IL}	Low Level Input Voltage	V_{CC} = 4.75V	●			0.8	V
I_{IH}	High Level Input Current	V_{IN} = V_{CC}	●			2.5	µA
I_{IL}	Low Level Input Current	V_{IN} = 0V	●			–2.5	µA
V_{OH}	High Level Output Voltage	V_{CC} = 4.75V, I_{OUT} = –10µA			4.7		V
		V_{CC} = 4.75V, I_{OUT} = –360µA	●	2.4	4.0		V
V_{OL}	Low Level Output Voltage	V_{CC} = 4.75V, I_{OUT} = 1.6mA	●			0.4	V
I_{OZ}	High Z Output Leakage	V_{OUT} = V_{CC}, $\overline{CS}$ High	●			3	µA
		V_{OUT} = 0V, $\overline{CS}$ High	●			–3	µA
I_{SOURCE}	Output Source Current	V_{OUT} = 0V			–20		mA
I_{SINK}	Output Sink Current	V_{OUT} = V_{CC}			20		mA
I_{CC}	Positive Supply Current	$\overline{CS}$ High	●		6	12	mA
		$\overline{CS}$ High Power Shutdown CLK Off	●		5	10	µA

Note 1: Absolute Maximum Ratings are those values beyond which the life of a device may be impaired.

Note 2: All voltage values are with respect to ground (unless otherwise noted).

Note 3: V_{CC} = 5V, CLK = 1.0MHz unless otherwise specified.

Note 4: One LSB is equal to V_{CC} divided by 4096. For example, when V_{CC} = 5V, 1LSB = 5V/4096 = 1.22mV.

Note 5: Linearity error is specified between the actual end points of the A/D transfer curve. The deviation is measured from the center of the quantization band.

Note 6: Recommended operating conditions.

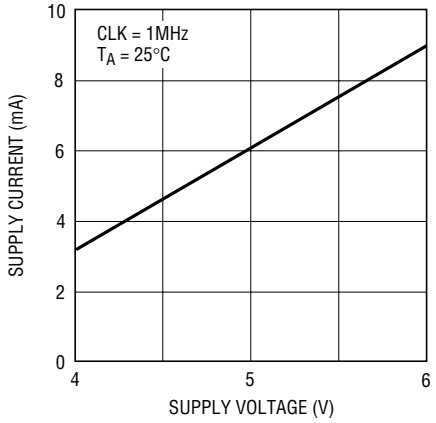
Note 7: Two on-chip diodes are tied to each analog input which will conduct for analog voltages one diode drop below GND or one diode drop above V_{CC}. Be careful during testing at low V_{CC} levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperature, and cause errors for inputs near full scale. This spec allows 50mV forward bias of either diode. This means that as long as the analog input does not exceed the supply voltage by more than 50mV, the output code will be correct.

Note 8: Channel leakage current is measured after the channel selection.

Note 9: Increased leakage currents at elevated temperatures cause the S/H to droop, therefore it is recommended that $f_{CLK} \geq 125kHz$ at 125°C, $f_{CLK} \geq 30kHz$ at 85°C and $f_{CLK} \geq 3kHz$ at 25°C.

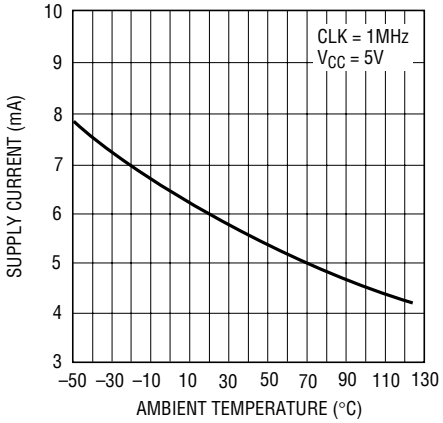
TYPICAL PERFORMANCE CHARACTERISTICS

Supply Current vs Supply Voltage



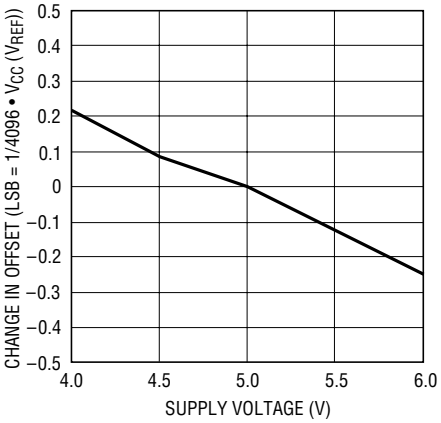
1291 G01

Supply Current vs Temperature



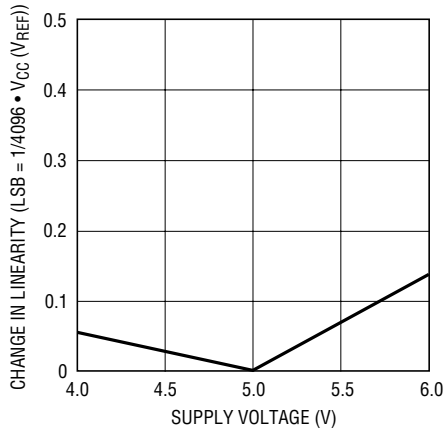
1291 G02

Change in Offset vs Supply Voltage



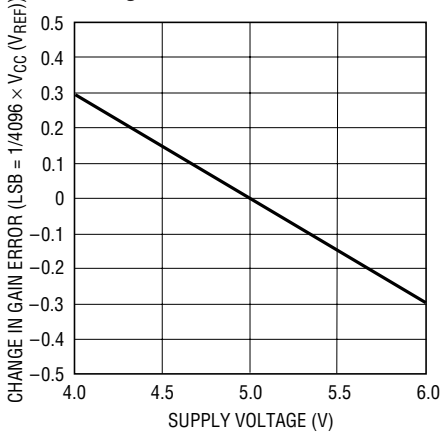
1291 G03

Change in Linearity vs Supply Voltage



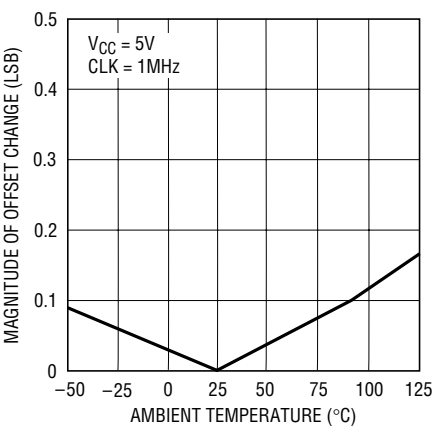
1291 G04

Change in Gain Error vs Supply Voltage



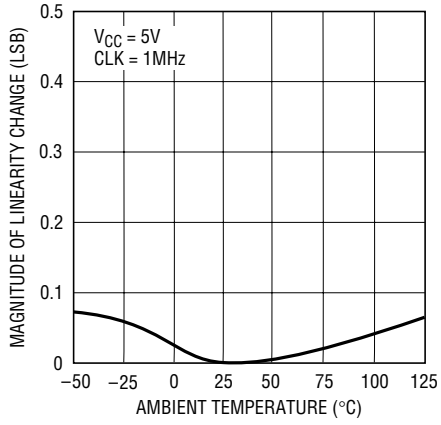
1291 G05

Change in Offset vs Temperature



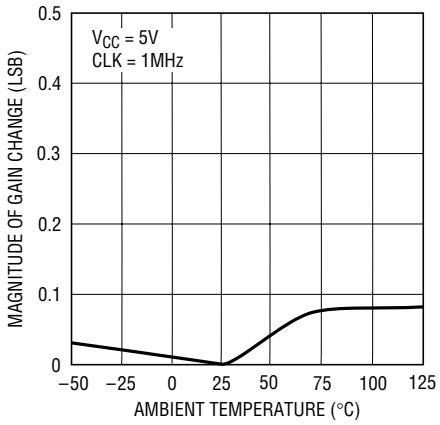
1291 G06

Change in Linearity vs Temperature



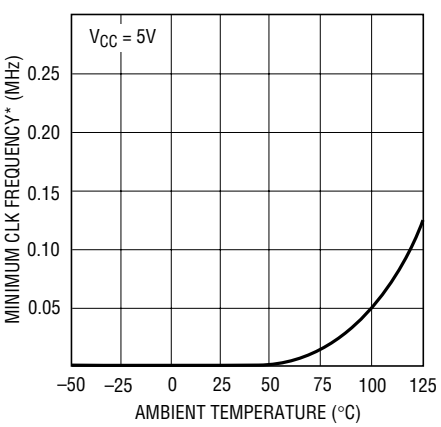
1291 G07

Change in Gain vs Temperature



1291 G08

Minimum Clock Rate for 0.1 LSB Error

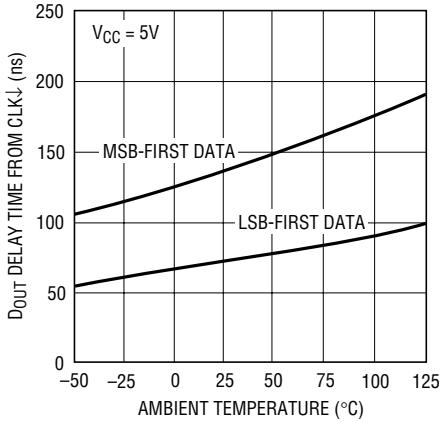


1291 G09

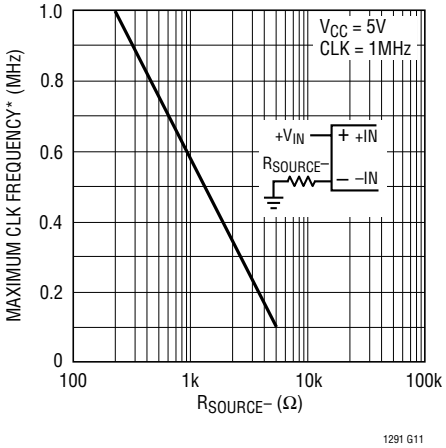
* AS THE CLK FREQUENCY IS DECREASED FROM 1MHz, MINIMUM CLK FREQUENCY (ΔERROR ≤ 0.1LSB) REPRESENTS THE FREQUENCY AT WHICH A 0.1LSB SHIFT IN ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED

TYPICAL PERFORMANCE CHARACTERISTICS

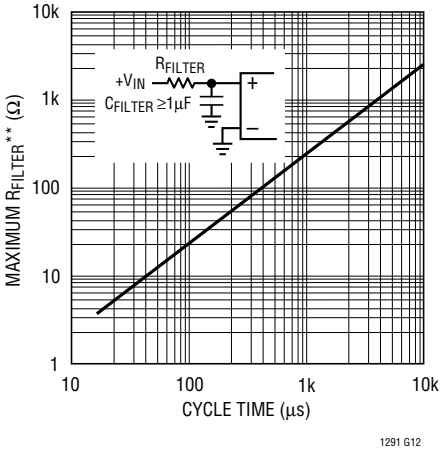
D_{OUT} Delay Time vs Temperature



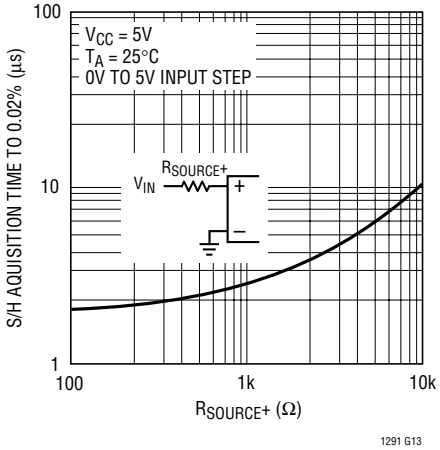
Maximum Clock Rate vs Source Resistance



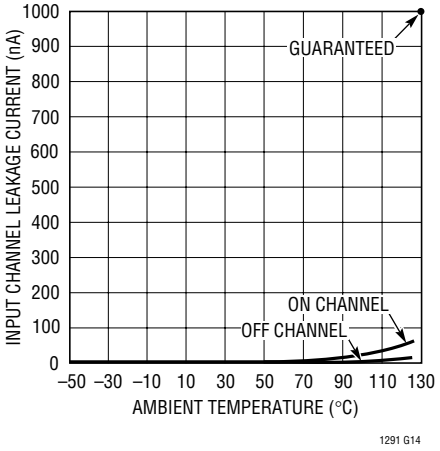
Maximum Filter Resistor vs Cycle Time



Sample-and-Hold Acquisition Time vs Source Resistance



Input Channel Leakage Current vs Temperature



* MAXIMUM CLK FREQUENCY REPRESENTS THE CLK FREQUENCY AT WHICH A 0.1LSB SHIFT IN THE ERROR AT ANY CODE TRANSITION FROM ITS 1MHz VALUE IS FIRST DETECTED

** MAXIMUM R_{FILTER} REPRESENTS THE FILTER RESISTOR VALUE AT WHICH A 0.1LSB CHANGE IN FULL SCALE ERROR FROM ITS VALUE AT R_{FILTER} = 0Ω IS FIRST DETECTED

PIN FUNCTIONS

$\overline{CS}$ (Pin 1): Chip Select Input. A logic low on this input enables the LTC1291.

CH0, CH1 (Pins 2, 3): Analog Inputs. These inputs must be free of noise with respect to GND.

GND (Pin 4): Analog Ground. GND should be tied directly to an analog ground plane.

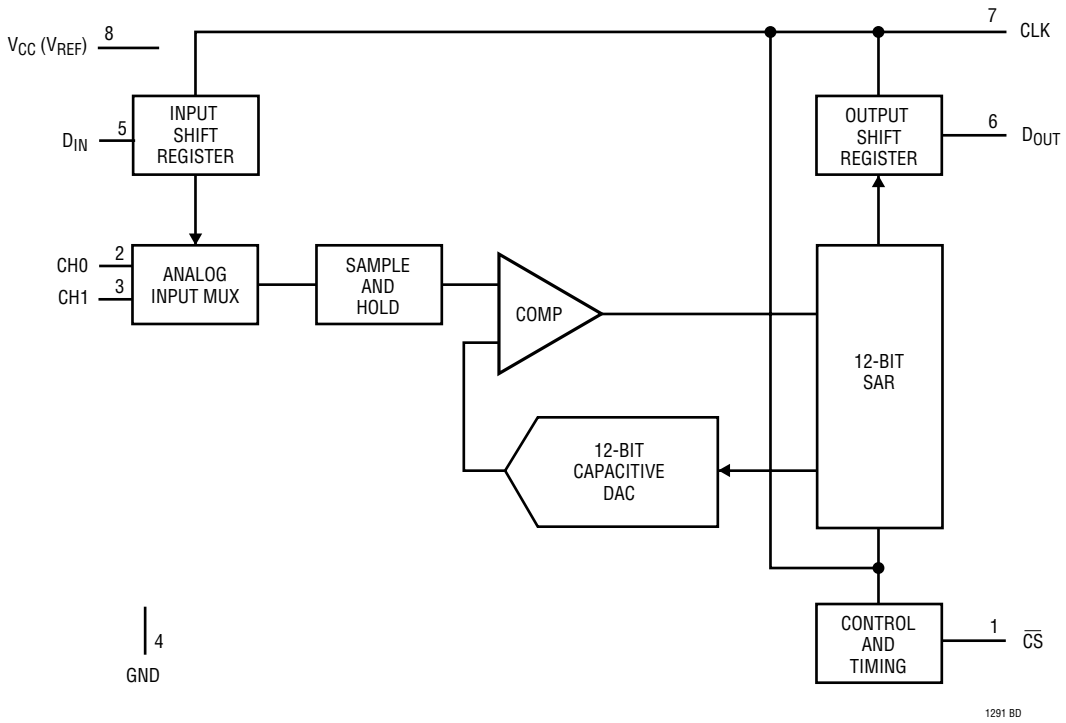
D_{IN} (Pin 5): Digital Data Input. The multiplexer address is shifted into this input.

D_{OUT} (Pin 6): Digital Data Output. The A/D conversion result is shifted out of this output.

CLK (Pin 7): Shift Clock. This clock synchronizes the serial data transfer.

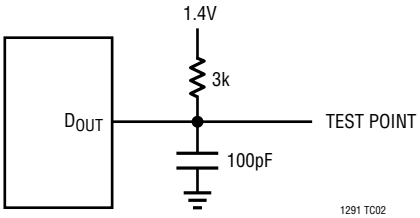
V_{CC}(V_{REF}) (Pin 8): Positive Supply and Reference Voltage. This pin provides power and defines the span of the A/D converter. This supply must be kept free of noise and ripple by bypassing directly to the analog ground plane.

BLOCK DIAGRAM

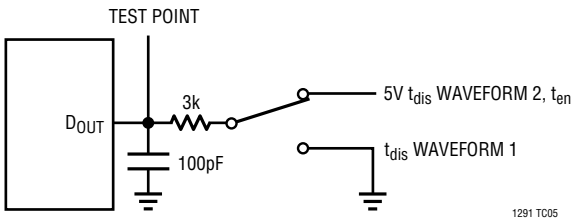


TEST CIRCUITS

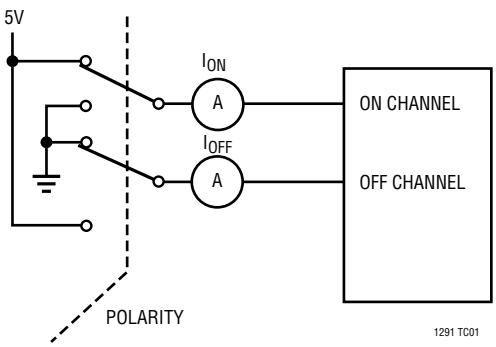
Load Circuit for t_{dDO}, t_r and t_f



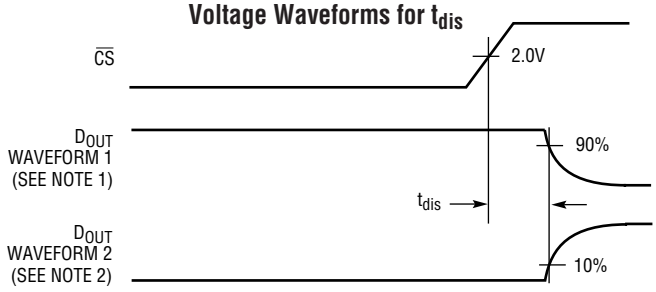
Load Circuit for t_{dis} and t_{en}



On and Off Channel Leakage Current



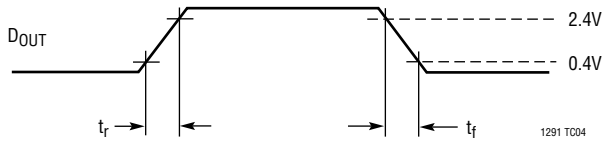
Voltage Waveforms for t_{dis}



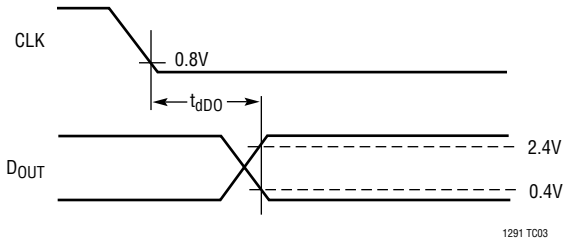
NOTE 1: WAVEFORM 1 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS HIGH UNLESS DISABLED BY THE OUTPUT CONTROL.
NOTE 2: WAVEFORM 2 IS FOR AN OUTPUT WITH INTERNAL CONDITIONS SUCH THAT THE OUTPUT IS LOW UNLESS DISABLED BY THE OUTPUT CONTROL.

TEST CIRCUITS

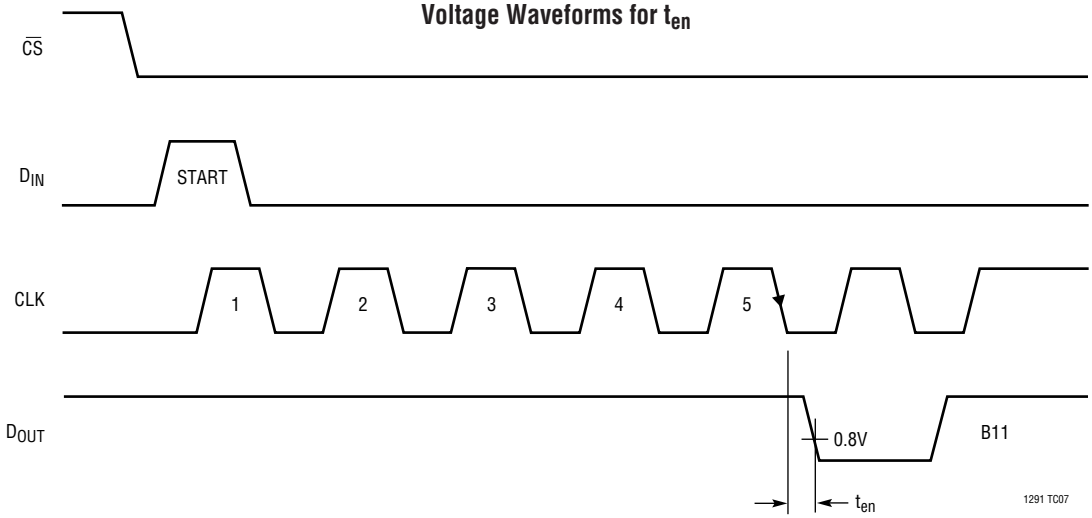
Voltage Waveforms for D_{OUT} Rise and Fall Times, t_r, t_f



Voltage Waveforms for D_{OUT} Delay Time, t_{dDO}



Voltage Waveforms for t_{en}



APPLICATIONS INFORMATION

The LTC1291 is a data acquisition component which contains the following functional blocks:

1. 12-bit successive approximation capacitive A/D converter
2. Analog multiplexer (MUX)
3. Sample-and-hold (S/H)
4. Synchronous, half duplex serial interface
5. Control and timing logic

DIGITAL CONSIDERATIONS

Serial Interface

The LTC1291 communicates with microprocessors and other external circuitry via a synchronous, half duplex, 4-wire serial interface (see Operating Sequence). The clock (CLK) synchronizes the data transfer with each bit being transmitted on the falling CLK edge and captured on the rising CLK edge in both transmitting and receiving systems.

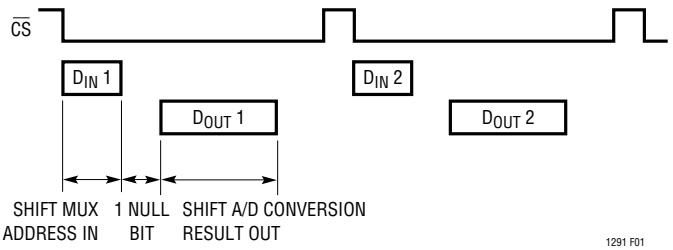


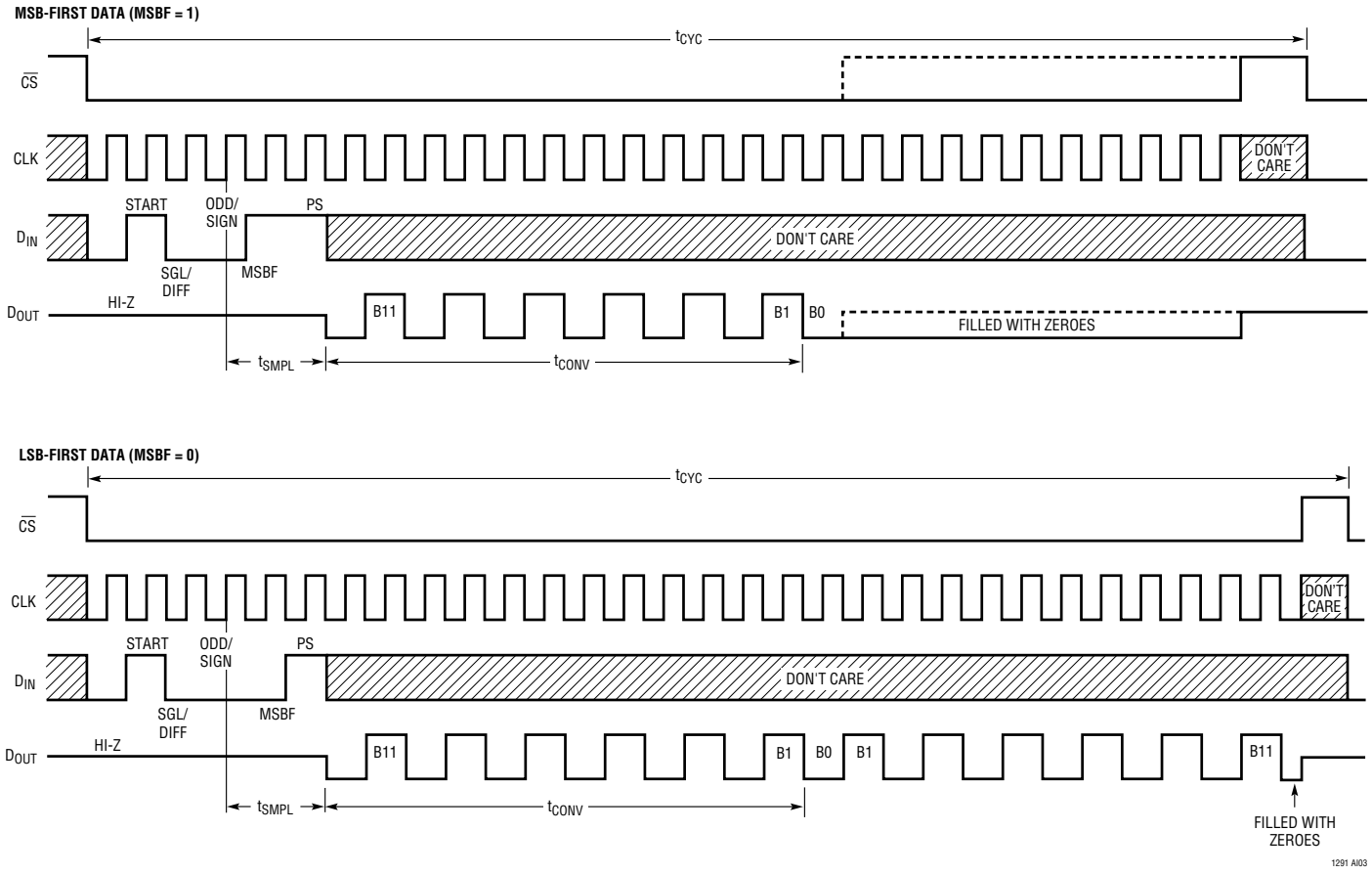
Figure 1

The input data is first received and then the A/D conversion result is transmitted (half duplex). Because of the half duplex operation D_{IN} and D_{OUT} may be tied together allowing transmission over just 3 wires: $\overline{CS}$, CLK and

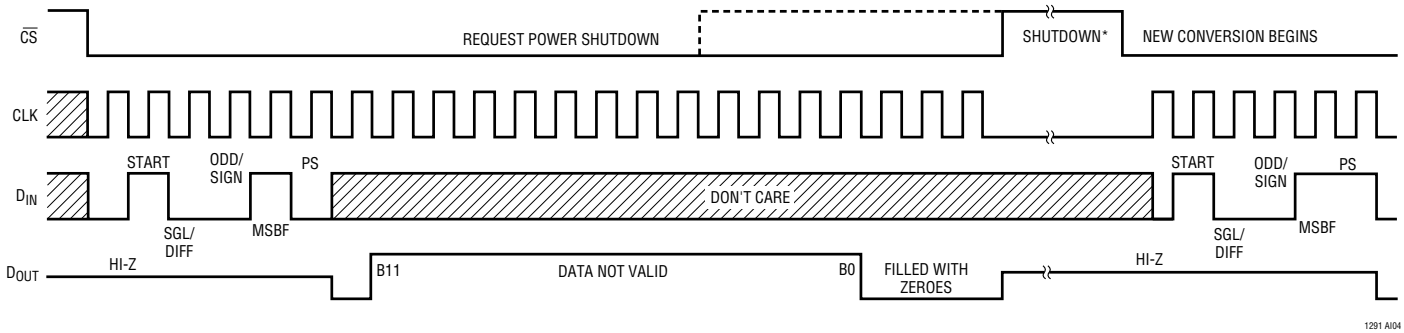
APPLICATIONS INFORMATION

DATA (D_{IN}/D_{OUT}). Data transfer is initiated by a falling chip select ($\overline{CS}$) signal. After $\overline{CS}$ falls, the LTC1291 looks for a start bit. After the start bit is received, a 4-bit input word is shifted into the D_{IN} input which configures the LTC1291 and starts the conversion. After one null bit, the result of the conversion appears MSB-first on the D_{OUT} line. The conversion result is output, bit by bit, as the conversion is performed. At the end of the data exchange, $\overline{CS}$ should be brought high. This resets the LTC1291 in preparation for the next data exchange.

Operating Sequence
(Example: Differential Inputs (CH0$^+$, CH1$^-$))



Power Shutdown Operating Sequence
(Example: Differential Inputs (CH0$^+$, CH1$^-$) and MSB-First Data)



* STOPPING THE CLOCK WILL HELP REDUCE POWER CONSUMPTION
$\overline{CS}$ CAN BE BROUGHT HIGH ONCE D_{IN} HAS BEEN CLOCKED IN

APPLICATIONS INFORMATION

Input Data Word

The 4-bit data word is clocked into the D_{IN} pin on the rising edge of the clock after chip select goes low and the start bit has been recognized. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle. The input word is defined as follows:

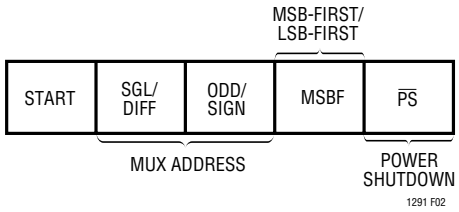


Figure 2. Input Data Word

Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer and all leading zeroes which precede this logical one will be ignored. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

MUX Address

The bits of the input word following the START BIT assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the "+" and "–" signs in the selected row of the following table. In single-ended mode, all input channels are measured with respect to GND. Only the "+" inputs have sample-and-holds. Signals applied at the "–" inputs must not change more than the required accuracy during the conversion.

Multiplexer Channel Selection

MUX ADDRESS		CHANNEL #		
SGL/DIFF	ODD/SIGN	0	1	GND
1	0	+		–
1	1		+	–
0	0	+	–	
0	1	–	+	

MSB-First/LSB-First (MSBF)

The output data of the LTC1291 is programmed for MSB-first or LSB-first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB-first format. Logical zeroes will be filled in indefinitely following the last data bit to accommodate longer word lengths required by some microprocessors. When the MSBF bit is a logical zero, LSB-first data will follow the normal MSB-first data on the D_{OUT} line (see Operating Sequence).

Power Shutdown

The power shutdown feature of the LTC1291 is activated by making the $\overline{PS}$ bit a logical zero. If $\overline{CS}$ remains low after the PS bit has been received, a 12-bit D_{OUT} word with all logical ones will be shifted out followed by logical zeroes until $\overline{CS}$ goes high. Then the D_{OUT} line will go into its high impedance state. The LTC1291 will remain in the shutdown mode until the next $\overline{CS}$ cycle. There is no warm-up or wait period required after coming out of the power shutdown cycle so a conversion can commence after $\overline{CS}$ goes low (see Power Shutdown Operating Sequence).

APPLICATIONS INFORMATION

Output Code

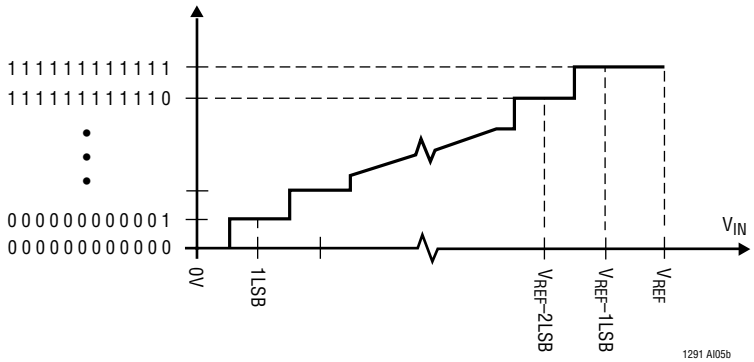
The LTC1291 performs a unipolar conversion. The following shows the output code and transfer curve:

Unipolar Output Code

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5V)
1 1 1 1 1 1 1 1 1 1 1 1	V_{REF} – 1LSB	4.9988V
1 1 1 1 1 1 1 1 1 1 1 0	V_{REF} – 2LSB	4.9976V
•	•	•
•	•	•
•	•	•
0 0 0 0 0 0 0 0 0 0 0 1	1LSB	0.0012V
0 0 0 0 0 0 0 0 0 0 0 0	0V	0V

1291 AI05a

Unipolar Transfer Curve



1291 AI05b

Microprocessor Interfaces

The LTC1291 can interface directly (without external hardware) to most popular microprocessors's (MPU) synchronous serial formats (see Table 1). If an MPU without a dedicated serial port is used, then three of the MPU's parallel port lines can be programmed to form the serial link to the LTC1291. Included here are one serial interface example and one example showing a parallel port programmed to form the serial interface.

Motorola SPI (MC68HC11)

The MC68HC11 has been chosen as an example of an MPU with a dedicated serial port. This MPU transfers data MSB -first and in 8-bit increments. The D_{IN} word sent to the data register starts the SPI process. With three 8-bit transfers, the A/D result is read into the MPU. The second 8-bit transfer clocks B11 through B8 of the A/D conversion result into the processor. The third 8-bit transfer clocks the remaining bits, B7 through B0, into the MPU. The data is right justified in the two memory locations. ANDing the second byte with $0D_{HEX}$ clears the four most significant bits. This operation was not included in the code. It can be inserted in the data gathering loop or outside the loop when the data is processed.

Table 1. Microprocessor with Hardware Serial Interfaces Compatible with the LTC1291**

PART NUMBER	TYPE OF INTERFACE
Motorola	
MC6805S2, S3	SPI
MC68HC11	SPI
MC68HC05	SPI
RCA	
CDP68HC05	SPI
Hitachi	
HD6305	SCI Synchronous
HD6301	SCI Synchronous
HD63701	SCI Synchronous
HD6303	SCI Synchronous
HD64180	SCI Synchronous
National Semiconductor	
COP400 Family	MICROWIRE†
COP800 Family	MCROWIRE/PLUS†
NS8050U	MICROWIRE/PLUS
HPC16000 Family	MICROWIRE/PLUS
Texas Instruments	
TMS7002	Serial Port
TMS7042	Serial Port
TMS70C02	Serial Port
TMS70C42	Serial Port
TMS32011*	Serial Port
TMS32020*	Serial Port
TMS370C050	SPI

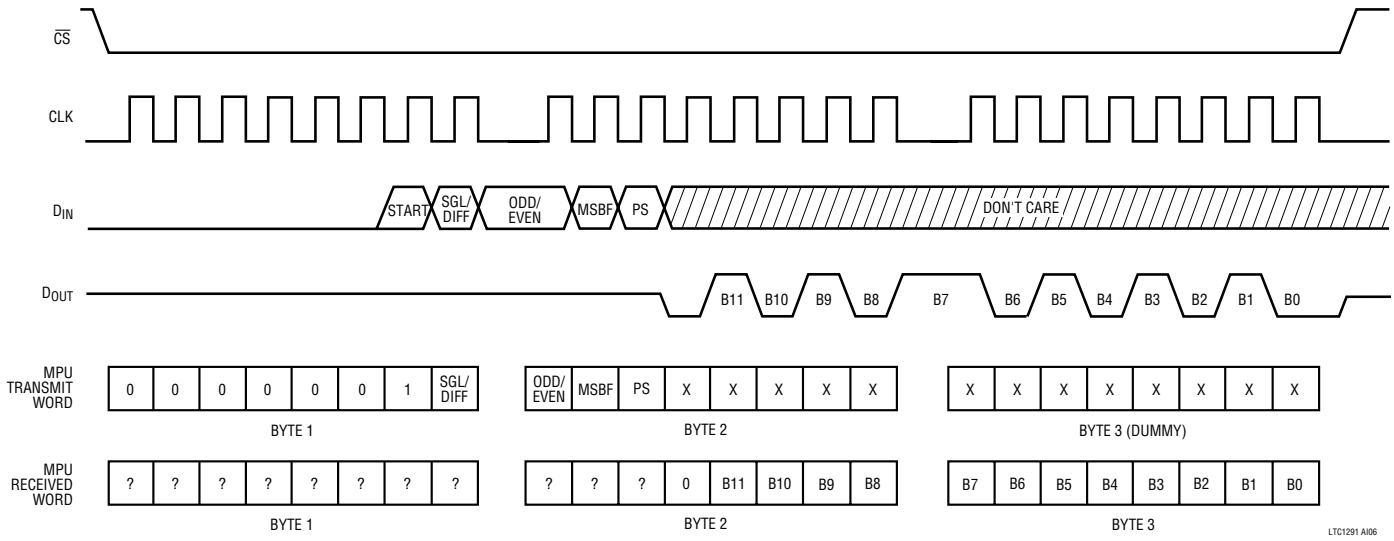
* Requires external hardware

** Contact LTC marketing for interface information for processors not on this list

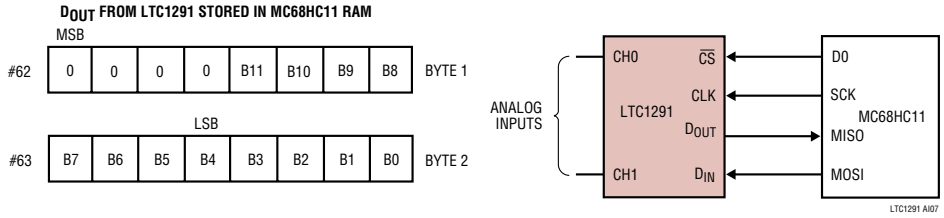
† MICROWIRE and MICROWIRE/PLUS are trademarks of National Semiconductor Corporation.

APPLICATIONS INFORMATION

Timing Diagram for Interface to the MC68HC11



Hardware and Software Interface to Motorola MC68HC11



MC68HC11 CODE

In this example the D_{IN} word configures the input MUX for a single-ended input to be applied to CH0. The conversion result is output MSB-first.

LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	#$50	CONFIGURATION DATA FOR SPCR		LDAA	#$00	LOAD DUMMY DIN WORD INTO ACC A
	STAA	$1028	LOAD DATA INTO SPCR ($1028)		STAA	$52	LOAD DUMMY DIN DATA INTO $52
	LDAA	#$1B	CONFIG. DATA FOR PORT D DDR		LDX	#$1000	LOAD INDEX REGISTER X WITH $1000
	STAA	$1009	LOAD DATA INTO PORT D DDR				
	LDAA	#$03	LOAD DIN WORD INTO ACC A	LOOP	BCLR	$08,X,#$01	D0 GOES LOW ($\overline{CS}$ GOES LOW)
	STAA	$50	LOAD DIN DATA INTO $50		LDAA	$50	LOAD DIN INTO ACC A FROM $50
	LDAA	#$60	LOAD DIN WORD INTO ACC A		STAA	$102A	LOAD DIN INTO SPI, START SCK
	STAA	$51	LOAD DIN DATA INTO $51				

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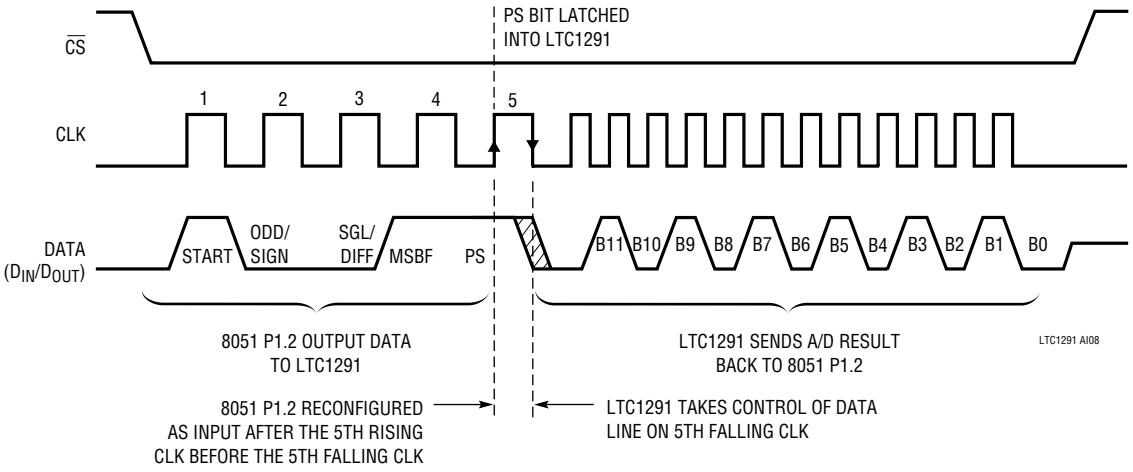
LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	LDAA	$1029	CHECK SPI STATUS REG		STAA	$102A	LOAD DUMMY DIN INTO SPI, START SCK
WAIT1	BPL	WAIT1	CHECK IF TRANSFER IS DONE				
	LDAA	$51	LOAD DIN INTO ACC A FROM $51	WAIT3	LDAA	$1029	CHECK SPI STATUS REG
	STAA	$102A	LOAD DIN INTO SPI, START SCK		BPL	WAIT3	CHECK IF TRANSFER IS DONE
WAIT2	LDAA	$1029	CHECK SPI STATUS REG		BSET	$08,X#$01	D0 GOES HIGH ($\overline{CS}$ GOES HIGH)
	BPL	WAIT2	CHECK IF TRANSFER IS DONE		LDAA	$102A	LOAD LTC1291 LSBs IN ACC
	LDAA	$102A	LOAD LTC1291 MSBs INTO ACC A		STAA	$63	STORE LSBs IN $63
	STAA	$62	STORE MSBs IN $62				
	LDAA	$52	LOAD DUMMY DIN INTO ACC A FROM $52		JMP	LOOP	START NEXT CONVERSION

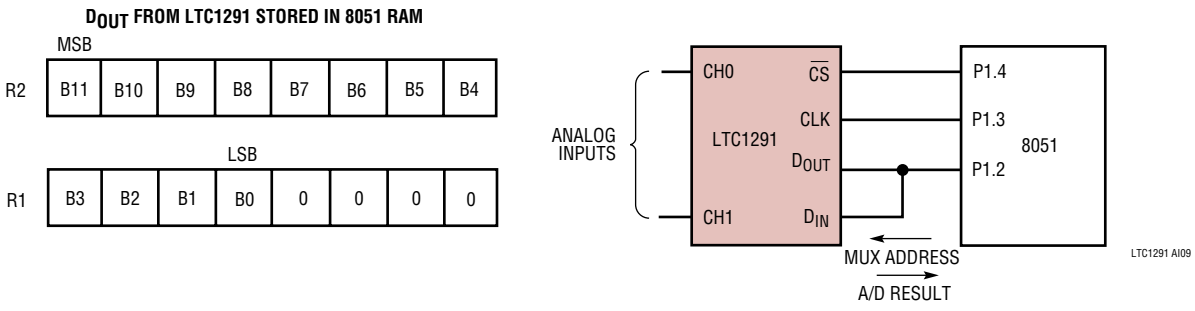
Interfacing to the Parallel Port of the Intel 8051 Family

The Intel 8051 has been chosen to show the interface between the LTC1291 and parallel port microprocessors. Usually the signals $\overline{CS}$, D_{IN} and CLK are generated on three port lines and the D_{OUT} signal is read on a fourth port line. This works very well. One can save a line by tying the D_{IN} and D_{OUT} lines together. The 8051 first sends the start bit and MUX Address to the LTC1291 over the line connected to P1.2. Then P1.2 is reconfigured as an input and the 8051 reads back the 12-bit A/D result over the same data line.

Timing Diagram for Interface to Intel 8051



Hardware and Software Interface to Intel 8051



APPLICATIONS INFORMATION

8051 Code

In this example the input MUX is configured to accept a differential input between CH0 and CH1. The result from the conversion is clocked out MSB-first.

LABEL	MNEMONIC	OPERAND	COMMENTS	LABEL	MNEMONIC	OPERAND	COMMENTS
	SETB	P1.4	$\overline{CS}$ GOES HIGH		CLR	P1.3	CLK GOES LOW
CONT	MOV	A,#98H	DIN WORD FOR LTC1291		CLR	A	CLEAR ACC
	CLR	P1.4	$\overline{CS}$ GOES LOW		RLC	A	ROTATE DATA BIT (B3) INTO ACC
	MOV	R4,#05H	LOAD COUNTER		MOV	C,P1.2	READ DATA BIT INTO CARRY
LOOP1	RLC	A	ROTATE DIN BIT INTO CARRY		RLC	A	ROTATE DATA BIT (B2) INTO ACC
	CLR	P1.3	CLK GOES LOW		SETB	P1.3	CLK GOES HIGH
	MOV	P1.2,C	OUTPUT DIN BIT TO LTC1291		CLR	P1.3	CLK GOES LOW
	SETB	P1.3	CLK GOES HIGH		MOV	C,P1.2	READ DATA BIT INTO CARRY
	DJNZ	R4,LOOP1	NEXT DIN BIT		RLC	A	ROTATE DATA BIT (B1) INTO ACC
	MOV	P1,#04H	P1.2 BECOMES AN INPUT		SETB	P1.3	CLK GOES HIGH
	CLR	P1.3	CLK GOES LOW		CLR	P1.3	CLK GOES LOW
	MOV	R4,#09H	LOAD COUNTER		MOV	C,P1.2	READ DATA BIT INTO CARRY
LOOP	MOV	C,P1.2	READ DATA BIT INTO CARRY		SETB	P1.4	$\overline{CS}$ GOES HIGH
	RLC	A	ROTATE DATA BIT (B3) INTO ACC		RRC	A	ROTATE DATA BIT (B0) INTO ACC
	SETB	P1.3	CLK GOES HIGH		RRC	A	ROTAGE RIGHT INTO ACC
	CLR	P1.3	CLK GOES LOW		RRC	A	ROTAGE RIGHT INTO ACC
	DJNZ	R4,LOOP	NEXT DOUT BIT		RRC	A	ROTAGE RIGHT INTO ACC
	MOV	R2,A	STORE MSBS IN R2		MOV	R3,A	STORE LSBs IN R3
	MOV	C,P1.2	READ DATA BIT INTO CARRY		AJMP	CONT	START NEXT CONVERSION
	SETB	P1.3	CLK GOES HIGH				

Sharing the Serial Interface

The LTC1291 can share the same 3-wire serial interface with other peripheral components or other LTC1291s (Figure 3). The $\overline{CS}$ signals decide which LTC1291 is being addressed by MPU.

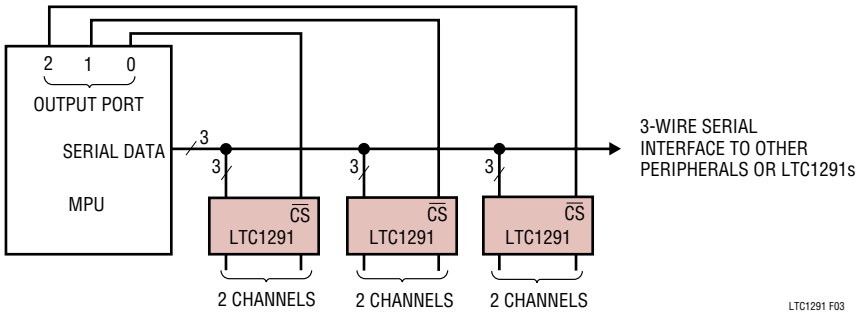


Figure 3. Several LTC1291s Sharing One 3-Wire Serial Interface

APPLICATIONS INFORMATION

ANALOG CONSIDERATIONS

Grounding

The LTC1291 should be used with an analog ground plane and single point grounding techniques. Do not use wire wrapping techniques to breadboard and evaluate the device. To achieve the optimum performance, use a PC board. The ground pin (Pin 4) should be tied directly to the ground plane with minimum lead length. Figure 4 shows an example of an ideal LTC1291 ground plane for a two-sided board. Of course this much ground plane will not always be possible, but users should strive to get as close to this ideal as possible.

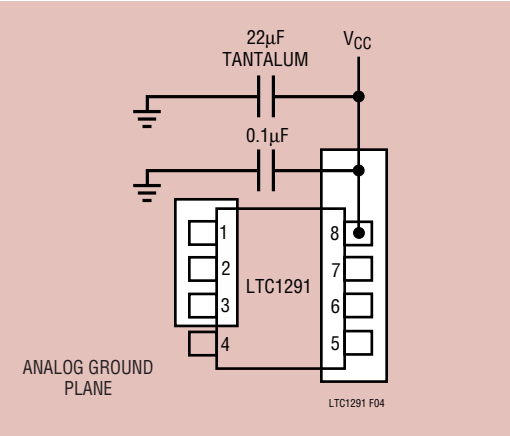


Figure 4. Example Ground Plane for the LTC1291

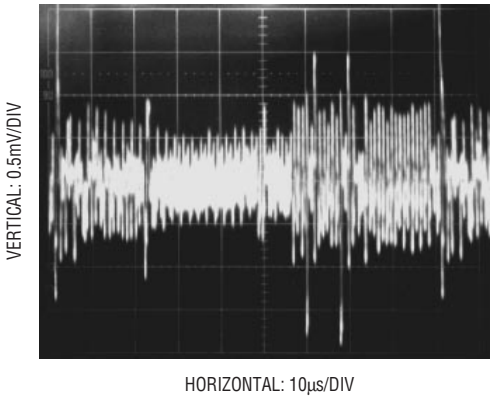


Figure 5. Poor V_{CC} Bypassing. Noise and Ripple Can Cause A/D Errors

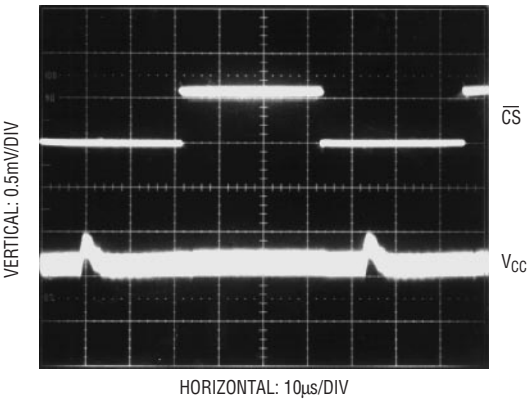


Figure 6. Good V_{CC} Bypassing Keeps Noise and Ripple on V_{CC} Below 1mV

Bypassing

For good performance, V_{CC} must be free of noise and ripple. Any changes in the V_{CC} voltage with respect to ground during the conversion cycle can induce error or noise in the output code. V_{CC} noise and ripple can be kept below 0.5mV by bypassing the V_{CC} pin directly to the analog ground plane with a minimum of 22µF tantalum capacitor and with leads as short as possible. A 0.1µF ceramic disk capacitor should also be placed directly across V_{CC} (Pin 8) and GND (Pin 4) as close to the pins as possible. The V_{CC} supply should have a low output impedance such as that obtained from a voltage regulator (e.g., LT323A). Figures 5 and 6 show the effects of good and poor V_{CC} bypassing.

Analog Inputs

Because of the capacitive redistribution A/D conversion techniques used, the analog inputs of the LTC1291 have capacitive switching input current spikes. These current spikes settle quickly and do not cause a problem. If large source resistances are used or if slow settling op amps drive the inputs, take care to insure the transients caused by the current spikes settle completely before the conversion begins.

Minimizing Gain and Offset Error

Because the LTC1291's reference is taken from the power supply pin (V_{CC}), proper PC board layout and supply bypassing is important for attaining the best performance from the A/D converter. Any parasitic resistance in the V_{CC}

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or GND lead will cause gain errors and offset errors (Figure 7). For the best performance the LTC1291 should be soldered directly to the PC board. If the source can not be placed next to the pin and the gain parameter is important, the pin should be Kelvin-sensed to eliminate parasitic resistances due to long PC traces. For example, 0.1Ω of resistance in the V_{CC} lead can typically cause 0.5LSB (I_{CC} • 0.1Ω/V_{CC}) of gain error for V_{CC} = 5V.

When the input MUX is selected for single-ended input the minus terminal is connected to GND internally on the die. Any parasitic resistance from the GND pin to the ground plane will lead to an offset voltage (I_{CC} • R_{P2}).

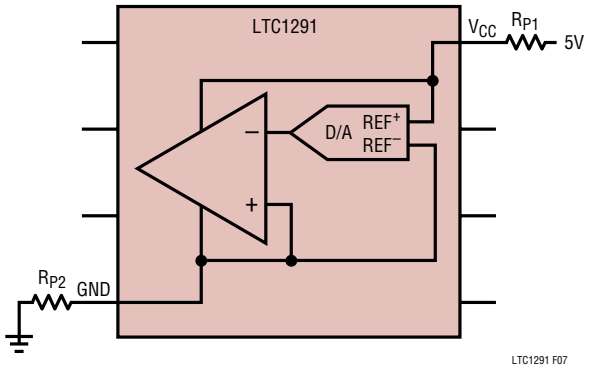

Figure 7. Parasitic Resistance in the V_{CC} and GND Leads

Source Resistance

The analog inputs of the LTC1291 look like a 100pF capacitor (C_{IN}) in series with a 500Ω resistor (R_{ON}). C_{IN} gets switched between "+" and "–" inputs once during each conversion cycle. Large external source resistors and capacitances will slow the settling of the inputs. It is important that the overall RC time constant is short enough to allow the analog inputs to settle completely within the allowed time.

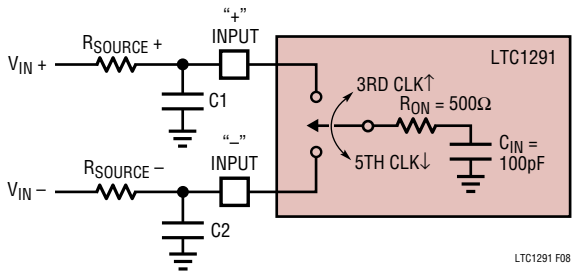

Figure 8. Analog Input Equivalent Circuit

"+" Input Settling

The input capacitor is switched onto the "+" input during the sample phase (t_{SMPL}, see Figure 9). The sample period is 2.5 CLK cycles before a conversion starts. The voltage on the "+" input must settle completely within the sample period. Minimizing R_{SOURCE}+ and C1 will improve the settling time. If large "+" input source resistance must be used, the sample time can be increased by using a slower CLK frequency. With the minimum possible sample time of 2.5µs, **R_{SOURCE}+ < 1.0k and C1 < 20pF will provide adequate settle time.**

"–" Input Settling

At the end of the sample phase the input capacitor switches to the "–" input and the conversion starts (see Figure 9). During the conversion, the "+" input voltage is effectively "held" by the sample-and-hold and will not affect the conversion result. It is critical that the "–" input voltage be free of noise and settle completely during the first CLK cycle of the conversion. Minimizing R_{SOURCE}– and C2 will improve settling time. If large "–" input source resistance must be used, the time can be extended by using a slower CLK frequency. At the maximum CLK frequency of 1MHz, **R_{SOURCE}– < 250Ω and C2 < 20pF will provide adequate settling.**

Input Op Amps

When driving the analog inputs with an op amp, it is important that the op amp settles within the allowed time (see Figure 9). Again the "+" and "–" input sampling times can be extended as described above to accommodate slower op amps. Most op amps including the LT1006 and LT1013 single supply op amps can be made to settle well even with the minimum settling windows of 2.5µs ("+" input) and 1µs ("–" input) that occurs at the maximum clock rate of 1MHz. Figures 10 and 11 show examples adequate and poor op amp settling.

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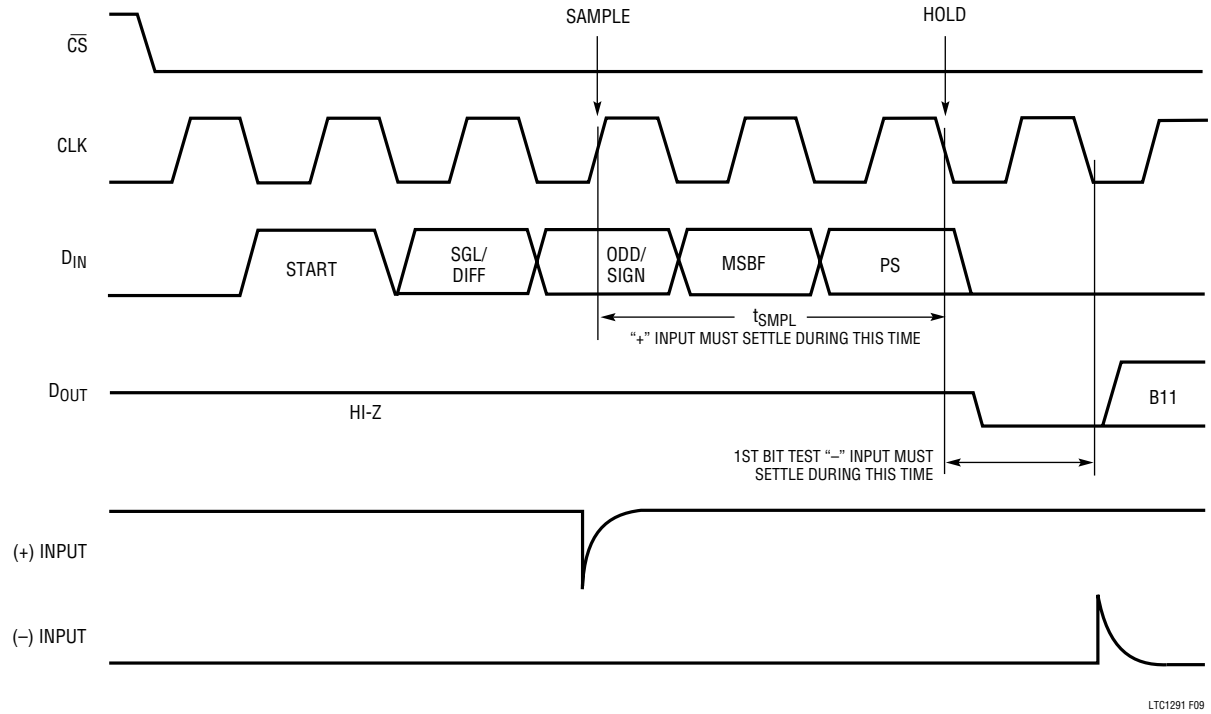

Figure 9. "+" and "–" Input Settling Windows

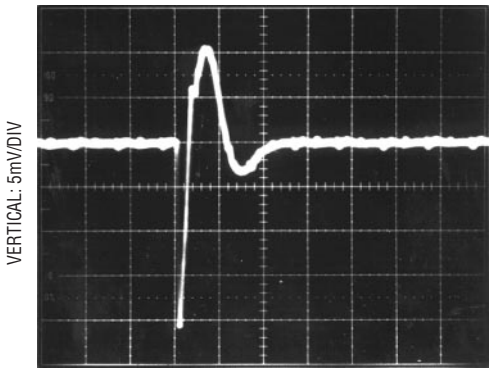

Figure 10. Adequate Settling of Op Amp Driving Analog Input

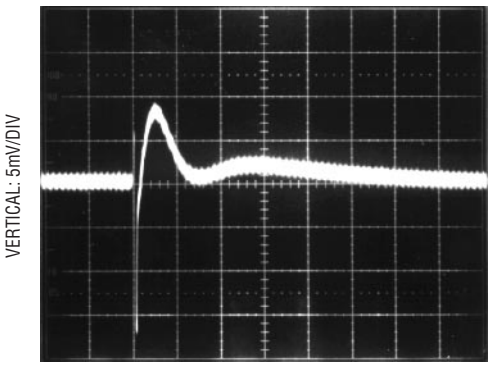

Figure 11. Poor Op Amp Settling Can Cause A/D Errors (Note Horizontal Scale)

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RC Input Filtering

It is possible to filter the inputs with an RC network as shown in Figure 12. For large values of C_F (e.g., 1µF) the capacitive input switching currents are averaged into a net DC current. A filter should be chosen with a small resistor and a large capacitor to prevent DC drops across the resistor. The magnitude of the DC current is approximately $I_{DC} = 100pF \bullet V_{IN}/t_{CYC}$ and is roughly proportional to V_{IN}. When running at the minimum cycle time of 18.5µs, the input current equals 27µA at $V_{IN} = 5V$. Here a filter resistor of 4.5Ω will cause 0.1LSB of full-scale error. If a large filter resistor must be used, errors can be reduced by increasing the cycle time as shown in the Typical Performance Characteristics curve Maximum Filter Resistor vs Cycle Time.

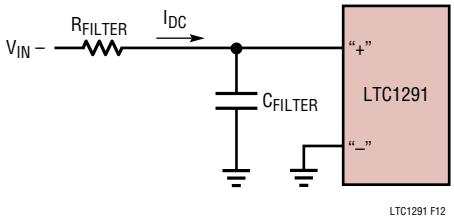

Figure 12. RC Input Filtering

Input Leakage Current

Input leakage currents also can create errors if the source resistance gets too large. For example, the maximum input leakage specification of 1µA (at 125°C) flowing through a source resistance of 1k will cause a voltage drop of 1mV or 0.8LSB. This error will be much reduced at lower temperatures because leakage drops rapidly (see typical performance characteristics curve Input Channel Leakage Current vs Temperature).

SAMPLE-AND-HOLD

Single-Ended Input

The LTC1291 provides a built-in sample-and-hold (S/H) function on the +IN input for signals acquired in the single-ended mode (–IN pin grounded). The sample-and-hold allows the LTC1291 to convert rapidly varying signals (see typical performance characteristics curve of S/H Acquisition Time vs Source Resistance). The input voltage is sampled during the t_{SMPL} time as shown in Figure 9. The sampling interval begins as the bit preceding the MSBF bit is shifted in and continues until the falling edge of the PS bit is received. On this falling edge, the S/H goes into the hold mode and the conversion begins.

Differential Input

With a differential input the A/D no longer converts a single voltage but converts the difference between two voltages. The voltage on the +IN pin is sampled and held and can be rapidly time varying. The voltage on the –IN pin must remain constant and be free of noise and ripple throughout the conversion time. Otherwise the differencing operation will not be done accurately. The conversion time is 12 CLK cycles. Therefore a change in the –IN input voltage during this interval can cause conversion errors. For a sinusoidal voltage on the –IN input this error would be:

$$V_{ERROR(MAX)} = \left(2\pi f_{(-IN)} V_{PEAK}\right)\left(\frac{12}{f_{CLK}}\right)$$

Where $f_{(-IN)}$ is the frequency of the –IN input voltage, V_{PEAK} is its peak amplitude and f_{CLK} is the frequency of the CLK. Usually V_{ERROR} will not be significant. For a 60Hz signal on the –IN input to generate a 0.25LSB error (300µV) with the converter running at CLK = 1MHz, its peak value would have to be 66mV. Rearranging the above equation, the maximum sinusoidal signal that can be digitized to a given accuracy is given as:

$$f_{(-IN)} = \left(\frac{V_{ERROR(MAX)}}{2\pi V_{PEAK}}\right)\left(\frac{f_{CLK}}{12}\right)$$

For 0.25LSB error (300µV), the maximum input sinusoid with a 5V peak amplitude that can be digitized is 0.8Hz.

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Overvoltage Protection

Applying signals to the LTC1291's analog inputs that exceed the positive supply or that go below ground will degrade the accuracy of the A/D and possibly damage the device. For example, this condition will occur if a signal is applied to the analog inputs before power is applied to the LTC1291. It can also happen if the input source is operating from supplies of larger value than the LTC1291 supply. These conditions should be prevented either with proper supply sequencing or by use of external circuitry to clamp, or current limit the input source.

There are two ways to protect the inputs. In Figure 13 diode clamps from the inputs to V_{CC} and GND are used. The second method is to put resistors in series with the analog inputs for current limiting. Limit the current to 15mA per channel. The +IN input can accept a resistor value of 1k but the –IN input cannot accept more than 250Ω when clocked at its maximum clock frequency of 1MHz. If the LTC1291 is clocked at the maximum clock frequency and 250Ω is not enough to current limit the input source, then the clamp diodes are recommended (Figures 14 and 15). The reason for the limit on the resistor value is that the MSB bit test is affected by the value of the resistor placed at the –IN input (see discussion on Analog Inputs and the typical performance characteristics Maximum CLK Rate vs Source Resistance).

Because a unique input protection structure is used on the digital input pins, the signal levels on these pins can exceed the device V_{CC} without damaging the device.

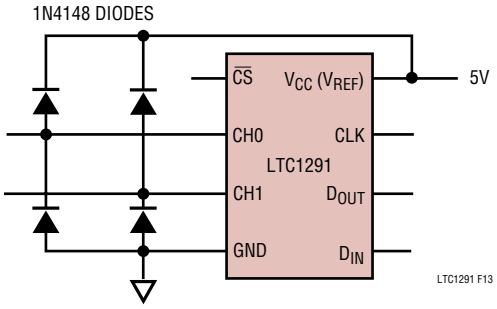


Figure 13. Overvoltage Protection for Inputs

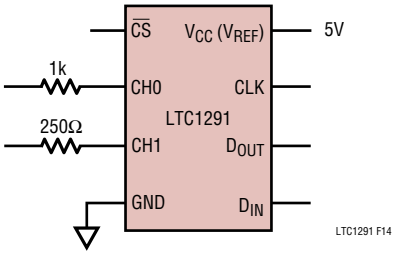


Figure 14. Overvoltage Protection for Inputs

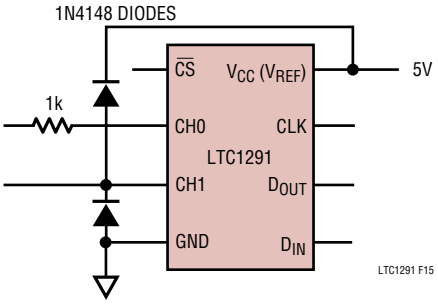


Figure 15. Overvoltage Protection for Inputs

APPLICATIONS INFORMATION

A "Quick Look" Circuit for the LTC1291

Users can get a quick look at the function and timing of the LTC1291 by using the following simple circuit (Figure 16). D_{IN} is tied to V_{CC}. This requires V_{IN} be applied to CH1 with respect to the ground plane. The data is output MSB-first. $\overline{CS}$ is driven at 1/64, the clock frequency by the 74HC393 and D_{OUT} outputs the data. The output data from the D_{OUT} pin can be viewed on a oscilloscope that is set up to trigger on the falling edge of $\overline{CS}$ (Figure 17).

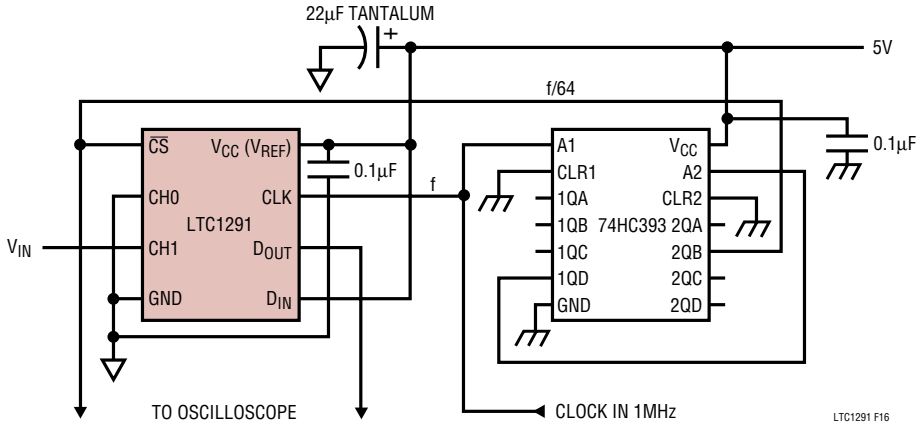


Figure 16. "Quick Look" Circuit for the LTC1291

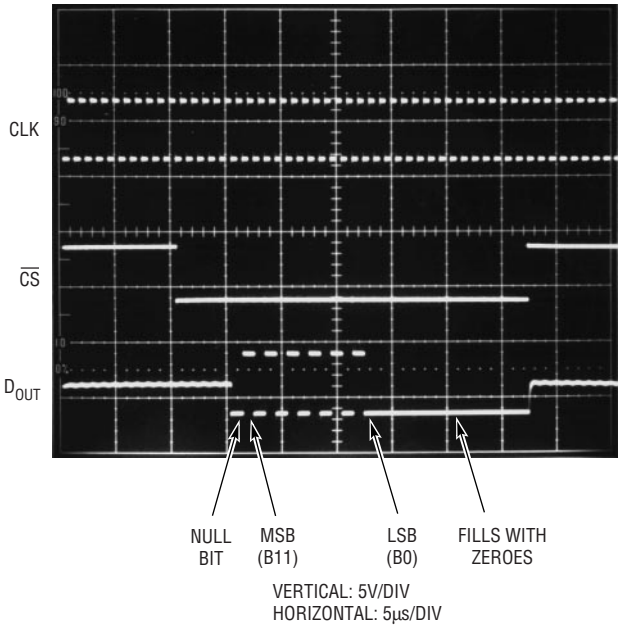
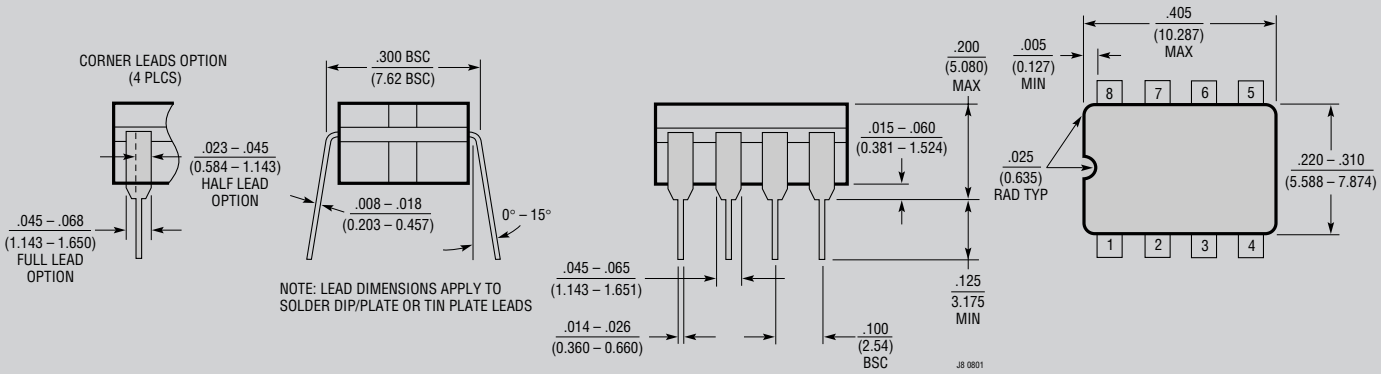


Figure 17. Scope Trace of the LTC1291 "Quick Look" Circuit Showing Output 101010101010 (AAA_{HEX})

Information furnished by Linear Technology Corporation is believed to be accurate and reliable. However, no responsibility is assumed for its use. Linear Technology Corporation makes no representation that the interconnection of its circuits as described herein will not infringe on existing patent rights.

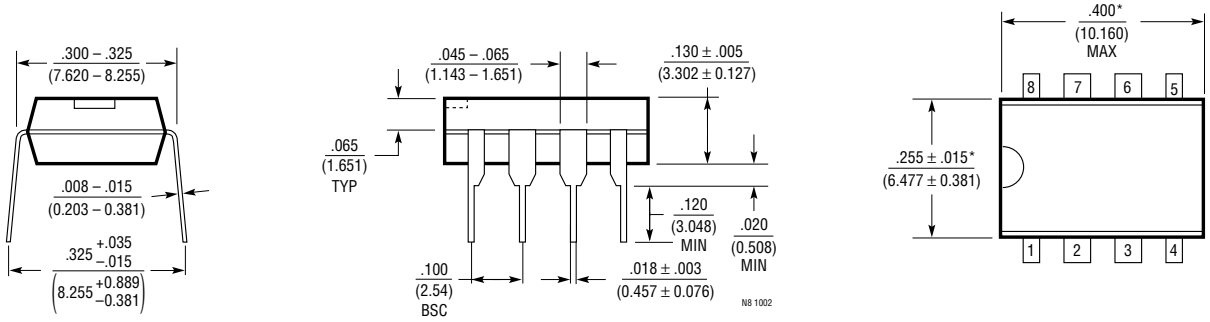
PACKAGE DESCRIPTION

J8 Package
8-Lead CERDIP (Narrow .300 Inch, Hermetic)
(Reference LTC DWG # 05-08-1110)



OBSOLETE PACKAGE

N8 Package
8-Lead PDIP (Narrow .300 Inch)
(Reference LTC DWG # 05-08-1510)



NOTE:
1. DIMENSIONS ARE INCHES / MILLIMETERS

*THESE DIMENSIONS DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS.
MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED .010 INCH (0.254mm)

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC1298	12-bit, 2-Channel, Micropower ADC in SO-8	11.1ksps, Autoshutdown
LTC1861	12-bit, 2-Channel, 250ksps ADC in MSOP	850µA Supply Current, 2µA at 1ksps
LTC1865	16-bit, 2-Channel, 250ksps ADC in MSOP	850µA Supply Current, 2µA at 1ksps

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