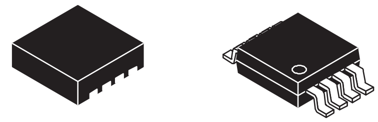


3.1-W MONO FULLY DIFFERENTIAL AUDIO POWER AMPLIFIER

Check for Samples: TPA6211A1

FEATURES

- **Designed for Wireless or Cellular Handsets and PDAs**
- **3.1 W Into 3Ω From a 5-V Supply at THD = 10% (Typ)**
- **Low Supply Current: 4 mA Typ at 5 V**
- **Shutdown Current: 0.01 μA Typ**
- **Fast Startup With Minimal Pop**
- **Only Three External Components**
  - **Improved PSRR (-80 dB) and Wide Supply Voltage (2.5 V to 5.5 V) for Direct Battery Operation**
  - **Fully Differential Design Reduces RF Rectification**
  - **-63 dB CMRR Eliminates Two Input Coupling Capacitors**

APPLICATIONS

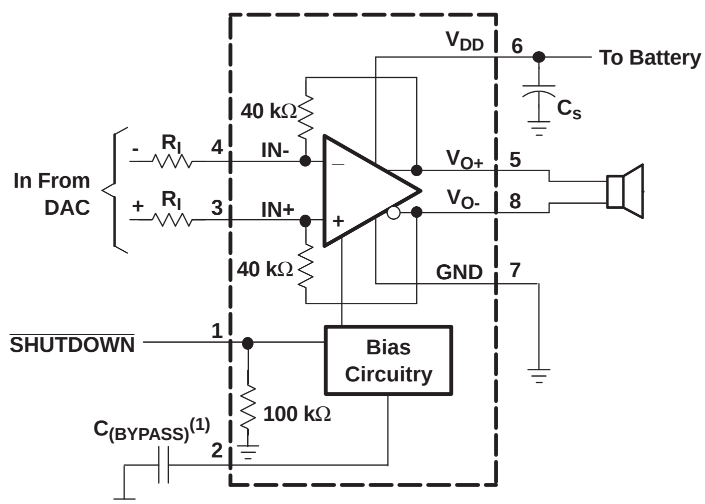
- **Ideal for Wireless Handsets, PDAs, and Notebook Computers**

DESCRIPTION

The TPA6211A1 is a 3.1-W mono fully-differential amplifier designed to drive a speaker with at least 3-Ω impedance while consuming only 20 mm^2 total printed-circuit board (PCB) area in most applications. The device operates from 2.5 V to 5.5 V, drawing only 4 mA of quiescent supply current. The TPA6211A1 is available in the space-saving 3-mm × 3-mm QFN (DRB) and the 8-pin MSOP (DGN) PowerPAD™ packages.

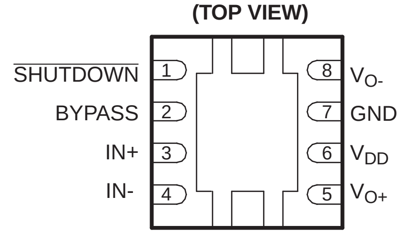
Features like –80 dB supply voltage rejection from 20 Hz to 2 kHz, improved RF rectification immunity, small PCB area, and a fast startup with minimal pop makes the TPA6211A1 ideal for PDA/smart phone applications.

APPLICATION CIRCUIT

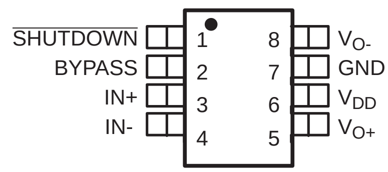


(1) $C_{(BYPASS)}$ is optional.

8-PIN QFN (DRB) PACKAGE (TOP VIEW)



DGN PACKAGE (TOP VIEW)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION

T_A	PACKAGED DEVICES[1]		EVALUATION MODULES
	SMALL OUTLINE (DRB)	MSOP PowerPAD™ (DGN)	
–40°C to 85°C	TPA6211A1DRB	TPA6211A1DGN	TPA6211A1EVM

(1) The DGN and DRB are available taped and reeled. To order taped and reeled parts, add the suffix R to the part number (TPA6211A1DGNR or TPA6211A1DRBR).

Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	DRB, DGN		
IN-	4	I	Negative differential input
IN+	3	I	Positive differential input
V_{DD}	6	I	Power supply
V_{O+}	5	O	Positive BTL output
GND	7	I	High-current ground
V_{O-}	8	O	Negative BTL output
$\overline{\text{SHUTDOWN}}$	1	I	Shutdown terminal (active low logic)
BYPASS	2		Mid-supply voltage, adding a bypass capacitor improves PSRR
Thermal Pad	-	-	Connect to ground. Thermal pad must be soldered down in all applications to properly secure device on the PCB.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted[1]

		UNIT
V_{DD}	Supply voltage	–0.3 V to 6 V
V_I	Input voltage	–0.3 V to V_{DD} + 0.3 V
	Continuous total power dissipation	See Dissipation Rating Table
T_A	Operating free-air temperature	–40°C to 85°C
T_J	Junction temperature	–40°C to 150°C
T_{stg}	Storage temperature	–65°C to 150°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

PACKAGE DISSIPATION RATINGS

PACKAGE	$T_A \leq 25°C$ POWER RATING	DERATING FACTOR[1]	$T_A = 70°C$ POWER RATING	$T_A = 85°C$ POWER RATING
DGN	2.13 W	17.1 mW/°C	1.36 W	1.11 W
DRB	2.7 W	21.8 mW/°C	1.7 W	1.4 W

(1) Derating factor based on high-k board layout.

RECOMMENDED OPERATION CONDITIONS

			MIN	TYP	MAX	UNIT
V_{DD}	Supply voltage		2.5		5.5	V
V_{IH}	High-level input voltage	$\overline{\text{SHUTDOWN}}$	1.55			V
V_{IL}	Low-level input voltage	$\overline{\text{SHUTDOWN}}$			0.5	V
T_A	Operating free-air temperature		–40		85	°C

ELECTRICAL CHARACTERISTICS

T_A = 25°C

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
V_{OS}	Output offset voltage (measured differentially)	V_I = 0 V differential, Gain = 1 V/V, V_{DD} = 5.5 V			-9	0.3	9	mV
PSRR	Power supply rejection ratio	V_{DD} = 2.5 V to 5.5 V				–85	–60	dB
V_{IC}	Common mode input range	V_{DD} = 2.5 V to 5.5 V			0.5		V_{DD}-0.8	V
CMRR	Common mode rejection ratio	V_{DD} = 5.5 V,	V_{IC} = 0.5 V to 4.7 V			-63	–40	dB
		V_{DD} = 2.5 V,	V_{IC} = 0.5 V to 1.7 V			-63	–40	
	Low-output swing	R_L = 4 Ω, V_{IN+} = V_{DD}, V_{IN+} = 0 V,	Gain = 1 V/V, V_{IN-} = 0 V or V_{IN-} = V_{DD}	V_{DD} = 5.5 V		0.45		V
				V_{DD} = 3.6 V		0.37		
				V_{DD} = 2.5 V		0.26	0.4	
	High-output swing	R_L = 4 Ω, V_{IN+} = V_{DD}, V_{IN-} = V_{DD}	Gain = 1 V/V, V_{IN-} = 0 V or V_{IN+} = 0 V	V_{DD} = 5.5 V		4.95		V
				V_{DD} = 3.6 V		3.18		
				V_{DD} = 2.5 V	2	2.13		
$\lvert I_{IH} \rvert$	High-level input current, shutdown	V_{DD} = 5.5 V,	V_I = 5.8 V			58	100	μA
$\lvert I_{IL} \rvert$	Low-level input current, shutdown	V_{DD} = 5.5 V,	V_I = –0.3 V			3	100	μA
I_Q	Quiescent current	V_{DD} = 2.5 V to 5.5 V, no load				4	5	mA
$I_{(SD)}$	Supply current	V($\overline{\text{SHUTDOWN}}$) ≤ 0.5 V, V_{DD} = 2.5 V to 5.5 V, R_L = 4Ω				0.01	1	μA
	Gain	R_L = 4Ω			$\frac{38\ k\Omega}{R_I}$	$\frac{40\ k\Omega}{R_I}$	$\frac{42\ k\Omega}{R_I}$	V/V
	Resistance from shutdown to GND					100		kΩ

OPERATING CHARACTERISTICS

T_A = 25°C, Gain = 1 V/V

PARAMETER		TEST CONDITIONS			MIN	TYP	MAX	UNIT
P_O	Output power	THD + N= 1%, f = 1 kHz, R_L = 3 Ω		V_{DD} = 5 V		2.45		W
				V_{DD} = 3.6 V		1.22		
				V_{DD} = 2.5 V		0.49		
		THD + N= 1%, f = 1 kHz, R_L = 4 Ω		V_{DD} = 5 V		2.22		
				V_{DD} = 3.6 V		1.1		
				V_{DD} = 2.5 V		0.47		
		THD + N= 1%, f = 1 kHz, R_L = 8 Ω		V_{DD} = 5 V		1.36		
				V_{DD} = 3.6 V		0.72		
				V_{DD} = 2.5 V		0.33		
THD+N	Total harmonic distortion plus noise	f = 1 kHz, R_L = 3 Ω	P_O = 2 W	V_{DD} = 5 V		0.045%		
			P_O = 1 W	V_{DD} = 3.6 V		0.05%		
			P_O = 300 mW	V_{DD} = 2.5 V		0.06%		
		f = 1 kHz, R_L = 4 Ω	P_O = 1.8 W	V_{DD} = 5 V		0.03%		
			P_O = 0.7 W	V_{DD} = 3.6 V		0.03%		
			P_O = 300 mW	V_{DD} = 2.5 V		0.04%		
		f = 1 kHz, R_L = 8 Ω	P_O = 1 W	V_{DD} = 5 V		0.02%		
			P_O = 0.5 W	V_{DD} = 3.6 V		0.02%		
			P_O = 200 mW	V_{DD} = 2.5 V		0.03%		
k_{SVR}	Supply ripple rejection ratio	V_{DD} = 3.6 V, Inputs ac-grounded with C_i = 2 μF, $V_{(RIPPLE)}$ = 200 mV_{pp}		f = 217 Hz		-80		dB
				f = 20 Hz to 20 kHz		-70		
SNR	Signal-to-noise ratio	V_{DD} = 5 V, P_O = 2 W, R_L = 4 Ω				105		dB
V_n	Output voltage noise	V_{DD} = 3.6 V, f = 20 Hz to 20 kHz, Inputs ac-grounded with C_i = 2 μF		No weighting		15		μV_{RMS}
				A weighting		12		
CMRR	Common mode rejection ratio	V_{DD} = 3.6 V, V_{IC} = 1 V_{pp}		f = 217 Hz		-65		dB
Z_I	Input impedance				38	40	44	kΩ
	Start-up time from shutdown	V_{DD} = 3.6 V, No C_{BYPASS}				4		μs
		V_{DD} = 3.6 V, C_{BYPASS} = 0.1 μF				27		ms

TYPICAL CHARACTERISTICS

Table of Graphs

			FIGURE
P_O	Output power	vs Supply voltage	1
		vs Load resistance	2
P_D	Power dissipation	vs Output power	3, 4
THD+N	Total harmonic distortion + noise	vs Output power	5, 6, 7
		vs Frequency	8-12
		vs Common-mode input voltage	13
K_{SVR}	Supply voltage rejection ratio	vs Frequency	14, 15, 16, 17
K_{SVR}	Supply voltage rejection ratio	vs Common-mode input voltage	18
	GSM Power supply rejection	vs Time	19
	GSM Power supply rejection	vs Frequency	20
CMRR	Common-mode rejection ratio	vs Frequency	21
		vs Common-mode input voltage	22
	Closed loop gain/phase	vs Frequency	23
	Open loop gain/phase	vs Frequency	24
I_{DD}	Supply current	vs Supply voltage	25
		vs Shutdown voltage	26
	Start-up time	vs Bypass capacitor	27

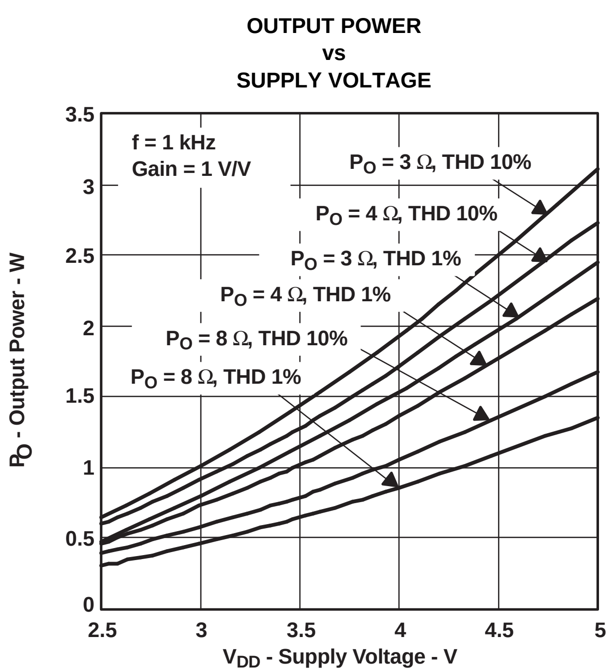


Figure 1.

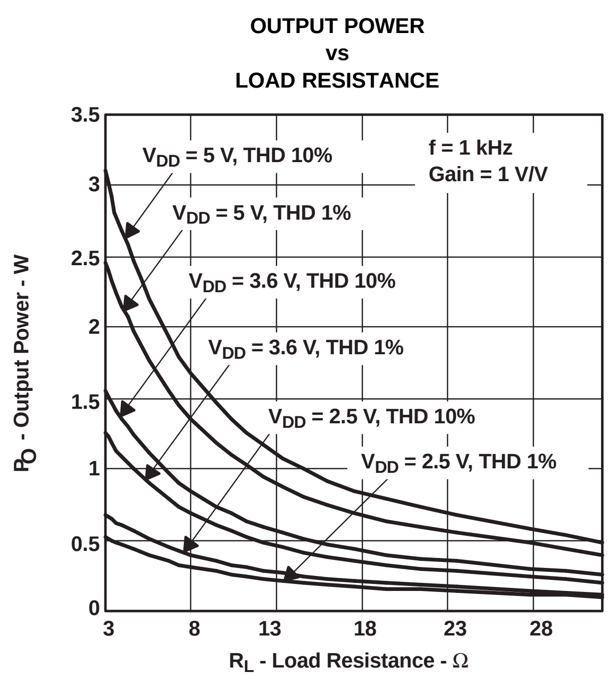


Figure 2.

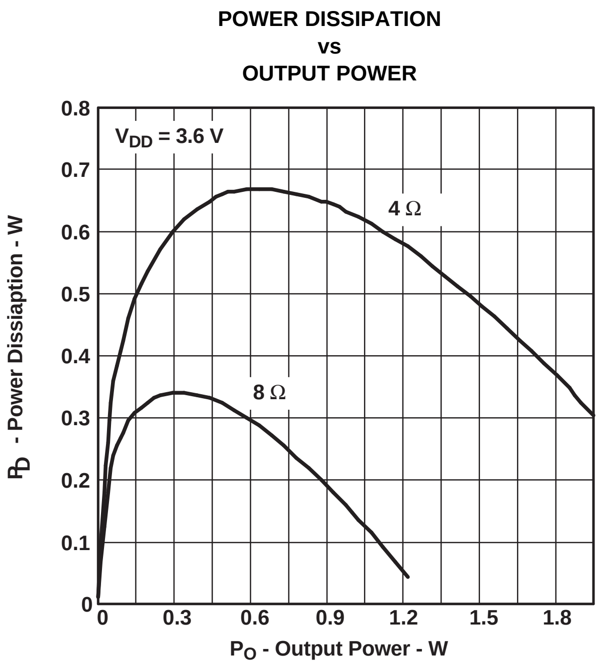


Figure 3.

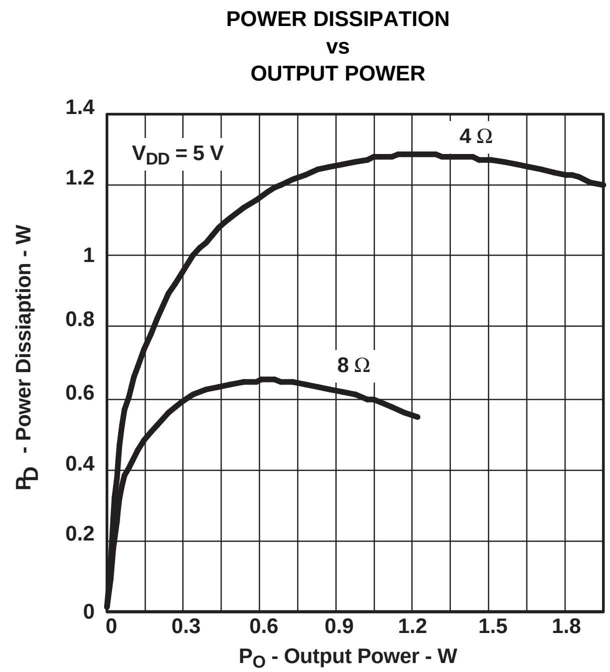


Figure 4.

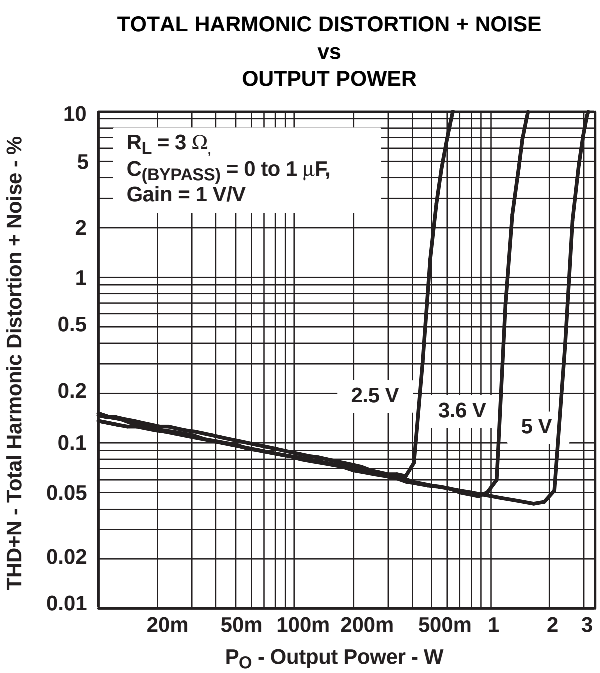


Figure 5.

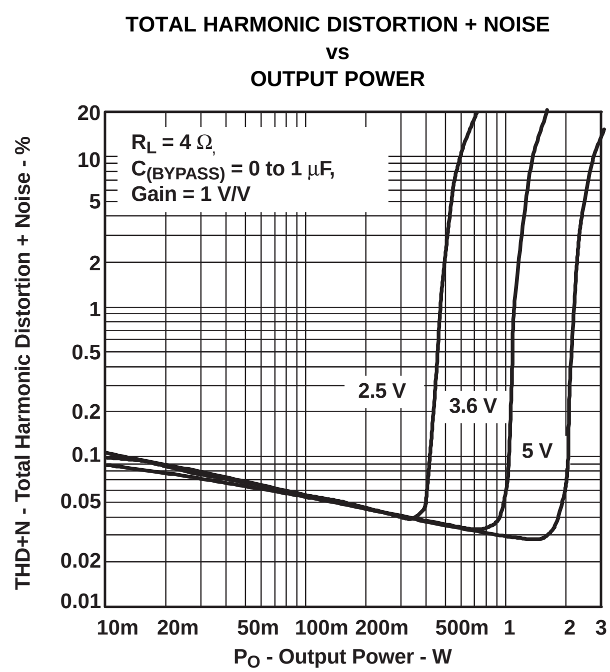


Figure 6.

TOTAL HARMONIC DISTORTION + NOISE vs OUTPUT POWER

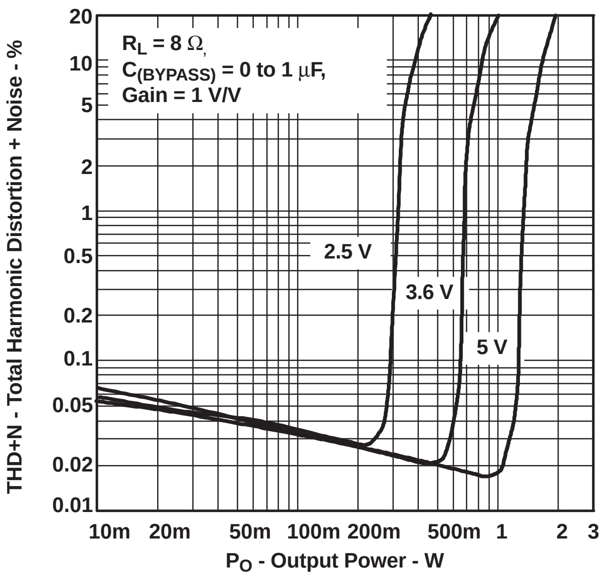


Figure 7.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

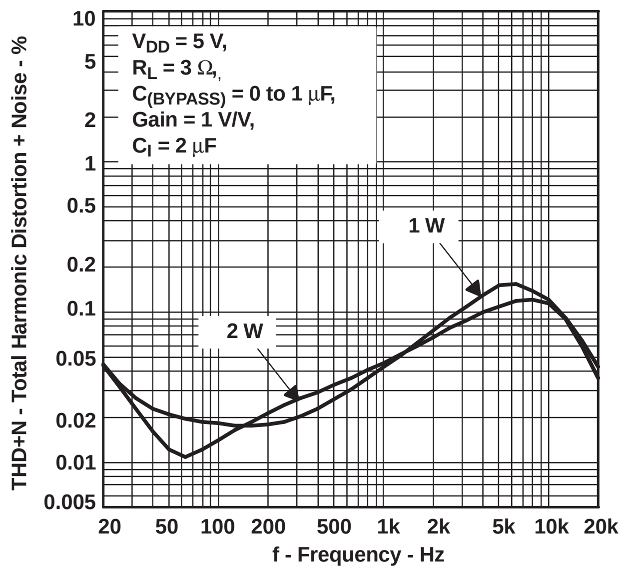


Figure 8.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

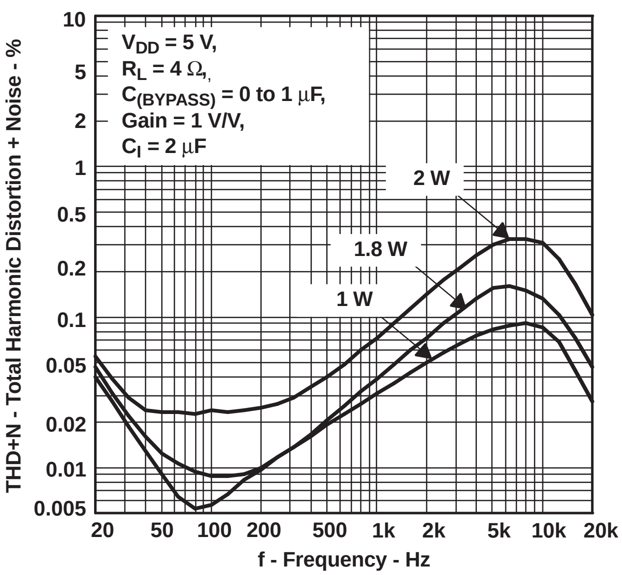


Figure 9.

TOTAL HARMONIC DISTORTION + NOISE vs FREQUENCY

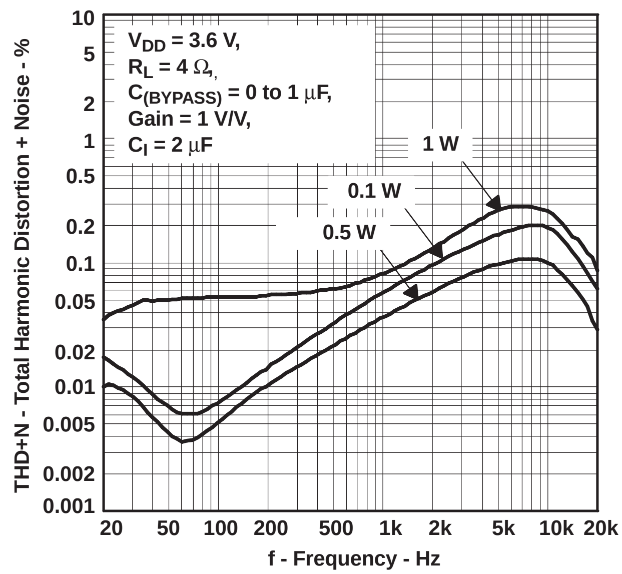


Figure 10.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

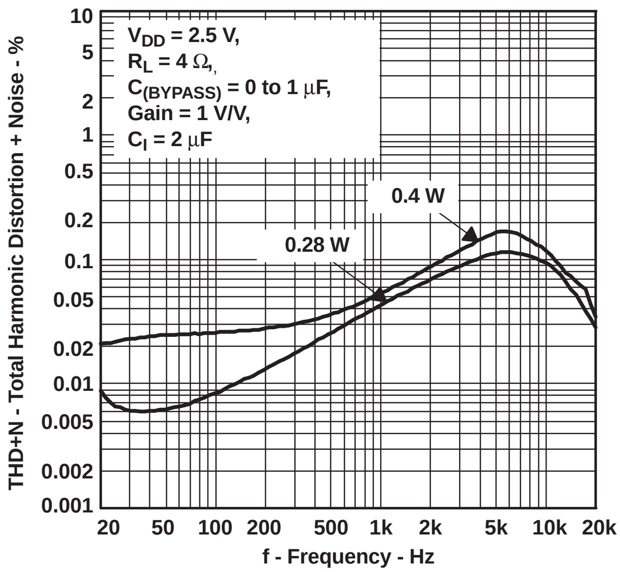


Figure 11.

TOTAL HARMONIC DISTORTION + NOISE
vs
FREQUENCY

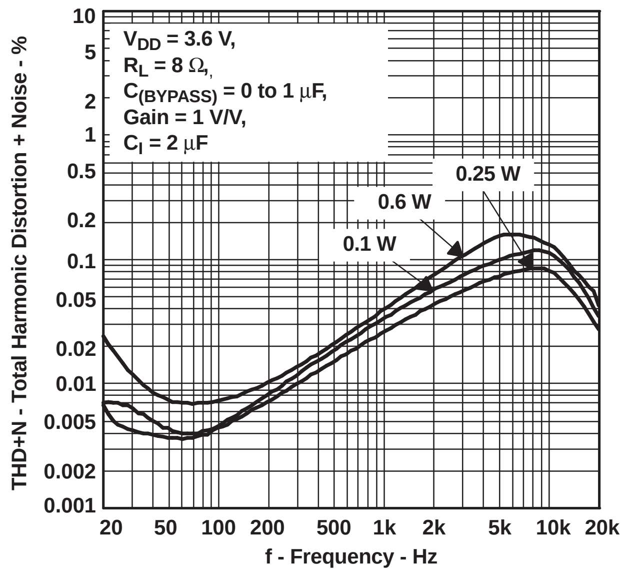


Figure 12.

TOTAL HARMONIC DISTORTION + NOISE
vs
COMMON MODE INPUT VOLTAGE

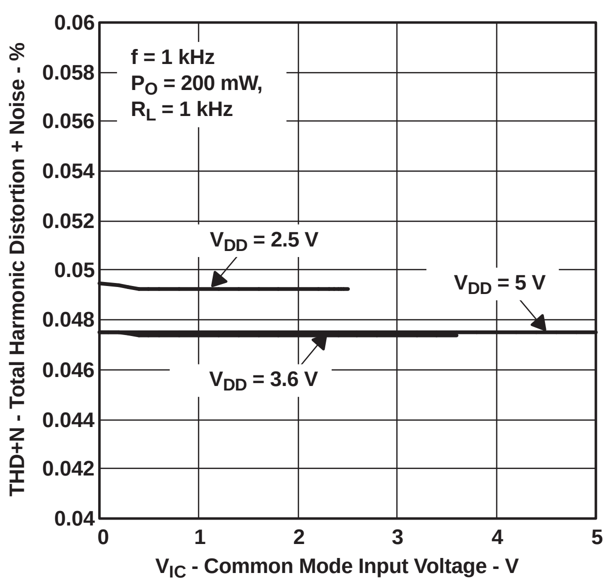


Figure 13.

SUPPLY VOLTAGE REJECTION RATIO
vs
FREQUENCY

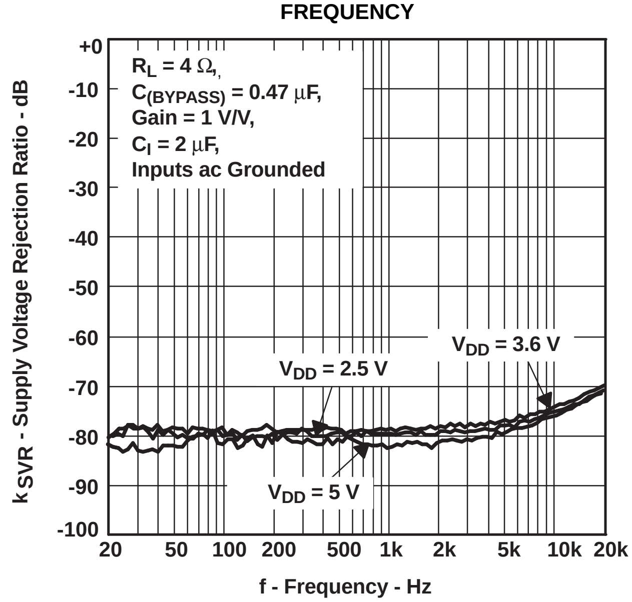


Figure 14.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

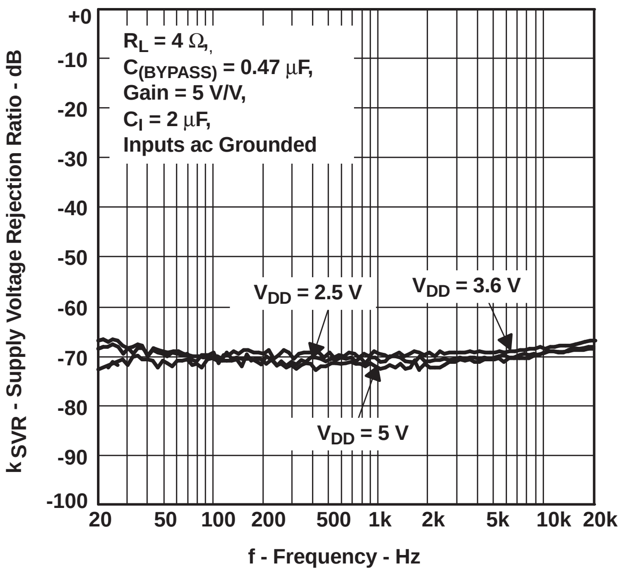


Figure 15.

SUPPLY RIPPLE REJECTION RATIO vs FREQUENCY

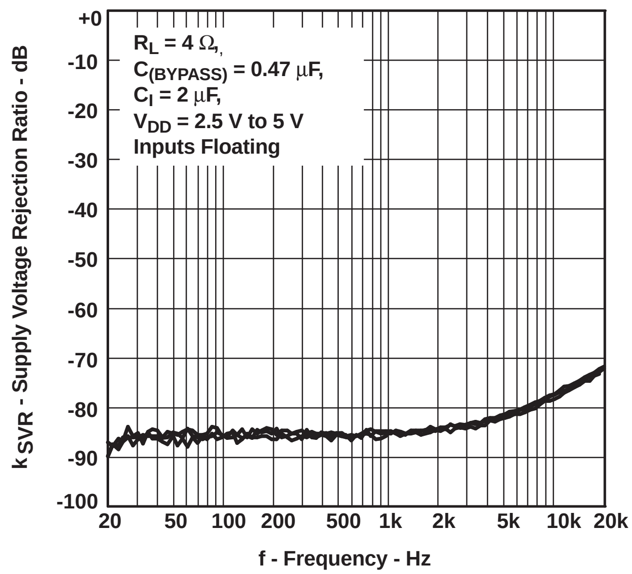


Figure 16.

SUPPLY VOLTAGE REJECTION RATIO vs FREQUENCY

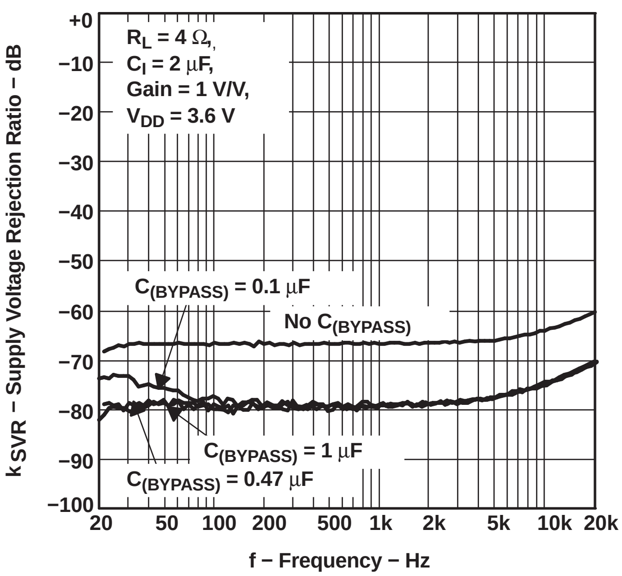


Figure 17.

SUPPLY VOLTAGE REJECTION RATIO vs DC COMMON MODE INPUT

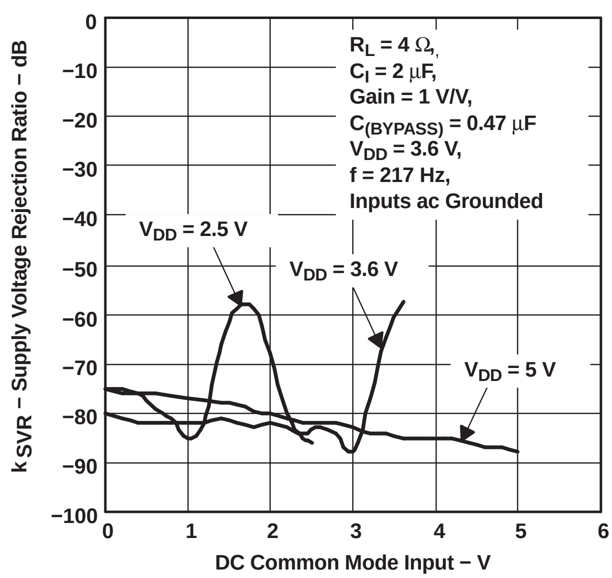


Figure 18.

GSM POWER SUPPLY REJECTION
vs
TIME

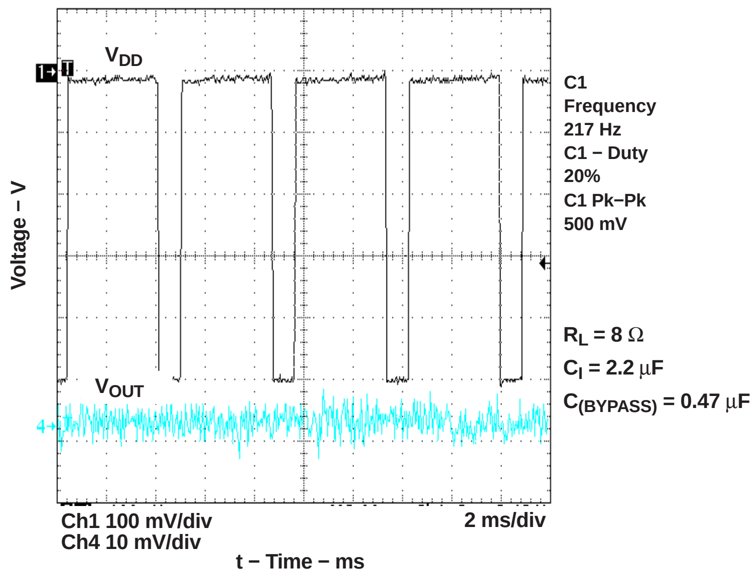


Figure 19.

GSM POWER SUPPLY REJECTION
vs
FREQUENCY

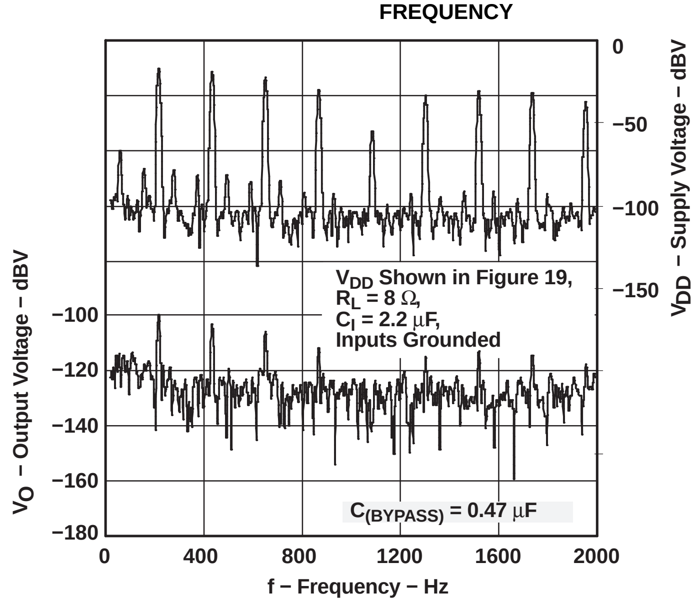


Figure 20.

COMMON MODE REJECTION RATIO
vs
FREQUENCY

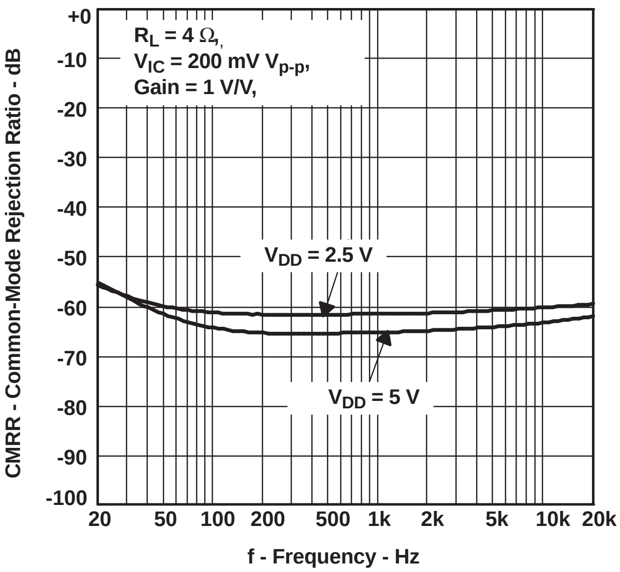


Figure 21.

COMMON-MODE REJECTION RATIO
vs
COMMON-MODE INPUT VOLTAGE

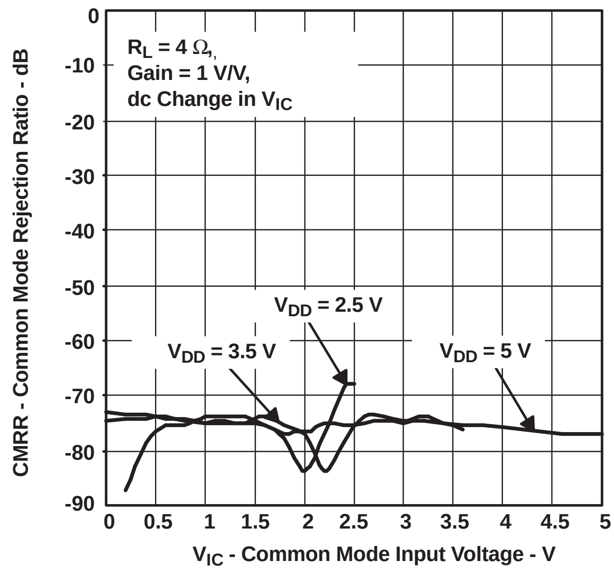


Figure 22.

CLOSED LOOP GAIN/PHASE
vs
FREQUENCY

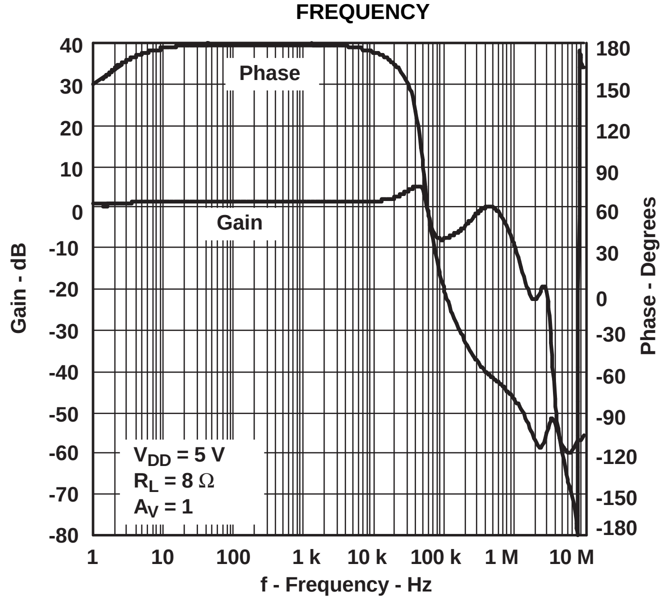


Figure 23.

OPEN LOOP GAIN/PHASE
vs
FREQUENCY

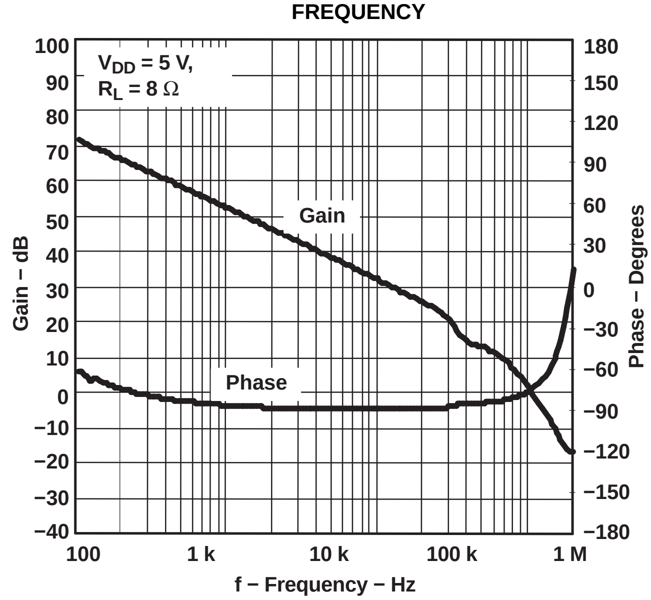


Figure 24.

SUPPLY CURRENT
vs
SUPPLY VOLTAGE

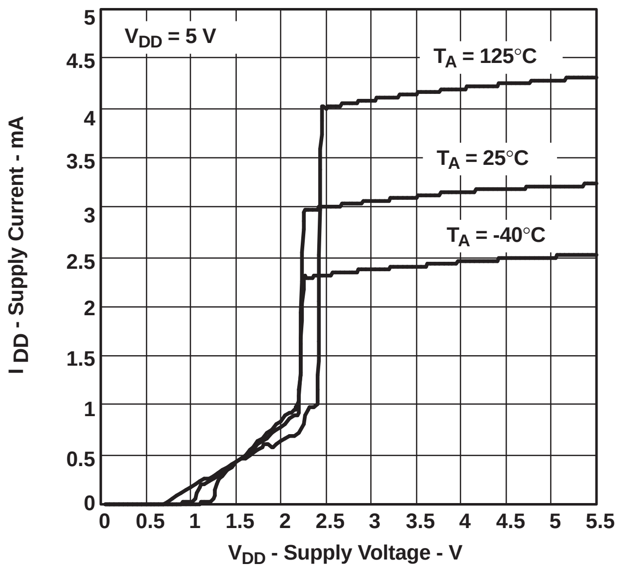


Figure 25.

SUPPLY CURRENT
vs
SHUTDOWN VOLTAGE

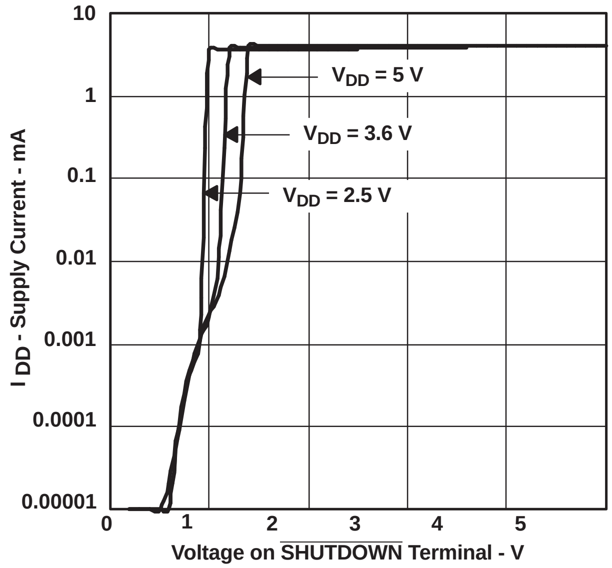


Figure 26.

START-UP TIME
vs
BYPASS CAPACITOR

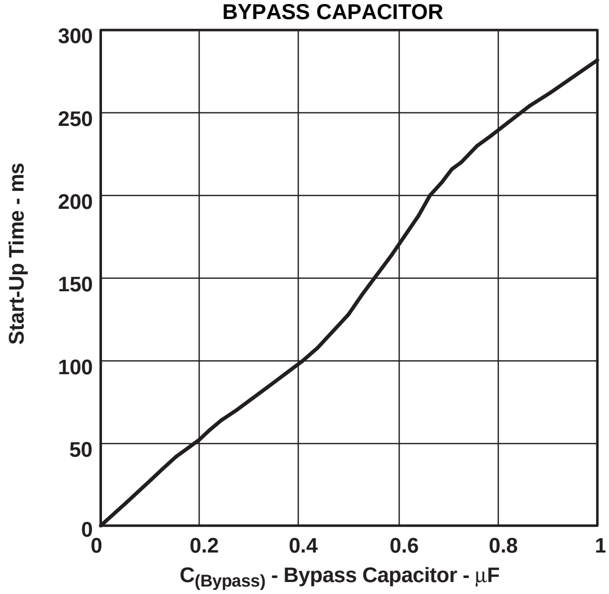


Figure 27.

APPLICATION INFORMATION

FULLY DIFFERENTIAL AMPLIFIER

The TPA6211A1 is a fully differential amplifier with differential inputs and outputs. The fully differential amplifier consists of a differential amplifier and a common- mode amplifier. The differential amplifier ensures that the amplifier outputs a differential voltage that is equal to the differential input times the gain. The common-mode feedback ensures that the common-mode voltage at the output is biased around $V_{DD}/2$ regardless of the common- mode voltage at the input.

Advantages of Fully Differential Amplifiers

- **Input coupling capacitors not required:** A fully differential amplifier with good CMRR, like the TPA6211A1, allows the inputs to be biased at voltage other than mid-supply. For example, if a DAC has a lower mid-supply voltage than that of the TPA6211A1, the common-mode feedback circuit compensates, and the outputs are still biased at the mid-supply point of the TPA6211A1. The inputs of the TPA6211A1 can be biased from 0.5 V to V_{DD} - 0.8 V. If the inputs are biased outside of that range, input coupling capacitors are required.
- **Mid-supply bypass capacitor, $C_{(BYPASS)}$, not required:** The fully differential amplifier does not require a bypass capacitor. Any shift in the mid-supply voltage affects both positive and negative channels equally, thus canceling at the differential output. Removing the bypass capacitor slightly worsens power supply rejection ratio (k_{SVR}), but a slight decrease of k_{SVR} may be acceptable when an additional component can be eliminated (See Figure 17).
- **Better RF-immunity:** GSM handsets save power by turning on and shutting off the RF transmitter at a rate of 217 Hz. The transmitted signal is picked-up on input and output traces. The fully differential amplifier cancels the signal much better than the typical audio amplifier.

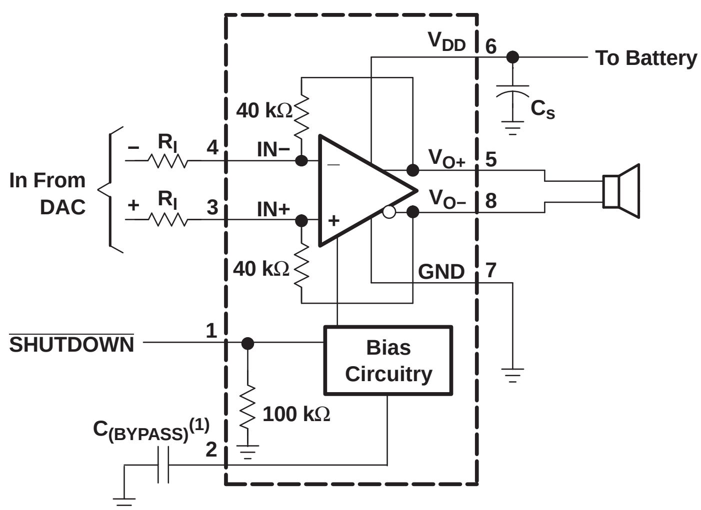
APPLICATION SCHEMATICS

Figure 28 through Figure 31 show application schematics for differential and single-ended inputs. Typical values are shown in Table 1.

Table 1. Typical Component Values

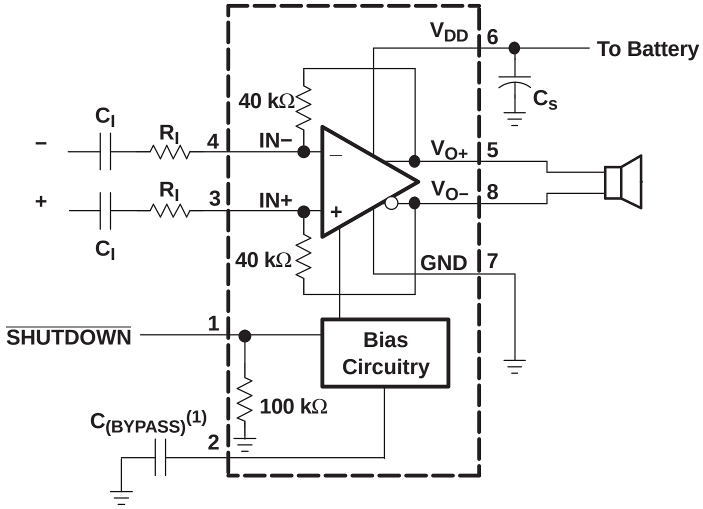
COMPONENT	VALUE
R_I	40 kΩ
$C_{(BYPASS)}$ (1)	0.22 µF
C_S	1 µF
C_I	0.22 µF

(1) $C_{(BYPASS)}$ is optional.



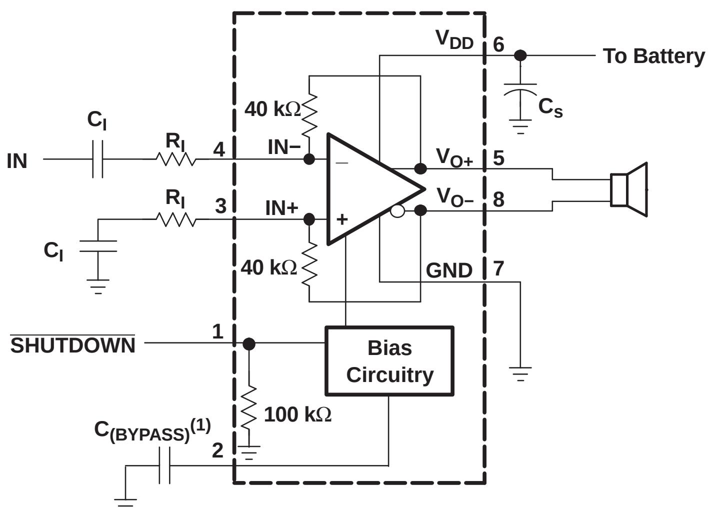
(1) $C_{(BYPASS)}$ is optional

Figure 28. Typical Differential Input Application Schematic



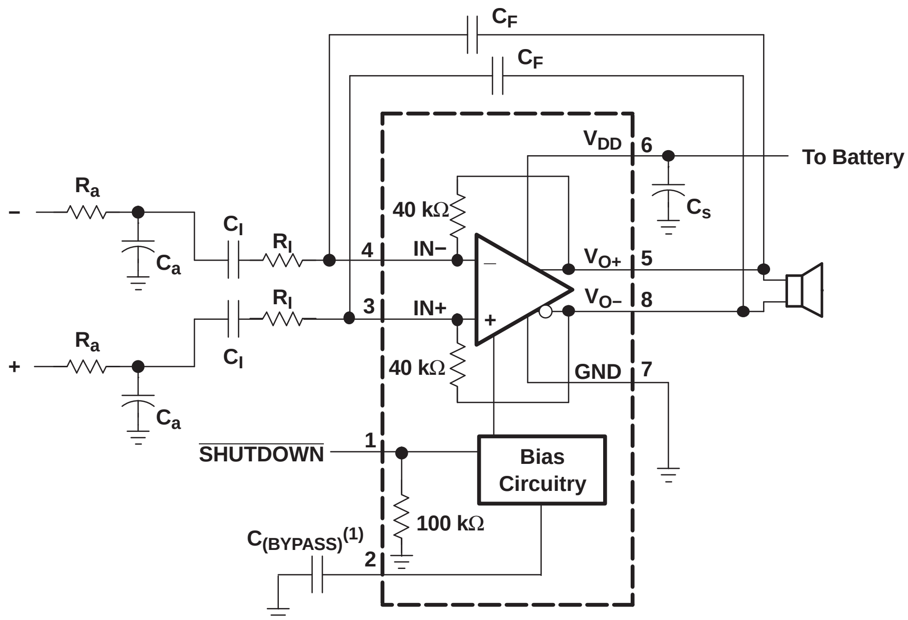
(1) $C_{(BYPASS)}$ is optional

Figure 29. Differential Input Application Schematic Optimized With Input Capacitors



(1) $C_{(BYPASS)}$ is optional

Figure 30. Single-Ended Input Application Schematic



(1) $C_{(BYPASS)}$ is optional

Figure 31. Differential Input Application Schematic With Input Bandpass Filter

Selecting Components

Resistors (R_I)

The input resistor (R_I) can be selected to set the gain of the amplifier according to equation 1.

$$\text{Gain} = R_F/R_I \tag{1}$$

The internal feedback resistors (R_F) are trimmed to 40 kΩ.

Resistor matching is very important in fully differential amplifiers. The balance of the output on the reference voltage depends on matched ratios of the resistors. CMRR, PSRR, and the cancellation of the second harmonic distortion diminishes if resistor mismatch occurs. Therefore, 1%-tolerance resistors or better are recommended to optimize performance.

Bypass Capacitor (C_{BYPASS}) and Start-Up Time

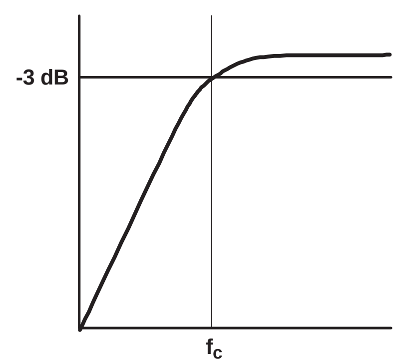
The internal voltage divider at the BYPASS pin of this device sets a mid-supply voltage for internal references and sets the output common mode voltage to $V_{DD}/2$. Adding a capacitor filters any noise into this pin, increasing k_{SVR}. $C_{(BYPASS)}$also determines the rise time of V_{O+} and V_{O-} when the device exits shutdown. The larger the capacitor, the slower the rise time.

Input Capacitor (C_I)

The TPA6211A1 does not require input coupling capacitors when driven by a differential input source biased from 0.5 V to V_{DD} - 0.8 V. Use 1% tolerance or better gain-setting resistors if not using input coupling capacitors.

In the single-ended input application, an input capacitor, C_I, is required to allow the amplifier to bias the input signal to the proper dc level. In this case, C_I and R_I form a high-pass filter with the corner frequency defined in Equation 2.

$$f_C = \frac{1}{2\pi R_I C_I} \tag{2}$$



The value of C_I is an important consideration. It directly affects the bass (low frequency) performance of the circuit. Consider the example where R_I is 10 kΩ and the specification calls for a flat bass response down to 100 Hz. Equation 2 is reconfigured as Equation 3.

$$C_I = \frac{1}{2\pi R_I f_c} \tag{3}$$

In this example, C_I is 0.16 μF, so the likely choice ranges from 0.22 μF to 0.47 μF. Ceramic capacitors are preferred because they are the best choice in preventing leakage current. When polarized capacitors are used, the positive side of the capacitor faces the amplifier input in most applications. The input dc level is held at $V_{DD}/2$, typically higher than the source dc level. It is important to confirm the capacitor polarity in the application.

Band-Pass Filter (R_a, C_a, and C_a)

It may be desirable to have signal filtering beyond the one-pole high-pass filter formed by the combination of C_I and R_I. A low-pass filter may be added by placing a capacitor (C_F) between the inputs and outputs, forming a band-pass filter.

An example of when this technique might be used would be in an application where the desirable pass-band range is between 100 Hz and 10 kHz, with a gain of 4 V/V. The following equations illustrate how the proper values of C_F and C_I can be determined.

Step 1: Low-Pass Filter

$$f_{c(LPF)} = \frac{1}{2\pi R_F C_F}$$

where R_F is the internal 40 kΩ resistor (4)

$$f_{c(LPF)} = \frac{1}{2\pi\ 40\ k\Omega\ C_F} \tag{5}$$

Therefore,

$$C_F = \frac{1}{2\pi\ 40\ k\Omega\ f_{c(LPF)}} \tag{6}$$

Substituting 10 kHz for $f_{c(LPF)}$ and solving for C_F:

C_F = 398 pF

Step 2: High-Pass Filter

$$f_{c(HPF)} = \frac{1}{2\pi R_I C_I}$$

where R_I is the input resistor (7)

Since the application in this case requires a gain of 4 V/V, R_I must be set to 10 kΩ.

Substituting R_I into equation 6.

$$f_{c(HPF)} = \frac{1}{2\pi\ 10\ k\Omega\ C_I} \tag{8}$$

Therefore,

$$C_I = \frac{1}{2\pi\ 10\ k\Omega\ f_{c(HPF)}} \tag{9}$$

Substituting 100 Hz for $f_{c(HPF)}$ and solving for C_I:

C_I = 0.16 μF

At this point, a first-order band-pass filter has been created with the low-frequency cutoff set to 100 Hz and the high-frequency cutoff set to 10 kHz.

The process can be taken a step further by creating a second-order high-pass filter. This is accomplished by placing a resistor (R_a) and capacitor (C_a) in the input path. It is important to note that R_a must be at least 10 times smaller than R_I; otherwise its value has a noticeable effect on the gain, as R_a and R_I are in series.

Step 3: Additional Low-Pass Filter

R_a must be at least 10x smaller than R_I, Set R_a = 1 kΩ

$$f_{c(LPF)} = \frac{1}{2\pi\ R_a\ C_a} \tag{10}$$

Therefore,

$$C_a = \frac{1}{2\pi\ 1k\Omega\ f_{c(LPF)}} \tag{11}$$

Substituting 10 kHz for $f_{c(LPF)}$ and solving for C_a:

C_a = 160 pF

Figure 32 is a bode plot for the band-pass filter in the previous example. Figure 31 shows how to configure the TPA6211A1 as a band-pass filter.

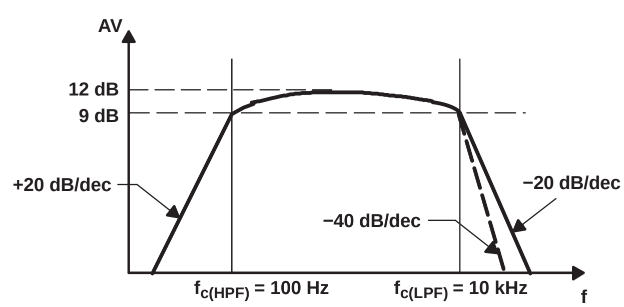


Figure 32. Bode Plot

Decoupling Capacitor (C_S)

The TPA6211A1 is a high-performance CMOS audio amplifier that requires adequate power supply decoupling to ensure the output total harmonic distortion (THD) is as low as possible. Power-supply decoupling also prevents oscillations for long lead lengths between the amplifier and the speaker. For higher frequency transients, spikes, or digital hash on the line, a good low equivalent-series-resistance (ESR) ceramic capacitor, typically 0.1 μF to 1 μF, placed as close as possible to the device V_{DD} lead works best. For filtering lower frequency noise signals, a 10-μF or greater capacitor placed near the audio power amplifier also helps, but is not required in most applications because of the high PSRR of this device.

USING LOW-ESR CAPACITORS

Low-ESR capacitors are recommended throughout this applications section. A real (as opposed to ideal) capacitor can be modeled simply as a resistor in series with an ideal capacitor. The voltage drop across this resistor minimizes the beneficial effects of the capacitor in the circuit. The lower the equivalent value of this resistance the more the real capacitor behaves like an ideal capacitor.

DIFFERENTIAL OUTPUT VERSUS SINGLE-ENDED OUTPUT

Figure 33 shows a Class-AB audio power amplifier (APA) in a fully differential configuration. The TPA6211A1 amplifier has differential outputs driving both ends of the load. One of several potential benefits to this configuration is power to the load. The differential drive to the speaker means that as one side is slewing up, the other side is slewing down, and vice versa. This in effect doubles the voltage swing on the load as compared to a ground-referenced load. Plugging 2 × $V_{O(PP)}$ into the power equation, where voltage is squared, yields 4× the output power from the same supply rail and load impedance Equation 12.

$$V_{(rms)} = \frac{V_{O(PP)}}{2\sqrt{2}}$$

$$\text{Power} = \frac{V_{(rms)}^{2}}{R_L} \tag{12}$$

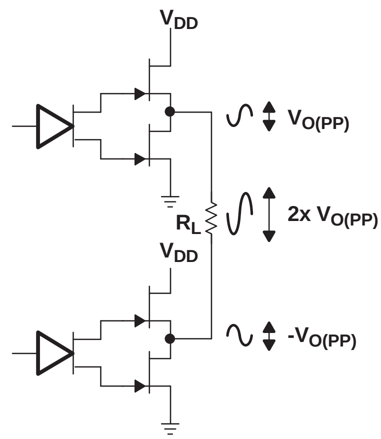


Figure 33. Differential Output Configuration

In a typical wireless handset operating at 3.6 V, bridging raises the power into an 8-Ω speaker from a singled-ended (SE, ground reference) limit of 200 mW to 800 mW. This is a 6-dB improvement in sound power—loudness that can be heard. In addition to increased power, there are frequency-response concerns. Consider the single-supply SE configuration shown in Figure 34. A coupling capacitor (C_C) is required to block the dc-offset voltage from the load. This capacitor can be quite large (approximately 33 μF to 1000 μF) so it tends to be expensive, heavy, occupy valuable PCB area, and have the additional drawback of limiting low-frequency performance. This frequency-limiting effect is due to the high-pass filter network created with the speaker impedance and the coupling capacitance. This is calculated with Equation 13.

$$f_c = \frac{1}{2\pi R_L C_C} \tag{13}$$

For example, a 68-µF capacitor with an 8-Ω speaker would attenuate low frequencies below 293 Hz. The BTL configuration cancels the dc offsets, which eliminates the need for the blocking capacitors. Low-frequency performance is then limited only by the input network and speaker response. Cost and PCB space are also minimized by eliminating the bulky coupling capacitor.

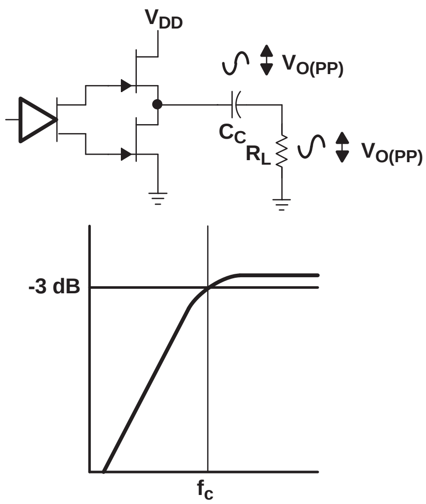


Figure 34. Single-Ended Output and Frequency Response

Increasing power to the load does carry a penalty of increased internal power dissipation. The increased dissipation is understandable considering that the BTL configuration produces 4× the output power of the SE configuration.

FULLY DIFFERENTIAL AMPLIFIER EFFICIENCY AND THERMAL INFORMATION

Class-AB amplifiers are inefficient, primarily because of voltage drop across the output-stage transistors. The two components of this internal voltage drop are the headroom or dc voltage drop that varies inversely to output power, and the sinewave nature of the output. The total voltage drop can be calculated by subtracting the RMS value of the output voltage from V_{DD}. The internal voltage drop multiplied by the average value of the supply current, I_{DD}(avg), determines the internal power dissipation of the amplifier.

An easy-to-use equation to calculate efficiency starts out as being equal to the ratio of power from the power supply to the power delivered to the load. To accurately calculate the RMS and average values of power in the load and in the amplifier, the current and voltage waveform shapes must first be understood (see Figure 35).

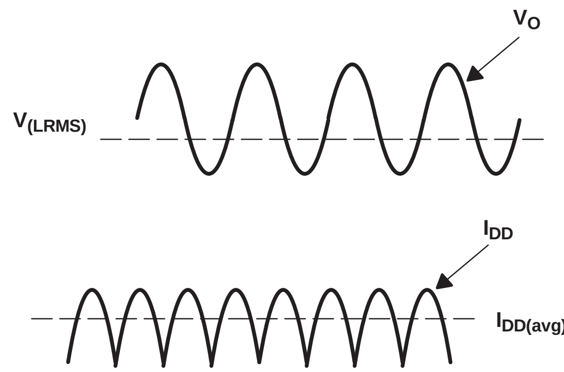


Figure 35. Voltage and Current Waveforms for BTL Amplifiers

Although the voltages and currents for SE and BTL are sinusoidal in the load, currents from the supply are different between SE and BTL configurations. In an SE application the current waveform is a half-wave rectified shape, whereas in BTL it is a full-wave rectified waveform. This means RMS conversion factors are different. Keep in mind that for most of the waveform both the push and pull transistors are not on at the same time, which supports the fact that each amplifier in the BTL device only draws current from the supply for half the waveform. The following equations are the basis for calculating amplifier efficiency.

$$\text{Efficiency of a BTL amplifier} = \frac{P_L}{P_{SUP}}$$

Where:

$$P_L = \frac{V_L rms^2}{R_L}, \text{ and } V_{LRMS} = \frac{V_P}{\sqrt{2}}, \text{ therefore, } P_L = \frac{V_P^{\;2}}{2R_L}$$

$$\text{and } P_{SUP} = V_{DD}\, I_{DD}avg \quad \text{and} \quad I_{DD}avg = \frac{1}{\pi}\int_0^{\pi} \frac{V_P}{R_L}\sin(t)\,dt = -\frac{1}{\pi} \times \frac{V_P}{R_L}\left[\cos(t)\right]_0^{\pi} = \frac{2V_P}{\pi R_L}$$

Therefore,

$$P_{SUP} = \frac{2\,V_{DD}\,V_P}{\pi\,R_L}$$

substituting P_L and P_{SUP} into equation 6,

$$\text{Efficiency of a BTL amplifier} = \frac{\dfrac{V_P^{\;2}}{2\,R_L}}{\dfrac{2\,V_{DD}\,V_P}{\pi\,R_L}} = \frac{\pi\,V_P}{4\,V_{DD}}$$

Where:

$$V_P = \sqrt{2\,P_L\,R_L}$$

P_L = Power delivered to load
P_{SUP} = Power drawn from power supply
V_{LRMS} = RMS voltage on BTL load
R_L = Load resistance
V_P = Peak voltage on BTL load
$I_{DD}avg$ = Average current drawn from the power supply
V_{DD} = Power supply voltage
η_{BTL} = Efficiency of a BTL amplifier

(14)

Therefore,

$$\eta_{BTL} = \frac{\pi\sqrt{2\,P_L\,R_L}}{4\,V_{DD}} \qquad (15)$$

Table 2. Efficiency and Maximum Ambient Temperature vs Output Power

Output Power (W)	Efficiency (%)	Internal Dissipation (W)	Power From Supply (W)	Max Ambient Temperature (1) (°C)
5-V, 3-Ω Systems				
0.5	27.2	1.34	1.84	85 (2)
1	38.4	1.60	2.60	76
2.45	60.2	1.62	4.07	75
3.1	67.7	1.48	4.58	82
5-V, 4-Ω BTL Systems				
0.5	31.4	1.09	1.59	85 (2)
1	44.4	1.25	2.25	85 (2)
2	62.8	1.18	3.18	85 (2)
2.8	74.3	0.97	3.77	85 (2)
5-V, 8-Ω Systems				
0.5	44.4	0.625	1.13	85 (2)
1	62.8	0.592	1.60	85 (2)
1.36	73.3	0.496	1.86	85 (2)
1.7	81.9	0.375	2.08	85 (2)

(1) DRB package
(2) Package limited to 85°C ambient

Table 2 employs Equation 15 to calculate efficiencies for four different output power levels. Note that the efficiency of the amplifier is quite low for lower power levels and rises sharply as power to the load is increased resulting in a nearly flat internal power dissipation over the normal operating range. Note that the internal dissipation at full output power is less than in the half power range. Calculating the efficiency for a specific system is the key to proper power supply design. For a 2.8-W audio system with 4-Ω loads and a 5-V supply, the maximum draw on the power supply is almost 3.8 W.

A final point to remember about Class-AB amplifiers is how to manipulate the terms in the efficiency equation to the utmost advantage when possible. Note that in Equation 15, V_{DD} is in the denominator. This indicates that as V_{DD} goes down, efficiency goes up.

A simple formula for calculating the maximum power dissipated, P_{Dmax}, may be used for a differential output application:

$$P_{Dmax} = \frac{2V_{DD}^2}{\pi^2 R_L} \quad (16)$$

P_{Dmax} for a 5-V, 4-Ω system is 1.27 W.

The maximum ambient temperature depends on the heat sinking ability of the PCB system. The derating factor for the 3 mm ×3 mm DRB package is shown in the dissipation rating table. Converting this to θ_{JA}:

$$\theta_{JA} = \frac{1}{\text{Derating Factor}} = \frac{1}{0.0218} = 45.9°C/W \quad (17)$$

Given θ_{JA}, the maximum allowable junction temperature, and the maximum internal dissipation, the maximum ambient temperature can be calculated with Equation 18. The maximum recommended junction temperature for the TPA6211A1 is 150°C.

$$\begin{aligned} T_A\,Max &= T_J\,Max - \theta_{JA} P_{Dmax} \\ &= 150 - 45.9(1.27) = 91.7°C \end{aligned} \quad (18)$$

Equation 18 shows that the maximum ambient temperature is 91.7°C (package limited to 85°C ambient) at maximum power dissipation with a 5-V supply.

Table 2 shows that for most applications no airflow is required to keep junction temperatures in the specified range. The TPA6211A1 is designed with thermal protection that turns the device off when the junction temperature surpasses 150°C to prevent damage to the IC. In addition, using speakers with an impedance higher than 4-Ω dramatically increases the thermal performance by reducing the output current.

PCB LAYOUT

Use the following land pattern for board layout with the 8-pin QFN (DRB) package. Note that the solder paste should use a hatch pattern to fill solder paste at 50% to ensure that there is not too much solder paste under the package.

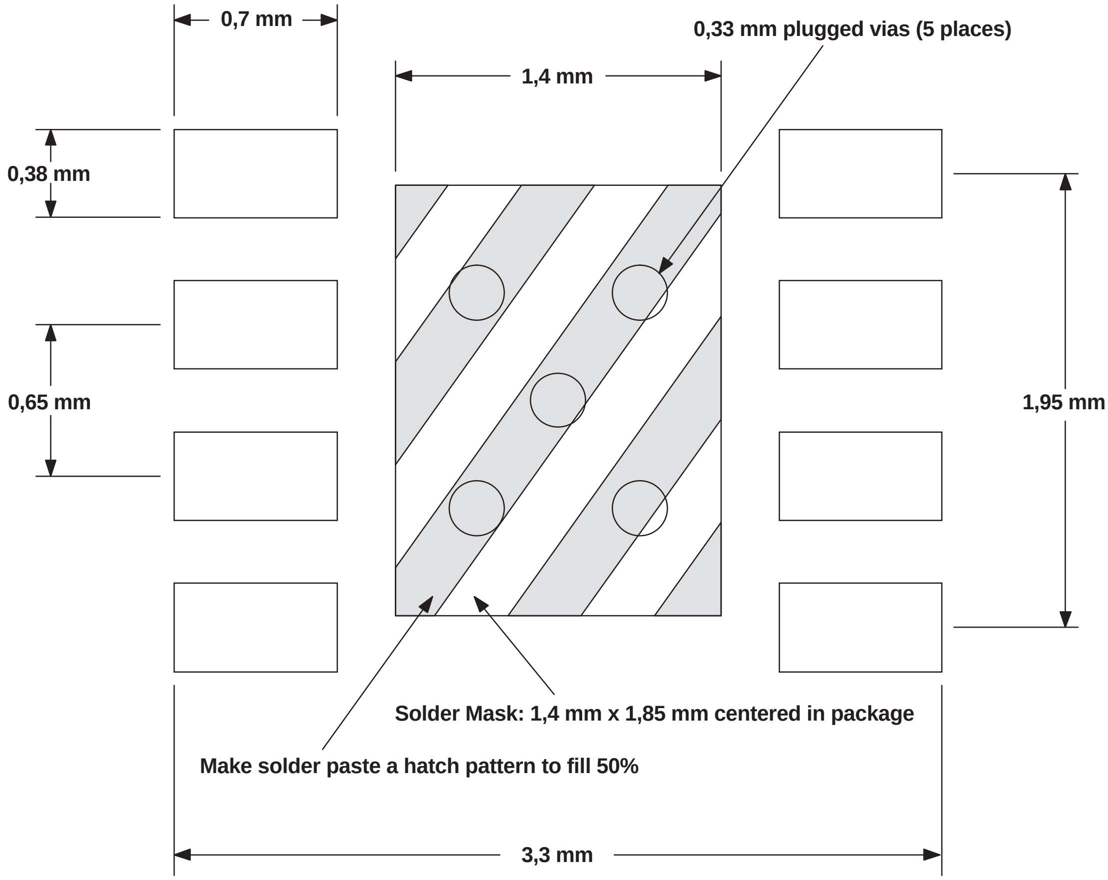


Figure 36. TPA6211A1 8-Pin QFN (DRB) Board Layout (Top View)

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TPA6211A1DGN	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM		AYK	Samples
TPA6211A1DGNG4	ACTIVE	MSOP-PowerPAD	DGN	8	80	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		AYK	Samples
TPA6211A1DGNR	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU | CU NIPDAUAG	Level-1-260C-UNLIM		AYK	Samples
TPA6211A1DGNRG4	ACTIVE	MSOP-PowerPAD	DGN	8	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM		AYK	Samples
TPA6211A1DRB	ACTIVE	SON	DRB	8	121	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		AYN	Samples
TPA6211A1DRBG4	ACTIVE	SON	DRB	8	121	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		AYN	Samples
TPA6211A1DRBR	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		AYN	Samples
TPA6211A1DRBRG4	ACTIVE	SON	DRB	8	3000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR		AYN	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

[4] There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

[5] Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

[6] Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

OTHER QUALIFIED VERSIONS OF TPA6211A1 :

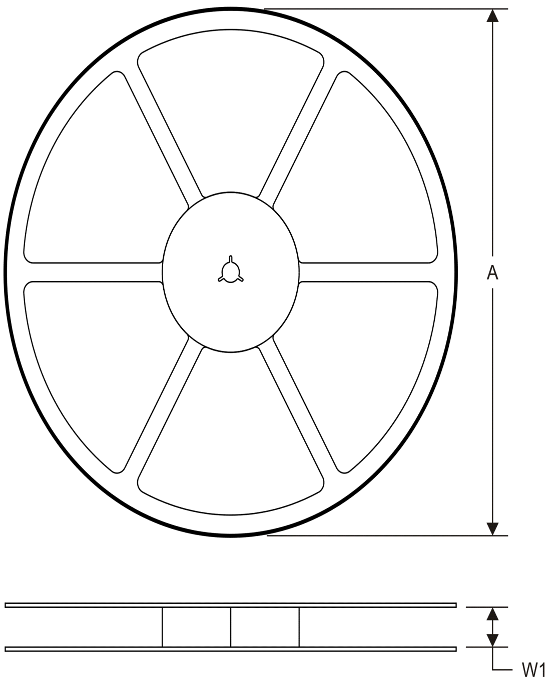
- Automotive: TPA6211A1-Q1

NOTE: Qualified Version Definitions:

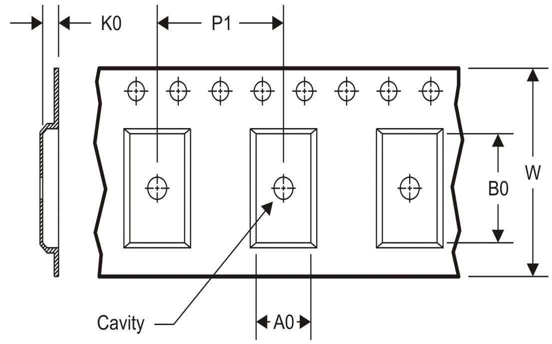
- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



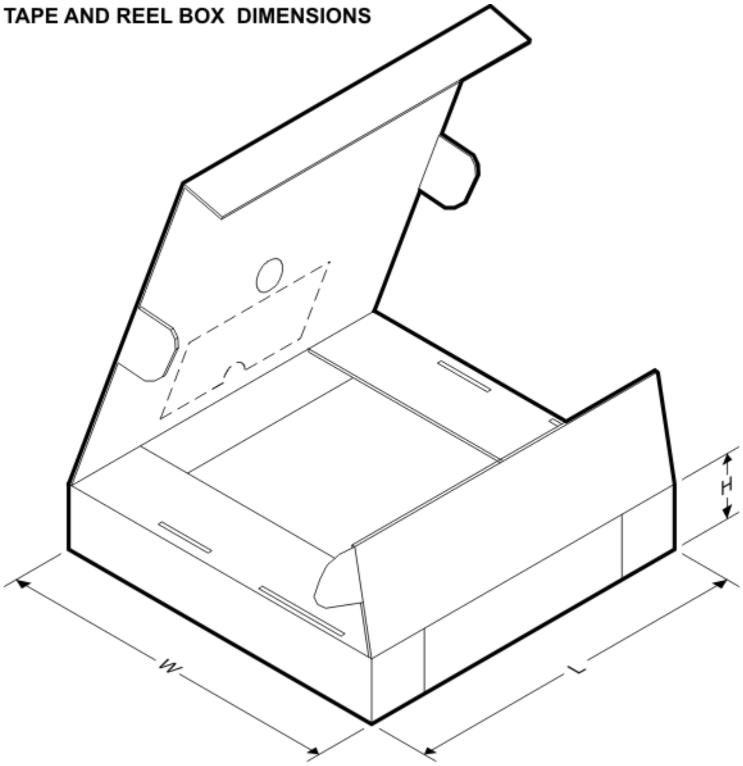
A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

TAPE AND REEL INFORMATION

*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TPA6211A1DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6211A1DGNR	MSOP-Power PAD	DGN	8	2500	330.0	12.4	5.3	3.4	1.4	8.0	12.0	Q1
TPA6211A1DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2
TPA6211A1DRBR	SON	DRB	8	3000	330.0	12.4	3.3	3.3	1.1	8.0	12.0	Q2

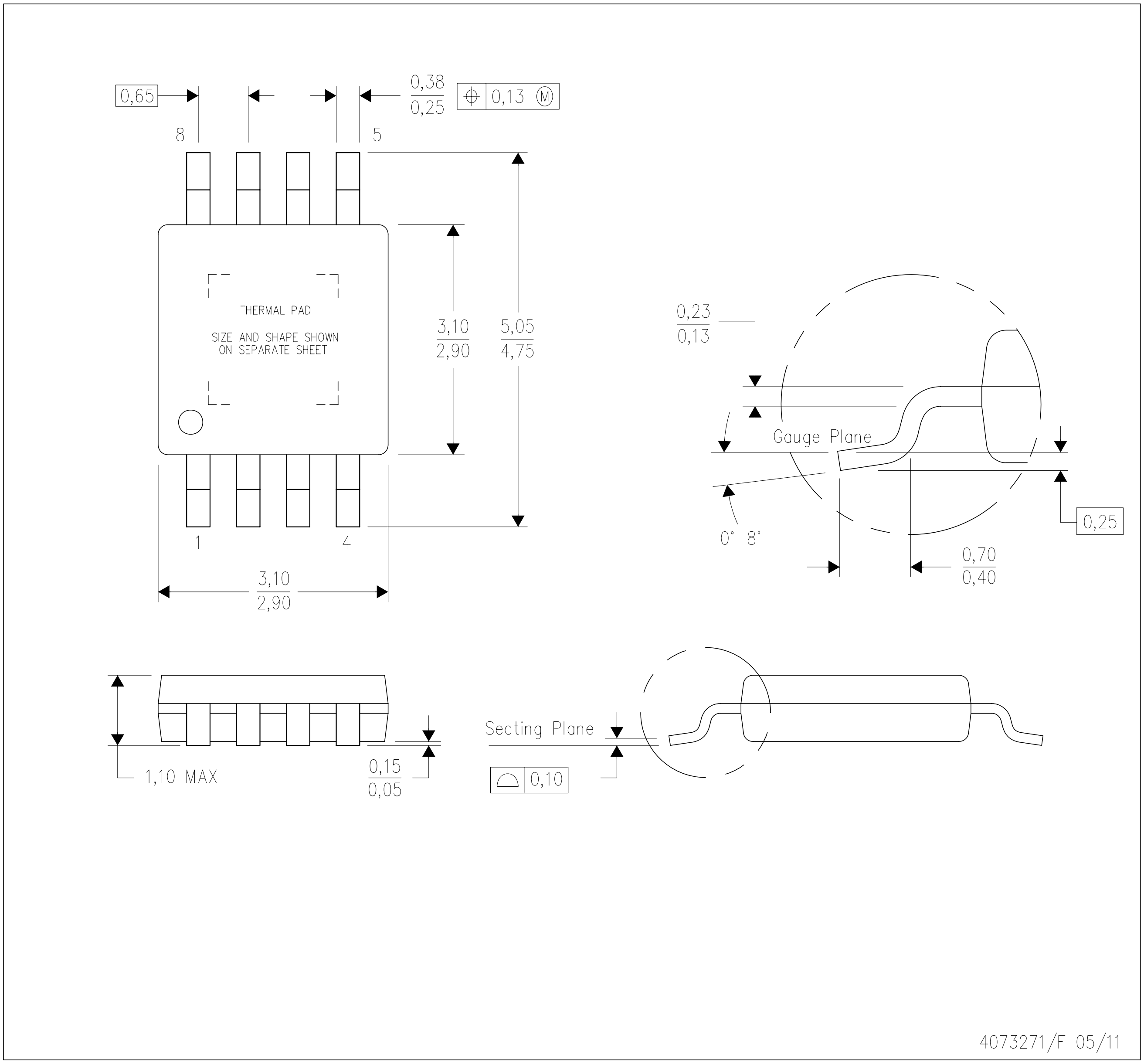
TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TPA6211A1DGNR	MSOP-PowerPAD	DGN	8	2500	358.0	335.0	35.0
TPA6211A1DGNR	MSOP-PowerPAD	DGN	8	2500	364.0	364.0	27.0
TPA6211A1DRBR	SON	DRB	8	3000	367.0	367.0	35.0
TPA6211A1DRBR	SON	DRB	8	3000	367.0	367.0	35.0

DGN (S-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <http: //www.ti.com>.
- E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
- F. Falls within JEDEC MO-187 variation AA-T

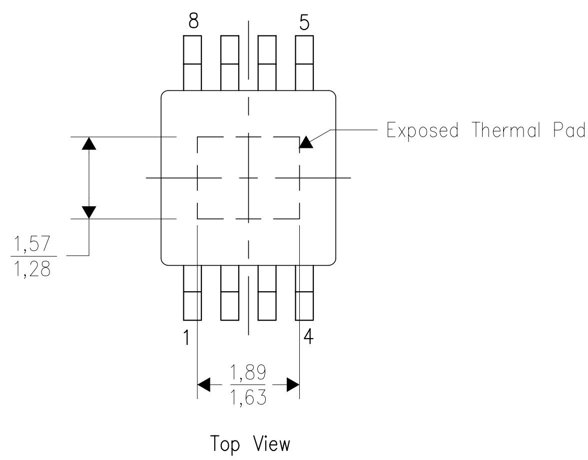
DGN (S–PDSO–G8) PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



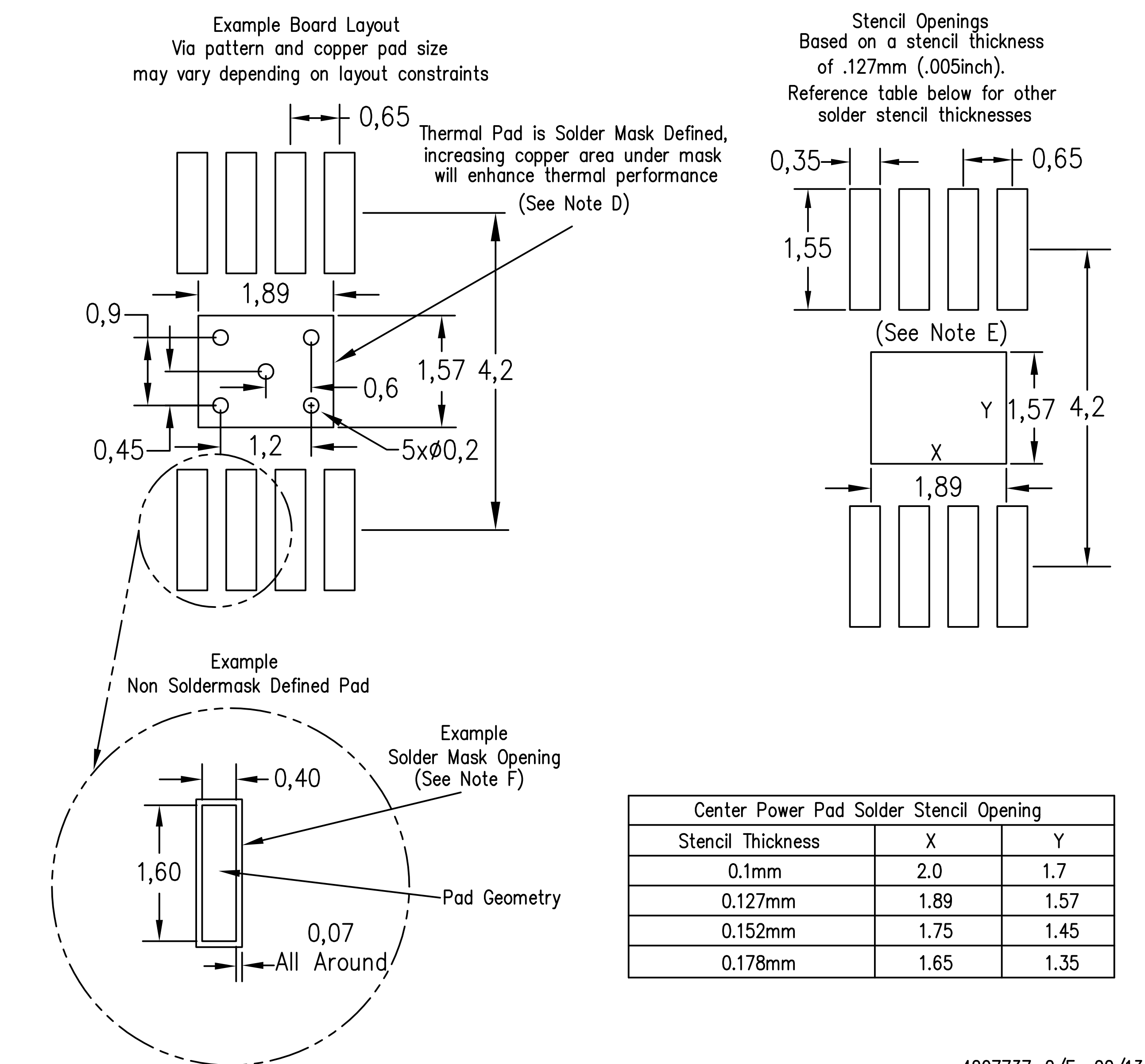
Exposed Thermal Pad Dimensions

4206323–2/I 12/11

NOTE: All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments

DGN (R-PDSO-G8) PowerPAD™ PLASTIC SMALL OUTLINE



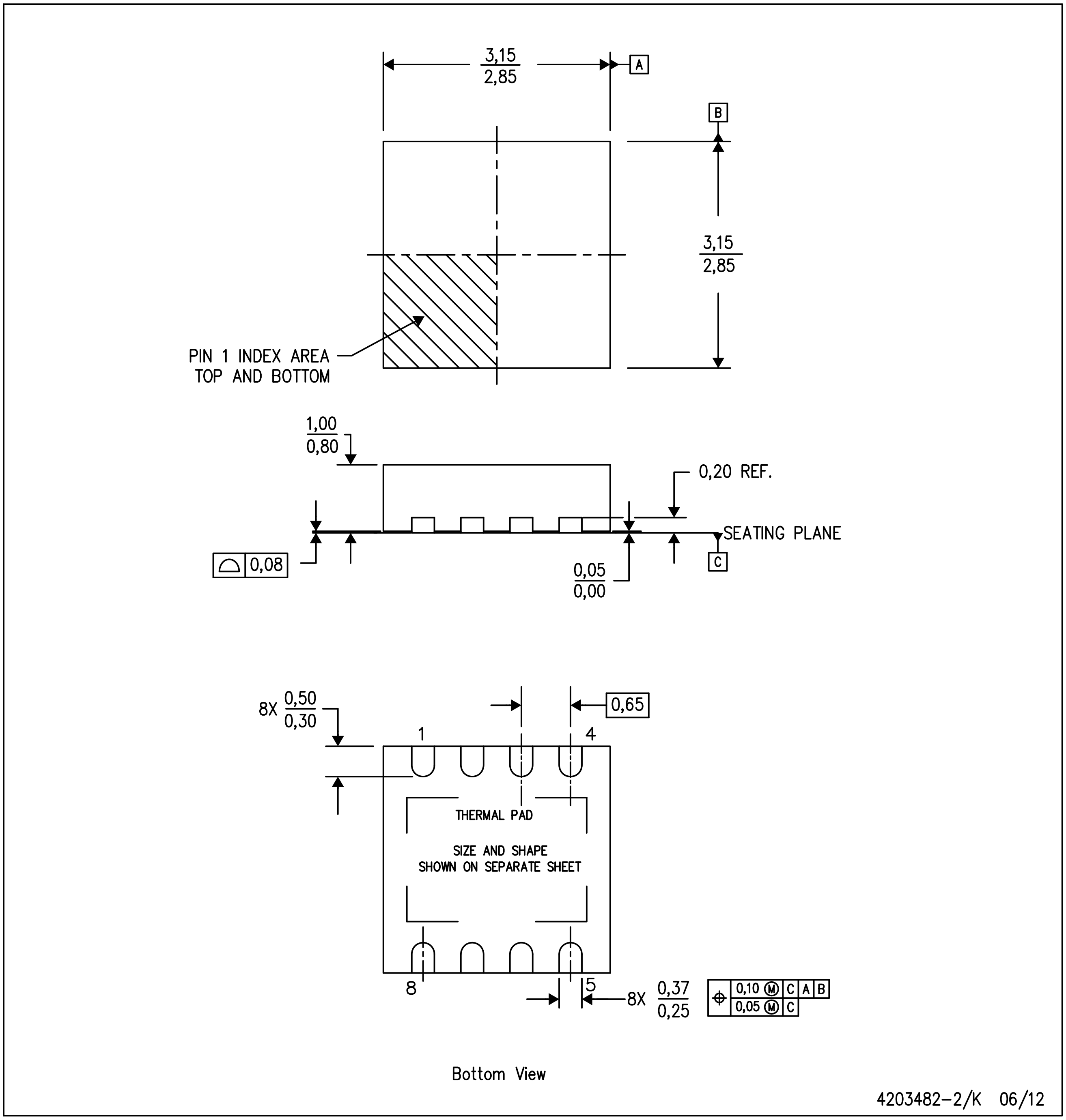
Center Power Pad Solder Stencil Opening		
Stencil Thickness	X	Y
0.1mm	2.0	1.7
0.127mm	1.89	1.57
0.152mm	1.75	1.45
0.178mm	1.65	1.35

4207737-2/F 02/13

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
- F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments

DRB (S–PVSON–N8) PLASTIC SMALL OUTLINE NO–LEAD



NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Small Outline No–Lead (SON) package configuration.
D. The package thermal pad must be soldered to the board for thermal and mechanical performance.
E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.

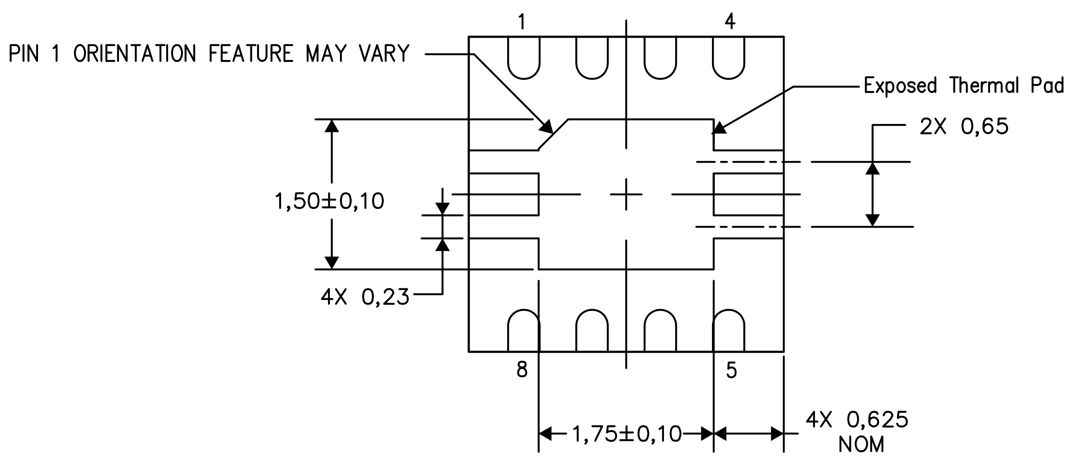
DRB (S-PVSON-N8) PLASTIC SMALL OUTLINE NO-LEAD

THERMAL INFORMATION

This package incorporates an exposed thermal pad that is designed to be attached directly to an external heatsink. The thermal pad must be soldered directly to the printed circuit board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For information on the Quad Flatpack No-Lead (QFN) package and its advantages, refer to Application Report, QFN/SON PCB Attachment, Texas Instruments Literature No. SLUA271. This document is available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Bottom View

Exposed Thermal Pad Dimensions

4206340-2/N 09/12

NOTE: All linear dimensions are in millimeters

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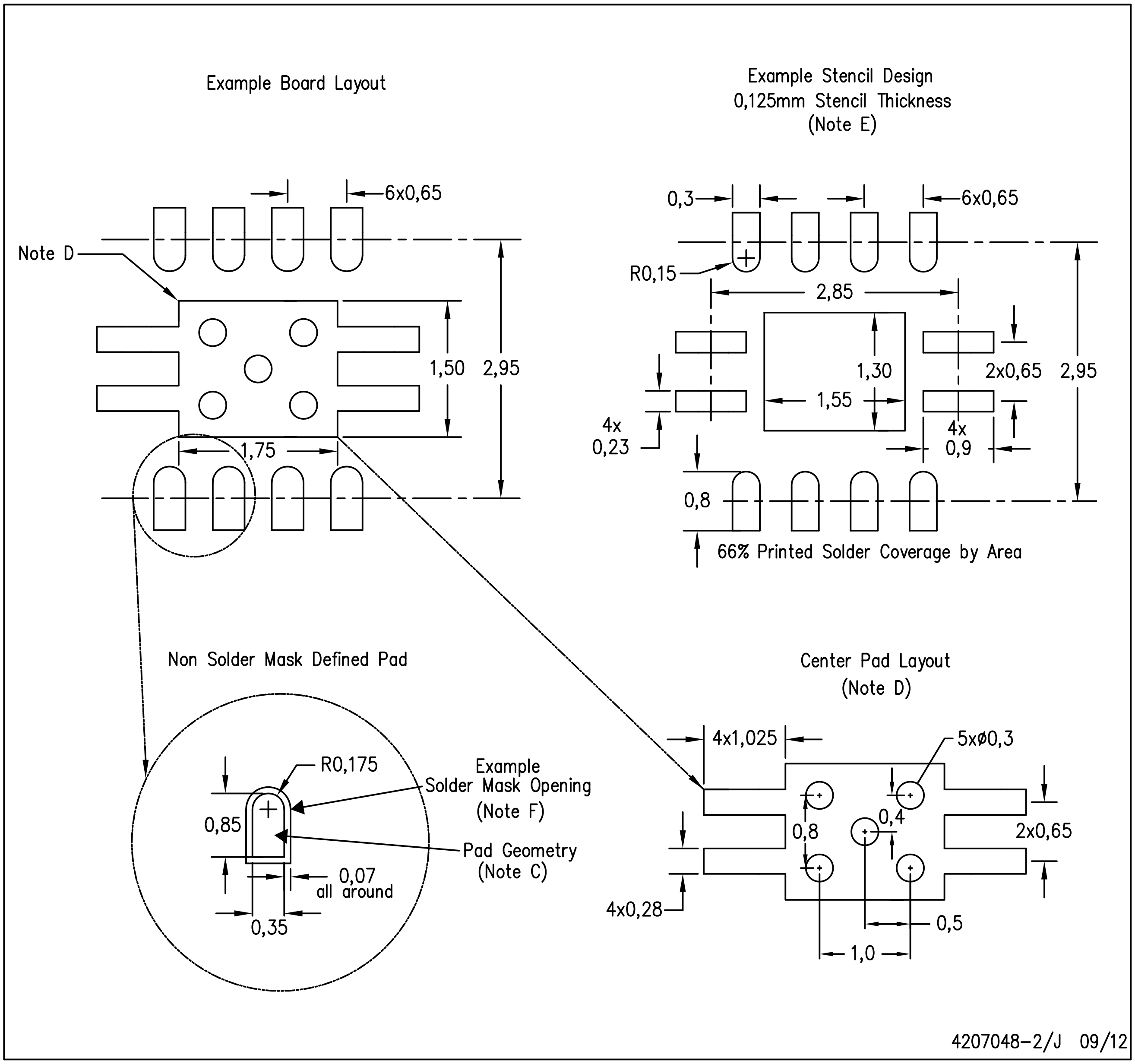

NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–7351 is recommended for alternate designs.
- D. This package is designed to be soldered to a thermal pad on the board. Refer to Application Note, QFN Packages, Texas Instruments Literature No. SLUA271, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <http: //www.ti.com>.
- E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC 7525 for stencil design considerations.
- F. Customers should contact their board fabrication site for solder mask tolerances.

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