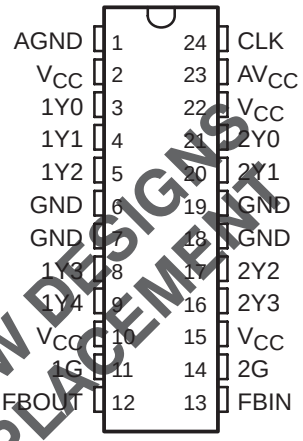
- **Use *CDCVF2509A* as a Replacement for this Device**
- **Spread Spectrum Clock Compatible**
- **100-MHz Maximum Frequency**
- **Available in Plastic 24-Pin TSSOP**
- **Phase-Lock Loop Clock Distribution for Synchronous DRAM Applications**
- **Distributes One Clock Input to One Bank of Five and One Bank of Four Outputs**
- **Separate Output Enable for Each Output Bank**
- **External Feedback (FBIN) Pin Is Used to Synchronize the Outputs to the Clock Input**
- **On-Chip Series Damping Resistors**
- **No External RC Network Required**
- **Operates at 3.3-V $V_{CC}$**

**PW PACKAGE**
**(TOP VIEW)**




NOT RECOMMENDED FOR NEW DESIGNS
USE CDCVF2509A AS A REPLACEMENT

## description

The CDC2509A is a high-performance, low-skew, low-jitter, phase-lock loop (PLL) clock driver. It uses a PLL to precisely align, in both frequency and phase, the feedback (FBOUT) output to the clock (CLK) input signal. It is specifically designed for use with synchronous DRAMs. The CDC2509A operates at 3.3-V $V_{CC}$ and provides integrated series-damping resistors that make it ideal for driving point-to-point loads.

One bank of five outputs and one bank of four outputs provide nine low-skew, low-jitter copies of CLK. Output signal duty cycles are adjusted to 50 percent, independent of the duty cycle at CLK. Each bank of outputs can be enabled or disabled separately via the control (1G and 2G) inputs. When the G inputs are high, the outputs switch in phase and frequency with CLK; when the G inputs are low, the outputs are disabled to the logic-low state.

Unlike many products containing PLLs, the CDC2509A does not require external RC networks. The loop filter for the PLL is included on-chip, minimizing component count, board space, and cost.

Because it is based on PLL circuitry, the CDC2509A requires a stabilization time to achieve phase lock of the feedback signal to the reference signal. This stabilization time is required, following power up and application of a fixed-frequency, fixed-phase signal at CLK, and following any changes to the PLL reference or feedback signals. The PLL can be bypassed for test purposes by strapping $AV_{CC}$ to ground.

The CDC2509A is characterized for operation from 0°C to 70°C.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

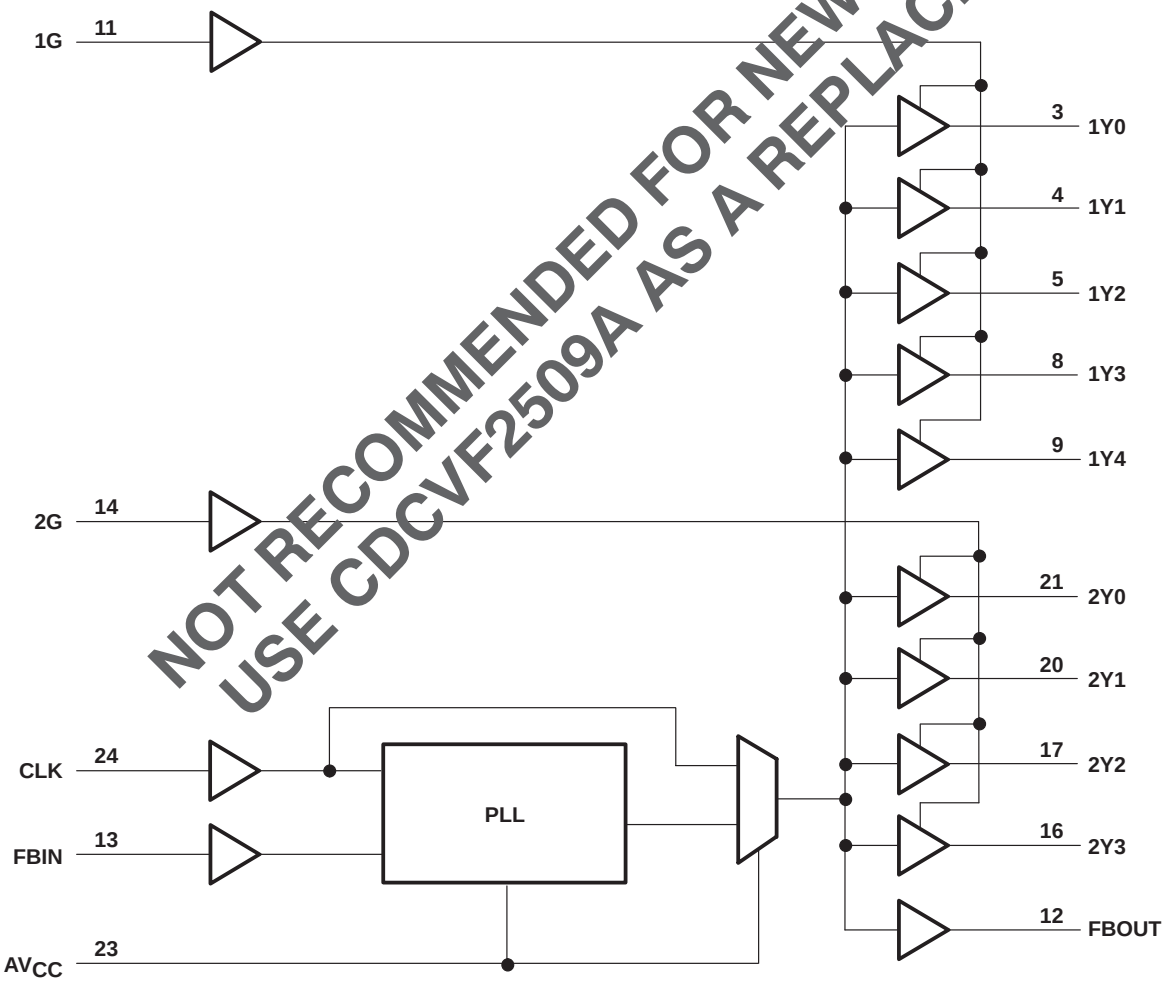
Copyright © 2001 − 2004, Texas Instruments Incorporated

**FUNCTION TABLE**

| INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|
| 1G | 2G | CLK | 1Y (0:4) | 2Y (0:3) | FBOUT |
| X | X | L | L | L | L |
| L | L | H | L | L | H |
| L | H | H | L | H | H |
| H | L | H | H | L | H |
| H | H | H | H | H | H |

NOT RECOMMENDED FOR NEW DESIGNS
USE CDCVF2509A AS A REPLACEMENT

## functional block diagram




**AVAILABLE OPTIONS**

| $T_A$ | PACKAGE |
|---|---|
| | SMALL OUTLINE (PW) |
| 0°C to 70°C | CDC2509APWR |

## Terminal Functions

| TERMINAL | | TYPE | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| CLK | 24 | I | Clock input. CLK provides the clock signal to be distributed by the CDC2509A clock driver. CLK is used to provide the reference signal to the integrated PLL that generates the clock output signals. CLK must have a fixed frequency and fixed phase for the PLL to obtain phase lock. Once the circuit is powered up and a valid CLK signal is applied, a stabilization time is required for the PLL to phase lock the feedback signal to its reference signal. |
| FBIN | 13 | I | Feedback input. FBIN provides the feedback signal to the internal PLL. FBIN must be hard-wired to FBOUT to complete the PLL. The integrated PLL synchronizes CLK and FBIN so that there is nominally zero phase error between CLK and FBIN. |
| 1G | 11 | I | Output bank enable. 1G is the output enable for outputs 1Y(0:4). When 1G is low, outputs 1Y(0:4) are disabled to a logic-low state. When 1G is high, all outputs 1Y(0:4) are enabled and switch at the same frequency as CLK. |
| 2G | 14 | I | Output bank enable. 2G is the output enable for outputs 2Y(0:3). When 2G is low, outputs 2Y(0:3) are disabled to a logic low state. When 2G is high, all outputs 2Y(0:3) are enabled and switch at the same frequency as CLK. |
| FBOUT | 12 | O | Feedback output. FBOUT is dedicated for external feedback. It switches at the same frequency as CLK. When externally wired to FBIN, FBOUT completes the feedback loop of the PLL. FBOUT has and integrated 25-Ω series-damping resistor. |
| 1Y (0:4) | 3, 4, 5, 8, 9 | O | Clock outputs. These outputs provide low-skew copies of CLK. Output bank 1Y(0:4) is enabled via the 1G input. These outputs can be disabled to a logic-low state by deasserting the 1G control input. Each output has an integrated 25-Ω series-damping resistor. |
| 2Y (0:3) | 16, 17, 20, 21 | O | Clock outputs. These outputs provide low-skew copies of CLK. Output bank 2Y(0:3) is enabled via the 2G input. These outputs can be disabled to a logic-low state by deasserting the 2G control input. Each output has an integrated 25-Ω series-damping resistor. |
| $AV_{CC}$ | 23 | Power | Analog power supply. $AV_{CC}$ provides the power reference for the analog circuitry. In addition, $AV_{CC}$ can be used to bypass the PLL for test purposes. When $AV_{CC}$ is strapped to ground, PLL is bypassed and CLK is buffered directly to the device outputs. |
| AGND | 1 | Ground | Analog ground. AGND provides the ground reference for the analog circuitry. |
| $V_{CC}$ | 2, 10, 15, 22 | Power | Power supply |
| GND | 6, 7, 18, 19 | Ground | Ground |

NOT RECOMMENDED FOR NEW DESIGNS
USE CDCVF2509A AS A REPLACEMENT

### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $AV_{CC}$ (see Note 1) . . . . . $AV_{CC} < V_{CC}$ +0.7 V
Supply voltage range, $V_{CC}$ . . . . . −0.5 V to 4.6 V
Input voltage range, $V_I$ (see Note 2) . . . . . −0.5 V to 6.5 V
Voltage range applied to any output in the high or low state,
$V_O$ (see Notes 2 and 3) . . . . . −0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I < 0$) . . . . . −50 mA
Output clamp current, $I_{OK}$ ($V_O < 0$ or $V_O > V_{CC}$) . . . . . ±50 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±50 mA
Continuous current through each $V_{CC}$ or GND . . . . . ±100 mA
Maximum power dissipation at $T_A$ = 55°C (in still air) (see Note 4) . . . . . 0.7 W
Storage temperature range, $T_{stg}$ . . . . . −65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. $AV_{CC}$ **must not** exceed $V_{CC}$.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. This value is limited to 4.6 V maximum.
4. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils. For more information, refer to the *Package Thermal Considerations* application note in the *ABT Advanced BiCMOS Technology Data Book*, literature number SCBD002.

NOT RECOMMENDED FOR NEW DESIGNS
USE CDCVF2509A AS A REPLACEMENT

### recommended operating conditions (see Note 5)

| | MIN | MAX | UNIT |
|---|---|---|---|
| Supply voltage, $V_{CC}$, $AV_{CC}$ | 3 | 3.6 | V |
| High-level input voltage, $V_{IH}$ | 2 | | V |
| Low-level input voltage, $V_{IL}$ | | 0.8 | V |
| Input voltage, $V_I$ | 0 | $V_{CC}$ | V |
| High-level output current, $I_{OH}$ | | −12 | mA |
| Low-level output current, $I_{OL}$ | | 12 | mA |
| Operating free-air temperature, $T_A$ | 0 | 70 | °C |

NOTE 5: Unused inputs must be held high or low to prevent them from floating.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | $V_{CC}$, $AV_{CC}$ | MIN | TYP‡ | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| $V_{IK}$ | $I_I$ = −18 mA | | 3 V | | | −1.2 | V |
| $V_{OH}$ | $I_{OH}$ = −100 µA | | MIN to MAX | $V_{CC}$−0.2 | | | V |
| | $I_{OH}$ = −12 mA | | 3 V | 2.1 | | | |
| | $I_{OH}$ = −6 mA | | 3 V | 2.4 | | | |
| $V_{OL}$ | $I_{OL}$ = 100 µA | | MIN to MAX | | | 0.2 | V |
| | $I_{OL}$ = 12 mA | | 3 V | | | 0.8 | |
| | $I_{OL}$ = 6 mA | | 3 V | | | 0.55 | |
| $I_I$ | $V_I = V_{CC}$ or GND | | 3.6 V | | | ±5 | µA |
| $I_{CC}$§ | $V_I = V_{CC}$ or GND, | $I_O$ = 0, Outputs: low or high | 3.6 V | | | 10 | µA |
| $\Delta I_{CC}$ | One input at $V_{CC}$ − 0.6 V, | Other inputs at $V_{CC}$ or GND | 3.3 V to 3.6 V | | | 500 | µA |
| $C_i$ | $V_I = V_{CC}$ or GND | | 3.3 V | | 4 | | pF |
| $C_o$ | $V_O = V_{CC}$ or GND | | 3.3 V | | 6 | | pF |

‡ For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.
§ For $I_{CC}$ of $AV_{CC}$, see Figure 5.

NOT RECOMMENDED FOR NEW DESIGNS
USE CDCVF2509A AS A REPLACEMENT

## timing requirements over recommended ranges of supply voltage and operating free-air temperature

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $f_{clk}$ | Clock frequency | 80 | 100 | MHz |
| | Input clock duty cycle | 40% | 60% | |
| | Stabilization time† | | 1 | ms |

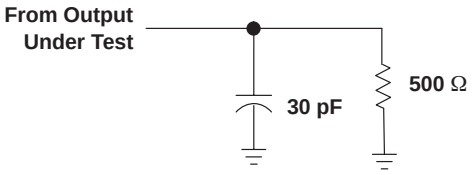
† Time required for the integrated PLL circuit to obtain phase lock of its feedback signal to its reference signal. For phase lock to be obtained, a fixed-frequency, fixed-phase reference signal must be present at CLK. Until phase lock is obtained, the specifications for propagation delay, skew, and jitter parameters given in the switching characteristics table are not applicable. This parameter does not apply for input modulation under SSC application.

## switching characteristics over recommended ranges of supply voltage and operating free-air temperature, $C_L$ = 30 pF (see Note 6 and Figures 1 and 2)‡

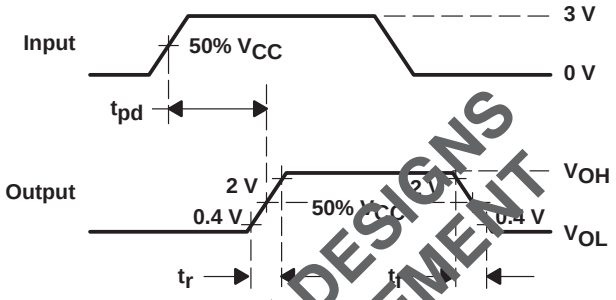
| PARAMETER | FROM (INPUT)/CONDITION | TO (OUTPUT) | $V_{CC}$, $AV_{CC}$ = 3.3 V ± 0.165 V | | | $V_{CC}$, $AV_{CC}$ = 3.3 V ± 0.3 V | | | UNIT |
|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | TYP | MAX | |
| $t_{phase\ error}$, reference (see Note 7, Figure 3) | 80 MHz < CLKIN↑ ≤ 100 MHz | FBIN↑ | | | | −700 | | −300 | ps |
| $t_{phase\ error}$, − jitter (see Note 8) | CLKIN↑ = 100 MHz | FBIN↑ | −750 | | −350 | | −540 | | ps |
| $t_{sk(o)}$§ | Any Y or FBOUT | Any Y or FBOUT | | | | | | 200 | ps |
| $Jitter_{(pk-pk)}$ (see Figure 4) | Clkin = 100 MHz | Any Y or FBOUT | | | | −150 | | 150 | ps |
| Duty cycle | F(clkin > 80 MHz) | Any Y or FBOUT | | | | 45% | | 55% | |
| $t_r$ | | Any Y or FBOUT | | 1.3 | 1.9 | 0.8 | | 2.1 | ns |
| $t_f$ | | Any Y or FBOUT | | 1.7 | 2.5 | 1.2 | | 2.7 | ns |

‡ These parameters are not production tested.
§ The $t_{sk(o)}$ specification is only valid for equal loading of all outputs.
NOTES: 6. The specifications for parameters in this table are applicable only after any appropriate stabilization time has elapsed.
7. This is considered as static phase error.
8. Phase error does not include jitter. The total phase error is −900 ps to −200 ps for the 5% $V_{CC}$ range.

## PARAMETER MEASUREMENT INFORMATION




LOAD CIRCUIT FOR OUTPUTS




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES

NOTES: A. $C_L$ includes probe and jig capacitance.
B. All input pulses are supplied by generators having the following characteristics: PRR ≤ 100 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 1.2 ns, $t_f$ ≤ 1.2 ns.
C. The outputs are measured one at a time with one transition per measurement.

**Figure 1. Load Circuit and Voltage Waveforms**

NOT RECOMMENDED FOR NEW DESIGNS
USE CDCVF2509A AS A REPLACEMENT

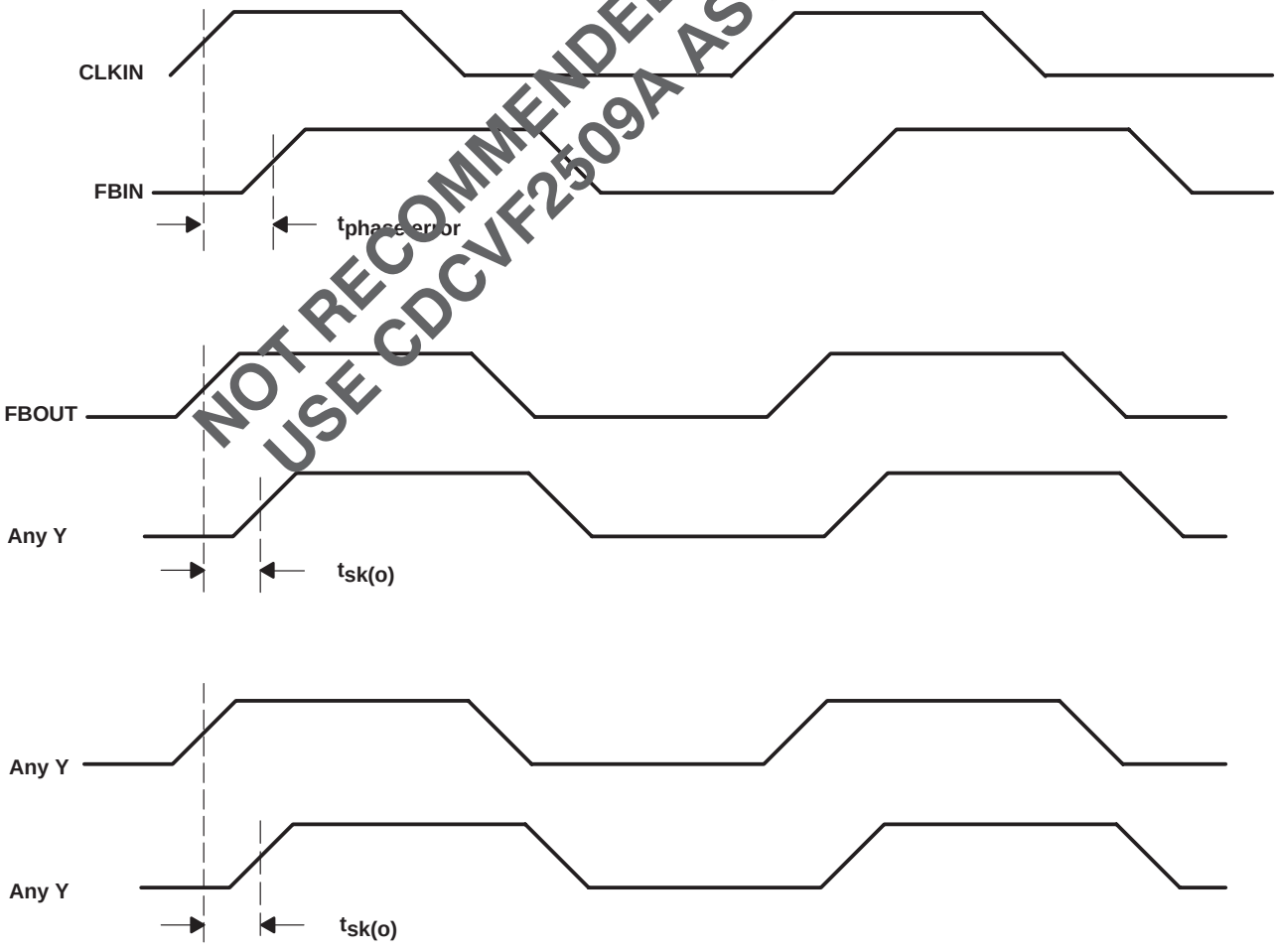



**Figure 2. Phase Error and Skew Calculations**

## TYPICAL CHARACTERISTICS

**STATIC PHASE ERROR vs CLOCK FREQUENCY**

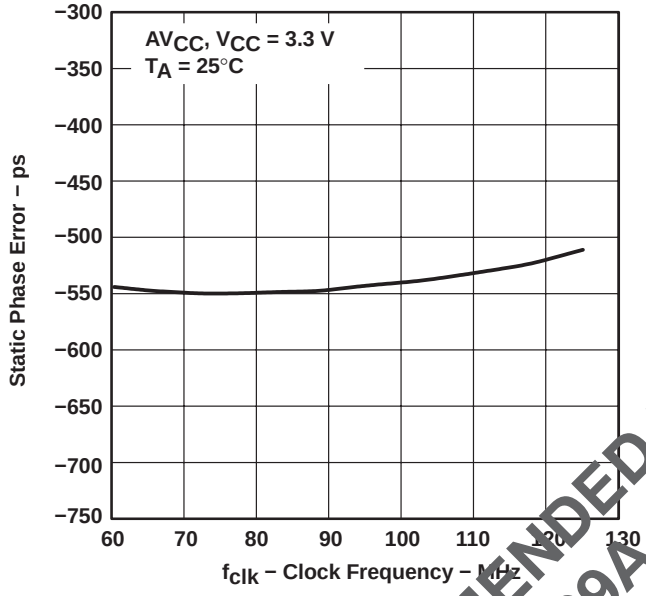



Figure 3

**JITTER (PEAK-TO-PEAK) vs CLOCK FREQUENCY**

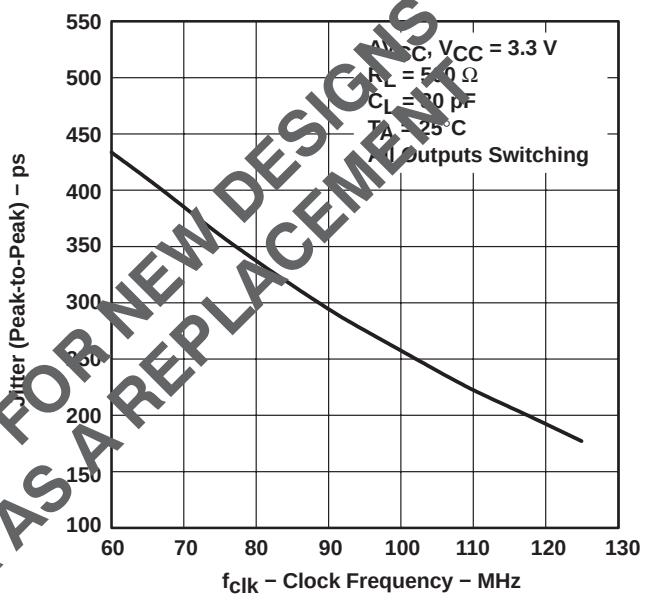



Figure 4

**ANALOG SUPPLY CURRENT vs CLOCK FREQUENCY**

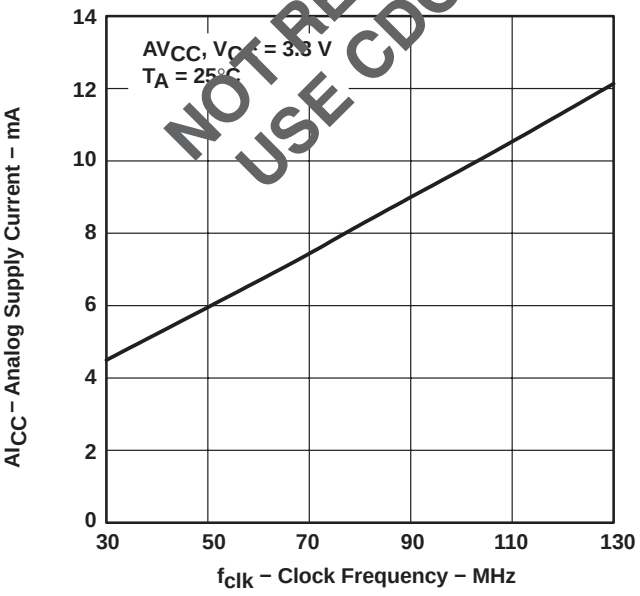



Figure 5

**SUPPLY CURRENT vs CLOCK FREQUENCY**

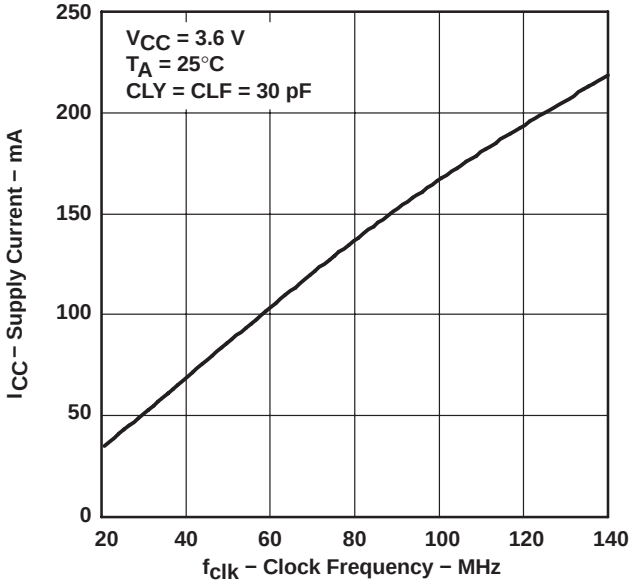



Figure 6

NOT RECOMMENDED FOR NEW DESIGNS
USE CDCVF2509A AS A REPLACEMENT

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish | MSL Peak Temp (3) | Op Temp (°C) | Top-Side Markings (4) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CDC2509APWR | NRND | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CK2509A | |
| CDC2509APWRG4 | NRND | TSSOP | PW | 24 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM | 0 to 70 | CK2509A | |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

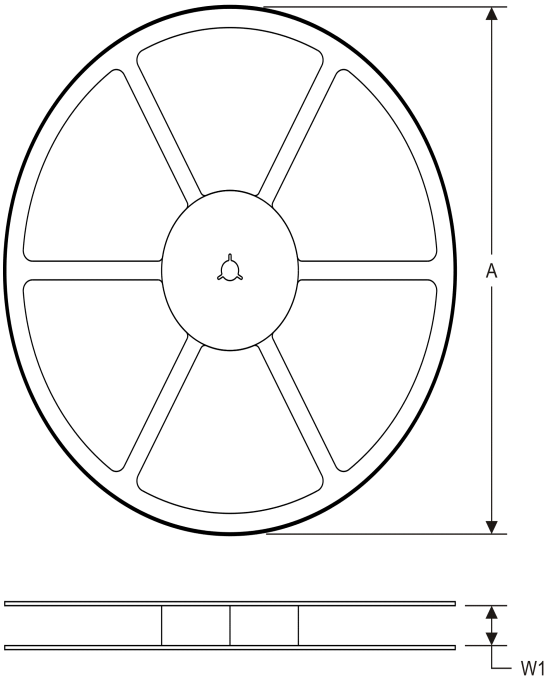
(4) Multiple Top-Side Markings will be inside parentheses. Only one Top-Side Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Top-Side Marking for that device.

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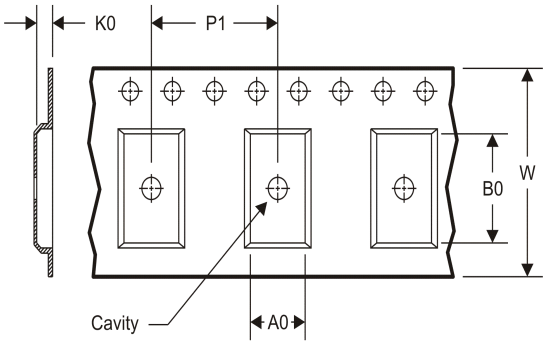
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## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**




**TAPE DIMENSIONS**



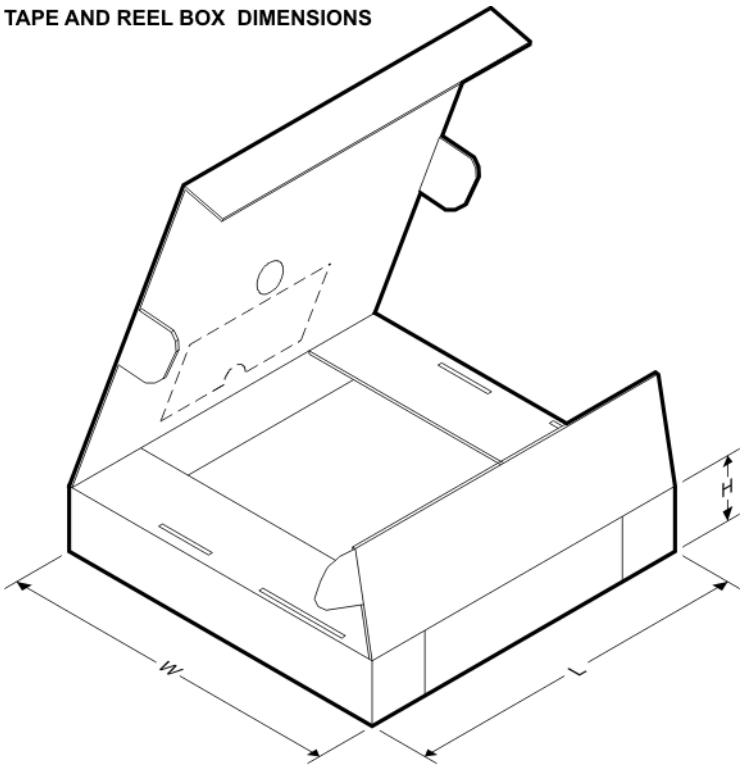

| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**TAPE AND REEL INFORMATION**

*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| CDC2509APWR | TSSOP | PW | 24 | 2000 | 330.0 | 16.4 | 6.95 | 8.3 | 1.6 | 8.0 | 16.0 | Q1 |

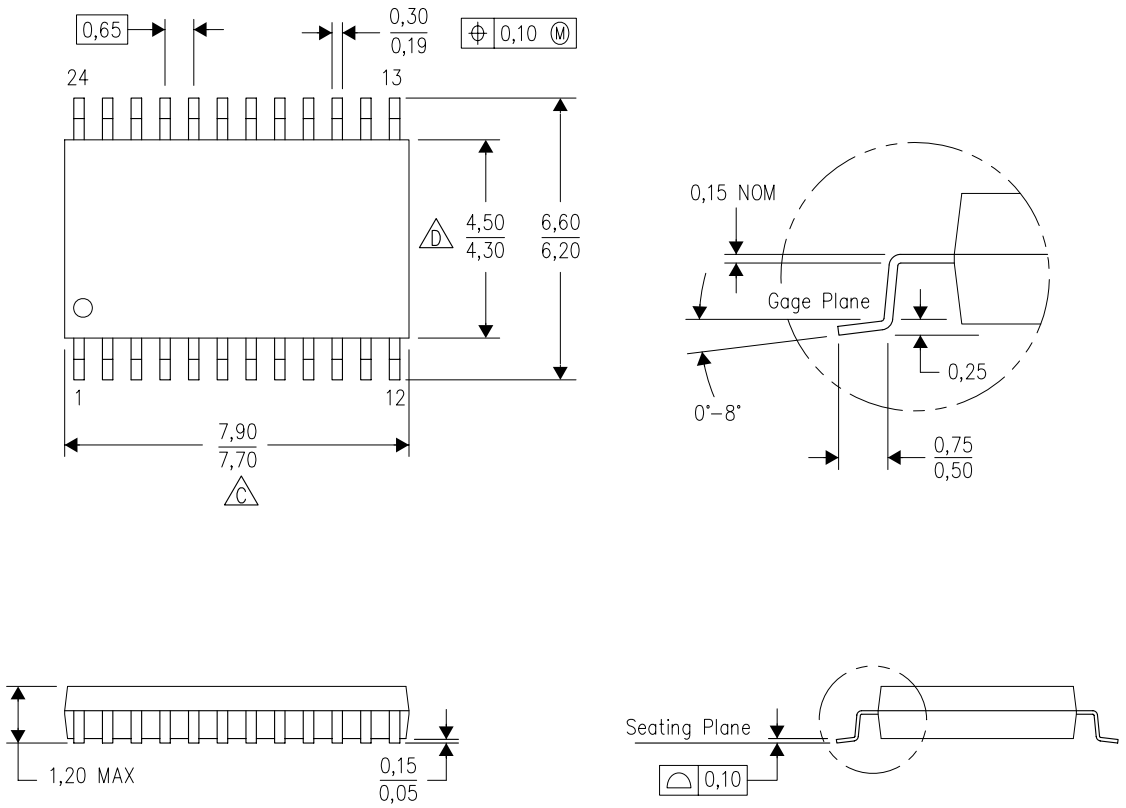
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| CDC2509APWR | TSSOP | PW | 24 | 2000 | 367.0 | 367.0 | 38.0 |

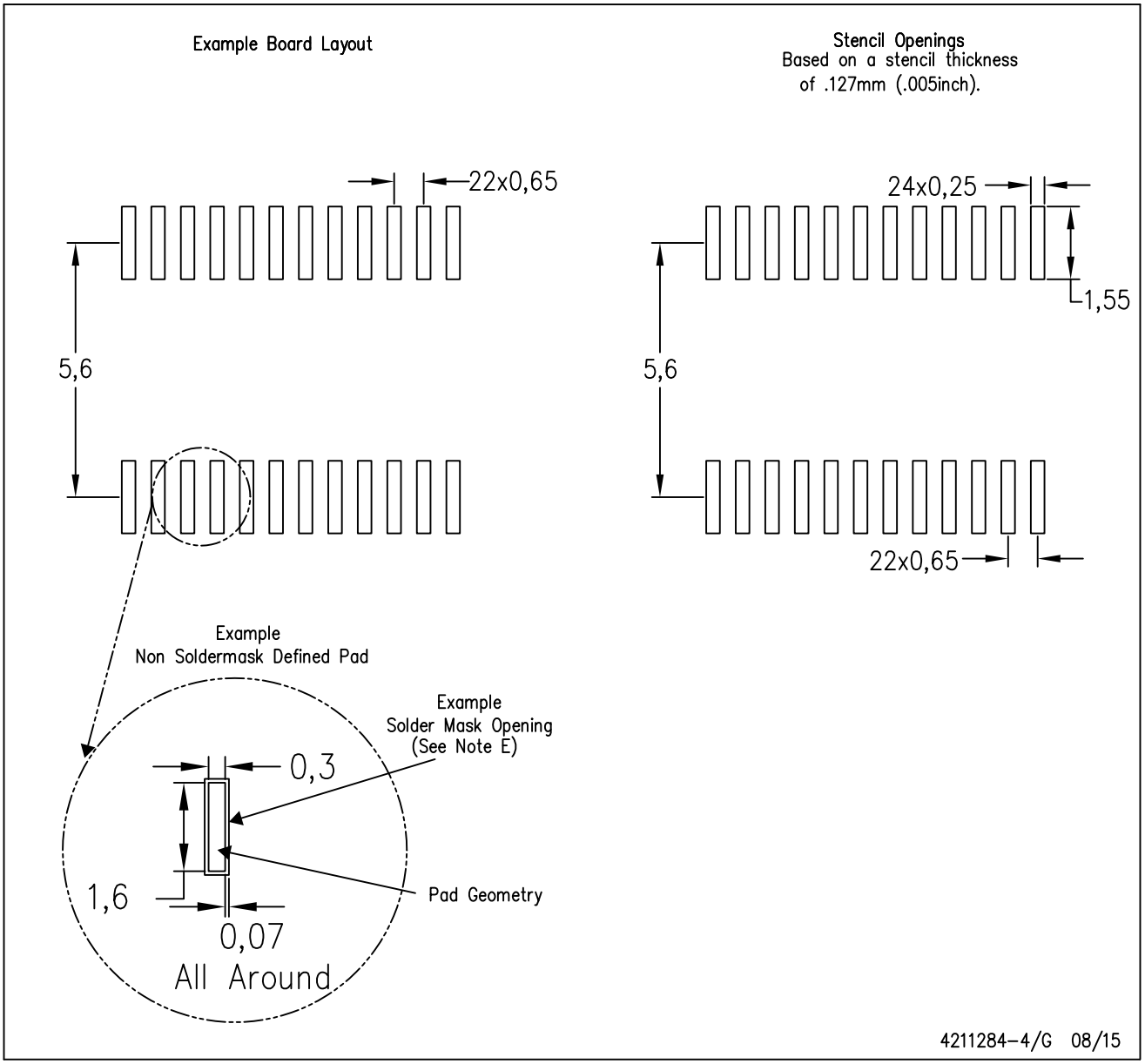
PW (R–PDSO–G24) PLASTIC SMALL OUTLINE




4040064–6/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G24) PLASTIC SMALL OUTLINE




NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

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Only those TI components which TI has specifically designated as military grade or “enhanced plastic” are designed and intended for use in military/aerospace applications or environments. Buyer acknowledges and agrees that any military or aerospace use of TI components which have ***not*** been so designated is solely at the Buyer's risk, and that Buyer is solely responsible for compliance with all legal and regulatory requirements in connection with such use.

TI has specifically designated certain components as meeting ISO/TS16949 requirements, mainly for automotive use. In any case of use of non-designated products, TI will not be responsible for any failure to meet ISO/TS16949.

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