

DATA SHEET



GPC10024D

Sound Controller with 24KB ROM

MAY 13, 2008

Version 1.2

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Table of Contents

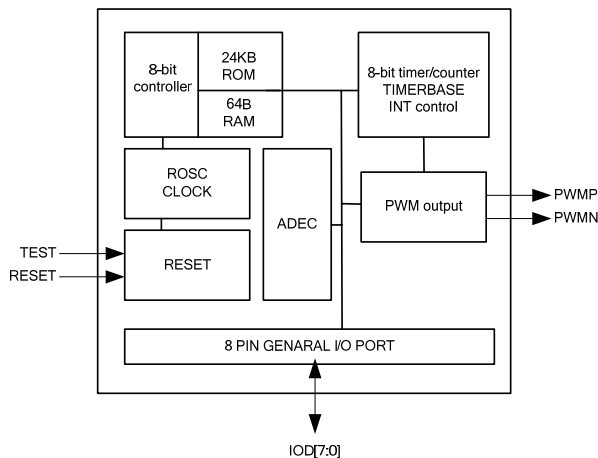
	<u>PAGE</u>
1. GENERAL DESCRIPTION	3
2. BLOCK DIAGRAM	3
3. FEATURES.....	3
4. APPLICATION FIELD	3
5. SIGNAL DESCRIPTIONS	4
5.1. PAD ASSIGNMENT	5
6. FUNCTIONAL DESCRIPTIONS.....	6
6.1. CPU	6
6.2. RAM AREA.....	6
6.3. ROM AREA	6
6.4. MAP OF MEMORY AND I/OS	6
6.5. I/O PORT	6
6.6. POWER SAVING MODE	6
6.7. LOW VOLTAGE RESET	7
6.8. TIMER/COUNTER.....	7
6.9. SPEECH AND MELODY	7
7. ELECTRICAL SPECIFICATIONS	8
7.1. ABSOLUTE MAXIMUM RATINGS	8
7.2. DC CHARACTERISTICS (VDD = 5.0V, T _A = 25°C)	8
7.3. DC CHARACTERISTICS (VDD = 3.0V, T _A = 25°C).....	8
8. APPLICATION CIRCUITS.....	10
8.1. 8 I/O	10
8.2. 4 I/O, 4LED	11
8.3. PCB LAYOUT GUIDE	12
9. PACKAGE/PAD LOCATIONS	13
9.1. ORDERING INFORMATION	13
10. DISCLAIMER	14
11. REVISION HISTORY	15

SOUND CONTROLLER WITH 24KB ROM

1. GENERAL DESCRIPTION

The GPC10024D, a speech/wavetable synthesizer, equips an 8-bit CMOS microprocessor, and 24K-byte Working ROM, 64-byte working SRAM. Other primary features include two 8-bit Timer/Counters and can cascade to one 16-bit timer/counter, 24 Software Selectable I/Os, a pair of PWM output. It operates at a wide voltage range of 2.4V - 5.5V. Plus, a Clock Stop mode is built in for power savings. The unique power saving mode saves the RAM contents, but freezes the oscillator to stop executing other functions. The maximum CPU frequency can run up to 8MHz and the instruction cycle is two clock cycles (min.) ~ six clock cycles (max.). The GPC10024D loads, not only the latest technology, but also the full commitment and technical support of Generalplus.

2. BLOCK DIAGRAM



3. FEATURES

- 8-bit microprocessor
- 24K bytes ROM
- 64-byte working SRAM
- Software-based audio processing
- Wide operating voltage: 2.4V - 5.5V @ 6.0MHz
3.6V - 5.5V @ 8.0MHz
- Built-in R-oscillator, code option to 6MHz or 8 MHz.
- Max. CPU clock: 6.0MHz @ 3.0V, 8MHz @ 5.0V
- Standby mode (Clock Stop mode) for power savings
Max. 2.0μA @ 5.0V
- 333ns instruction cycle time @ 6.0MHz CPU clock
- 8 general I/Os (include 4 high brightness LED driving I/O)
- Low Voltage Reset (LVR) function
- Two 8-bit timer/counters and can cascade to one 16-bit timer/counter
- Six INT sources
- Key wake -up function
- IR function
- External feedback input
- Watch dog function
- A pair of PWM output

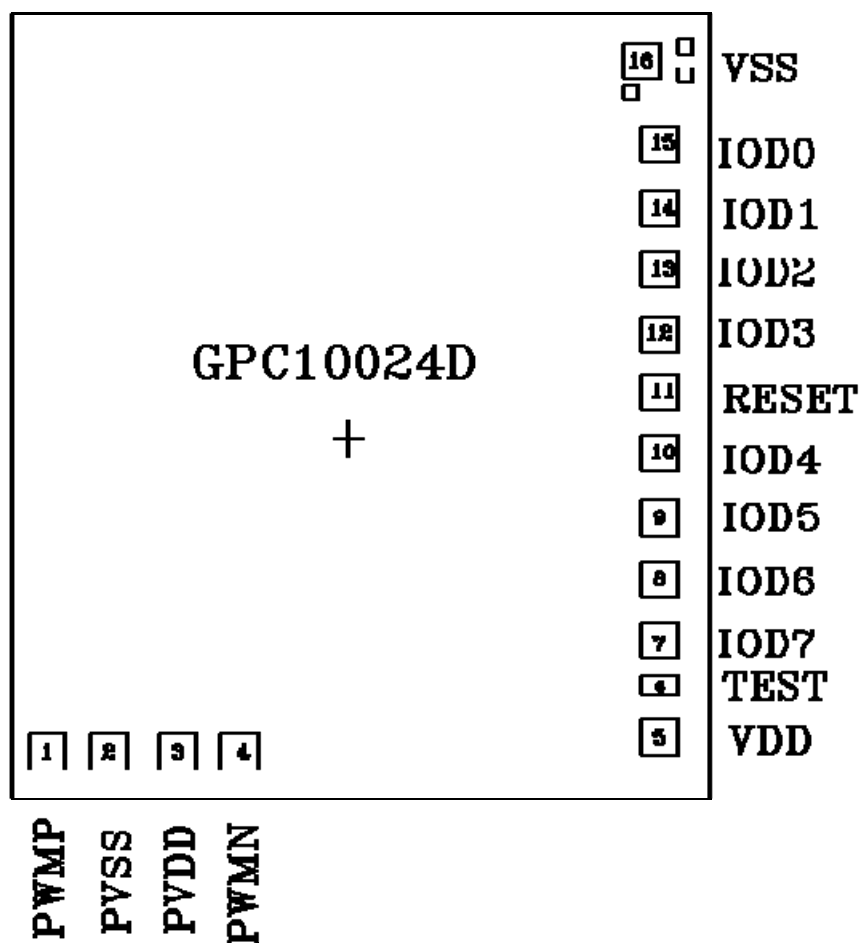
4. APPLICATION FIELD

- Intelligent education toys
Ex. Pattern to voice (animal, car, color, etc.)
Spelling (English or Chinese)
Math
- Advanced toy controller
- General speech synthesizer
- Industrial controller

5. SIGNAL DESCRIPTIONS

Mnemonic	PIN No	Type	Description
VDD	5	I	Digital Power Pad
VSS	16	I	Digital Ground
PVDD	3	I	PWM Power Pad
PVSS	2	I	PWM Ground
RESET	11	I	Reset pin, active low to reset whole system
TEST	6	I	Test pin, NC
PWMP	1	O	PWM output
PWMN	4	O	PWM output
IOD0	15	I/O	Bit-controlled programmable I/O pins
IOD1	14	I/O	In input mode, port D can be either pure or pull-low states
IOD2	13	I/O	In output mode, port D can be buffer
IOD3	12	I/O	Port D are the key wakeup I/O pins
IOD4	10	I/O	IOD[3:0] can drive high brightness LED
IOD5	9	I/O	IOD4: feedback input of clock generator
IOD6	8	I/O	IOD5: feedback output of clock generator
IOD7	7	I/O	IOD6 : external interrupt
			IOD7: IR transmitter

5.1. PAD Assignment



The IC substrate should be connected to VSS

Note1: To ensure that the IC functions properly, please bond all of VDD and VSS pins.

Note2: The 0.1μF capacitor between VDD and VSS should be placed to IC as close as possible.

6. FUNCTIONAL DESCRIPTIONS

6.1. CPU

The microprocessor in GPC10024D is a high performance 8-bit processor equipped Accumulator, Program Counter, X and Y Register, Stack pointer and Processor Status Register (the same as the 6502 instruction structure). The maximum CPU speed of 8.0MHz is capable of bringing you the cleaner speech, pleasant music as well as achieving the best performance.

6.2. RAM Area

The total RAM size is 64-bytes (including Stack) starting from address \$00C0 through \$00FF or mapping to \$01C0 through \$01FF.

6.3. ROM Area

The GPC10024D provides a 24K-byte ROM that can be defined as the program area, audio data area, or both.

6.4. Map of Memory and I/Os

0x0000	IO
0x0017	
	Reserved
0x00C0	SRAM
0x00FF	Reserved
0x01C0	SRAM (Mapping)
0x01FF	
0x0200	Test Program
0x0600	User's Program & Data Area
0x4FFF	Dummy Area
0x7000	User's Program & Data Area
0x7FFF	

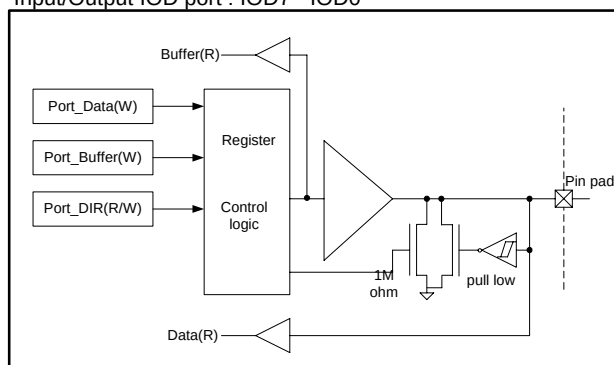
6.5. I/O Port

There are 8 IOs in the GPC10024D. IOD7-0 are bit-controlled IOs. They can be programmed as input (pure input or pull-low) or output buffer. As pull-low input IOD7-0 keep a less impedance to get good noise immunity. While pressing the key (IOD7-0 to VDD), a large impedance remained to save the DC power. IOD4, IOD5 can be programmed as a RC clock generator by adding external resistor and capacitor. IOD6 can be programmed as a external interrupt source. IOD7 can be programmed as a IR transmitter.

IOD3:0] can sink high current to drive high brightness LED.

IO port configuration:

Input/Output IOD port : IOD7 - IOD0



6.6. Power Saving Mode

The GPC10024D includes a power saving mode (Standby mode) for those applications that require very low standby current. To enter standby mode, the Wake-Up Register must be enabled and then stop the CPU clock by writing the STOP CLOCK Register to enter standby mode. In such mode, RAM and I/Os will remain in their previous states until being awoken. Port IOD7-0 is the wake-up source in the GPC10024D. After the GPC10024D is awoken, the internal CPU will go to the RESET State ($T_w \geq 64 \times T_1$) and continue to execute program. Wakeup Reset will not affect RAM nor I/Os.

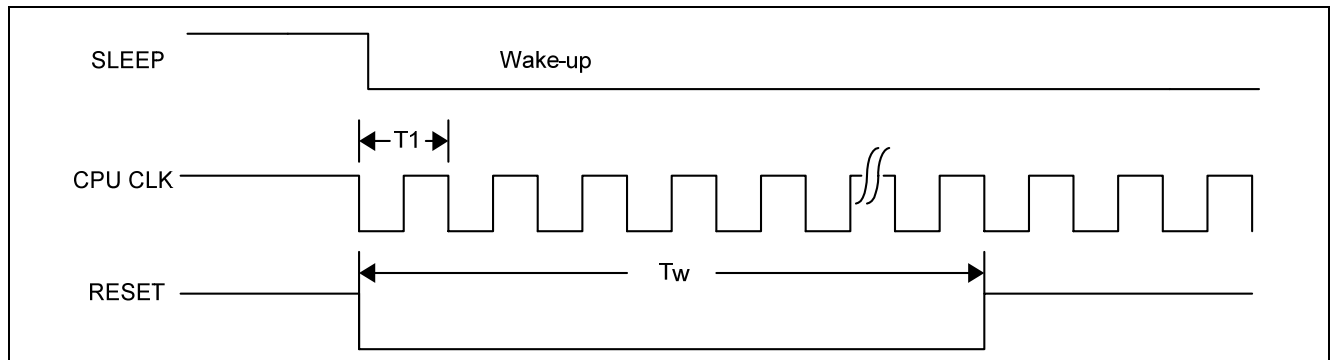


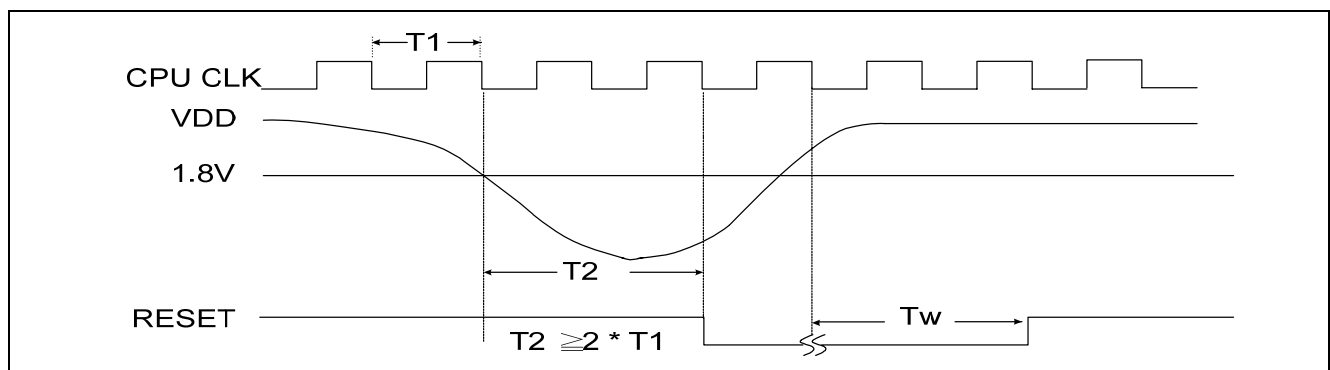
FIG. 1

$$T1 = 1 / (F_{CPU}), Tw \geq 64 \times T1$$

6.7. Low Voltage Reset

The GPC10024D has a Low Voltage Reset (LVR) function. In general, the CPU becomes unstable and malfunctions when the power voltage drops below certain operating voltage. With the

unique design of Low Voltage Reset in GPC10024D, it is able to reset all functions to the initial operational (stable) state if the VDD power-supply voltage drops around 1.8V.



(The LVR function is the same as Power ON Reset or External Reset.)

6.8. Timer/Counter

The GPC10024D has two 8-bit timer/counters, TMA and TMB respectively. TMA can be specified as a timer, but TMB can be used as a timer or a counter. In the timer mode, TMA and TMB are re-loaded up-counters. When timer rollovers from \$FF to \$00, the carry (overflow) signal will make the user's preset value to be loaded into timer automatically and up-count again. At the same

time, the carry signal will generate an INT signal if the corresponding bit is enabled in the INT ENABLE Register. Suppose TMB is specified as a counter, users can reset it by loading #0 into the counter. After the counter has been activated, the value in the counter can also be read at the same time. The read instruction will not affect the value of the counter nor reset it.

Clock source of Timer/Counter can be selected as follows:

Timer/Counter		Clock Source
TMA	8-BIT TIMER	CPU CLOCK (T) or T/8, T/64, TMB overflow
TMB	8-BIT TIMER	T, T/65536, EXTCLK, 0, 1

6.9. Speech and Melody

In speech synthesis, the GPC10024D can use NMI for accurate sampling frequency. The user can store the speech data in ROM and play it back with realistic sound quality. Several algorithms

are recommended for high fidelity and compression of sound: PCM, LOG PCM, ADPCM and SACMA3400.

7. ELECTRICAL SPECIFICATIONS

7.1. Absolute Maximum Ratings

Characteristics	Symbol	Ratings
DC Supply Voltage	V_+	< 7.0V
Input Voltage Range	V_{IN}	-0.5V to $V_+ + 0.5V$
Operating Temperature	T_A	0°C to +60°C
Storage Temperature	T_{STO}	-50°C to +150°C

Note: Stresses beyond those given in the Absolute Maximum Rating table may cause operational errors or damage to the device. For normal operational conditions see AC/DC Electrical Characteristics.

7.2. DC Characteristics (VDD = 5.0V, $T_A = 25^\circ\text{C}$)

Characteristics	Symbol	Limit			Unit	Test Condition
		Min.	Typ.	Max.		
Operating Voltage	VDD	3.6	-	5.5	V	-
Operating Current	I_{OP}	-	5.0	-	mA	$F_{CPU} = 6.0\text{MHz @ } 5.0V$
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 5.0V
Input High Level	V_{IH}	3.0	-	-	V	VDD = 5.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 5.0V
Output Source Current (IOD[7:0])	I_{OH}	-	-10	-	mA	VDD = 5.0V, $V_{OH} = 4V$
Output Sink Current (IOD[7:4])	I_{OL}	-	21	-	mA	VDD = 5.0V, $V_{OL} = 1V$
Output Sink Current (IOD[3:0])	I_{OL}	-	44	-	mA	VDD = 5.0V, $V_{OL} = 1V$
PWM Output Current	I_{OH}	-	-208	-	mA	VDD = 5.0V, $V_{OH} = 4.0V$
	I_{OL}	-	263	-	mA	VDD = 5.0V, $V_{OL} = 1.0V$
Input Resistor (IOD)	R_{IN}	-	85	-	$K\Omega$	VDD = 5.0V, $V_{IN} = 0V$
Input Resistor (IOD)	R_{IN}	-	745	-	$K\Omega$	VDD = 5.0V, $V_{IN} = VDD$
Built in R-oscillator Frequency	F_{ROSC}^*	-	6 or 8**	-	MHz	VDD = 3.6V - 5.5V

Note*: R_{OSC} frequency deviation: $\pm 7\%$ @ 6.0MHz, VDD= 2.4V - 5.5V, room temperature.

Note:** Code option.

7.3. DC Characteristics (VDD = 3.0V, $T_A = 25^\circ\text{C}$)

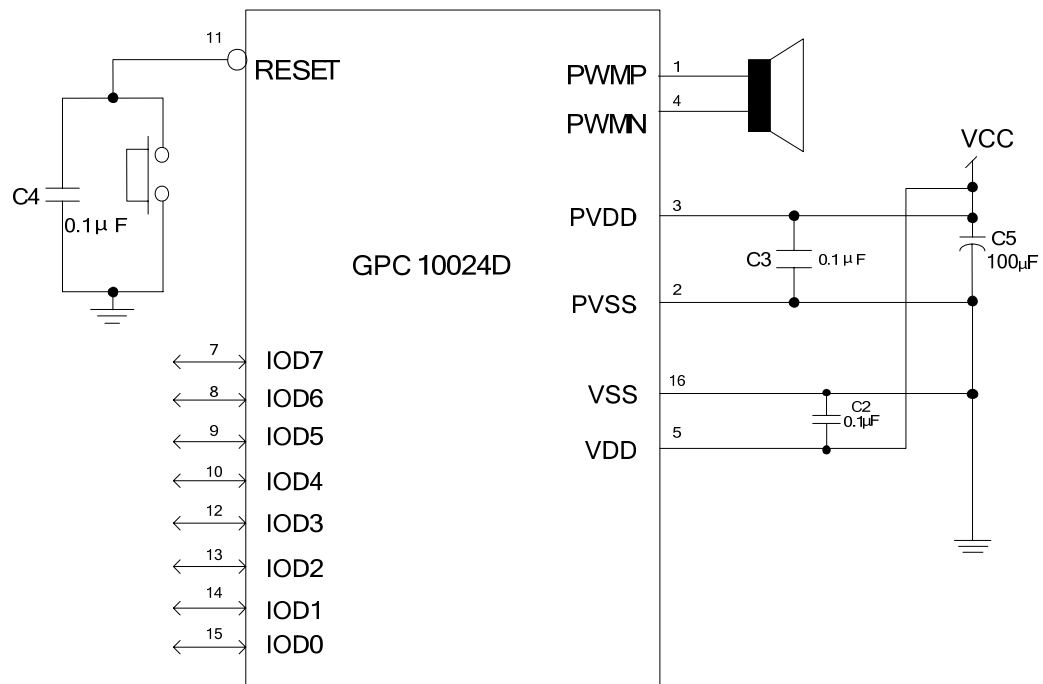
Characteristics	Symbol	Limit			Unit	Test condition
		Min	Typ	Max		
Operating Voltage	VDD	2.4	-	3.6	V	-
Operating Current	I_{OP}	-	1.7	-	mA	$F_{CPU} = 6.0\text{MHz @ } 3.0V$
Standby Current	I_{STBY}	-	-	2.0	μA	VDD = 3.0V
Input High Level	V_{IH}	2.0	-	-	V	VDD = 3.0V
Input Low Level	V_{IL}	-	-	0.8	V	VDD = 3.0V
Output Source Current (IOD[7:0])	I_{OH}	-	-4.6	-	mA	VDD = 3.0V, $V_{OH} = 2.4V$
Output Sink Current (IOD[7:4])	I_{OL}	-	10	-	mA	VDD = 3.0V, $V_{OL} = 0.6V$
Output Sink Current (IOD[3:0])	I_{OL}	-	23	-	mA	VDD = 3.0V, $V_{OL} = 0.6V$
PWM Output Current	I_{OH}	-	-110	-	mA	VDD = 3.0V, $V_{OH} = 2.4V$

Characteristics	Symbol	Limit			Unit	Test condition
		Min	Typ	Max		
	I_{OL}	-	146	-	mA	VDD = 3.0V, V_{OL} = 0.6V
Input Resistor (IOD)	R_{IN}	-	170	-	K Ω	VDD = 3.0V, V_{IN} = 0V
Input Resistor (IOD)	R_{IN}	-	1610	-	K Ω	VDD = 3.0V, V_{IN} = VDD
Built in R-oscillator Frequency	F_{ROSC}^*	-	6	-	MHz	VDD = 2.4V - 5.5V

Note*: R_{OSC} frequency deviation: $\pm 7\%$ @ 6.0MHz, VDD= 2.4V - 5.5V, room temperature.

8. APPLICATION CIRCUITS

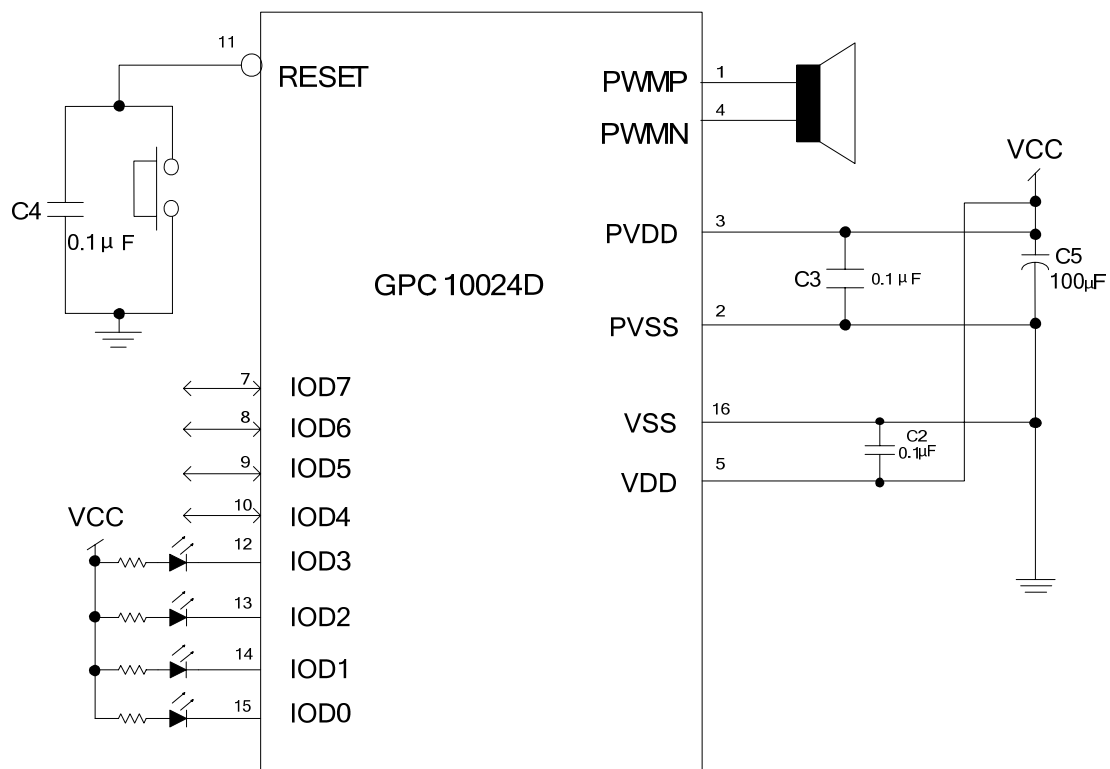
8.1. 8 I/O



PCB Layout Guidelines :

- 1.VDD,PVDD must be connected to power input port directly, not to be the branch of each other.
- 2.VSS,PVSS must be connected to ground input port directly, not to be the branch of each other.
- 3.C2 should be as close as possible to VDD/VSS pin.
- 4.C3 should be as close as possible to PVDD/PVSS pin.

8.2. 4 I/O, 4LED



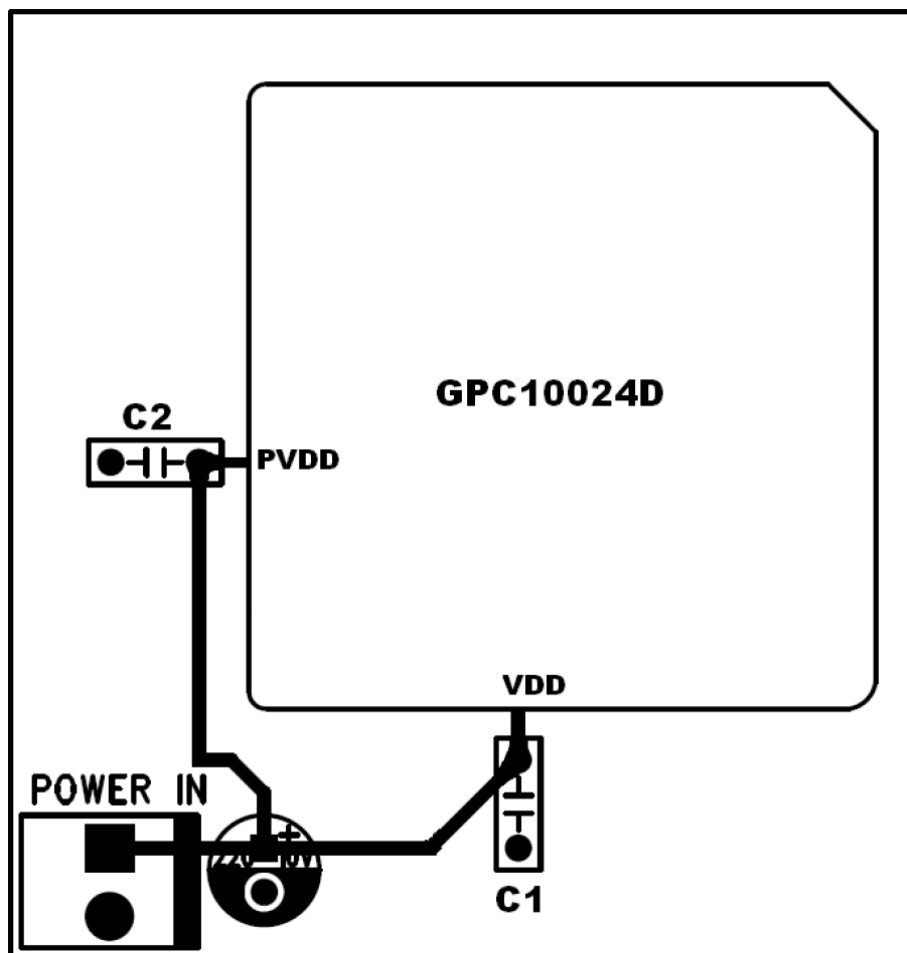
PCB Layout Guidelines :

- 1.VDD,PVDD must be connected to power input port directly, not to be the branch of each other.
- 2.VSS,PVSS must be connected to ground input port directly, not to be the branch of each other.
- 3.C2 should be as close as possible to VDD/VSS pin.
- 4.C3 should be as close as possible to PVDD/PVSS pin.

8.3. PCB Layout Guide

To avoid the unexpected noises to end up with abnormal CPU operations, the following cares must be exercised while doing the PCB layout:

1. Bond all VDD and VSS pins out.
2. The 0.1 μ F capacitor (C1-C2) placed between VDD and VSS must be as closed as possible to IC itself. The PCB layout examples are given as follows:



9. PACKAGE/PAD LOCATIONS

9.1. Ordering Information

Product Number	Package Type
GPC10024D - NnnV - C	Chip form

Note1: Code number is assigned for customer.

Note2: Code number (N = A - Z or 0 - 9, nn = 00 - 99); version (V = A - Z).

10. DISCLAIMER

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11. REVISION HISTORY

Date	Revision #	Description	Page
MAY 13, 2008	1.2	Add section 8.3 PCB Layout Guide.	12
SEP. 10, 2007	1.1	1. Modify "FEATURES" in section 3.	3
		2. Add "Built in R-oscillator Frequency" to section 7.2 and 7.3.	7
MAR. 19, 2007	1.0	Modify the "APPLICATION CIRCUITS" in section 8.	8
JAN. 08, 2007	0.1	Original	12