# Highly Integrated Wireless Receiver Qi (WPC V1.1) Compliant Power Supply

**Check for Samples: bq51010B**

## FEATURES

- **Integrated Wireless Power Supply Receiver Solution with a 7V Regulated Supply**
  - **93% Overall Peak AC-DC Efficiency**
  - **Full Synchronous Rectifier**
  - **WPC v1.1 Compliant Communication Control**
  - **Output Voltage Conditioning**
  - **Only IC Required Between RX coil and 7V Output**
- **WPC v1.1 Compliant (FOD Enabled) Highly Accurate Current Sense**
- ***Dynamic Rectifier Control* for Improved Load Transient Response**
- ***Dynamic Efficiency Scaling* for Optimized Performance Over wide Range of Output Power**
- ***Adaptive Communication Limit* for Robust Communication**
- **Supports 20-V Maximum Input**
- **Low-power Dissipative Rectifier Overvoltage Clamp ($V_{OVP}$ = 15V)**
- **Thermal Shutdown**
- **Multifunction NTC and Control Pin for Temperature Monitoring, Charge Complete and Fault Host Control**
- **1.9 x 3mm DSBGA**

## APPLICATIONS

- **WPC Compliant Receivers**
- **Cell Phones, Smart Phones**
- **Headsets**
- **Digital Cameras**
- **Portable Media Players**
- **Hand-held Devices**

## DESCRIPTION

The bq51010B is a family of advanced, flexible, secondary-side devices for wireless power transfer in portable applications. The bq51010B devices provide the AC/DC power conversion and regulation while integrating the digital control required to comply with the Qi v1.1 communication protocol. Together with the bq50xxx primary-side controller, the bq51010B enables a complete contact-less power transfer system for a wireless power supply solution. Global feedback is established from the secondary to the primary in order to control the power transfer process utilizing the Qi v1.1 protocol.

The bq51010B devices integrate a low resistance synchronous rectifier, low-dropout regulator, digital control, and accurate voltage and current loops to ensure high efficiency and low power dissipation.

The bq51010B also includes a digital controller that can calculate the amount of power received by the mobile device within the limits set by the WPC v1.1 standard. The controller will then communicate this information to the transmitter in order to allow the transmitter to determine if a foreign object is present within the magnetic interface and introduces a higher level of safety within magnetic field. This Foreign Object Detection (FOD) method is part of the new requirements under the WPC v1.1 specification.

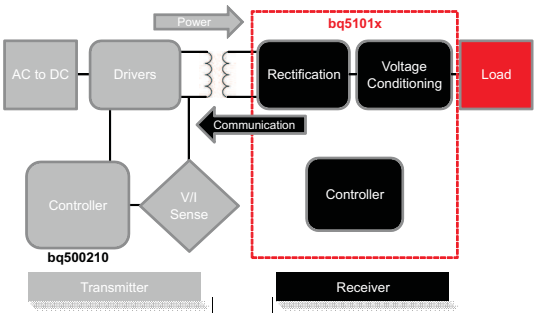


**Figure 1. Wireless Power Consortium (WPC or Qi) Inductive Power System**

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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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## ORDERING INFORMATION

| Part NO | Marking | Function | Package | Ordering Number (Tape and Reel) | Quantity |
|---|---|---|---|---|---|
| bq51010B | bq51010B | 7V Regulated Power Supply | DSBGA-YFP | bq51010BYFPR | 3000 |
| | | | | bq51010BYFPT | 250 |

## AVAILABLE OPTIONS

| Device | Function | WPC Version | $V_{RECT-OVP}$ | $V_{OUT-(REG)}$ | Over Current Shutdown | AD-OVP | Termination | Communication Current Limit(1)(2) |
|---|---|---|---|---|---|---|---|---|
| bq51010B | 7V Power Supply | v1.1 | 15V | 7V | Disabled | Disabled | Disabled | Adaptive + 1s Hold-Off |

(1) Enabled if EN2 is low and disabled if EN2 is high
(2) Communication current limit is disabled for 1 second at startup

## ABSOLUTE MAXIMUM RATINGS(1)(2)

over operating free-air temperature range (unless otherwise noted)

| | | VALUES | | UNITS |
|---|---|---|---|---|
| | | MIN | MAX | |
| Input Voltage | AC1, AC2 | –0.8 | 20 | V |
| | RECT, COM1, COM2, OUT, $\overline{WPG}$, CLAMP1, CLAMP2 | –0.3 | 20 | V |
| | AD, $\overline{AD\text{-}EN}$ | –0.3 | 30 | V |
| | BOOT1, BOOT2 | –0.3 | 26 | V |
| | EN1, EN2, TERM, FOD, TS-CTRL, ILIM | –0.3 | 7 | V |
| Input Current | AC1, AC2 | | 1.5 | A(RMS) |
| Output Current | OUT | | 750 | mA |
| Output Sink Current | $\overline{WPG}$ | | 15 | mA |
| | COM1, COM2 | | 1 | A |
| Junction temperature, $T_J$ | | –40 | 150 | °C |
| Storage temperature, $T_{STG}$ | | –65 | 150 | °C |
| ESD Rating (HBM) (100pF, 1.5KΩ) | All | 2 | | kV |
| | CDM | 500 | | V |

(1) All voltages are with respect to the VSS terminal, unless otherwise noted.
(2) Stresses beyond those listed under absolute maximum ratings may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under recommended operating conditions is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.


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## THERMAL INFORMATION

| THERMAL METRIC[1] | | YFP 28 PINS | UNITS |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance | 58.9 | °C/W |
| $\theta_{JCtop}$ | Junction-to-case (top) thermal resistance | 0.2 | |
| $\theta_{JB}$ | Junction-to-board thermal resistance | 9.1 | |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 1.4 | |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 8.9 | |
| $\theta_{JCbot}$ | Junction-to-case (bottom) thermal resistance | n/a | |

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, SPRA953.

## RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range (unless otherwise noted)

| | | | MIN | MAX | UNITS |
|---|---|---|---|---|---|
| $V_{IN}$ | Input voltage range | RECT | 4 | 10 | V |
| $I_{IN}$ | Input current | RECT | | 1 | A |
| $I_{OUT}$ | Output current | OUT | | 750 | mA |
| $I_{AD\text{-}EN}$ | Sink current | $\overline{\text{AD-EN}}$ | | 1 | mA |
| $I_{COMM}$ | COMM sink current | COMM | | 400 | mA |
| $T_J$ | Junction Temperature | | 0 | 125 | °C |

## TYPICAL APPLICATION SCHEMATICS

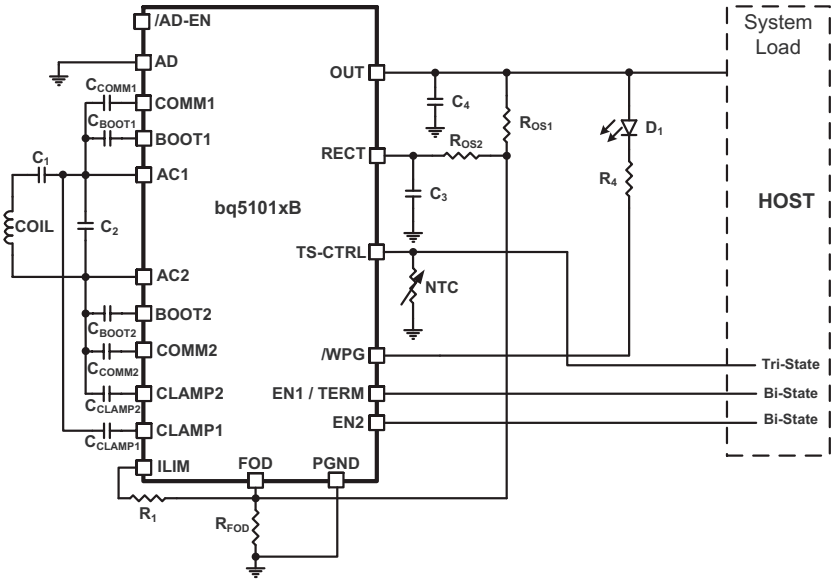


**Figure 2. bq51010B Used as a Wireless Power Receiver and Power Supply for System Loads Only one of $R_{OS1}$ or $R_{OS2}$ needed**

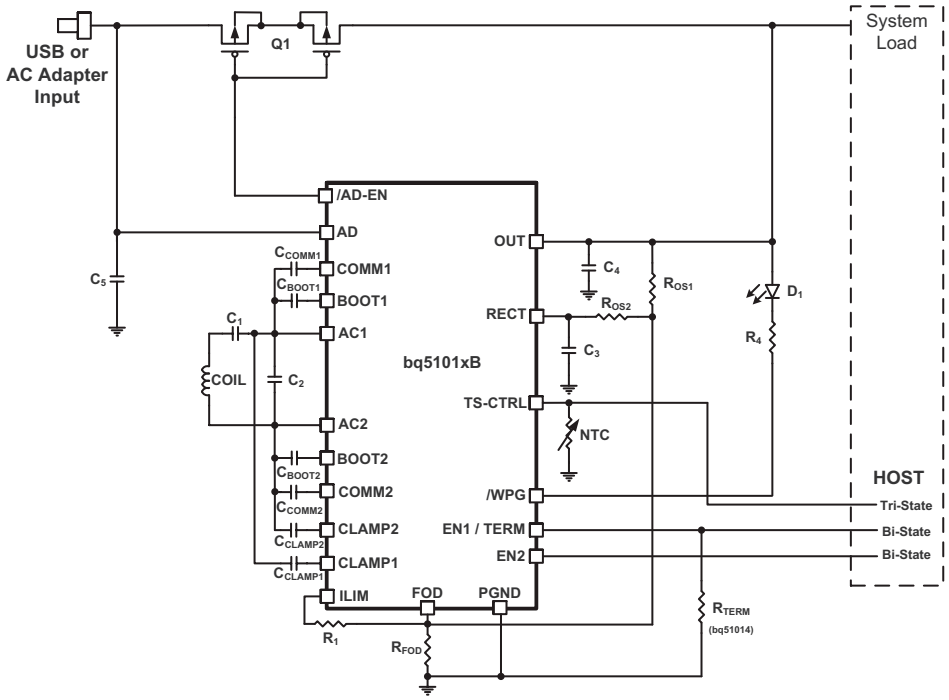


**Figure 3. bq51010B Used as a Wireless Power Receiver and Power Supply for System Loads With Adapter Power-Path Multiplexing – Only one of $R_{OS1}$ or $R_{OS2}$ Needed**

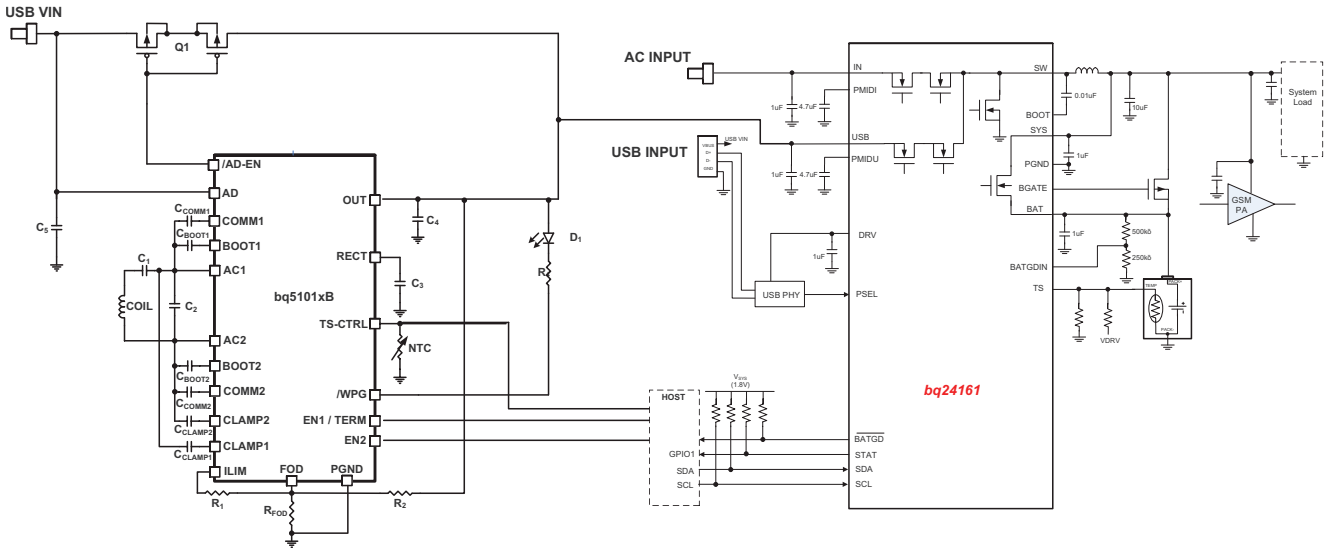


**Figure 4. bq51010B Used as a Wireless Power Supply with Adapter Multiplexing on a Two Input Charger**


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## ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, 0°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| UVLO | Undervoltage lock-out | $V_{RECT}$: 0V → 3V | 2.6 | 2.7 | 2.8 | V |
| $V_{HYS}$ | Hysteresis on UVLO | $V_{RECT}$: 3V → 2V | | 250 | | mV |
| | Hysteresis on OVP | $V_{RECT}$: 16V → 5V | | 150 | | mV |
| $V_{RECT}$ | Input overvoltage threshold | $V_{RECT}$: 5V → 16V | 14.5 | 15 | 15.5 | V |
| $V_{RECT-REG}$ | Dynamic $V_{RECT}$ Threshold 1 | $I_{LOAD}$ < 0.1 x $I_{IMAX}$ ($I_{LOAD}$ rising) | | 9.08 | | V |
| | Dynamic $V_{RECT}$ Threshold 2 | 0.1 x $I_{IMAX}$ < $I_{LOAD}$ < 0.2 x $I_{IMAX}$ ($I_{LOAD}$ rising) | | 8.28 | | |
| | Dynamic $V_{RECT}$ Threshold 3 | 0.2 x $I_{IMAX}$ < $I_{LOAD}$ < 0.4 x $I_{IMAX}$ ($I_{LOAD}$ rising) | | 7.53 | | |
| | Dynamic $V_{RECT}$ Threshold 4 | $I_{LOAD}$ > 0.4 x $I_{IMAX}$ ($I_{LOAD}$ rising) | | 7.11 | | |
| | $V_{RECT}$ TRACKING | In current limit voltage above $V_{OUT}$ | | $V_O$+0.250 | | |
| $I_{LOAD}$ | $I_{LOAD}$ Hysteresis for dynamic $V_{RECT}$ thresholds as a % of $I_{ILIM}$ | $I_{LOAD}$ falling | | 4% | | |
| $V_{RECT-DPM}$ | Rectifier undervoltage protection, restricts $I_{OUT}$ at $V_{RECT-DPM}$ | | 3 | 3.1 | 3.2 | V |
| $V_{RECT-REV}$ | Rectifier reverse voltage protection at the output | $V_{RECT-REV}$ = $V_{OUT}$ - $V_{RECT}$, $V_{OUT}$ = 10V | | 8 | 9 | V |
| **QUIESCENT CURRENT** | | | | | | |
| $I_{RECT}$ | Active chip quiescent current consumption from RECT | $I_{LOAD}$ = 0 mA, 0°C ≤ $T_J$ ≤ 85°C | | 8 | 10 | mA |
| | | $I_{LOAD}$ = 300 mA, 0°C ≤ $T_J$ ≤ 85°C | | 2 | 3 | mA |
| $I_{OUT}$ | Quiescent current at the output when wireless power is disabled (Standby) | $V_{OUT}$ = 7 V, 0°C ≤ $T_J$ ≤ 85°C | | 28 | 40 | µA |
| **$I_{LIM}$ SHORT CIRCUIT** | | | | | | |
| $R_{ILIM}$ | Highest value of $I_{LIM}$ resistor considered a fault (short). Monitored for $I_{OUT}$ > 100 mA | $R_{ILIM}$: 200Ω → 50Ω. $I_{OUT}$ latches off, cycle power to reset | | | 120 | Ω |
| $t_{DGL}$ | Deglitch time transition from $I_{LIM}$ short to $I_{OUT}$ disable | | | 1 | | ms |
| $I_{LIM_SC}$ | $I_{LIM-SHORT,OK}$ enables the $I_{LIM}$ short comparator when $I_{OUT}$ is greater than this value | $I_{LOAD}$: 0 → 200mA | 110 | 145 | 165 | mA |
| | Hysteresis for $I_{LIM-SHORT,OK}$ comparator | $I_{LOAD}$: 0 → 200 mA | | 30 | | mA |
| $I_{OUT}$ | Maximum output current limit, $C_L$ | Maximum $I_{LOAD}$ that will be delivered for 1 ms when $I_{LIM}$ is shorted | | | 2.45 | A |
| **OUTPUT** | | | | | | |
| $V_{OUT-REG}$ | Regulated output voltage | $I_{LOAD}$ = 750 mA | 6.90 | 6.96 | 7.02 | V |
| | | $I_{LOAD}$ = 10 mA | 6.90 | 6.95 | 7.05 | |
| $K_{ILIM}$ | Current programming factor for hardware protection | $R_{LIM}$ = $K_{ILIM}$ / $I_{ILIM}$, where $I_{ILIM}$ is the hardware current limit. $I_{OUT}$ = 750mA | 303 | 314 | 322 | AΩ |
| $K_{IMAX}$ | Current programming factor for the nominal operating current | $I_{IMAX}$ = $K_{IMAX}$ / $R_{LIM}$ where $I_{MAX}$ is the maximum normal operating current. $I_{OUT}$ = 750mA | | 262 | | AΩ |
| $I_{OUT}$ | Current limit programming range | | | | 1.5 | A |
| $I_{COMM}$ | Current limit during WPC communication | $I_{OUT}$ > 300 mA | | $I_{OUT}$ + 50 | | mA |
| | | $I_{OUT}$ < 300 mA | 343 | 378 | 425 | mA |
| $t_{HOLD}$ | Hold off time for the communication current limit during startup | | | 1 | | s |

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## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, 0°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **TS / CTRL** | | | | | | |
| $V_{TS}$ | Internal TS Bias Voltage | $I_{TS\text{-}Bias}$ < 100 µA (periodically driven see $t_{TS\text{-}CTRL}$) | 2 | 2.2 | 2.4 | V |
| $V_{COLD}$ | Rising threshold | $V_{TS}$: 50% → 60% | 56.5 | 58.7 | 60.8 | $\%V_{TS\text{-}Bias}$ |
| | Falling hysteresis | $V_{TS}$: 60% → 50% | | 2 | | |
| $V_{HOT}$ | Falling threshold | $V_{TS}$: 20% → 15% | 18.5 | 19.6 | 20.7 | |
| | Rising hysteresis | $V_{TS}$: 15% → 20% | | 3 | | |
| $V_{CTRL}$ | CTRL pin threshold for a high | $V_{TS/CTRL}$: 50 → 150mV | 80 | 100 | 130 | mV |
| | CTRL pin threshold for a low | $V_{TS/CTRL}$: 150 → 50mV | 50 | 80 | 100 | mV |
| $t_{TS\text{-}CTRL}$ | Time VTS-Bias is active when TS measurements occur | Synchronous to the communication period | | 24 | | ms |
| $t_{TS}$ | Deglitch time for all TS comparators | | | 10 | | ms |
| $R_{TS}$ | Pull-up resistor for the NTC network. Pulled up to the voltage bias | | 18 | 20 | 22 | kΩ |
| **THERMAL PROTECTION** | | | | | | |
| $T_J$ | Thermal shutdown temperature | | | 155 | | °C |
| | Thermal shutdown hysteresis | | | 20 | | °C |
| **OUTPUT LOGIC LEVELS ON $\overline{WPG}$** | | | | | | |
| $V_{OL}$ | Open drain $\overline{WPG}$ pin | $I_{SINK}$ = 5 mA | | | 500 | mV |
| $I_{OFF}$ | $\overline{WPG}$ leakage current when disabled | $V_{\overline{WPG}}$ = 20 V | | | 1 | µA |
| **COMM PIN** | | | | | | |
| $R_{DS(ON)}$ | COM1 and COM2 | $V_{RECT}$ = 2.6 V | | 1.5 | | Ω |
| $f_{COMM}$ | Signaling frequency on COMM pin | | | 2.00 | | Kb/s |
| $I_{OFF}$ | Comm pin leakage current | $V_{COM1}$ = 20 V, $V_{COM2}$ = 20 V | | | 1 | µA |
| **CLAMP PIN** | | | | | | |
| $R_{DS(ON)}$ | Clamp1 and Clamp2 | | | 0.8 | | Ω |
| **ADAPTER ENABLE** | | | | | | |
| $V_{\overline{AD\text{-}EN}}$ | $V_{AD}$ Rising threshold voltage. EN-UVLO | $V_{AD}$ 0 → 5 V | 3.5 | 3.6 | 3.8 | V |
| | $V_{\overline{AD\text{-}EN}}$ hysteresis, EN-HYS | $V_{AD}$ 5 → 0 V | | 400 | | mV |
| $I_{AD}$ | Input leakage current | $V_{RECT}$ = 0V, $V_{AD}$ = 5V | | | 60 | µA |
| $R_{AD}$ | Pull-up resistance from $\overline{AD\text{-}EN}$ to OUT when adapter mode is disabled and $V_{OUT} > V_{AD}$, EN-OUT | $V_{AD}$ = 0, $V_{OUT}$ = 5 | | 200 | 350 | Ω |
| $V_{AD}$ | Voltage difference between $V_{AD}$ and $V_{\overline{AD\text{-}EN}}$ when adapter mode is enabled, EN-ON | $V_{AD}$ = 5 V, 0°C ≤ $T_J$ ≤ 85°C | 3 | 4.5 | 5 | V |


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## ELECTRICAL CHARACTERISTICS (continued)

over operating free-air temperature range, 0°C to 125°C (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **SYNCHRONOUS RECTIFIER** | | | | | | |
| $I_{OUT}$ | $I_{OUT}$ at which the synchronous rectifier enters half synchronous mode, SYNC_EN | $I_{LOAD}$ 200 → 0 mA | 80 | 100 | 130 | mA |
| | Hysteresis for $I_{OUT,RECT-EN}$ (full-synchronous mode enabled) | $I_{LOAD}$ 0 → 200 mA | | 25 | | mA |
| $V_{HS-DIODE}$ | High-side diode drop when the rectifier is in half synchronous mode | $I_{AC-VRECT}$ = 250 mA and $T_J$ = 25°C | | 0.7 | | V |
| **EN1 AND EN2** | | | | | | |
| $V_{IL}$ | Input low threshold for EN1 and EN2 | | | | 0.4 | V |
| $V_{IH}$ | Input high threshold for EN1 and EN2 | | 1.3 | | | V |
| $R_{PD}$ | EN1 and EN2 pull down resistance | | | 200 | | kΩ |
| **ADC (WPC Related Measurements and Coefficients)** | | | | | | |
| $I_{OUT}$ SENSE | Accuracy of the current sense over the load range | $I_{OUT}$ = 0 - 750mA | –1.5 | 0 | 0.9 | % |

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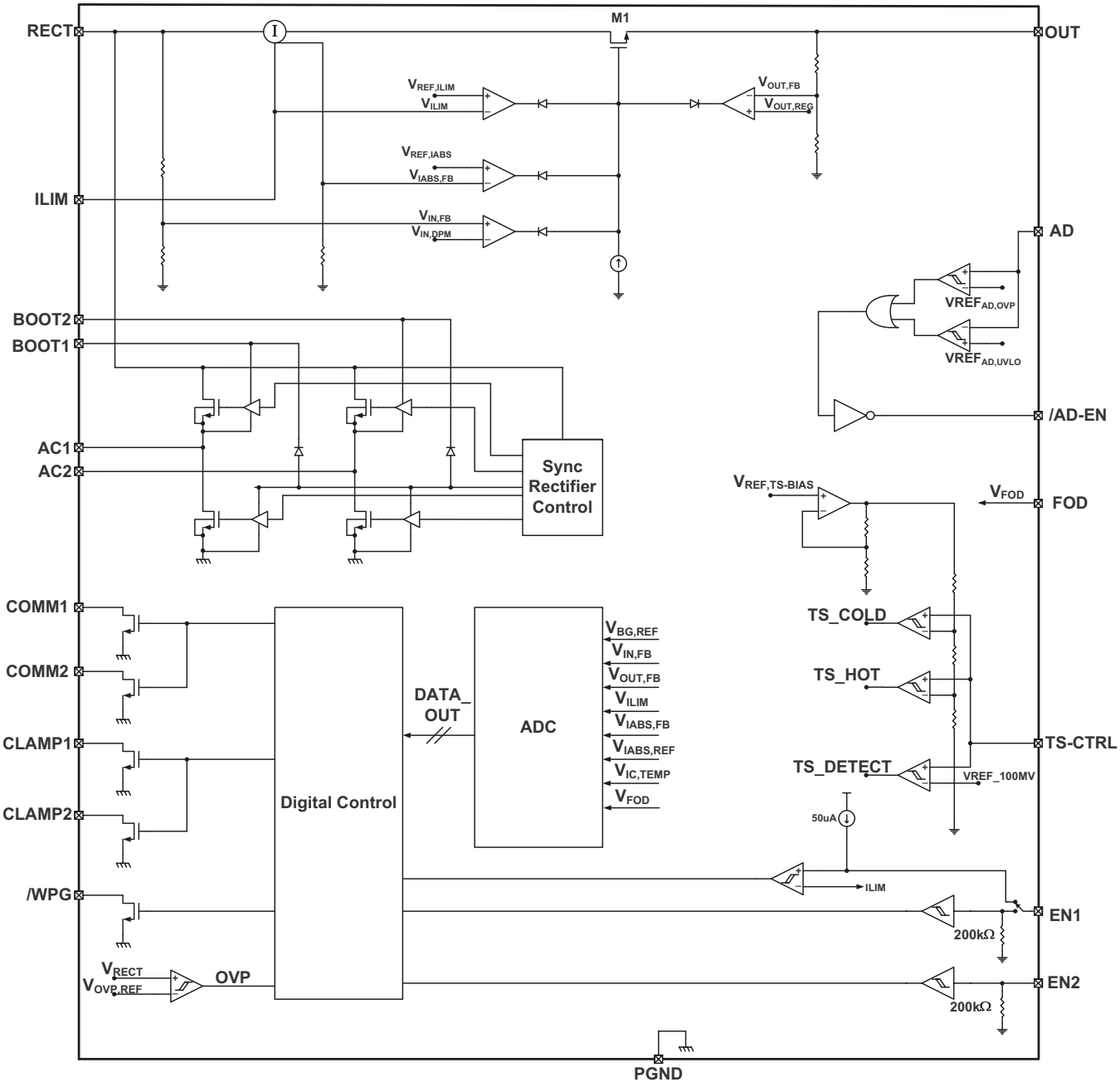
# DEVICE INFORMATION

## SIMPLIFIED BLOCK DIAGRAM





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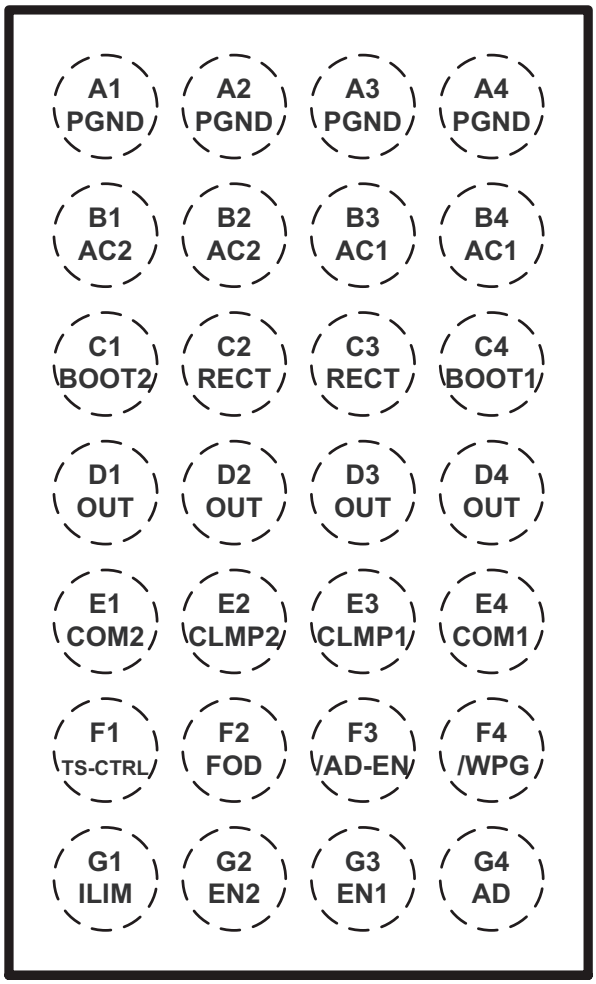
**YFP Package**
**(TOP VIEW)**




## PIN FUNCTIONS

| NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| AC1 | B3, B4 | I | AC input from receiver coil antenna. |
| AC2 | B1, B2 | I | |
| BOOT1 | C4 | O | Bootstrap capacitors for driving the high-side FETs of the synchronous rectifier. Connect a 10 nF ceramic capacitor from BOOT1 to AC1 and from BOOT2 to AC2. |
| BOOT2 | C1 | O | |
| RECT | C2, C3 | O | Filter capacitor for the internal synchronous rectifier. Connect a ceramic capacitor to PGND. Depending on the power levels, the value may be 4.7 µF to 22 µF. |
| OUT | D1, D2, D3, D4 | O | Output pin, delivers power to the load. |
| COM1 | E4 | O | Open-drain output used to communicate with primary by varying reflected impedance. Connect through a capacitor to either AC1 or AC2 for capacitive load modulation (COM2 must be connected to the alternate AC1 or AC2 pin). For resistive modulation connect COM1 and COM2 to RECT via a single resistor; connect through separate capacitors for capacitive load modulation. |
| COM2 | E1 | O | |
| CLMP2 | E2 | O | Open drain FETs which are utilized for a non-power dissipative over-voltage AC clamp protection. When the RECT voltage goes above 15 V, both switches will be turned on and the capacitors will act as a low impedance to protect the IC from damage. If used, Clamp1 is required to be connected to AC1, and Clamp2 is required to be connected to AC2 via 0.47µF capacitors. |
| CLMP1 | E3 | O | |

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## PIN FUNCTIONS (continued)

| NAME | NO. | I/O | DESCRIPTION |
|---|---|---|---|
| PGND | A1, A2, A3, A4 | | Power ground |
| ILIM | G1 | I/O | Programming pin for the over current limit. Connect external resistor to VSS. Size $R_{ILIM}$ with the following equation: $R_{ILIM} = 314 / I_{MAX}$ where IMAX is the expected maximum output current of the wireless power supply. The hardware current limit (IILIM) will be 20% greater than IMAX or 1.2 x $1_{MAX}$. If the supply is meant to operate in current limit use<br>$R_{ILIM} = 314 / I_{ILIM}$<br>$R_{ILIM} = R1 + R_{FOD}$ |
| AD | G4 | I | Connect this pin to the wired adapter input. When a voltage is applied to this pin wireless charging is disabled and AD_EN is driven low. Connect to GND through a 1 µF capacitor. If unused, capacitor is not required and should be grounded directly. |
| $\overline{\text{AD-EN}}$ | F3 | O | Push-pull driver for external PFET connecting AD and OUT. This node is pulled to the higher of OUT and AD when turning off the external FET. This voltage tracks approximately 4 V below AD when voltage is present at AD and provides a regulated VSG bias for the external FET. Float this pin if unused. |
| TS-CTRL | F1 | I | Must be connected to ground via a resistor. If an NTC function is not desired connect to GND with a 10 kΩ resistor. As a CTRL pin pull to ground to send end power transfer (EPT) fault to the transmitter or pull-up to an internal rail (i.e. 1.8 V) to send EPT termination to the transmitter. Note that a 3-state driver should be used to interface this pin (see the 3-state Driver section for further description) |
| EN1 | G3 | I | Inputs that allow user to enable/disable wireless and wired charging <EN1 EN2>:<br><00> wireless charging is enabled unless AD voltage > 3.6 V<br><01> Dynamic communication current limit disabled<br><10> $\overline{\text{AD-EN}}$ pulled low, wireless charging disabled<br><11> wired and wireless charging disabled. |
| EN2 | G2 | I | |
| FOD | F2 | I | Input for the received power measurement. Connect to GND with a 140 Ω resistor. See the FOD section for more detail. |
| $\overline{\text{WPG}}$ | F4 | O | Open-drain output – Active when the output of the wireless power supply is enabled. |

## TYPICAL CHARACTERISTICS

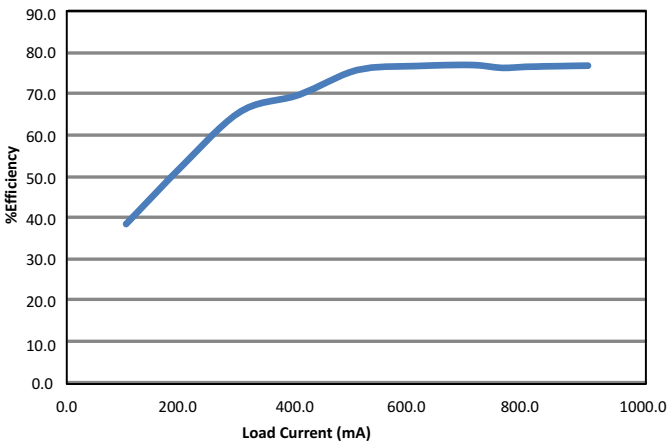


**Figure 5. System Efficiency from DC Input to DC Output**

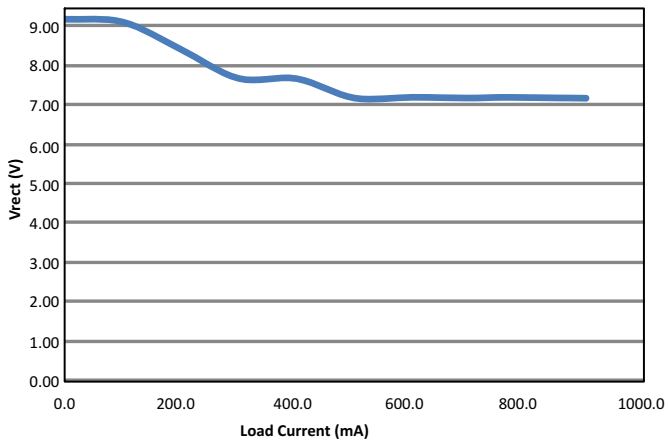


**Figure 6. Vrect Vs Load Current**


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## TYPICAL CHARACTERISTICS (continued)

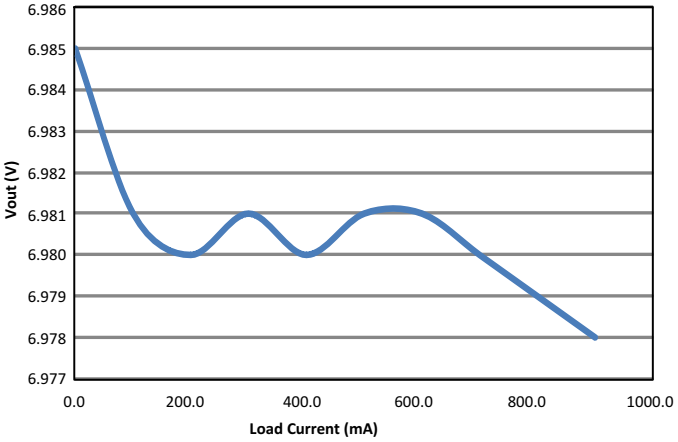


Figure 7. Load Current Sweep (I-V Curve)

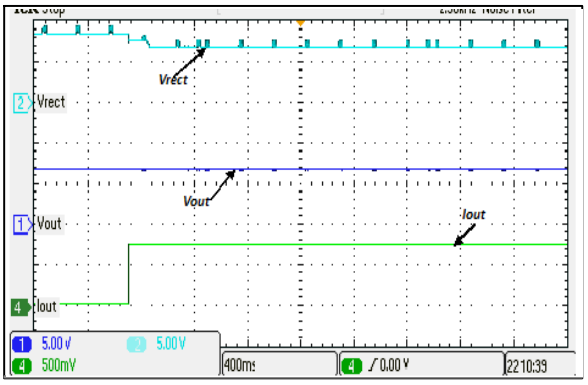


Figure 8. 720mA Load Step Full System Response

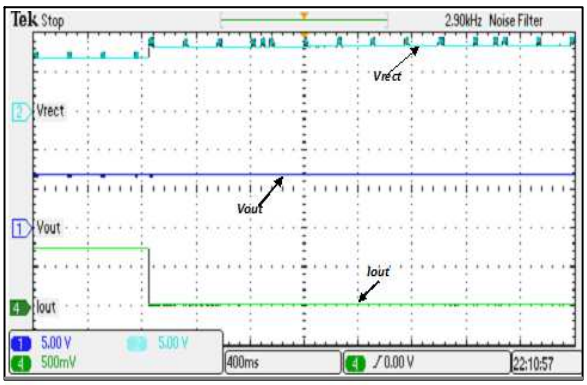


Figure 9. 720mA Load Dump Full System Response

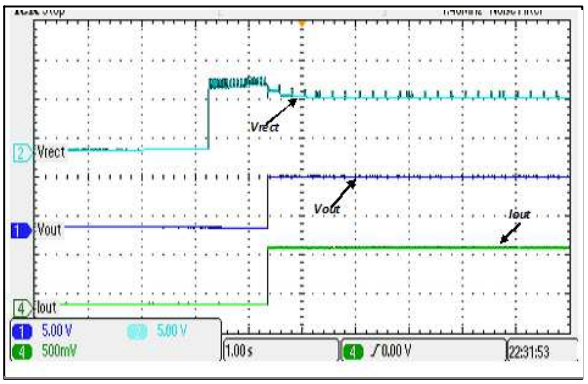


Figure 10. Typical Startup with a 720mA System Load

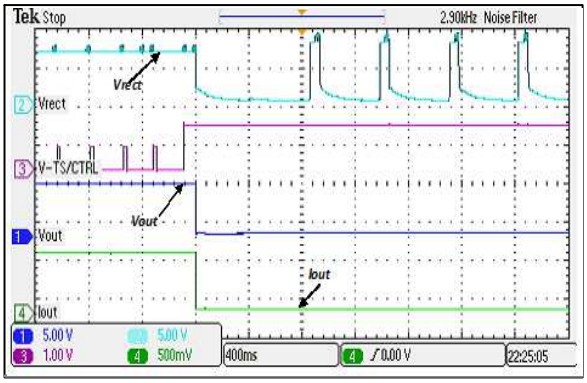


Figure 11. TS Fault

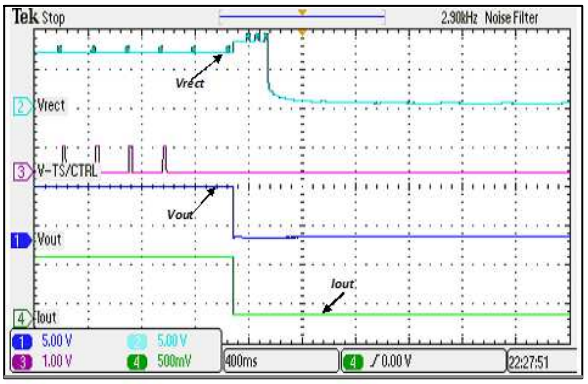


Figure 12. TS Fault GND

## PRINCIPLE OF OPERATION

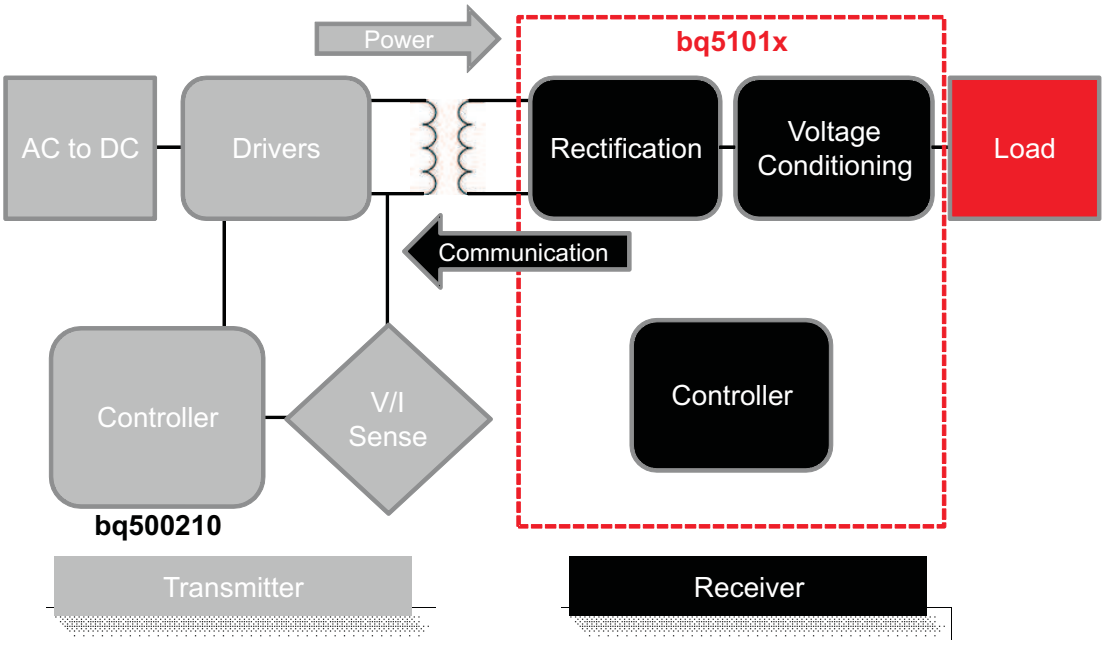


**Figure 13. WPC Wireless Power System Indicating the Functional Integration of the bq51010B**

### A Brief Description of the Wireless System:

A wireless system consists of a charging pad (transmitter or primary) and the secondary-side equipment (receiver or secondary). There is a coil in the charging pad and in the secondary equipment which are magnetically coupled to each other when the secondary is placed on the primary. Power is then transferred from the transmitter to the receiver via coupled inductors (e.g. an air-core transformer). Controlling the amount of power transferred is achieved by sending feedback (error signal) communication to the primary (e.g. to increase or decrease power).

The receiver communicates with the transmitter by changing the load seen by the transmitter. This load variation results in a change in the transmitter coil current, which is measured and interpreted by a processor in the charging pad. The communication is digital - packets are transferred from the receiver to the transmitter. Differential Bi-phase encoding is used for the packets. The bit rate is 2-kbps.

Various types of communication packets have been defined. These include identification and authentication packets, error packets, control packets, end power packets, and power usage packets.

The transmitter coil stays powered off most of the time. It occasionally wakes up to see if a receiver is present. When a receiver authenticates itself to the transmitter, the transmiter will remain powered on. The receiver maintains full control over the power transfer using communication packets.


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## Using the bq51010B as a Wireless Power Supply: (See Figure 3)

Figure 3 is the schematic of a system which uses the bq51010B as power supply while power multiplexing the wired (adapter) port.

When the system shown in Figure 3 is placed on the charging pad, the receiver coil is inductively coupled to the magnetic flux generated by the coil in the charging pad which consequently induces a voltage in the receiver coil. The internal synchronous rectifier feeds this voltage to the RECT pin which has the filter capacitor C3.

The bq51010B identifies and authenticates itself to the primary using the COM pins by switching on and off the COM FETs and hence switching in and out $C_{COMM}$. If the authentication is successful, the transmitter will remain powered on. The bq51010B measures the voltage at the RECT pin, calculates the difference between the actual voltage and the desired voltage $V_{RECT-REG}$, (threshold 1 at no load) and sends back error packets to the primary. This process goes on until the input voltage settles at $V_{RECT-REG}$. During a load transient, the dynamic rectifier algorithm will set the targets specified by $V_{RECT-REG}$ thresholds 1, 2, 3, and 4. This algorithm is termed Dynamic Rectifier Control and is used to enhance the transient response of the power supply.

During power-up, the LDO is held off until the $V_{RECT-REG}$ threshold 1 converges. The voltage control loop ensures that the output voltage is maintained at $V_{OUT-REG}$ to power the system. The bq51010B meanwhile continues to monitor the input voltage, and maintains sending error packets to the primary every 250ms. If a large overshoot occurs, the feedback to the primary speeds up to every 32ms in order to converge on an operating point in less time.

## Details of a Qi Wireless Power System and bq51010B Power Transfer Flow Diagrams

The bq51010B family integrates a fully compliant WPC v1.1 communication algorithm in order to streamline receiver designs (no extra software development required). Other unique algorithms such has Dynamic Rectifier Control are also integrated to provide best-in-class system performance. This section provides a high level overview of these features by illustrating the wireless power transfer flow diagram from startup to active operation.

During startup operation, the wireless power receiver must comply with proper handshaking to be granted a power contract from the Tx. The Tx will initiate the hand shake by providing an extended digital ping. If an Rx is present on the Tx surface, the Rx will then provide the signal strength, configuration and identification packets to the Tx (see volume 1 of the WPC specification for details on each packet). These are the first three packets sent to the Tx. The only exception is if there is a true shutdown condition on the EN1/EN2, AD, or TS-CTRL pins where the Rx will shut down the Tx immediately. See Table 4 for details. Once the Tx has successfully received the signal strength, configuration and identification packets, the Rx will be granted a power contract and is then allowed to control the operating point of the power transfer. With the use of the bq51010B Dynamic Rectifier Control algorithm, the Rx will inform the Tx to adjust the rectifier voltage above 9 V prior to enabling the output supply. This method enhances the transient performance during system startup. See Figure 14 for the startup flow diagram details.

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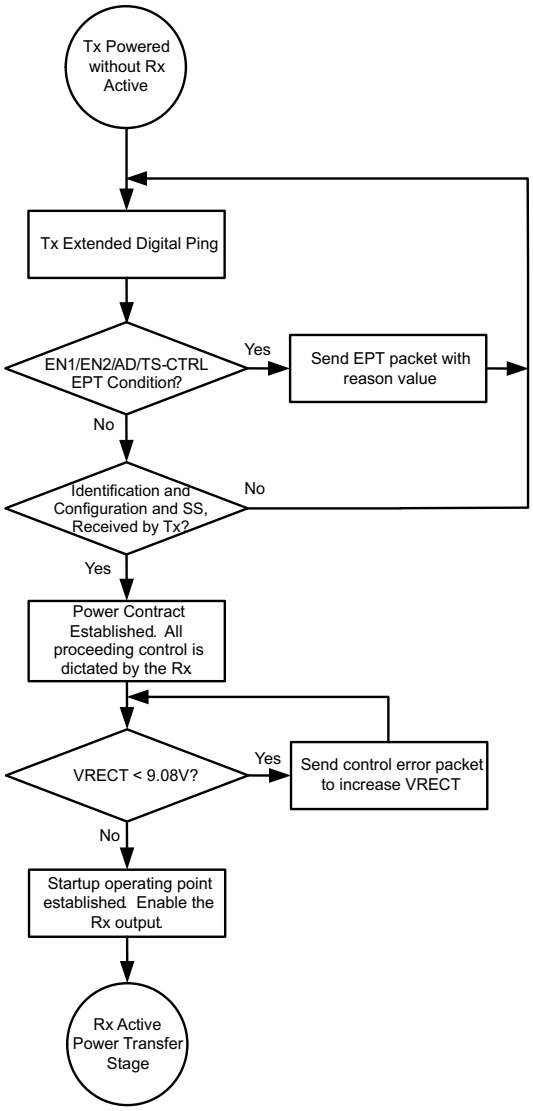


**Figure 14. Wireless Power Startup Flow Diagram**

Once the startup procedure has been established, the Rx will enter the active power transfer stage. This is considered the "main loop" of operation. The Dynamic Rectifier Control algorithm will determine the rectifier voltage target based on a percentage of the maximum output current level setting (set by $K_{IMAX}$ and the ILIM resistance to GND). The Rx will send control error packets in order to converge on these targets. As the output current changes, the rectifier voltage target will dynamically change. As a note, the feedback loop of the WPC system is relatively slow where it can take up to 90 ms to converge on a new rectifier voltage target. It should be understood that the instantaneous transient response of the system is open loop and dependent on the Rx coil output impedance at that operating point. More details on this will be covered in the section Receiver Coil Load-Line Analysis. The "main loop" will also determine if any conditions in Table 4 are true in order to discontinue power transfer. See Figure 15 which illustrates the active power transfer loop.


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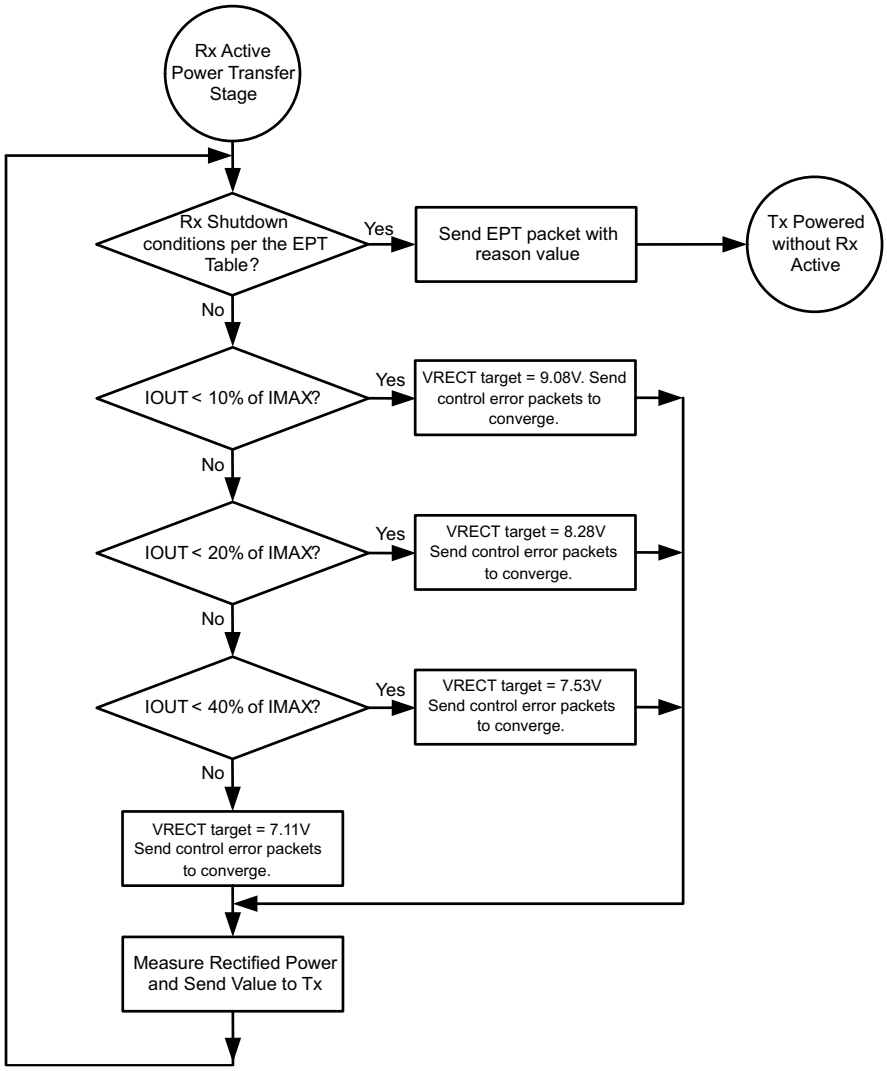


**Figure 15. Active Power Transfer Flow Diagram**

Another requirement of the WPC v1.1 specification is to send the measured recieved power. This task is enabled on the IC by measuring the voltage on the FOD pin which is proportional to the output current and can be scaled based on the choice of the resitor to ground on the FOD pin.

## Dynamic Rectifier Control

The Dynamic Rectifier Control algorithm offers the end system designer optimal transient response for a given max output current setting. This is achieved by providing enough voltage headroom across the internal regulator at light loads in order to maintain regulation during a load transient. The WPC system has a relatively slow global feedback loop where it can take more than 90 ms to converge on a new rectifier voltage target. Therefore, the transient response is dependent on the loosely coupled transformers output impedance profile. The Dynamic Rectifier Control allows for a 2 V change in rectified voltage before the transient response will be observed at the output of the internal regulator (output of the bq51010B). A 720mA application allows up to a 1.5 Ω output impedance.

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## Dynamic Efficiency Scaling

The Dynamic Efficiency Scaling feature allows for the loss characteristics of the bq51010B to be scaled based on the maximum expected output power in the end application. This effectively optimizes the efficiency for each application. This feature is achieved by scaling the loss of the internal LDO based on a percentage of the maximum output current. Note that the maximum output current is set by the $K_{IMAX}$ term and the $R_{ILIM}$ resistance (where $R_{ILIM} = K_{IMAX} / I_{MAX}$). The flow diagram show in Figure 15 illustrates how the rectifier is dynamically controlled (*Dynamic Rectifier Control*) based on a fixed percentage of the $I_{MAX}$ setting. The below table summarizes how the rectifier behavior is dynamically adjusted based on two different $R_{ILIM}$ settings.

**Table 1.**

| Output Current Percentage | $R_{ILIM}$ = 890Ω<br>$I_{MAX}$ = 0.350A | $R_{ILIM}$ = 417Ω<br>$I_{MAX}$ = 0.750A | $V_{RECT}$ |
|---|---|---|---|
| 0 to 10% | 0 A to 0.035 A | 0 A to 0.075 A | 9.08 V |
| 10 to 20% | 0.035 A to 0.070A | 0.075 A to 0.150 A | 8.28 V |
| 20 to 40% | 0.070 A to 0.140A | 0.150 A to 0.225 A | 7.53 V |
| >40% | > 0.140 A | >0.225A | 7.11 V |

## $R_{ILIM}$ Calculations

The bq51010B includes a means of providing hardware overcurrent protection by means of an analog current regulation loop. The hardware current limit provides an extra level of safety by clamping the maximum allowable output current (e.g. a current compliance). The $R_{ILIM}$ resistor size also sets the thresholds for the dynamic rectifier levels and thus providing efficiency tuning per each application's maximum system current. The calculation for the total $R_{ILIM}$ resistance is as follows:

$$R_{ILIM} = \frac{262}{I_{MAX}}$$

$$I_{ILIM} = 1.2 \times I_{MAX} = \frac{314}{R_{ILIM}}$$

$$R_{ILIM} = R_1 + R_{FOD} \quad (1)$$

Where $I_{MAX}$ is the expected maximum output current during normal operation and $I_{ILIM}$ is the hardware over current limit. When referring to the application diagram shown in Figure 2, $R_{ILIM}$ is the sum of $R_{FOD}$ and the $R_1$ resistance (e.g. the total resistance from the ILIM pin to GND).

## Input Overvoltage

If the input voltage suddenly increases in potential (e.g. due to a change in position of the equipment on the charging pad), the voltage-control loop inside the bq51010B becomes active, and prevents the output from going beyond $V_{OUT\text{-}REG}$. The receiver then starts sending back error packets to the transmitter every 30ms until the input voltage comes back to the $V_{RECT\text{-}REG}$ target, and then maintains the error communication every 250ms.

If the input voltage increases in potential beyond $V_{OVP}$, the IC switches off the LDO and communicates to the primary to bring the voltage back to $V_{RECT\text{-}REG}$. In addition, a proprietary voltage protection circuit is activated by means of $C_{CLAMP1}$ and $C_{CLAMP2}$ that protects the IC from voltages beyond the maximum rating of the IC (e.g. 20V).

## Adapter Enable Functionality and EN1/EN2 Control

Figure 3 is an example application that shows the bq51010B used as a wireless power receiver that can power mutliplex between wired or wireless power for the down-system electronics. In the default operating mode pins EN1 and EN2 are low, which activates the adapter enable functionality. In this mode, if an adapter is not present the AD pin will be low, and AD-EN pin will be pulled to the higher of the OUT and AD pins so that the PMOS between OUT and AD will be turned off. If an adapter is plugged in and the voltage at the AD pin goes above 3.6V then wireless charging is disabled and the AD-EN pin will be pulled approximately 4V below the AD pin to connect AD to the secondary charger. The difference between AD and AD-EN is regulated to a maximum of 7V to ensure the $V_{GS}$ of the external PMOS is protected.


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The EN1 and EN2 pins include internal 200kΩ pull-down resistors, so that if these pins are not connected bq51010B defaults to $\overline{\text{AD-EN}}$ control mode. However, these pins can be pulled high to enable other operating modes as described in Table 2:

**Table 2.**

| EN1 | EN2 | Result |
|---|---|---|
| 0 | 0 | Adapter control enabled. If adapter is present then secondary charger is powered by adapter, otherwise wireless charging is enabled when wireless power is available. Communication current limit is enabled. |
| 0 | 1 | Disables communication current limit. |
| 1 | 0 | $\overline{\text{AD-EN}}$ is pulled low, whether or not adapter voltage is present. This feature can be used, e.g., for USB OTG applications. |
| 1 | 1 | Adapter and wireless charging are disabled, i.e., power will never be delivered by the OUT pin in this mode. |

**Table 3.**

| EN1 | EN2 | Wireless Power | Wired Power | OTG Mode | Adaptive Communication Limit | EPT |
|---|---|---|---|---|---|---|
| 0 | 0 | Enabled | Priority(1) | Disabled | Enabled | Not Sent to Tx |
| 0 | 1 | Priority(1) | Enabled | Disabled | Disabled | Not Sent to Tx |
| 1 | 0 | Disabled | Enabled | Enabled(2) | N/A | No Response |
| 1 | 1 | Disabled | Disabled | Disabled | N/A | Termination |

(1) If both wired and wireless power are present, wired power is given priority.
(2) Allows for a boost-back supply to be driven from the output terminal of the Rx to the adapter port via the external back-to-back PMOS FET.

As described in Table 3, pulling EN2 high disables the adapter mode and only allows wireless charging. In this mode the adapter voltage will always be blocked from the OUT pin. An application example where this mode is useful is when USB power is present at AD, but the USB is in suspend mode so that no power can be taken from the USB supply. Pulling EN1 high enables the off-chip PMOS regardless of the presence of a voltage. This function can be used in USB OTG mode to allow a charger connected to the OUT pin to power the AD pin. Finally, pulling both EN1 and EN2 high disables both wired and wireless charging.

**NOTE**

It is required to connect a back-to-back PMOS between AD and OUT so that voltage is blocked in both directions. Also, when AD mode is enabled no load can be pulled from the RECT pin as this could cause an internal device overvoltage in bq51010B.

## End Power Transfer Packet (WPC Header 0x02)

The WPC allows for a special command for the receiver to terminate power transfer from the transmitter termed End Power Transfer (EPT) packet. Table 4 specifies the v1.1 reasons column and their corresponding data field value. The condition column corresponds to the methodology used by bq51010B to send equivalent message.

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**Table 4.**

| Message | Value | Condition |
|---|---|---|
| Unknown | 0x00 | AD > 3.6V |
| Charge Complete | 0x01 | TS/CTRL = 1, or EN1 = 1, or <EN1 EN2> = <11> |
| Internal Fault | 0x02 | $T_J$ > 150°C or $R_{ILIM}$ < 100Ω |
| Over Temperature | 0x03 | TS < $V_{HOT}$, TS > $V_{COLD}$, or TS/CTRL < 100mV |
| Over Voltage | 0x04 | Not Sent |
| Over Current | 0x05 | NOT USED |
| Battery Failure | 0x06 | Not Sent |
| Reconfigure | 0x07 | Not Sent |
| No Response | 0x08 | VRECT target doesn't converge |

## Status Outputs

The bq51010B has one status output, $\overline{WPG}$. This output is an open-drain NMOS device that is rated to 20V. The open-drain FET connected to the $\overline{WPG}$ pin will be turned on whenever the output of the power supply is enabled. Please note, the output of the power supply will not be enabled if the $V_{RECT-REG}$ does not converge at the no-load target voltage.

## WPC Communication Scheme

The WPC communication uses a modulation technique termed “back-scatter modulation” where the receiver coil is dynamically loaded in order to provide amplitude modulation of the transmitter's coil voltage and current. This scheme is possible due to the fundamental behavior between two loosely coupled inductors (e.g. between the Tx and Rx coil). This type of modulation can be accomplished by switching in and out a resistor at the output of the rectifier, or by switching in and out a capacitor across the AC1/AC2 net. Figure 16 shows how to implement resistive modulation.

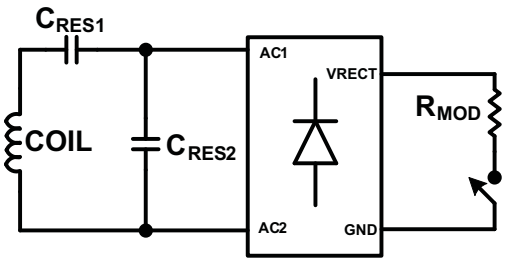


**Figure 16. Resistive Modulation**

Figure 17 Shows how to implement capacitive modulation.

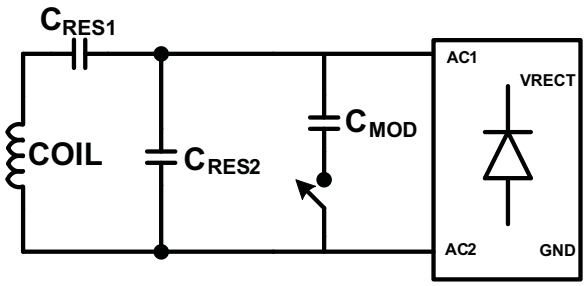


**Figure 17. Capacitive Modulation**

The amplitude change in Tx coil voltage or current can be detected by the transmitters decoder. The resulting signal observed by the Tx is shown in Figure 18.


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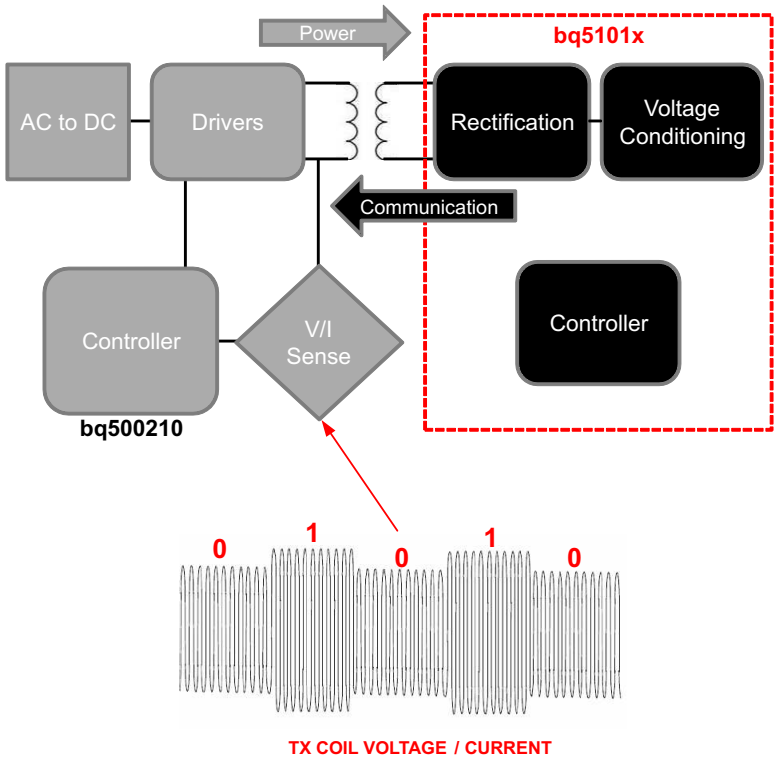


**Figure 18.**

The WPC protocol uses a differential bi-phase encoding scheme to modulate the data bits onto the Tx coil voltage/current. Each data bit is aligned at a full period of 0.5 ms ($t_{CLK}$) or 2 kHz. An encoded ONE results in two transitions during the bit period and an encoded ZERO results in a single transition. See Figure 19 for an example of the differential bi-phase encoding.

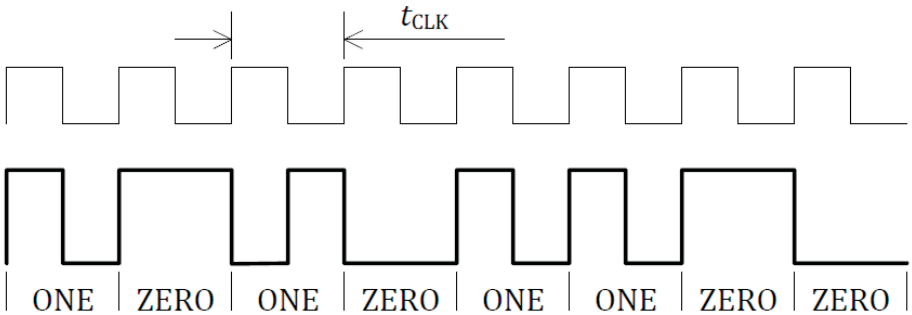


**Figure 19. Differential Bi-phase Encoding Scheme (WPC volume 1: Low Power, Part 1 Interface Definition)**

The bits are sent LSB first and use an 11-bit asynchronous serial format for each portion of the packet. This includes one start bit, n-data bytes, a parity bit, and a single stop bit. The start bit is always ZERO and the parity bit is odd. The stop bit is always ONE. Figure 20 shows the details of the asynchronous serial format.

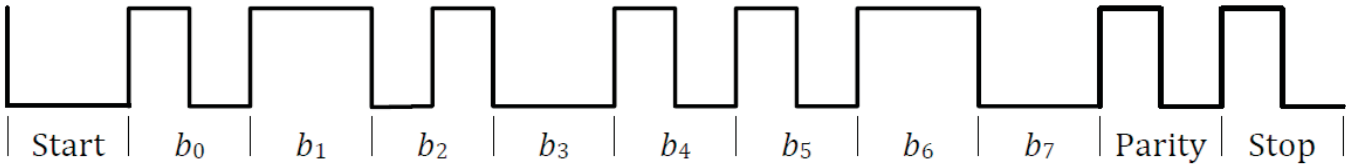


**Figure 20. Asynchronous Serial Formatting (WPC volume 1: Low Power, Part 1 Interface Definition)**

Each packet format is organized as shown in Figure 21.

**Figure 21. Packet Format (WPC volume 1: Low Power, Part 1 Interface Definition)**

## Communication Modulator

The bq51010B provides two identical, integrated communication FETs which are connected to the pins COM1 and COM2. These FETs are used for modulating the secondary load current which allows bq51010B to communicate error control and configuration information to the transmitter. Figure 22 below shows how the COMM pins can be used for resistive load modulation. Each COMM pin can handle at most a 24Ω communication resistor. Therefore, if a COMM resistor between 12Ω and 24Ω is required COM1 and COM2 pins must be connected in parallel. bq51010B does not support a COMM resistor less than 12Ω.

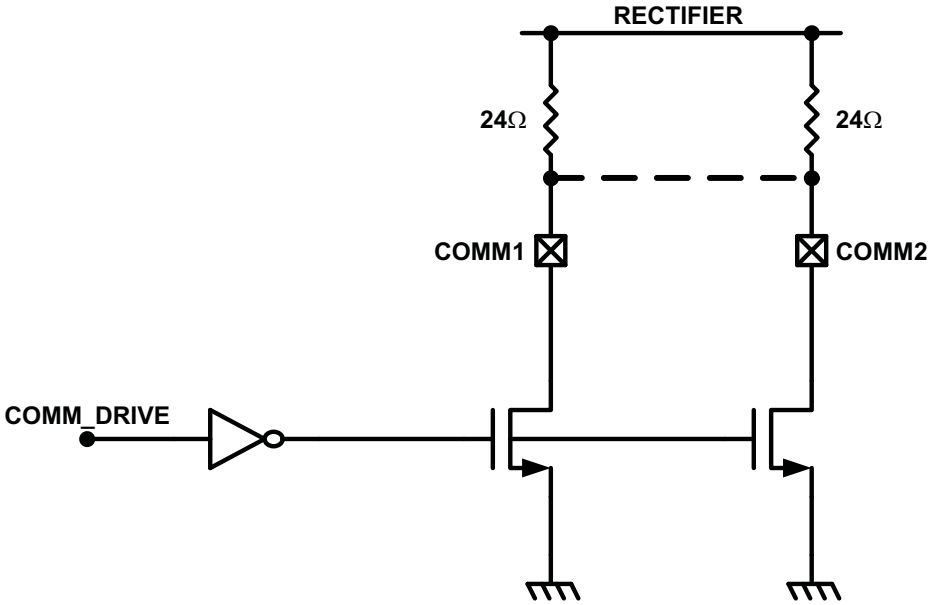


**Figure 22. Resistive Load Modulation**

In addition to resistive load modulation, the bq51010B is also capable of capacitive load modulation as shown in Figure 23 below. In this case, a capacitor is connected from COM1 to AC1 and from COM2 to AC2. When the COMM switches are closed there is effectively a 22 nF capacitor connected between AC1 and AC2. Connecting a capacitor in between AC1 and AC2 modulates the impedance seen by the coil, which will be reflected in the primary as a change in current.


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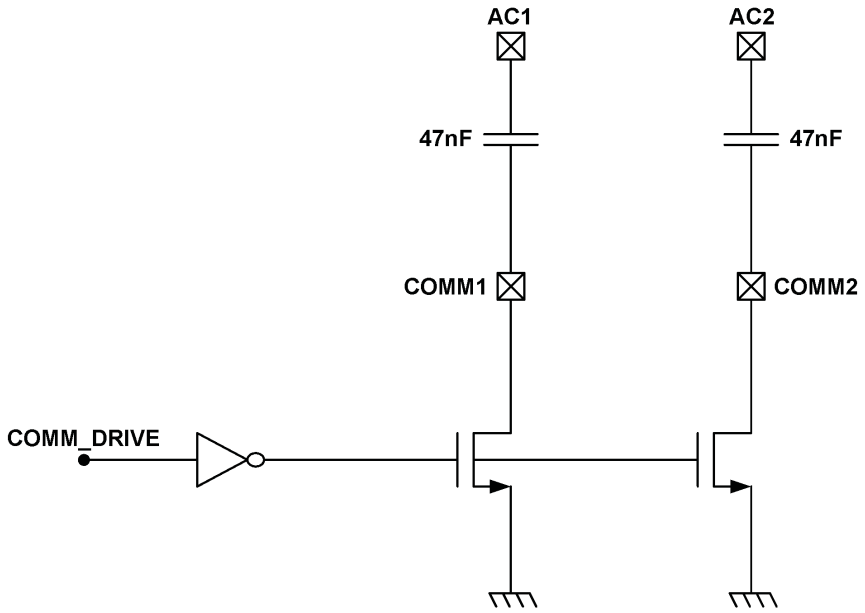


**Figure 23. Capacitive Load Modulation**

## Adaptive Communication Limit

The Qi communication channel is established via backscatter modulation as described in the previous sections. This type of modulation takes advantage of the loosely coupled inductor relationship between the Rx and Tx coil. Essentially the switching in-and-out of the communication capacitor or resistor adds a transient load to the Rx coil in order to modulate the Tx coil voltage/current waveform (amplitude modulation). The consequence of this technique is that a load transient (load current noise) from the mobile device has the same signature. In order to provide noise immunity to the communication channel, the output load transients must be isolated from the Rx coil. The proprietary feature *Adaptive Communication Limit* achieves this by dynamically adjusting the current limit of the regulator. When the regulator is put in current limit, any load transients will be offloaded to the battery in the system.

Note that this requires the battery charger IC to have input voltage regulation (weak adapter mode). The output of the Rx appears as a weak supply if a transient occurs above the current limit of the regulator.

The Adaptive Communication Limit feature has two current limit modes and is detailed in the table below:

**Table 5.**

| $I_{OUT}$ | Communication Current Limit |
|---|---|
| < 300 mA | Fixed 400 mA |
| > 300 mA | $I_{OUT}$ + 50 mA |

## Synchronous Rectification

The bq51010B provides an integrated, self-driven synchronous rectifier that enables high-efficiency AC to DC power conversion. The rectifier consists of an all NMOS H-Bridge driver where the backgates of the diodes are configured to be the rectifier when the synchronous rectifier is disabled. During the initial startup of the WPC system the synchronous rectifier is not enabled. At this operating point, the DC rectifier voltage is provided by the diode rectifier. Once $V_{RECT}$ is greater than UVLO, half synchronous mode will be enabled until the load current surpasses 120 mA. Above 120 mA the full synchronous rectifier stays enabled until the load current drops back below 100 mA where half synchronous mode is enabled instead.

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## Temperature Sense Resistor Network (TS)

bq51010B includes a ratiometric external temperature sense function. The temperature sense function has two ratiometric thresholds which represent a hot and cold condition. An external temperature sensor is recommended in order to provide safe operating conditions for the receiver product. This pin is best used for monitoring the surface that can be exposed to the end user (e.g. place the NTC resistor closest to the user).

Figure 24 allows for any NTC resistor to be used with the given $V_{HOT}$ and $V_{COLD}$ thresholds.

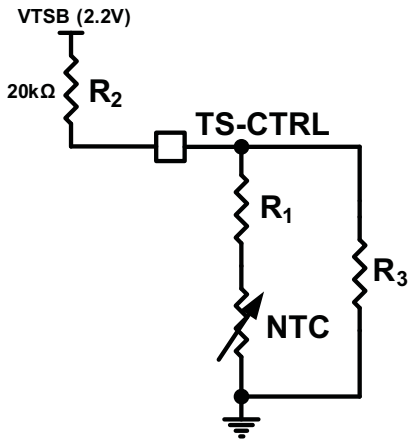


**Figure 24. NTC Circuit Used for Safe Operation of the Wireless Receiver Power Supply**

The resistors $R_1$ and $R_3$ can be solved by resolving the system of equations at the desired temperature thresholds. The two equations are:

$$\%V_{COLD} = \frac{\left(\frac{R_3\left(R_{NTC}\big|_{TCOLD} + R_1\right)}{R_3 + \left(R_{NTC}\big|_{TCOLD} + R_1\right)}\right)}{\left(\frac{R_3\left(R_{NTC}\big|_{TCOLD} + R_1\right)}{R_3 + \left(R_{NTC}\big|_{TCOLD} + R_1\right)}\right) + R2} \times 100$$

$$\%V_{HOT} = \frac{\left(\frac{R_3\left(R_{NTC}\big|_{THOT} + R_1\right)}{R_3 + \left(R_{NTC}\big|_{THOT} + R_1\right)}\right)}{\left(\frac{R_3\left(R_{NTC}\big|_{THOT} + R_1\right)}{R_3 + \left(R_{NTC}\big|_{THOT} + R_1\right)}\right) + R2} \times 100 \quad (2)$$

Where:

$$R_{NTC}\big|_{TCOLD} = R_o e^{\beta\left(1/T_{COLD} - 1/T_o\right)}$$

$$R_{NTC}\big|_{THOT} = R_o e^{\beta\left(1/T_{HOT} - 1/T_o\right)} \quad (3)$$

where, $T_{COLD}$ and $T_{HOT}$ are the desired temperature thresholds in degrees Kelvin. $R_O$ is the nominal resistance and β is the temperature coefficient of the NTC resistor. $R_O$ is fixed at 20 kΩ. An example solution is provided:

- R1 = 4.23kΩ
- R3 = 66.8kΩ

where the chosen parameters are:

- $\%V_{HOT}$ = 19.6%
- $\%V_{COLD}$ = 58.7%
- $T_{COLD}$ = –10°C


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- $T_{HOT}$ = 100°C
- β = 3380
- $R_O$ = 10kΩ

The plot of the percent $V_{TSB}$ vs. temperature is shown in Figure 25:

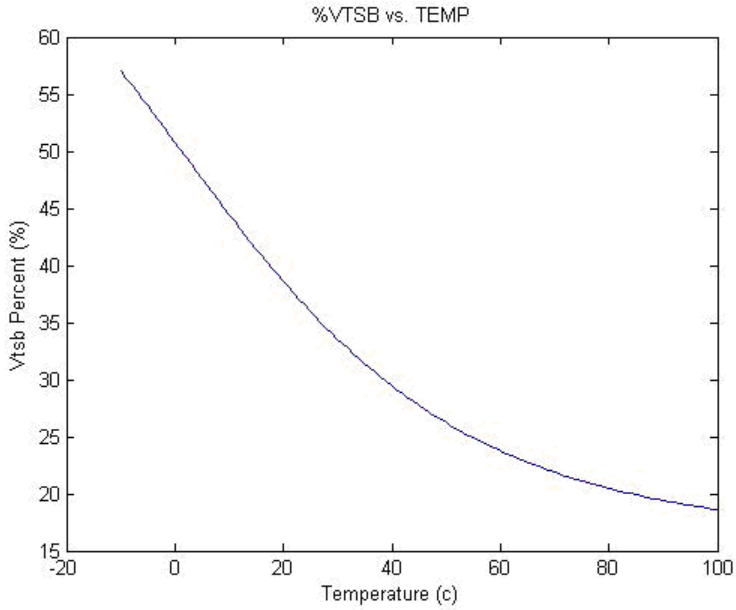


**Figure 25. Example Solution for an NTC resistor with $R_O$ = 10kΩ and β = 4500**

Figure 26 illustrates the periodic biasing scheme used for measuring the TS state. The TS_READ signal enables the TS bias voltage for 24ms. During this period the TS comparators are read (each comparator has a 10 ms deglitch) and appropriate action is taken based on the temperature measurement. After this 24ms period has elapsed, the TS_READ signal goes low, which causes the TS-Bias pin to become high impedance. During the next 35ms (priority packet period) or 235ms (standard packet period), the TS voltage is monitored and compared to 100mV. If the TS voltage is greater than 100mV then a secondary device is driving the TS/CTRL pin and a CTRL = '1' is detected.

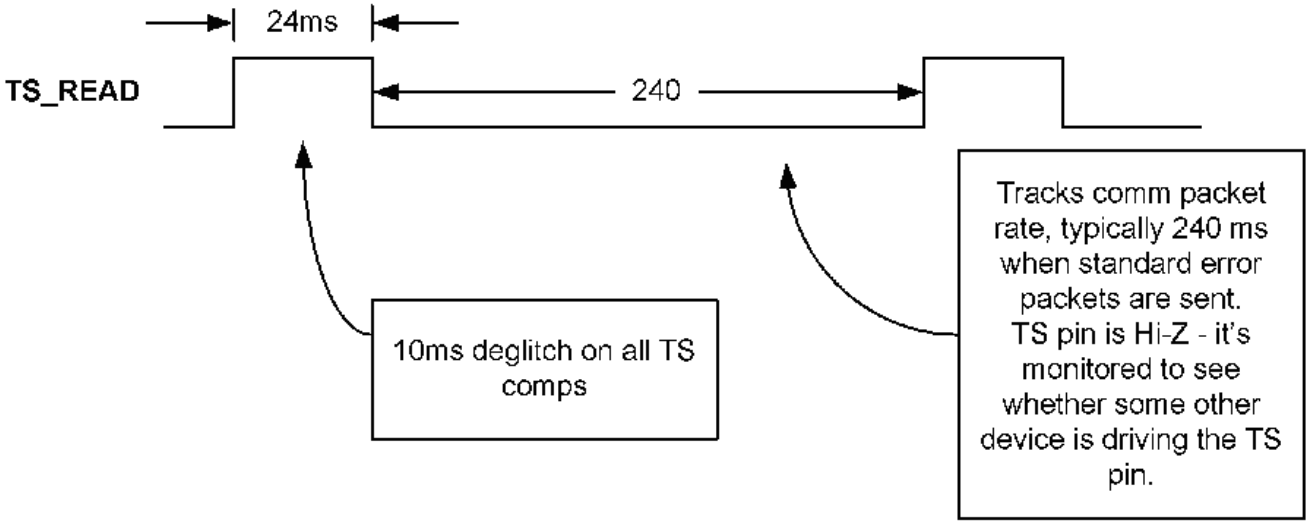


**Figure 26. Timing Diagram for TS Detection Circuit**

## 3-state Driver Recommendations for the TS-CTRL Pin

The TS-CTRL pin offers three functions with one 3-state driver interface

1. NTC temperature monitoring,
2. Fault indication,
3. Charge done indication

A 3-state driver can be implemented with the circuit in Figure 27 and the use of two GPIO connections.

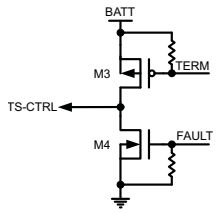


**Figure 27. 3-state Driver for TS-CTRL**

Note that the signals "TERM" and "FAULT" are given by two GPIOs. The truth table for this circuit is found in Table 6:

**Table 6.**

| TERM | FAULT | F (Result) |
|---|---|---|
| 1 | 0 | Z (Normal Mode) |
| 0 | 0 | Charge Complete |
| 1 | 1 | System Fault |

The default setting is TERM = 1 and FAULT = 0. In this condition, the TS-CTRL net is high impedance (hi-z) and; therefore, the NTC is function is allowed to operate. When the TS-CTRL pin is pulled to GND by setting FAULT = 1, the Rx is shutdown with the indication of a fault. When the TS-CTRL pin is pulled to the battery by setting TERM = 1, the Rx is shutdown with the indication of a charge complete condition. Therefore, the host controller can indicate whether the Rx is system is turning off due to a fault or due to a charge complete condition.

## Thermal Protection

The bq51010B includes a thermal shutdown protection. If the die temperature reaches $T_J$(OFF), the LDO is shut off to prevent any further power dissipation. In this case bq51010B will send an EPT message of internal fault (0x02).

## WPC 1.1 Compliance – Foreign Object Detection

The bq51010B is a WPC 1.1 compatible device. In order to enable a Power Transmitter to monitor the power loss across the interface as one of the possible methods to limit the temperature rise of Foreign Objects, the bq51010B reports its Received Power to the Power Transmitter. The Received Power equals the power that is available from the output of the Power Receiver plus any power that is lost in producing that output power (the power loss in the Secondary Coil and series resonant capacitor, the power loss in the Shielding of the Power Receiver, the power loss in the rectifier). In WPC1.1 specification, foreign object detection (FOD) is enforced. This means the bq51010B will send received power information with known accuracy to the transmitter.

WPC 1.1 defines Received Power as "the average amount of power that the Power Receiver receives through its Interface Surface, in the time window indicated in the Configuration Packet".

In order to receive certification as a WPC 1.1 receiver, the Device Under Test (DUT) is tested on a Reference Transmitter whose transmitted power is calibrated, the receiver must send a received power such that:

$$0 < (\text{TX PWR})_{REF} - (\text{RX PWR out})_{DUT} < -250\text{mW} \quad (4)$$

This 250mW bias ensures that system will remain interoperable.

WPC 1.1 Transmitter will be tested to see if they can detect reference Foreign Objects with a Reference receiver.

WPC1.1 Specification will allow much more accurate sensing of Foreign Objects.


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## Series and Parallel Resonant Capacitor Selection

Shown in Figure 2, the capacitors C1 (series) and C2 (parallel) make up the dual resonant circuit with the receiver coil. These two capacitors must be sized correctly per the WPC v1.1 specification. Figure 28 illustrates the equivalent circuit of the dual resonant circuit:

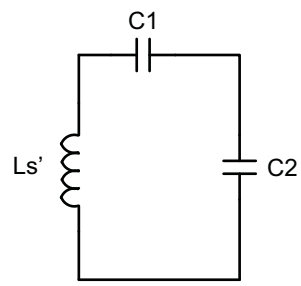


**Figure 28. Dual Resonant Circuit with the Receiver Coil**

Section 4.2 (Power Receiver Design Requirements) in Part 1 of the WPC v1.1 specification highlights in detail the sizing requirements. To summarize, the receiver designer will be required take inductance measurements with a fixed test fixture. The test fixture is shown in Figure 29:

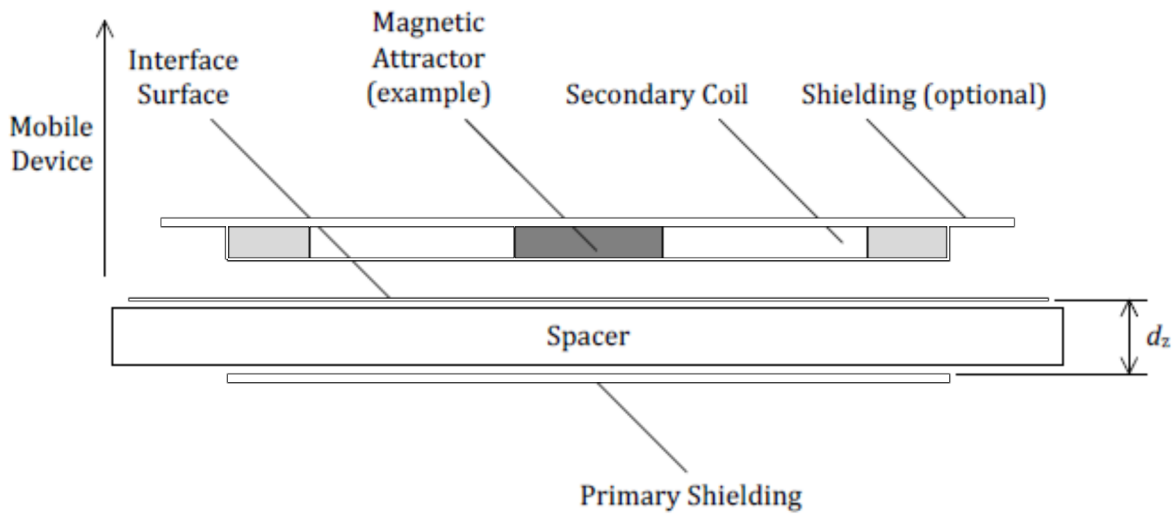


**Figure 29. WPC v1.1 Receiver Coil Test Fixture for the Inductance Measurement Ls' (copied from System Description Wireless Power Transfer, volume 1: Low Power, Part 1 Interface Definition, Version 1.1)**

The primary shield is to be 50 mm x 50 mm x 1 mm of Ferrite material PC44 from TDK Corp. The gap $d_Z$ is to be 3.4 mm. The receiver coil, as it will be placed in the final system (e.g. the back cover and battery must be included if the system calls for this), is to be placed on top of this surface and the inductance is to be measured at 1-V RMS and a frequency of 100 kHz. This measurement is termed Ls'. The same measurement is to be repeated without the test fixture shown in Figure 12. This measurement is termed Ls or the free-space inductance. Each capacitor can then be calculated using Equation 5:

$$C_1 = \left[ \left( f_S \cdot 2\pi \right)^2 \cdot L'_S \right]^{-1}$$

$$C_2 = \left[ \left( f_D \cdot 2\pi \right)^2 \cdot L_S - \frac{1}{C_1} \right]^{-1} \tag{5}$$

Where $f_S$ is 100 kHz +5/-10% and $f_D$ is 1 MHz ±10%. C1 must be chosen first prior to calculating C2.

The quality factor must be greater than 77 and can be determined by Equation 6:

$$Q = \frac{2\pi \cdot f_D \cdot L_S}{R} \tag{6}$$

where R is the DC resistance of the receiver coil. All other constants are defined above.

## Package Summary

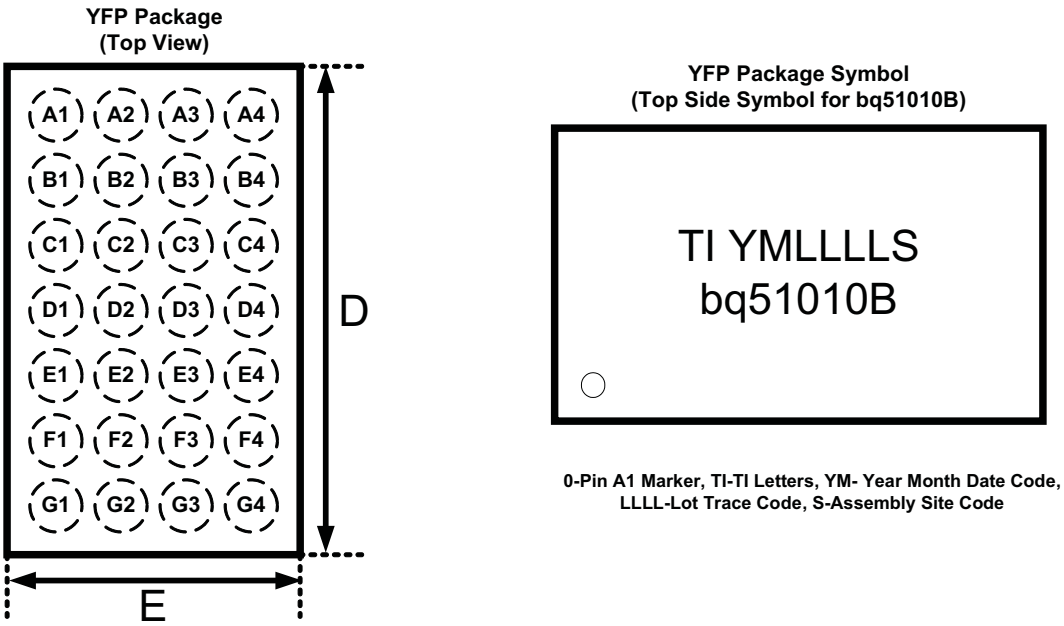


**Figure 30. Chip Scale Packaging Dimensions**

- D = 3.0mm ± 0.035mm
- E = 1.88mm ± 0.035mm


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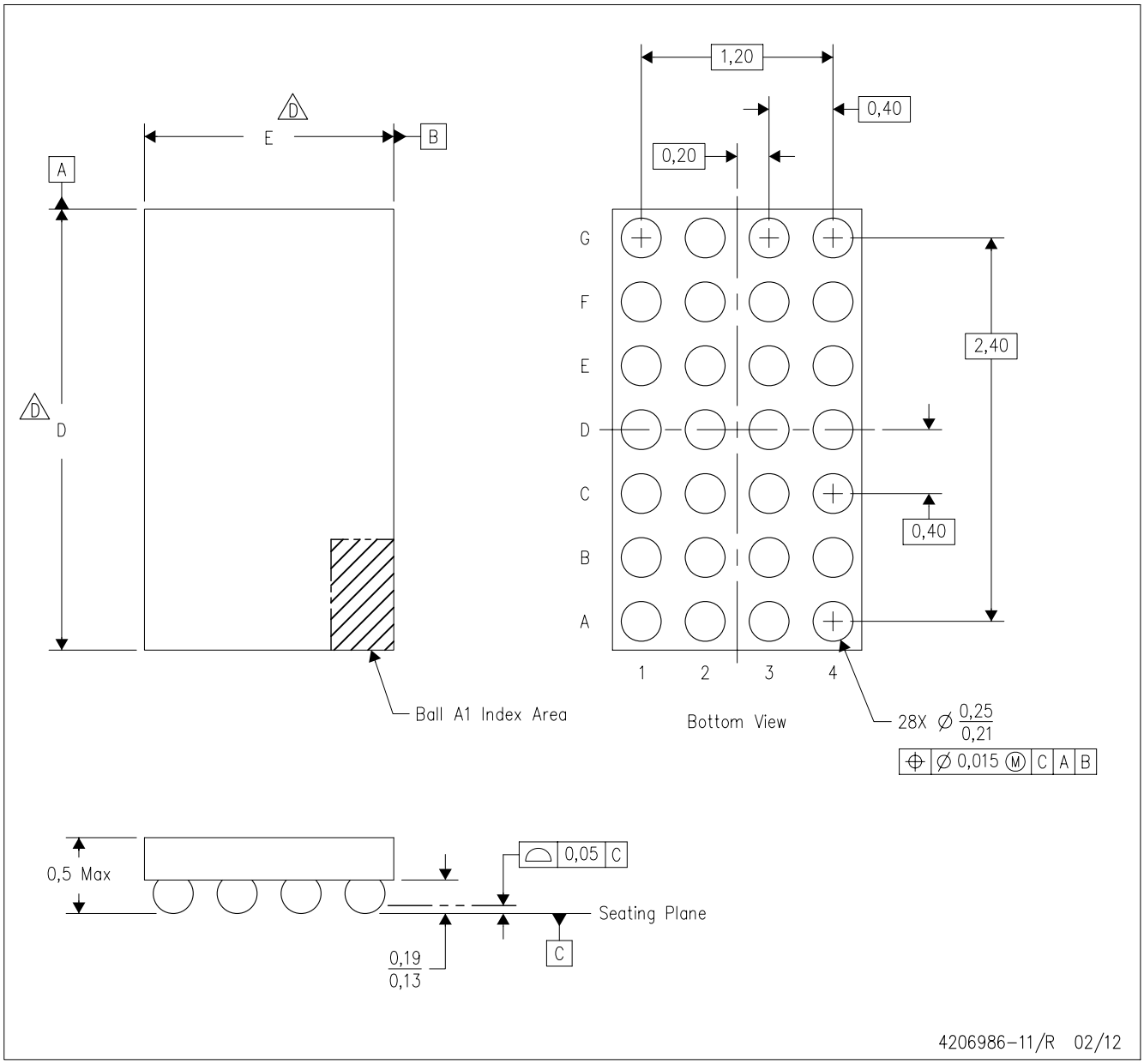
YFP (R–XBGA–N28) DIE–SIZE BALL GRID ARRAY




NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.
D. To determine the exact package size of a particular device, refer to the device datasheet or contact a local TI representative.
E. This package contains Pb–free balls.

**NanoFree is a trademark of Texas Instruments**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ51010BYFPR | ACTIVE | DSBGA | YFP | 28 | 3000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ51010B | Samples |
| BQ51010BYFPT | ACTIVE | DSBGA | YFP | 28 | 250 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM | -40 to 85 | BQ51010B | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
**TBD:** The Pb-Free/Green conversion plan has not been defined.
**Pb-Free (RoHS):** TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
**Pb-Free (RoHS Exempt):** This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
**Green (RoHS & no Sb/Br):** TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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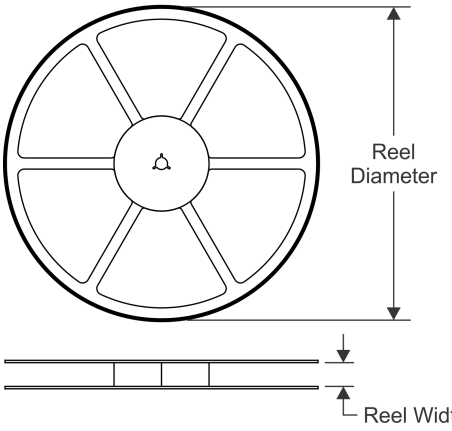
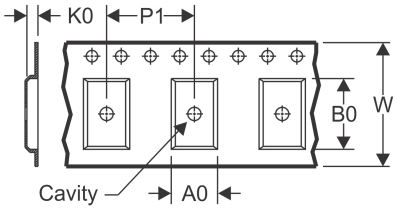
## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

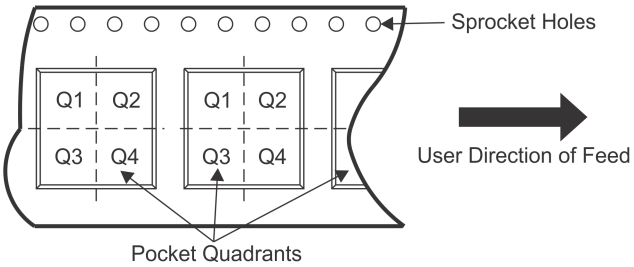



**TAPE DIMENSIONS**




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

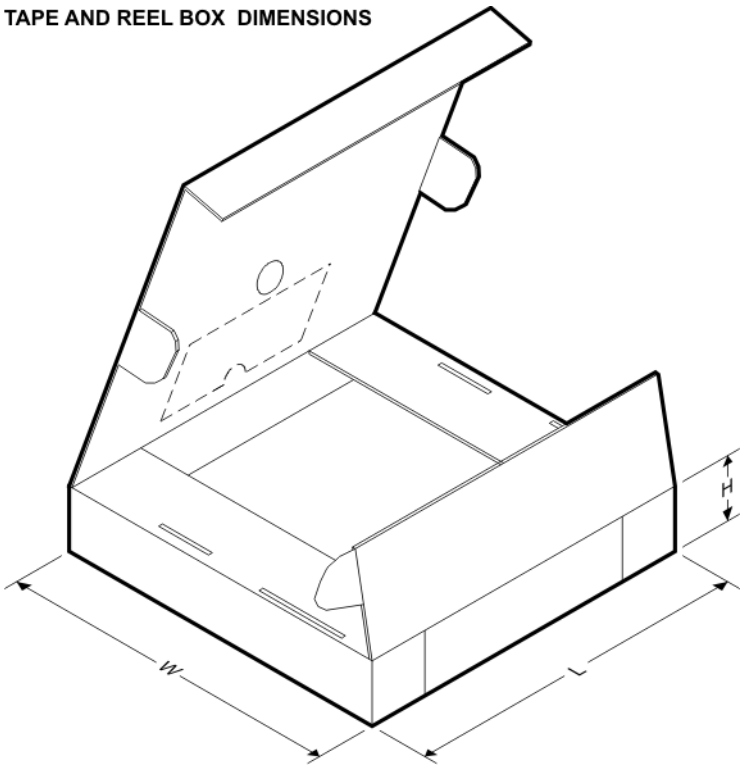
**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| BQ51010BYFPR | DSBGA | YFP | 28 | 3000 | 180.0 | 8.4 | 2.0 | 3.13 | 0.6 | 4.0 | 8.0 | Q1 |
| BQ51010BYFPT | DSBGA | YFP | 28 | 250 | 180.0 | 8.4 | 2.0 | 3.13 | 0.6 | 4.0 | 8.0 | Q1 |

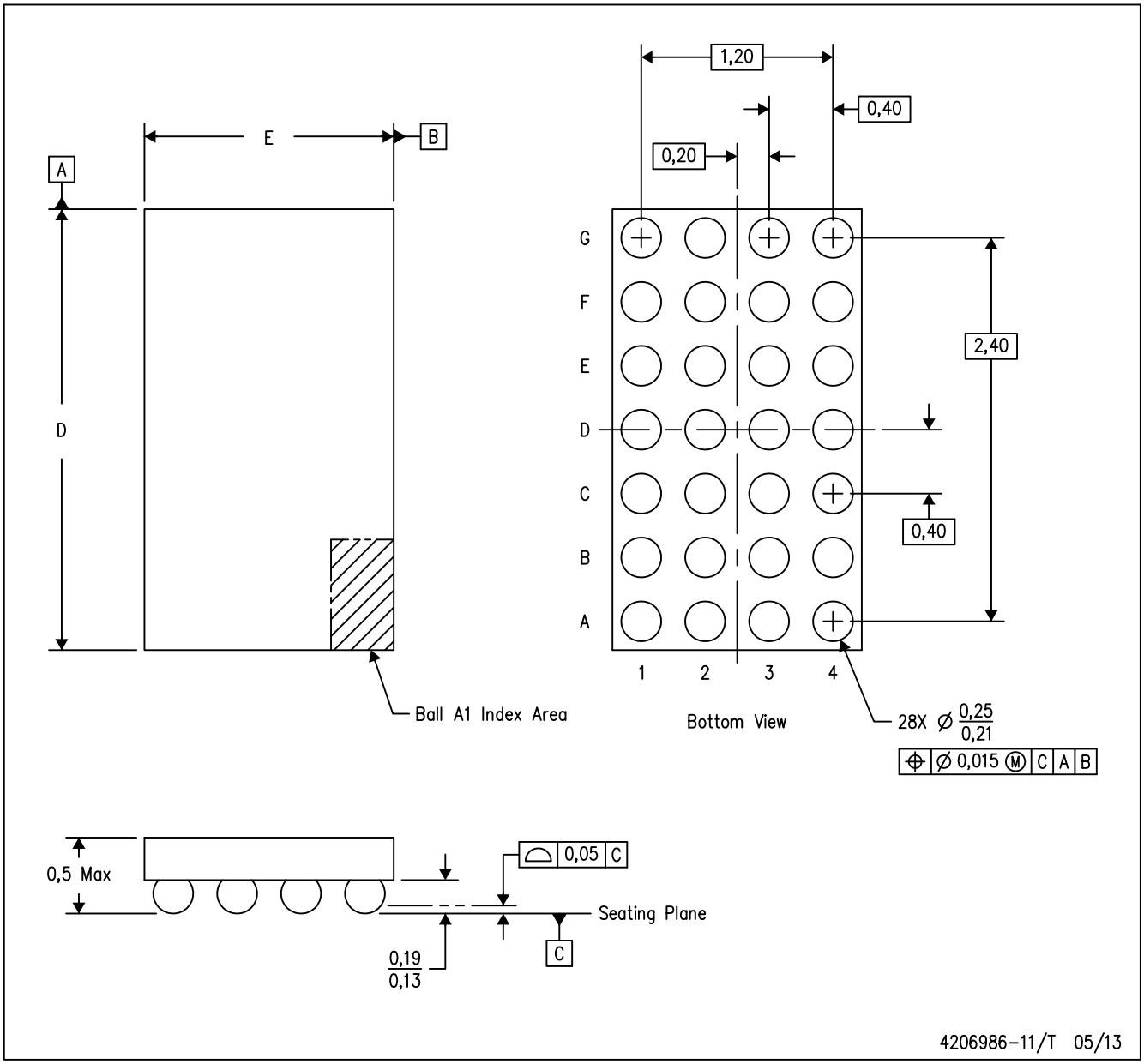
**TAPE AND REEL BOX DIMENSIONS**




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| BQ51010BYFPR | DSBGA | YFP | 28 | 3000 | 182.0 | 182.0 | 17.0 |
| BQ51010BYFPT | DSBGA | YFP | 28 | 250 | 182.0 | 182.0 | 17.0 |

YFP (R–XBGA–N28) DIE–SIZE BALL GRID ARRAY




NOTES: A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. NanoFree™ package configuration.

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