

GENERAL DESCRIPTION

The ME2303 is the P-Channel logic enhancement mode power field effect transistors are produced using high cell density , DMOS trench technology. This high density process is especially tailored to minimize on-state resistance. These devices are particularly suited for low voltage application such as cellular phone and notebook computer power management and other battery powered circuits where low in-line power loss are needed in a very small outline surface mount package.

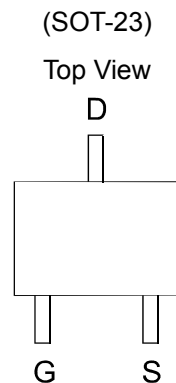
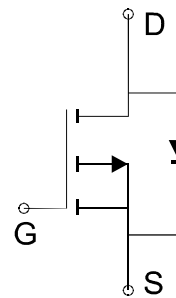
FEATURES

- $R_{DS(ON)} \leq 75m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 100m\Omega @ V_{GS} = -4.5V$
- Super high density cell design for extremely low $R_{DS(ON)}$

APPLICATIONS

- Power Management in Note book
- Portable Equipment
- Battery Powered System
- Load Switch
- DSC

PIN CONFIGURATION



Ordering Information: ME2303 (Pb-free)

ME2303-G (Green product)

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter		Symbol	Limit		Unit
Drain-Source Voltage		V _{DSS}	-30		V
Gate-Source Voltage		V _{GSS}	±20		V
Continuous Drain Current (T _j =150°C)*	T _A =25°C	I _D	-3.2		A
	T _A =70°C		-2.6		
Pulsed Drain Current		I _{DM}	-10		A
Maximum Power Dissipation	T _A =25°C	P _D	1.25		W
	T _A =70°C		0.8		
Operating Junction Temperature		T _J	-55 to 150		°C
Storage Temperature Range		T _{stg}	-55 to 150		°C
Thermal Resistance-Junction to Ambient*		R _{θJA}	Typical	Maximum	°C/W
			100	175	

* The device mounted on 1in² FR4 board with 2 oz copper



P-Channel Enhancement Mode Mosfet

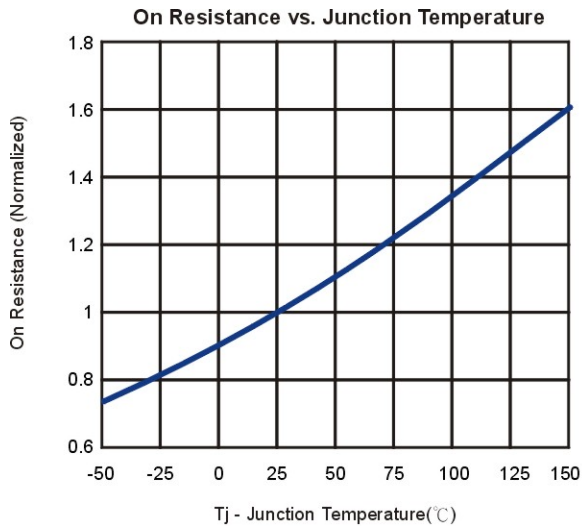
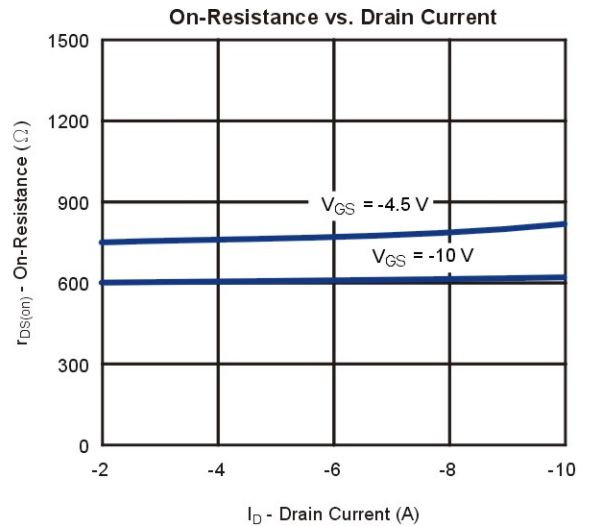
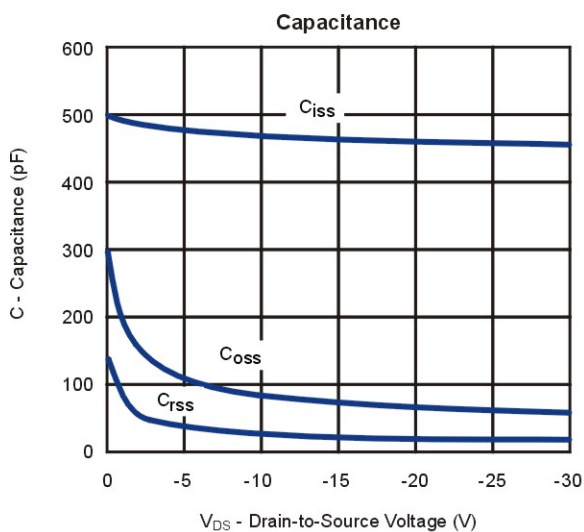
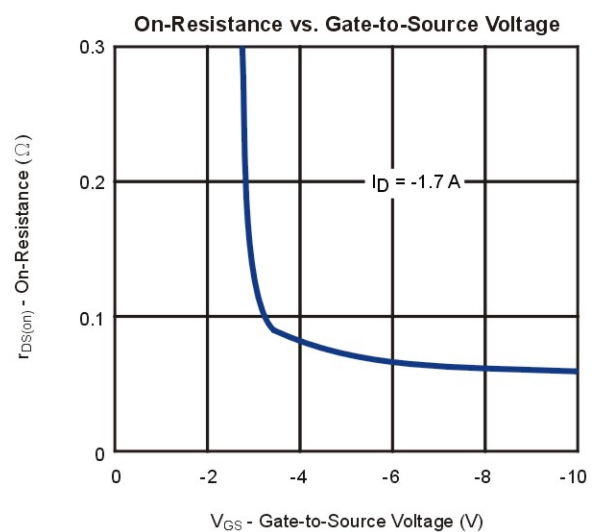
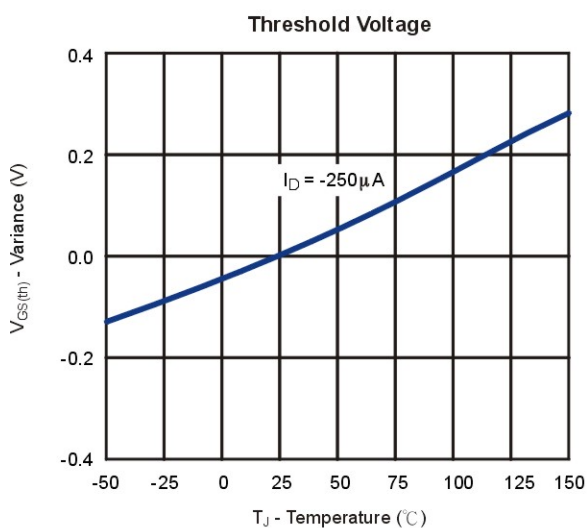
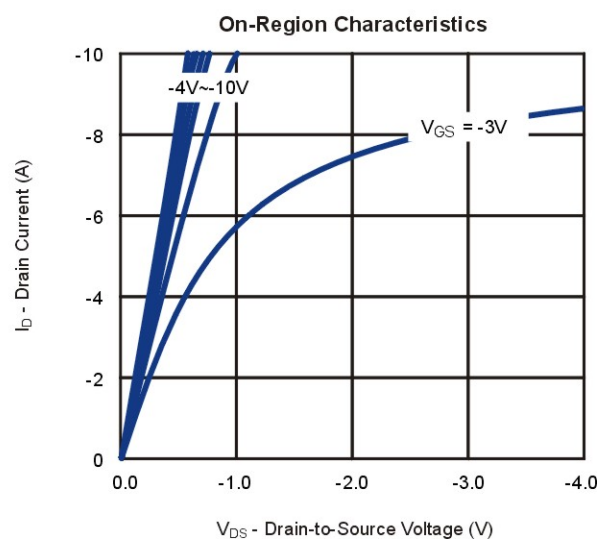
Electrical Characteristics (T_A=25°C Unless Otherwise Specified)

Symbol	Parameter	Limit	Min	Typ	Max	Unit
STATIC						
V _{(BR)DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =-250 μA	-30			V
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250 μA	-1		-3.0	V
I _{GSS}	Gate Leakage Current	V _{DS} =0V, V _{GS} =±20V			±100	nA
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-30V, V _{GS} =0V			-1	μA
R _{DS(ON)}	Drain-Source On-Resistance ^a	V _{GS} =-10V, I _D = -1.7A		60	75	mΩ
		V _{GS} =-4.5V, I _D = -1.3A		75	100	
V _{SD}	Diode Forward Voltage	I _S =-1.25A, V _{GS} =0V		-0.7	-1.4	V
DYNAMIC						
Q _g	Total Gate Charge	V _{DS} =-15V, V _{GS} =-10V, I _D =-1.7A		14.4		nC
Q _{gs}	Gate-Source Charge			2.7		
Q _{gd}	Gate-Drain Charge			3.6		
R _g	Gate resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz		4		Ω
C _{iss}	Input Capacitance	V _{DS} =-15V, V _{GS} =0V, f=1MHz		464		pF
C _{oss}	Output Capacitance			72		
C _{rss}	Reverse Transfer Capacitance			23		
t _{d(on)}	Turn-On Delay Time	V _{DS} =-15V, R _L =15Ω R _{GEN} =6Ω, V _{GS} =-10V		32		ns
t _r	Turn-On Rise Time			17		
t _{d(off)}	Turn-Off Delay Time			40		
t _f	Turn-Off Fall time			5		

Notes: a. Pulse test; pulse width ≤ 300us, duty cycle ≤ 2%



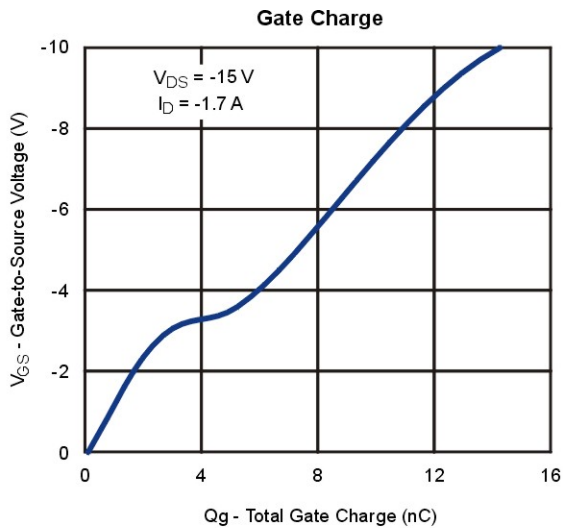
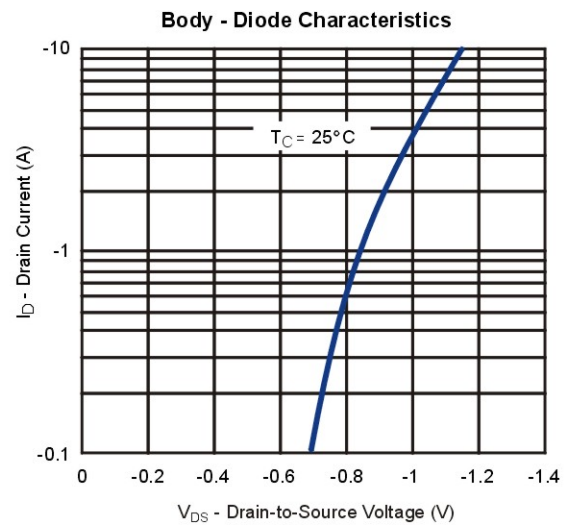
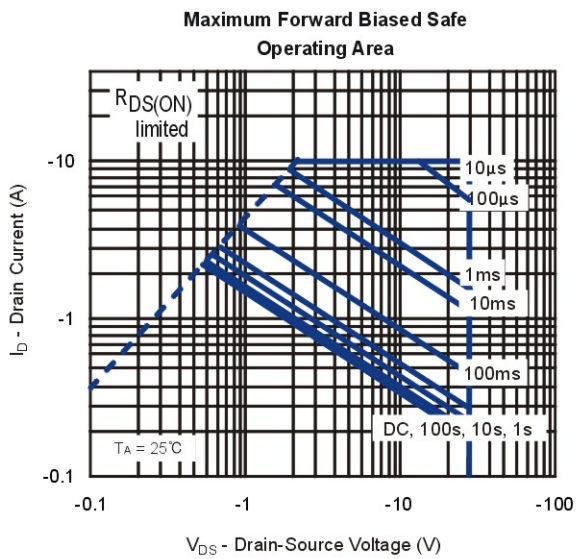
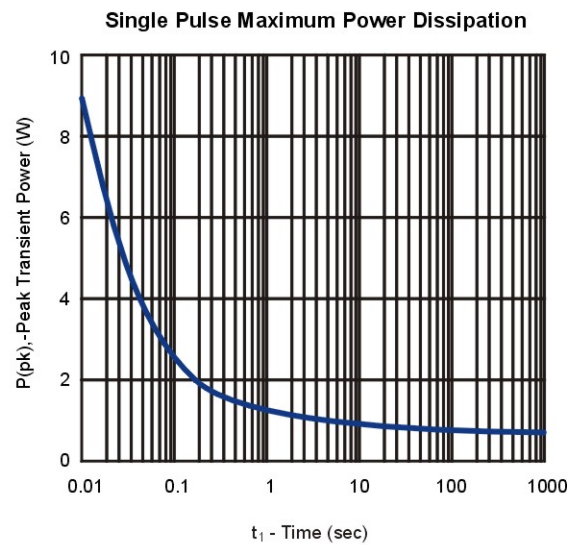
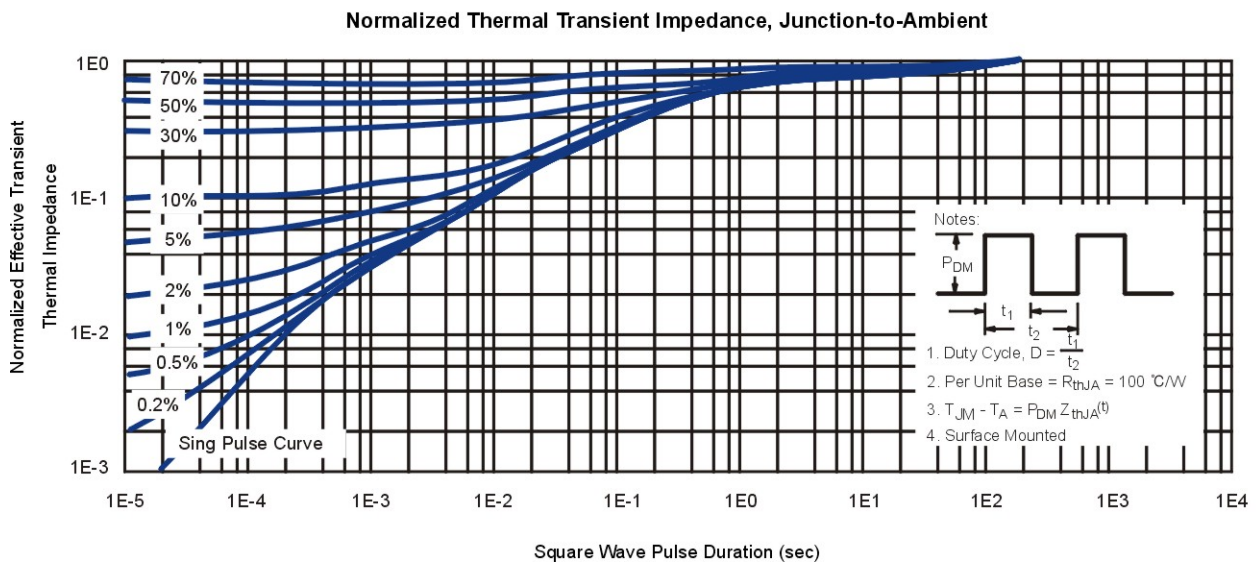
Typical Characteristics (T_J = 25°C Noted)



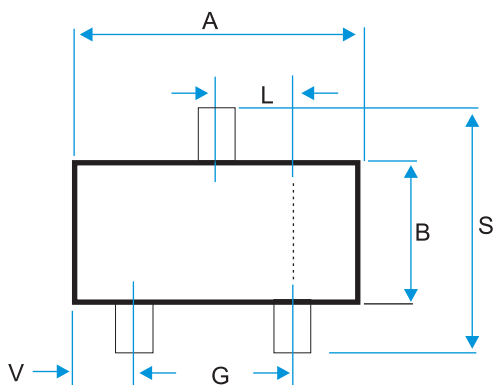


P-Channel Enhancement Mode Mosfet

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SOT-23 Package Outline



DIM	MILLIMETERS (mm)	
	MIN	MAX
A	2.800	3.00
B	1.200	1.70
C	0.900	1.30
D	0.350	0.50
G	1.780	2.04
H	0.010	0.15
J	0.085	0.20
K	0.300	0.65
L	0.890	1.02
S	2.100	3.00
V	0.450	0.60

