Brief Description

The ZSPM9015 is IDT's next-generation, fully optimized, ultra-compact, integrated MOSFET plus driver power stage solution for high-current, high-frequency, synchronous buck DC-DC applications. The ZSPM9015 integrates a driver IC, two power MOSFETs, and a bootstrap Schottky diode into a thermally enhanced, ultra-compact 6x6mm package.

With an integrated approach, the complete switching power stage is optimized with regard to driver and MOSFET dynamic performance, system inductance, and power MOSFET $R_{DS(ON)}$. The ZSPM9015 uses innovative high-performance MOSFET technology, which dramatically reduces switch ringing, eliminating the need for a snubber circuit in most buck converter applications.

A driver IC with reduced dead times and propagation delays further enhances the performance. A thermal warning function indicates if a potential over-temperature situation (>150°C) has occurred. An automatic thermal shutdown activates if an over-temperature condition (>180°C) is detected. The ZSPM9015 also incorporates a Zero Current Detection Mode (ZCD) for improved light-load efficiency and provides a tri-state 3.3V and 5V PWM input for compatibility with a wide range of PWM controllers.

The ZSPM9015 DrMOS is compatible with IDT's ZSPM1000, a leading-edge configurable digital power-management system controller designed for non-isolated point-of-load (POL) supplies.

Features

- High-current handling: up to 35A
- PWM input capable of 3.3V and 5V
- Optimized for switching frequencies up to 1MHz
- Zero-current detection and under-voltage lockout (UVLO)
- Thermal shutdown and warning flag for over-temperature conditions
- Driver output disable function (DISB# pin)
- Integrated Schottky diode technology in the low-side MOSFET
- Integrated bootstrap Schottky diode
- Adaptive gate drive timing for shoot-through protection

Benefits

- Improved efficiency with zero current detection
- Clean switching waveforms with minimal ringing
- Based on the Intel® 4.0 DrMOS standard
- 72% space-saving compared to conventional discrete solutions
- High current handling
- Optimized for use with IDT's ZSPM1000 true digital PWM controller

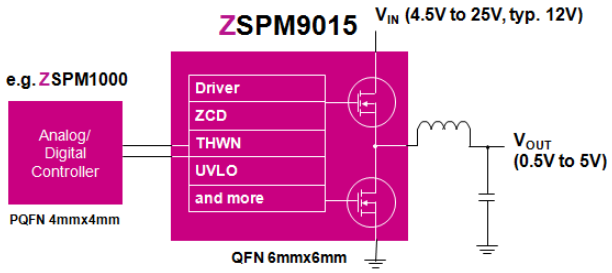
Available Support

- ZSPM8015-KIT: Evaluation Kit for ZSPM9015

Physical Characteristics

- Operation temperature: 0°C to +150°C
- V_{IN}: 4.5V to 25V (typical 12V)
- I_{OUT}: up to 35A
- Low-profile SMD package: 6mmx6mm QFN40
- IDT green packaging and RoHS compliant

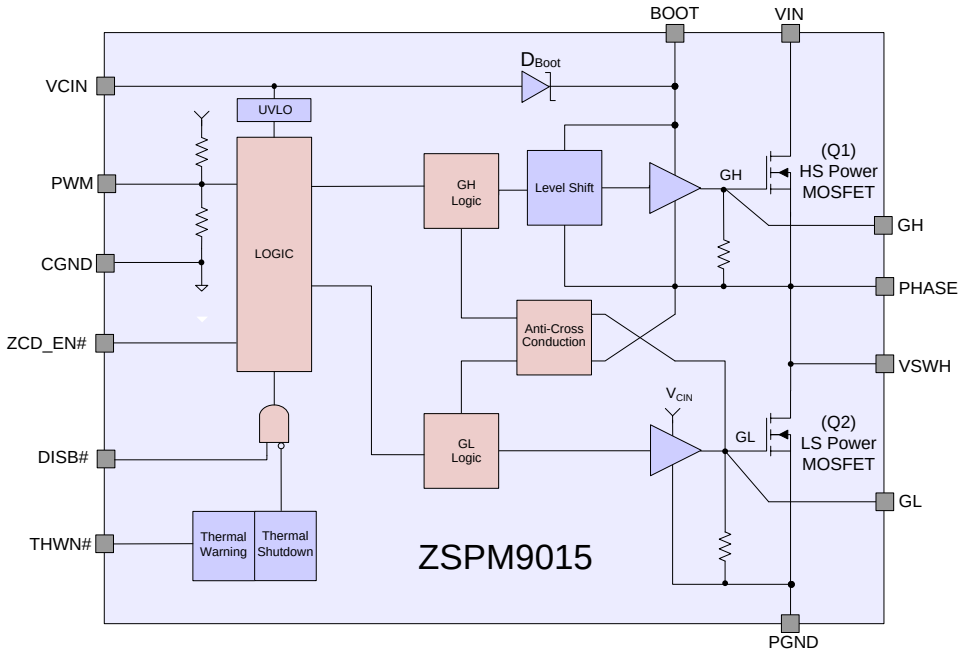
Typical Application



ZSPM9015 Block Diagram

Typical Applications

- High-performance gaming motherboards
- Compact blade servers, Vcore and non-Vcore DC-DC converters
- Desktop computers, Vcore and Non-Vcore DC-DC converters
- Workstations
- High-current DC-DC point-of-load converters
- Networking and telecom microprocessor voltage regulators
- Small form-factor voltage regulator modules



Ordering Information

Product Sales Code	Description	Package
ZSPM9015ZI1R	ZSPM9015 RoHS-Compliant QFN40 – Junction temperature range: 0°C to 150°C	Reel
ZSPM8015-KIT	Evaluation Kit for ZSPM9015	Kit

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

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1 IC Characteristics

1.1. Absolute Maximum Ratings

The absolute maximum ratings are stress ratings only. The device might not function or be operable above the recommended operating conditions. Stresses exceeding the absolute maximum ratings might also damage the device. In addition, extended exposure to stresses above the recommended operating conditions might affect device reliability. IDT does not recommend designing to the “Absolute Maximum Ratings.”

PARAMETER	SYMBOL	CONDITIONS	MIN		MAX	UNITS
Maximum Voltage – VCIN pin			-0.3		7.0	V
Maximum Voltage – PWM, DISB#, THWN# and ZCD_EN# pins			-0.3		6.5	V
Maximum Voltage – VIN and VSHW pins			-0.3		30	V
Maximum Voltage to BOOT pin – VSWH pin			-0.3		7.0	V
Maximum Voltage to BOOT pin – PGND pin					35.0	V
Maximum Voltage to BOOT pin – PGND pin		< 50ns			40.0	V
Maximum Sink Current – THWN# pin	$I_{THWN\#}$				30	mA
Maximum Output Current	I_{OUT}				35	A
Thermal Resistance, High-Side MOSFET	θ_{JPCB}			13		°C/W
Thermal Resistance, Low-Side MOSFET	θ_{JPCB}			5		°C/W
Operating Junction Temperature	T_j		0		+150	°C
Storage Temperature Range	T_{STOR}		-55		+150	°C
Electrostatic Discharge Protection	ESD	JEDEC JESD22-A114	HBM Class 1B			
Latch-Up Protection	LU	JEDEC JESD78	Class 1 Level A			
Moisture Sensitivity Level	MSL		3			

1.2. Recommended Operating Conditions

The “Recommended Operating Conditions” table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. IDT does not recommend exceeding them or designing to the “Absolute Maximum Ratings.”

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Control Input Voltage	V_{CIN}		4.5	5.0	5.5	V
Input Supply Voltage [1)]	V_{IN}		4.5	12.0	25	V

1) Operating at high V_{IN} can create excessive AC overshoots on the VSWH-to-GND and BOOT-to-GND nodes during MOSFET switching transients. For reliable DrMOS operation, VSWH-to-GND and BOOT-to-GND must remain at or below the "Absolute Maximum Ratings" shown in the table above. Refer to sections 3 and 5 of this datasheet for additional information.

1.3. Electrical Parameters

Note: Performance is guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J = T_A = 25°C$. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.

Typical values are V_{IN} = 12V, V_{CIN} = 5V, ambient temperature T_{AMB} = -10ºC to +100°C unless otherwise noted.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current						
VCIN Current (Normal Mode)		DISB# = 5V, PWM = OSC, FSW = 400kHz		14	20	mA
VCIN Current (Disabled Mode)		DISB# = GND		15	30	µA
Under-Voltage Lock-Out						
UVLO Threshold	UVLO	V_{CIN} rising	3.8	4.35	4.5	V
UVLO Hysteresis	$UVLO_{_Hyst}$		0.150	0.2	0.250	V
PWM Input						
PWM Input Resistance				63		kΩ
PWM Input Bias Voltage				1.7		V
PWM High-Level Voltage	V_{IH_PWM}		2.65			V
PWM Tri-state Level Voltage	V_{TRI_PWM}		1.4		2.0	V
PWM Low-Level Voltage	V_{IL_PWM}				0.7	V
Tri-state Shutoff Time	$t_{D_HOLD-OFF}$			250		ns

DISB# Input						
High-Level Input Voltage	$V_{IH_DISB\#}$		2.0			V
Low-Level Input Voltage	$V_{IL_DISB\#}$				0.8	V
Hysteresis				500		mV
Propagation Delay	t_{PD_DISB}			20	40	ns
Zero Current Detection						
High-Level Input Voltage	$V_{IH_ZCD_EN\#}$		2.0			V
Low-Level Input Voltage	$V_{IL_ZCD_EN\#}$				0.8	V
ZCD Threshold				-6		mV
ZCD Timer	t_{ZCD_DISB}			250		ns
Thermal Warning Flag						
Activation Temperature	T_{ACT}			150		°C
Reset Temperature	T_{RST}			135		°C
Thermal Shutdown						
Activation Temperature				180		ºC
Reset Temperature	T_{RST_SD}			135		°C
Boot Diode						
Forward-Voltage Drop	V_F	VCIN = 5V, forward bias current = 2mA	0.1	0.4	0.6	V

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1.4. Typical Performance Characteristics

Test conditions: V_{IN}=12V, V_{OUT}=1.0V, V_{CIN}=5V, L_{OUT}=250nH, T_{AMB}=25°C, and natural convection cooling, unless otherwise specified.

Figure 1.1 Power Loss vs. Output Current

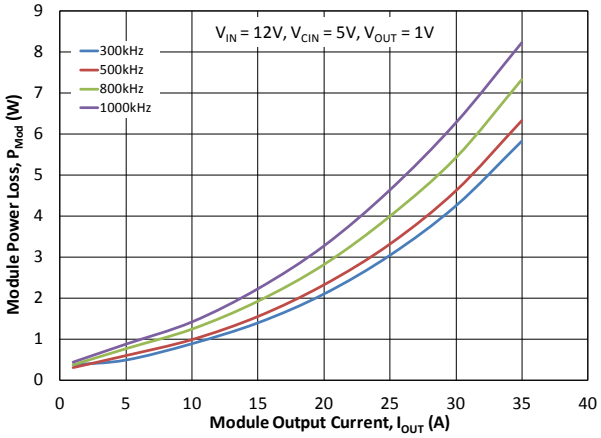


Figure 1.2 Efficiency vs. Output Current

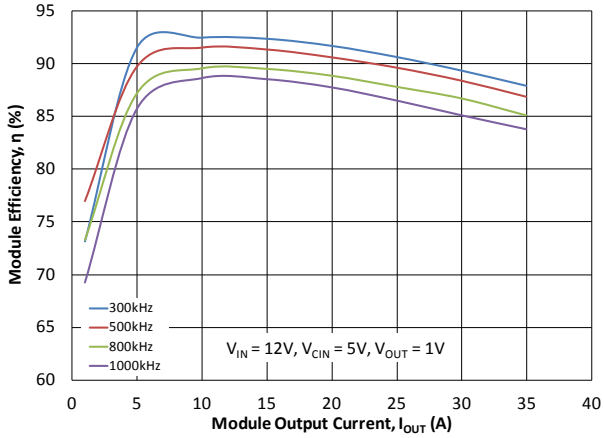


Figure 1.3 Power Loss vs. Output Current

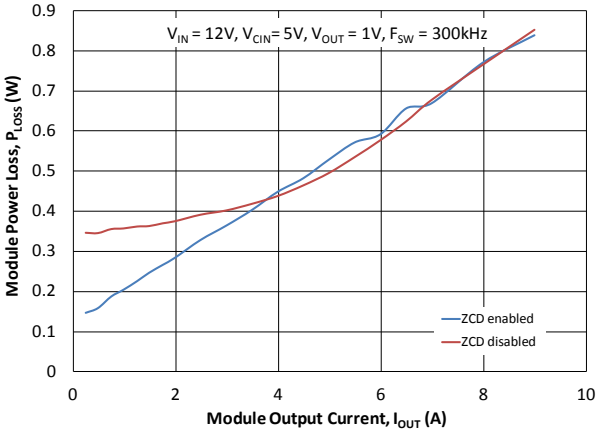


Figure 1.4 Efficiency vs. Output Current

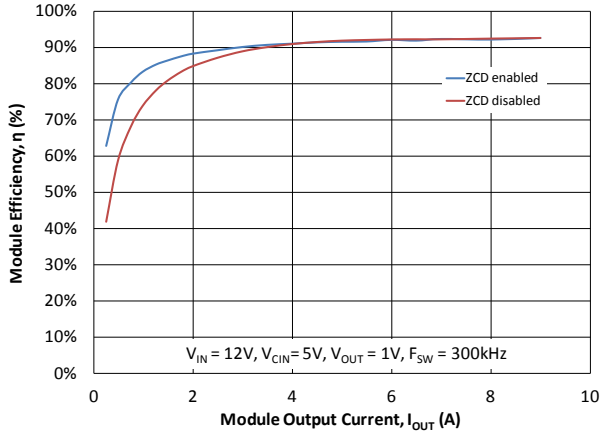


Figure 1.5 Power Loss vs. Switching Frequency

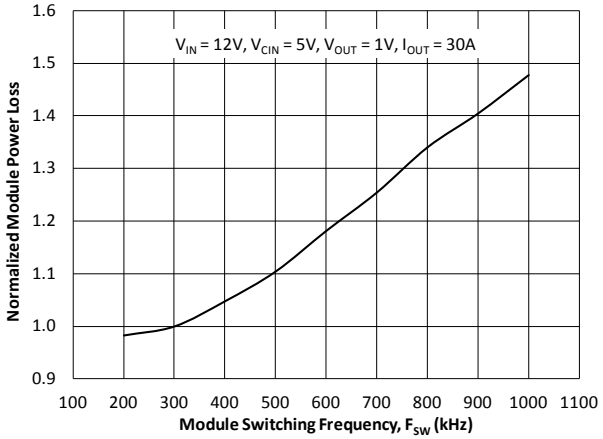


Figure 1.6 Power Loss vs. Input Voltage

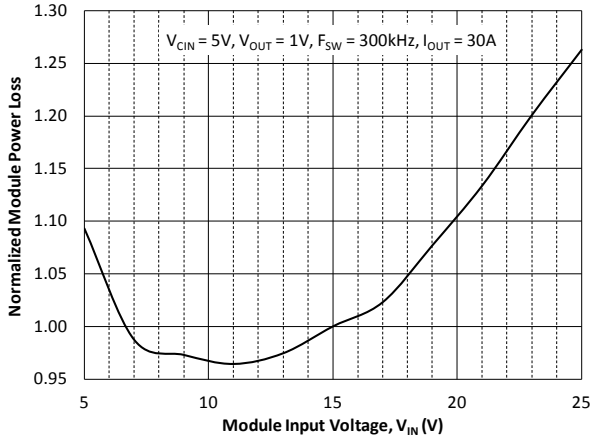


Figure 1.7 Power Loss vs. Control Input Voltage

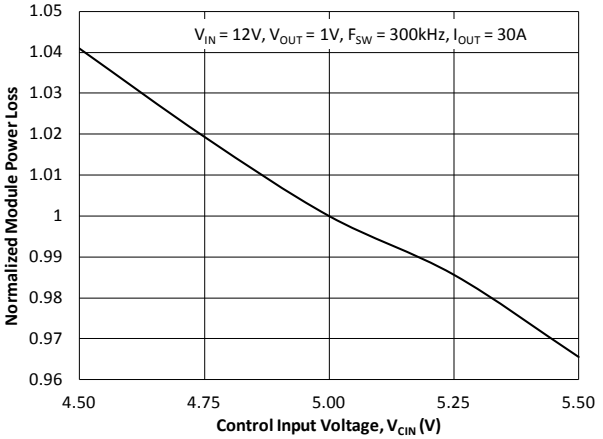


Figure 1.8 Power Loss vs. Output Voltage

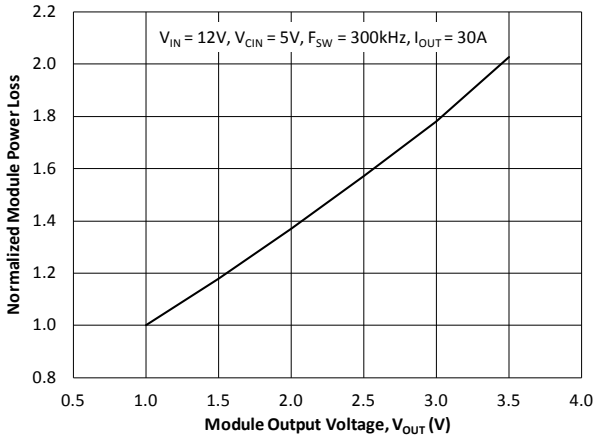


Figure 1.9 Control Input Current vs. Switching Frequency

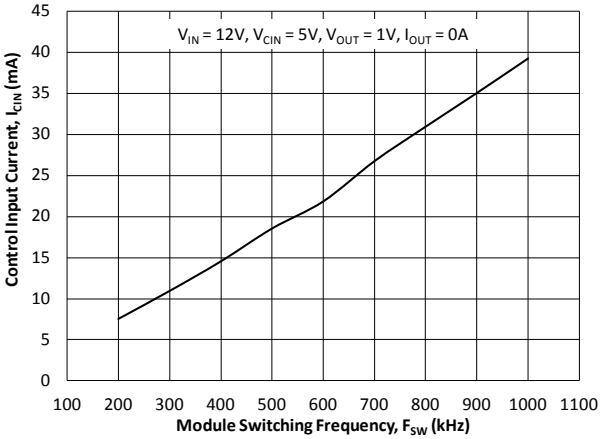
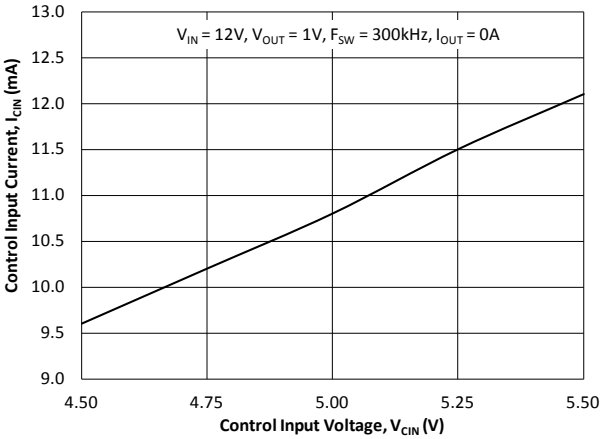


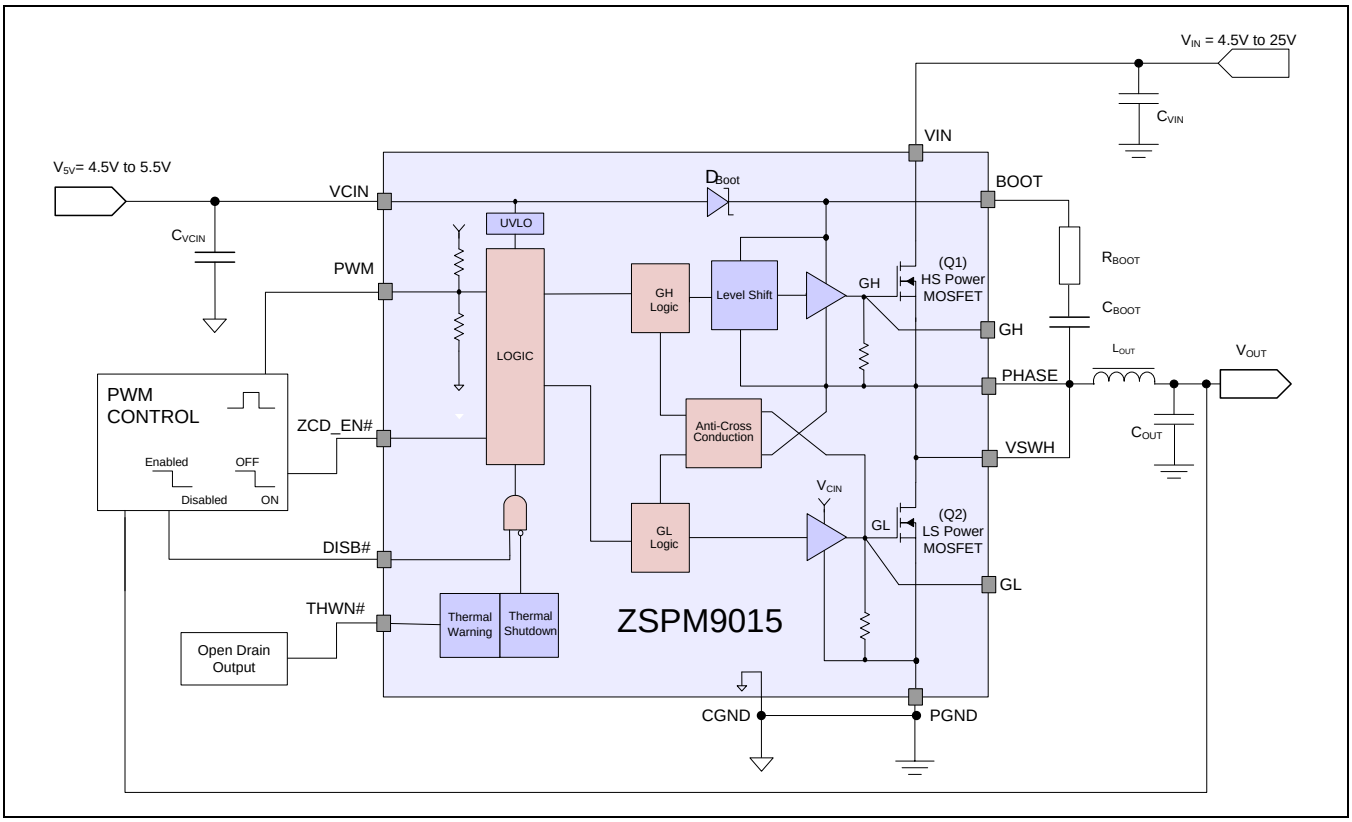
Figure 1.10 Control Input Current vs. Control Input Voltage



2 Functional Description

The ZSPM9015 is a driver-plus-MOSFET module optimized for the synchronous buck converter topology. A single PWM input signal is all that is required to properly drive the high-side and the low-side MOSFETs. It is capable of driving speeds up to 1MHz.

Figure 2.1 Block Diagram and Typical Application Circuit with PWM Control



2.1. VCIN and Disable (DISB#)

The VCIN pin is monitored by the under-voltage lockout (UVLO) circuit. When V_{CIN} rises above ~4.35V, the driver is enabled. When V_{CIN} falls below ~4.1V, the driver is disabled (GH, GL= 0; see Table 2.1 and section 4.2).

The driver can also be disabled by pulling the DISB# pin LOW (DISB# < $V_{IL_DISB\#}$; see section 1.3), which holds both GL and GH LOW regardless of the PWM input state. The driver can be enabled by raising the DISB# pin voltage HIGH (DISB# > $V_{IH_DISB\#}$). It is advisable not to leave the DISB# floating.

Table 2.1 UVLO and Disable Logic

UVLO Circuit	DISB#	Driver State
ON	X	Disabled (GH=0, GL=0)
OFF	Low	Disabled (GH=0, GL=0)
OFF	High	Enabled
OFF	Open	Disabled (GH=0, GL=0)

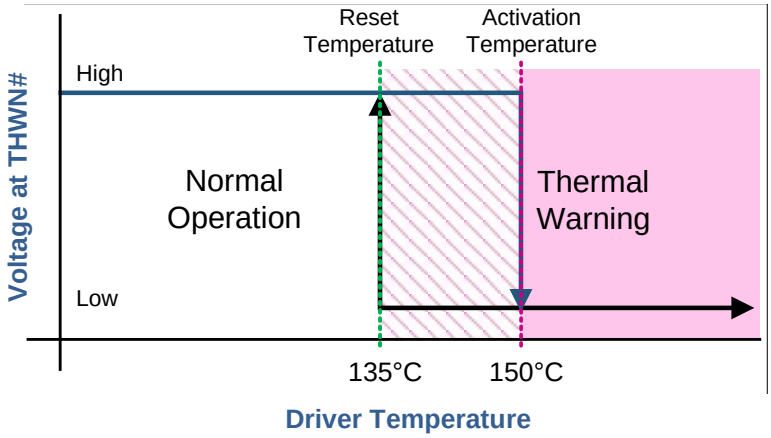
ON = ULVO circuit is active and the driver output is disabled. The output will not respond to the PWM input under any condition.

Off = ULVO is non-active and the output operates normally. The output will respond to the PWM input provided the conditions are correct; e.g., not in thermal shutdown.

2.2. Thermal Warning Flag (THWN#) and Thermal Shutdown

The ZSPM9015 provides a thermal warning flag (THWN#) to indicate over-temperature conditions. The thermal warning flag uses an open-drain output that pulls to CGND when the activation temperature (150°C) is reached. The THWN# output returns to the high-impedance state once the temperature falls to the reset temperature (135°C). For use, the THWN# output requires a pull-up resistor, which can be connected to VCIN.

Figure 2.2 Thermal Warning Flag (THWN#) Operation



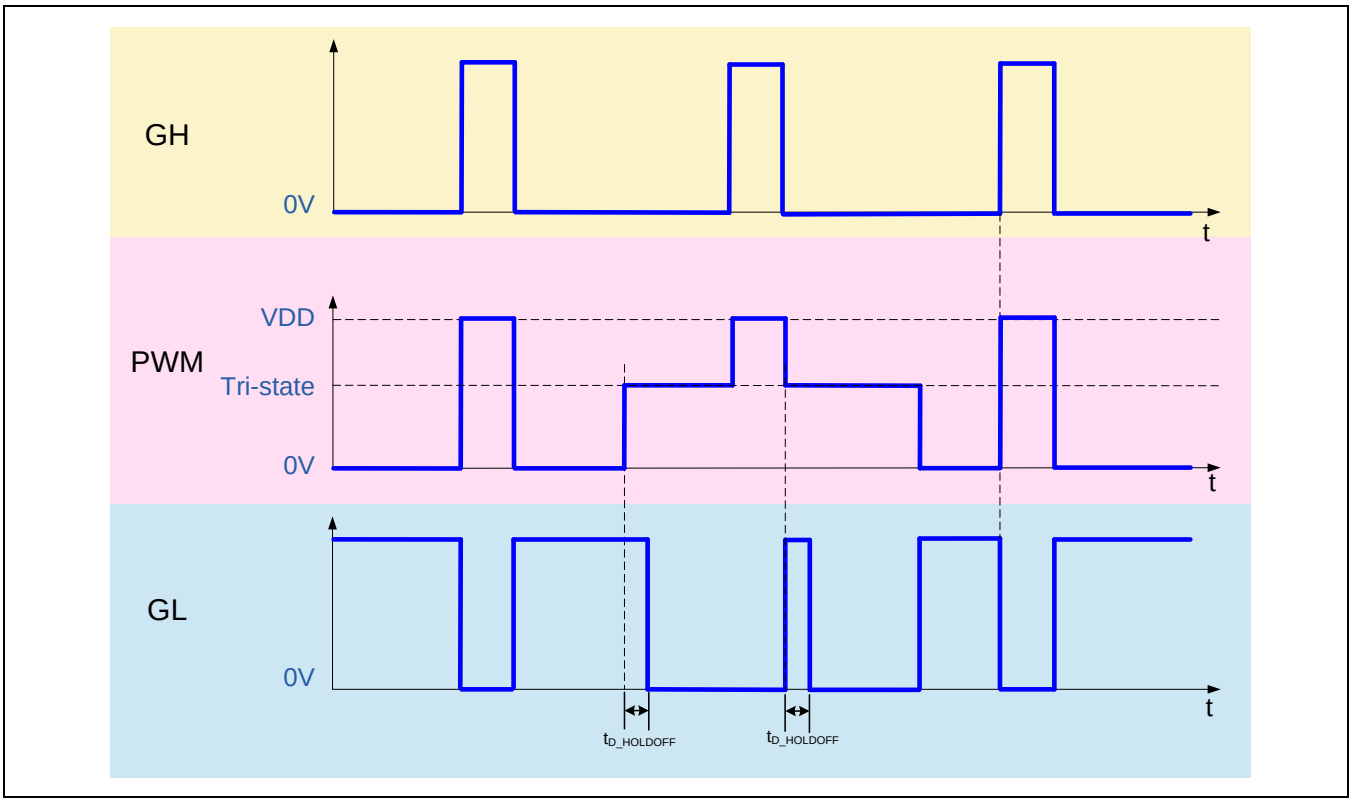
If the temperature exceeds 180ºC then the part will enter thermal shutdown and turn off both MOSFETs. Upon the temperature falling below 155ºC, the part will resume operation.

2.3. Tri-state PWM Input

The ZSPM9015 incorporates a tri-state PWM input gate drive design. The tri-state gate drive has both logic HIGH and LOW levels, with a tri-state shutdown voltage window. When the PWM input signal enters and remains within the tri-state voltage window for a defined hold-off time ($t_{D_HOLD-OFF}$), both GL and GH are pulled LOW. This feature enables the gate drive to shut down both the high and low side MOSFETs using only one control signal. For example, this can be used for phase shedding in multi-phase voltage regulators.

When exiting a valid tri-state condition, the ZSPM9015 follows the PWM input command. If the PWM input goes from tri-state to LOW, the low-side MOSFET is turned on. If the PWM input goes from tri-state to HIGH, the high-side MOSFET is turned on, as illustrated in Figure 2.3. The ZSPM9015's design allows for short propagation delays when exiting the tri-state window.

Figure 2.3 PWM and Tri-state Timing Diagram



2.4. Adaptive Gate Drive Circuit

The low-side driver (GL) is designed to drive a ground-referenced low $R_{DS(ON)}$ N-channel MOSFET. The bias voltage for GL is internally connected between VCIN and PGND. The GL output follows the inverse of the PWM input with the exception that it is held LOW under any of the following conditions: a) the driver is disabled (DISB#=0V); b) the PWM signal is held within the tri-state window for longer than the tri-state hold-off time, $t_{D_HOLDOFF}$; or c) specific circuit conditions that occur while in ZCD Mode (see section 2.5 for further details).

The high-side driver (GH) is designed to drive a floating N-channel MOSFET. The bias voltage for the high-side driver is developed by a bootstrap supply circuit referenced to the switch node (VSWH) pin. This circuit consists of an internal Schottky diode, an external bootstrap capacitor (C_{BOOT}), and the optional R_{BOOT} if used. During startup, the VSWH pin is held at PGND, allowing C_{BOOT} (see section 3.2) to charge to V_{CIN} through the internal diode. When the PWM input goes HIGH, GH begins to charge the gate of Q1, the high-side MOSFET. During this transition, the charge is removed from C_{BOOT} and delivered to the gate of Q1. As Q1 turns on, V_{SWH} rises to V_{IN}, forcing the BOOT pin to V_{IN} + V_{BOOT}, which provides sufficient V_{GS} enhancement for Q1.

To complete the switching cycle, Q1 is turned off by pulling GH to V_{SWH}. C_{BOOT} is then recharged to V_{CIN} when V_{SWH} falls to PGND. The GH output follows the PWM input except that it is held LOW when either a) the driver is disabled (DISB#=0V) or b) the PWM signal is held within the tri-state window for longer than the tri-state hold-off time, $t_{D_HOLDOFF}$.

The ZSPM9015 design ensures minimum MOSFET dead time while eliminating potential shoot-through (cross-conduction) currents. It achieves this by monitoring the state of the MOSFETs and adjusts the gate drive adaptively to prevent simultaneous conduction.

When the PWM input goes HIGH, the gate of the low side MOSFET (GL pin) will go low after a propagation delay. The time it takes for the low side MOSFET to turn off is dependent on the gate charge on the low side MOSFET gate. The ZSPM9015 monitors the gate voltage of both MOSFETs to determine the conduction status of the MOSFETs. Once the low-side MOSFET is turned off, an internal timer will delay the turn on of the high-side MOSFET. Similarly, when the PWM input pin goes low, the converse occurs.

2.5. Zero Current Detection Mode (ZCD_EN#)

Zero Current Detection (ZCD) Mode allows higher converter efficiency under light-load conditions.

When the ZCD feature is disabled (ZCD_EN# is high), the ZSPM9015 will operate in the normal PWM Mode in which the synchronous buck converter works in Synchronous Mode.

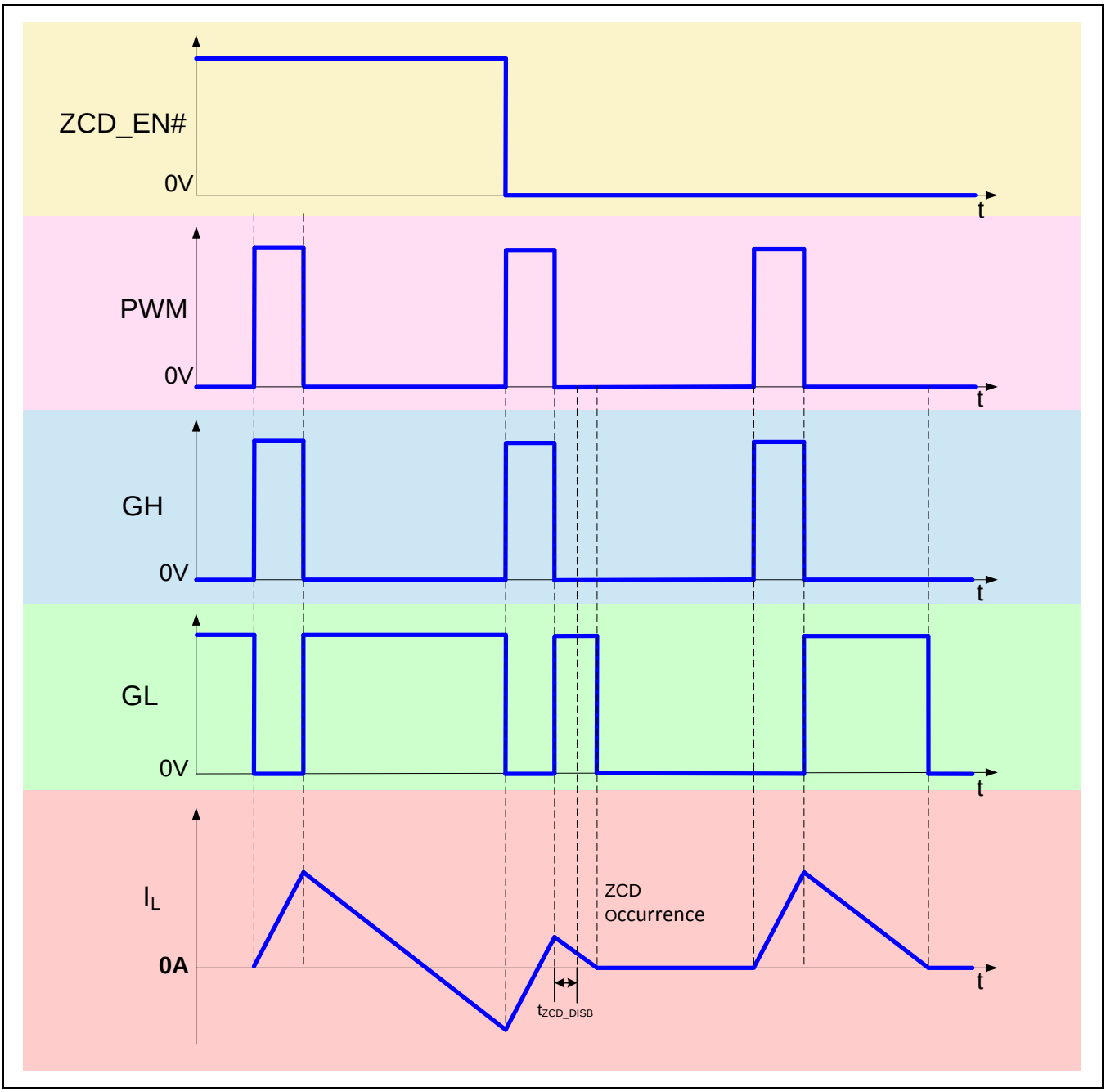
If the ZCD_EN# is set low, then the ZSPM9015 will operate in the ZCD Mode, and in this mode, the ZSPM9015 can prevent discharging of the output capacitors as the filter inductor current attempts reverse current flow. If the PWM goes high, GH will go high after the non-overlap delay time. During this period, the ZCD timer is inactive and thus reset. If the PWM goes low, GL will go high after the non-overlap delay time and stay high for the duration of the ZCD timer (t_{ZCD_DISB}); see section 1.3. During this period ZCD operation is disabled. Once this timer has expired, VSWH will be monitored for zero current detection and GL will go low if a zero-current condition is detected. The ZCD threshold (see section 1.3) on VSWH to determine zero current undergoes an auto-calibration cycle every time DISB# is brought from LOW to HIGH. This auto-calibration cycle takes 25µs to complete.

Table 2.2 ZCD Mode Operation (ZCD_EN# = LOW) and Switch States

PWM Input	ZCD Status	GH	GL
High	ZCD timer is reset (inactive)	High	Low
Low	Positive inductor current	Low	High
Low	Zero inductor current	Low	Low
Tri-state	X	Low	Low

Figure 2.4 ZCD_EN# Timing Diagram

See Figure 2.3 for the definitions of the timing parameters.



3 Application Design

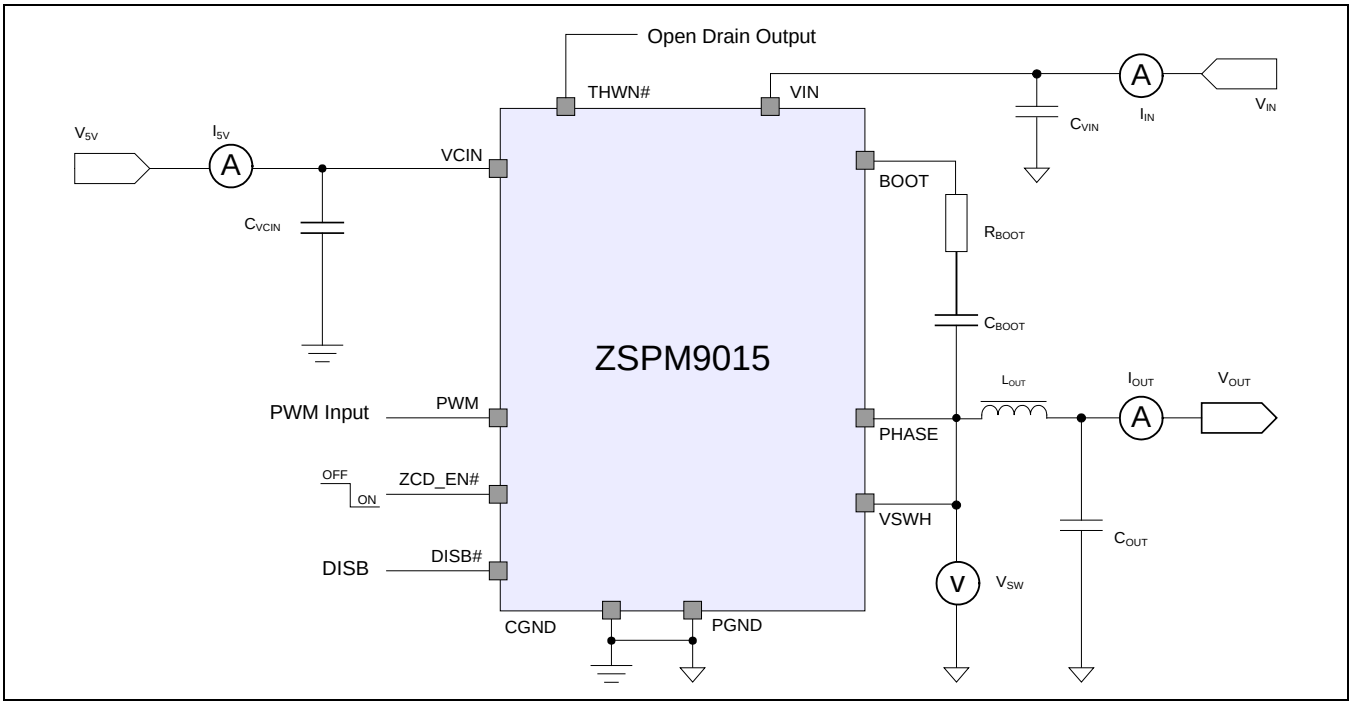
3.1. Supply Capacitor Selection

For the supply input (VCIN), a local ceramic bypass capacitor (C_{CVIN}) is required to reduce noise and is used to supply the peak transient currents during gate drive switching action. Recommendation: use at a 1µF to 4.7µF capacitor with an X7R or X5R dielectric. Keep this capacitor close to the VCIN pin, and connect it to the CGND ground plane with vias.

3.2. Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}), as shown in Figure 3.1. A bootstrap capacitance of 100nF using a X7R or X5R capacitor is typically adequate. A series bootstrap resistor might be needed for specific applications to improve switching noise immunity. The boot resistor might be required when operating with V_{IN} above 15V, and it is effective at controlling the high-side MOSFET turn-on slew rate and V_{SWH} overshoot. Typically, R_{BOOT} values from 0.5Ω to 3.0Ω are effective in reducing V_{SWH} overshoot.

Figure 3.1 Power Loss Measurement Block Diagram



3.3. Power Loss and Efficiency Testing Procedures

The circuit in Figure 3.1 has been used to measure power losses in the following example. The efficiency has been calculated based on the equations (1) through (7).

Power loss calculations in Watts:

$$P_{IN} = (V_{IN} * I_{IN}) + (V_{5V} * I_{5V}) \quad \textbf{(1)}$$

$$P_{SW} = (V_{SW} * I_{OUT}) \quad \textbf{(2)}$$

$$P_{OUT} = (V_{OUT} * I_{OUT}) \quad \textbf{(3)}$$

$$P_{LOSS_MODULE} = (P_{IN} - P_{SW}) \quad \textbf{(4)}$$

$$P_{LOSS_BOARD} = (P_{IN} - P_{OUT}) \quad \textbf{(5)}$$

Efficiency calculations:

$$EFF_{MODULE} = \left(100 * \frac{P_{SW}}{P_{IN}}\right)\% \quad \textbf{(6)}$$

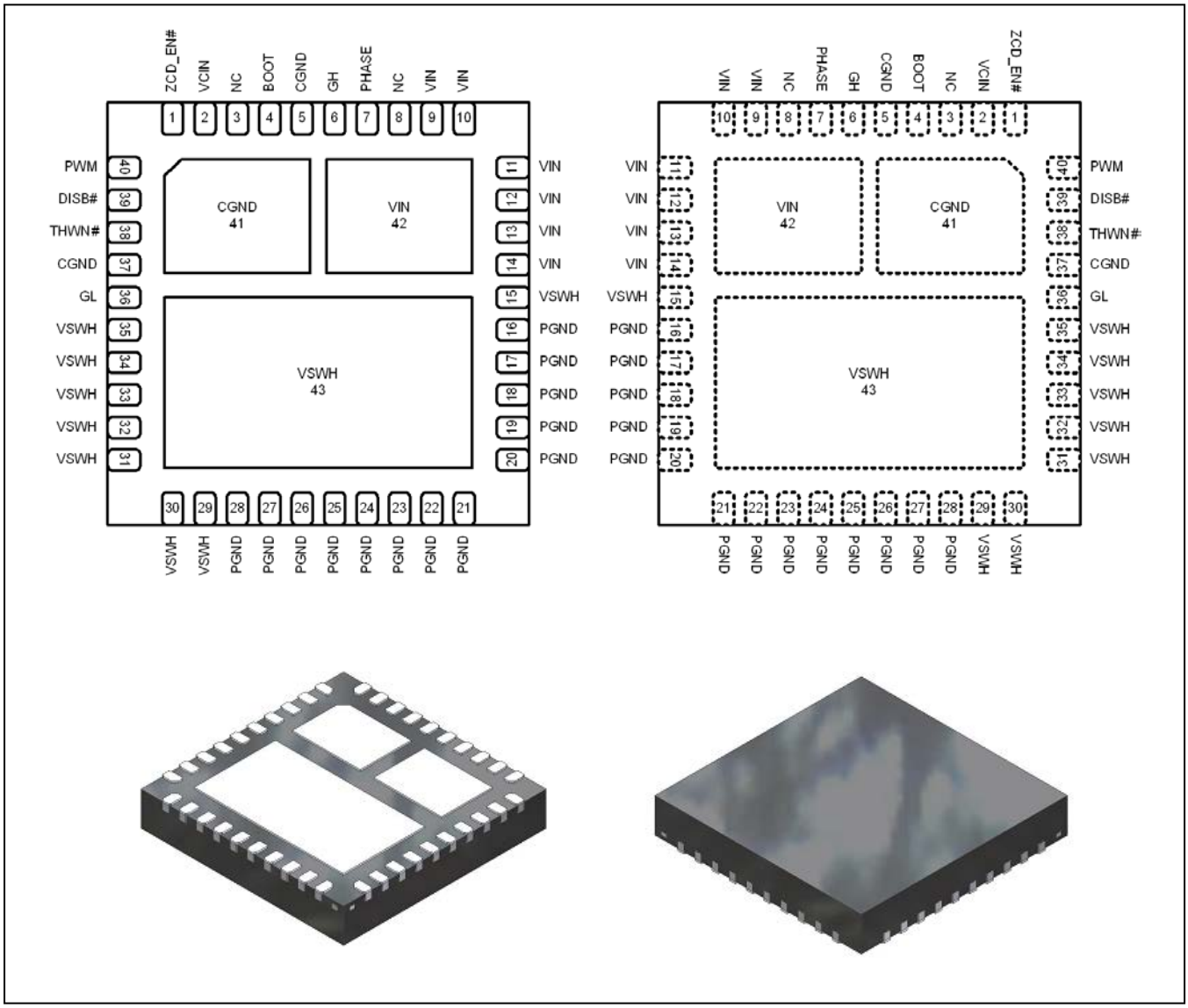
$$EFF_{BOARD} = \left(100 * \frac{P_{OUT}}{P_{IN}}\right)\% \quad \textbf{(7)}$$

4 Pin Configuration and Package

4.1. Available Packages

The ZSPM9015 is available in a 40-lead clip-bond QFN package. The pin-out is shown in Figure 4.1. See Figure 4.2 for the mechanical drawing of the package.

Figure 4.1 Pin-out PQFN40 Package

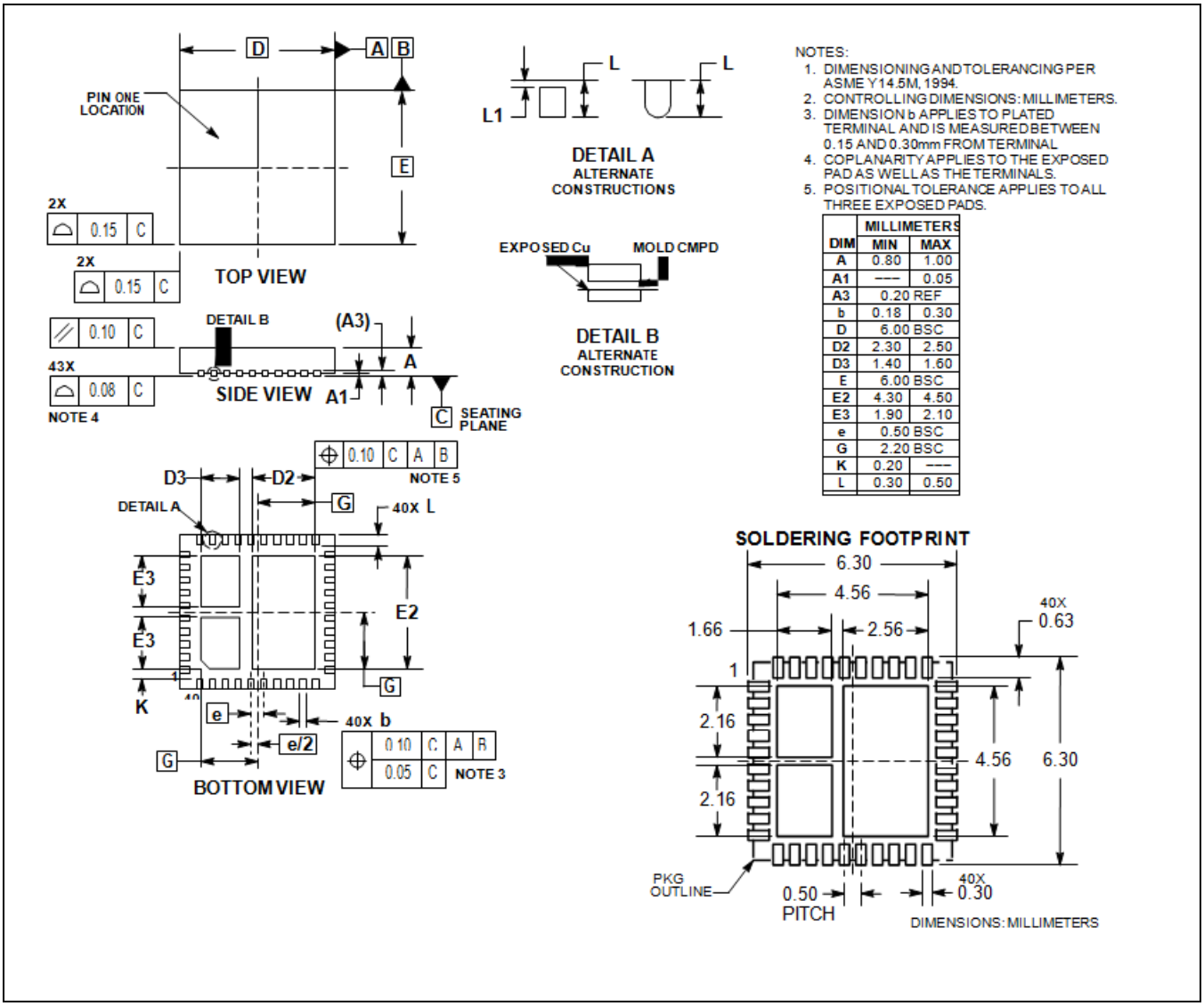


4.2. Pin Description

Pin	Name	Description
1	ZCD_EN#	Enable Zero Current Detection Mode. Advisable not to leave floating.
2	VCIN	IC bias supply. A 1µF (minimum) ceramic capacitor is recommended from this pin to CGND.
3	NC	No connection.
4	BOOT	Bootstrap supply input. Provides voltage supply to the high-side MOSFET driver. Connect a bootstrap capacitor from this pin to PHASE.
5, 37 & pad 41	CGND	IC ground. Ground return for ZSPM9015.
6	GH	Gate high. For manufacturing test only. This pin must float: it must not be connected.
7	PHASE	Switch node pin for bootstrap capacitor routing; electrically shorted to VSWH pin.
8	NC	No connection.
9 - 14 & pad 42	VIN	Input power voltage (output stage supply voltage).
15, 29 - 35 & pad 43	VSWH	Switch node. Provides return for high-side bootstrapped driver and acts as a sense point for the adaptive shoot-through protection.
16 – 28	PGND	Power ground (output stage ground). Source pin of the low-side MOSFET.
36	GL	Gate low. For manufacturing test only. This pin must float. It must not be connected.
38	THWN#	Thermal warning flag. When temperature exceeds the trip limit, the output is pulled LOW. This pin has a maximum current capability of 30mA.
39	DISB#	Output disable. When LOW, this pin disables the power MOSFET switching (GH and GL are held LOW). Advisable not to leave floating.
40	PWM	PWM signal input. This pin accepts a tri-state 3.3V or 5V PWM signal from the controller.

4.3. Package Dimensions

Figure 4.2 QFN40 Physical Dimensions and Recommended Footprint



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30mm FROM TERMINAL
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. POSITIONAL TOLERANCE APPLIES TO ALL THREE EXPOSED PADS.

DIM	MILLIMETERS MIN	MAX
A	0.80	1.00
A1	----	0.05
A3	0.20 REF	
b	0.18	0.30
D	6.00 BSC	
D2	2.30	2.50
D3	1.40	1.60
E	6.00 BSC	
E2	4.30	4.50
E3	1.90	2.10
e	0.50 BSC	
G	2.20 BSC	
K	0.20	----
L	0.30	0.50

5 Circuit Board Layout Considerations

Figure 5.1 provides an example of a proper layout for the ZSPM9015 and critical components. All of the high-current paths, such as the V_{IN}, V_{SWH}, V_{OUT}, and GND copper traces, should be short and wide for low inductance and resistance. This technique achieves a more stable and evenly distributed current flow, along with enhanced heat radiation and system performance.

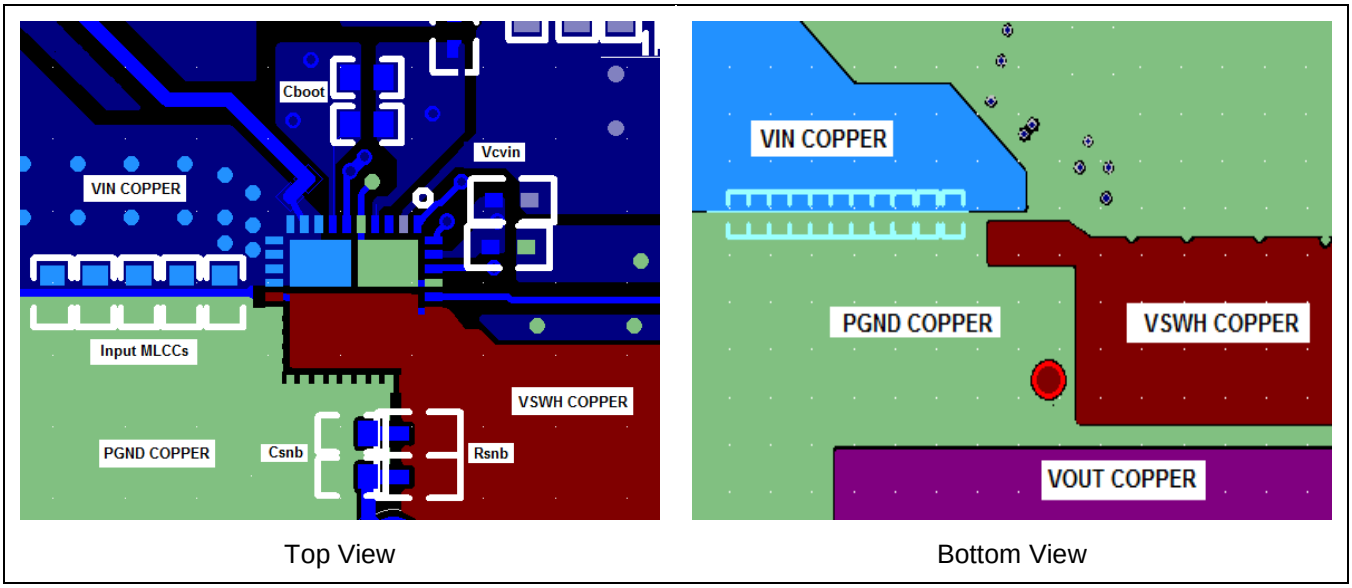
The following guidelines are recommendations for the printed circuit board (PCB) designer:

1. Input ceramic bypass capacitors must be placed close to the VIN and PGND pins. This helps reduce the high-current power loop inductance and the input current ripple induced by the power MOSFET switching operation.
2. The V_{SWH} copper trace serves two purposes. In addition to being the high-frequency current path from the DrMOS package to the output inductor, it also serves as a heat sink for the low-side MOSFET in the DrMOS package. The trace should be short and wide enough to present a low-impedance path for the high-frequency, high-current flow between the DrMOS and inductor to minimize losses and DrMOS temperature rise. Note that the VSWH node is a high-voltage and high-frequency switching node with a high noise potential. Care should be taken to minimize coupling to adjacent traces. Since this copper trace also acts as a heat sink for the lower MOSFET, the designer must balance using the largest area possible to improve DrMOS cooling with maintaining acceptable noise emission.
3. Locate the output inductor close to the ZSPM9015 to minimize the power loss due to the VSWH copper trace. Care should also be taken so that the inductor dissipation does not heat the DrMOS.
4. The power MOSFETs used in the output stage are effective for minimizing ringing due to fast switching. In most cases, no VSWH snubber is required. If a snubber is used, it should be placed close to the VSWH and PGND pins. The resistor and capacitor must be the proper size for the power dissipation.
5. VCIN and BOOT capacitors should be placed as close as possible the VCIN-to-CGND and BOOT-to-PHASE pin pairs to ensure clean and stable power. Routing width and length should be considered as well.
6. The layout should include a placeholder to insert a small-value series boot resistor (R_{BOOT}) between the boot capacitor (C_{BOOT}) and the ZSPM9015 BOOT pin. The boot-loop size, including R_{BOOT} and C_{BOOT}, should be as small as possible. The boot resistor may be required when operating with V_{IN} above 15V. The boot resistor is effective for controlling the high-side MOSFET turn-on slew rate and V_{SWH} overshoot. R_{BOOT} can improve the operating noise margin in synchronous buck designs that might have noise issues due to ground bounce or high positive and negative V_{SWH} ringing. However, inserting a boot resistance lowers the DrMOS efficiency. Efficiency versus noise trade-offs must be considered. R_{BOOT} values from 0.5Ω to 3.0Ω are typically effective in reducing V_{SWH} overshoot.
7. The VIN and PGND pins handle large current transients with frequency components greater than 100MHz. If possible, these pins should be connected directly to the VIN and board GND planes. Important: the use of thermal relief traces in series with these pins is discouraged since this adds inductance to the power path. Added inductance in series with the VIN or PGND pin degrades system noise immunity by increasing positive and negative V_{SWH} ringing.
8. Connect the CGND pad and PGND pins to the GND plane copper with multiple vias for stable grounding. Poor grounding can create a noise transient offset voltage level between CGND and PGND. This could lead to faulty operation of the gate driver and MOSFETs.

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9. Ringing at the BOOT pin is most effectively controlled by close placement of the boot capacitor. Do not add an additional BOOT to PGND capacitor; this could lead to excess current flow through the BOOT diode.
10. It is advisable not to float the ZCD_EN# and DISB# pins.
11. Use multiple vias on each copper area to interconnect top, inner, and bottom layers to help distribute current flow and heat conduction. Vias should be relatively large and of reasonably low inductance. Critical high-frequency components, such as $_{RBOOT}$, $_{CBOOT}$, RC snubber, and bypass capacitors, should be located as close to the respective ZSPM9015 module pins as possible on the top layer of the PCB. If this is not feasible, they can be connected from the backside through a network of low-inductance vias.

Figure 5.1 PCB Layout Example



Top View Bottom View

6 Glossary

Term	Description
CCM	Continuous Conduction Mode
DCM	Discontinuous Conduction Mode
DISB	Driver Disable
HS	High Side
LS	Low Side
THWN#	Thermal Warning Flag
ZCD	Zero Current Detection
IL	Inductor Current

7 Ordering Information

Product Sales Code	Description	Package
ZSPM9015ZI1R	ZSPM9015 RoHS-Compliant QFN40 – Junction temperature range: 0°C to 150°C	Reel
ZSPM8015-KIT	Evaluation Kit for ZSPM9015	Kit

8 Related Documents

Document
ZSPM8015-KIT Evaluation Kit Description

Visit IDT's website www.IDT.com or contact your nearest sales office for the latest version of these documents.

9 Document Revision History

Revision	Date	Description
1.00	April 26, 2013	First release
1.10	August 5, 2013	Minor updates to *1.1. Maximum Absolute Rating*: VSWH added; BOOT-PGND values corrected.
	January 25, 2016	Changed to IDT branding.

Corporate Headquarters
6024 Silver Creek Valley Road
San Jose, CA 95138
www.IDT.com

Sales
1-800-345-7015 or 408-284-8200
Fax: 408-284-2775
www.IDT.com/go/sales

Tech Support
www.IDT.com/go/support

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