ST8024

COM/SEG LCD Driver

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Datasheet

Version 2.1

2009/08/19

Sitronix Technology Corporation

1 FEATURES

- Number of LCD drive outputs: 240
- Supply voltage for LCD drive: +15.0 to +30.0 V
- Supply voltage for the logic system: +2.5 to +5.5 V
- Low power consumption
- Low output impedance

(Segment mode)

- Shift clock frequency
  - 20MHz(MAX.): V_{DD} = +5.0 ± 0.5V
  - 15MHz(MAX.): V_{DD} = +3.0 to + 4.5V
  - 12MHz(MAX.): V_{DD} = +2.5 to + 3.0V
- Adopts a data bus system
- 4-bit/8-bit parallel input modes are selectable with a mode (MD) pin
- Automatic transfer function of an enable signal
- Automatic counting function which, in the chip selection mode, causes the internal clock to be stopped by automatically counting 240 bits of input data
- Line latch circuits are reset when /DISPOFF active

(Common mode)

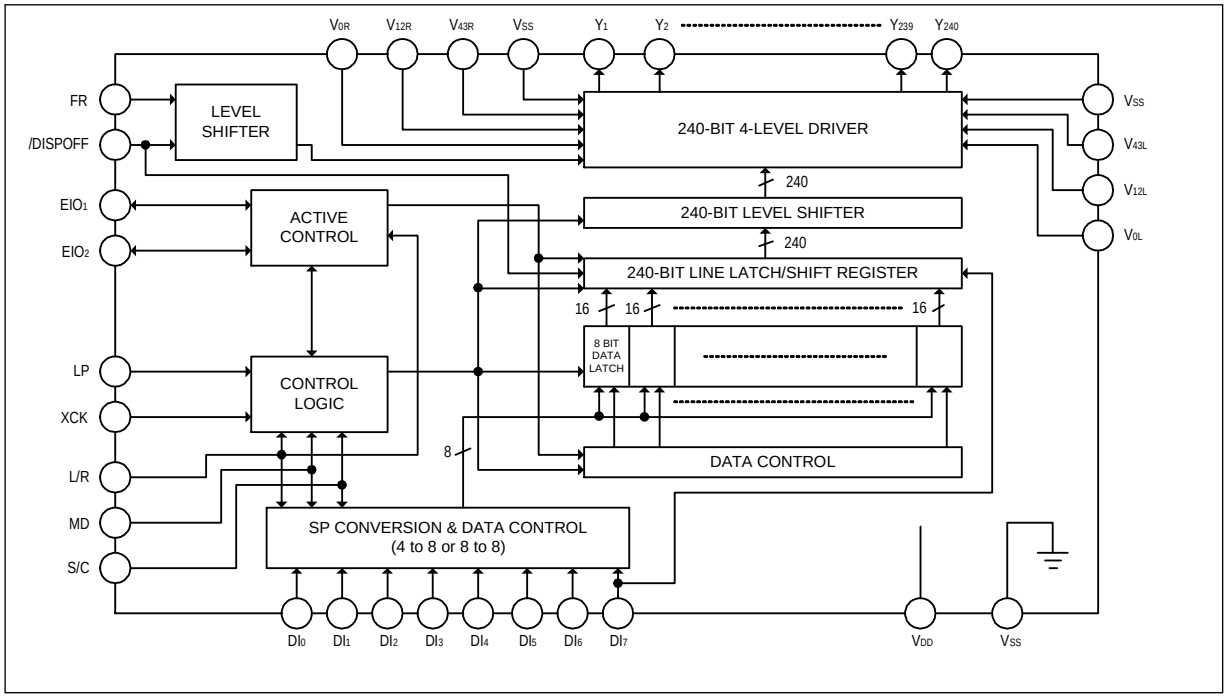
- Shift clock frequency: 4 MHz (MAX.)
- Built-in 240-bit bi-directional shift register (divisible into 120 bits x 2)
- Available in a single mode (240-bit shift register) or in a dual mode (120-bit shift register x 2)
  - Y_1->Y_{240} Single mode
  - Y_{240}->Y_1 Single mode
  - Y_1->Y_{I20}, Y_{121}->Y_{240} Dual mode
  - Y_{240}->Y_{121}, Y_{I20}->Y_1 Dual mode

  The above 4 shift directions are pin-selectable
- Shift register circuits are reset when /DISPOFF active

2 DESCRIPTION

The ST8024 is a 240-output segment/common driver IC suitable for driving large/medium scale dot matrix LCD panels, and is used in personal computers/work stations. The ST8024 is good both as a segment driver and a common driver, and it can create a low power consuming, high-resolution LCD.

3 BLOCK DIAGRAM



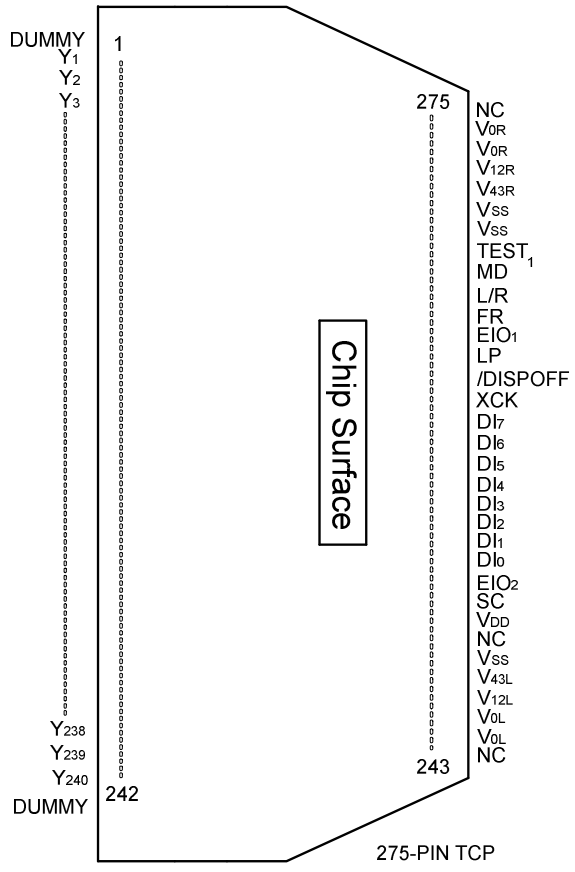
4 FUNCTIONAL OPERATIONS OF EACH BLOCK

BLOCK	FUNCTION
Active Control	In case of segment mode, controls the selection or non-selection of the chip. Following an LP signal input, and after the chip selection signal is input, a selection signal is generated internally until 240 bits of data have been read in. Once data input has been completed, a selection signal for cascade connection is output, and the chip is non-selected. In case of common mode, controls the input/output data of bi-directional pins.
SP Conversion & Data Control	In case of segment mode, keeps input data which are 2 clocks of XCK at 4-bit parallel input mode in latch circuit, or keeps input data which are 1 clock of XCK at 8-bit parallel input mode in latch circuit; after that they are put on the internal data bus 8 bits at a time.
Data Latch Control	In case of segment mode, selects the state of the data latch which reads in the data bus signals. The shift direction is controlled by the control logic. For every 16 bits of data read in, the selection signal shifts one bit based on the state of the control circuit.
Data Latch	In case of segment mode, latches the data on the data bus. The latch state of each LCD drive output pin is controlled by the control logic and the data latch control; 240 bits of data are read in 30 sets of 8 bits.
Line Latch/ Shift Register	In case of segment mode, all 240 bits which have been read into the data latch are simultaneously latched at the falling edge of the LP signal, and are output to the level shifter block. In case of common mode, shifts data from the data input pin at the falling edge of the LP signal.
Level Shifter	The logic voltage signal is level-shifted to the LCD drive voltage level, and is output to the driver block.
4-Level Driver	Drives the LCD drive output pins from the line latch/shift register data, and selects one of 4 levels (V_0, V_{12}, V_{43} or Vss) based on the S/C, FR and /DISPOFF signals.
Control Logic	Controls the operation of each block. In case of segment mode, when an LP signal has been input, all blocks are reset and the control logic waits for the selection signal output from the active control block. Once the selection signal has been output, operation of the data latch and data transmission is controlled, 240 bits of data are read in, and the chip is non-selected. In case of common mode, controls the direction of data shift.

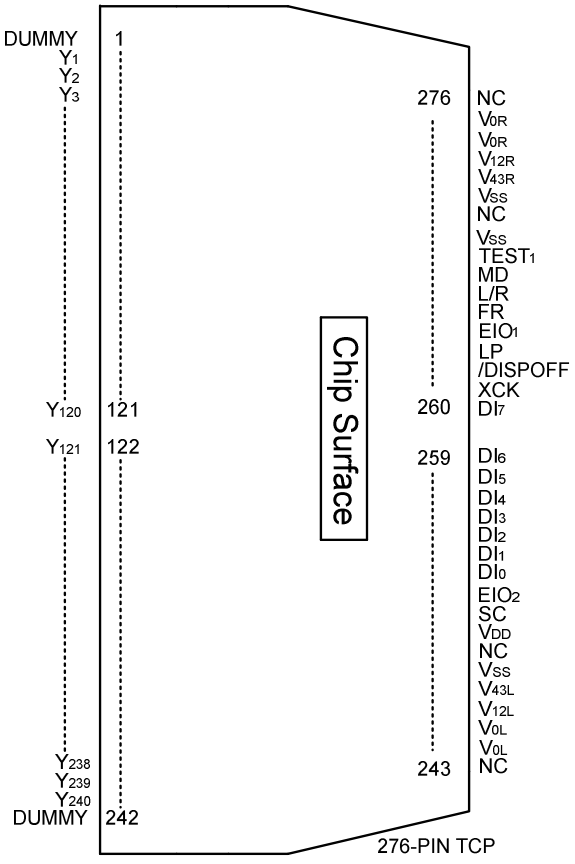
5 PIN DESCRIPTION (TCP TYPE)

SYMBOL	I/O	DESCRIPTION
Y_1-Y_{240}	O	LCD drive output
V_{0L}, V_{0R}	P	Power supply for LCD drive
V_{12L}, V_{12R}	P	Power supply for LCD drive
V_{43L}, V_{43R}	P	Power supply for LCD drive
L/R	I	Display data shift direction selection
V_{DD}	P	Power supply for logic system (+2.5 to +5.5 V)
S/C	I	Segment mode/common mode selection
EIO_2, EIO_1	I/O	Input/output for chip selection at segment mode Shift data input/output for shift register at common mode
DI_0-DI_6	I	Display data input at segment mode
DI_7	I	Display data input at segment mode/Dual mode data input at common mode
XCK	I	Clock input for taking display data at segment mode
/DISPOFF	I	Control input for output of non-select level
LP	I	Latch pulse input for display data at segment mode/ Shift clock input for shift register at common mode
FR	I	AC-converting signal input for LCD drive waveform
MD	I	4 or 8 bits mode selection input
V_{SS}	P	Ground (0 V)
TEST1	I	Connect to GND or floating

PS : Detail size see TCP drawing data



ST8024 F14 TCP



ST8024 F4 TCP

6 INPUT/OUTPUT CIRCUITS

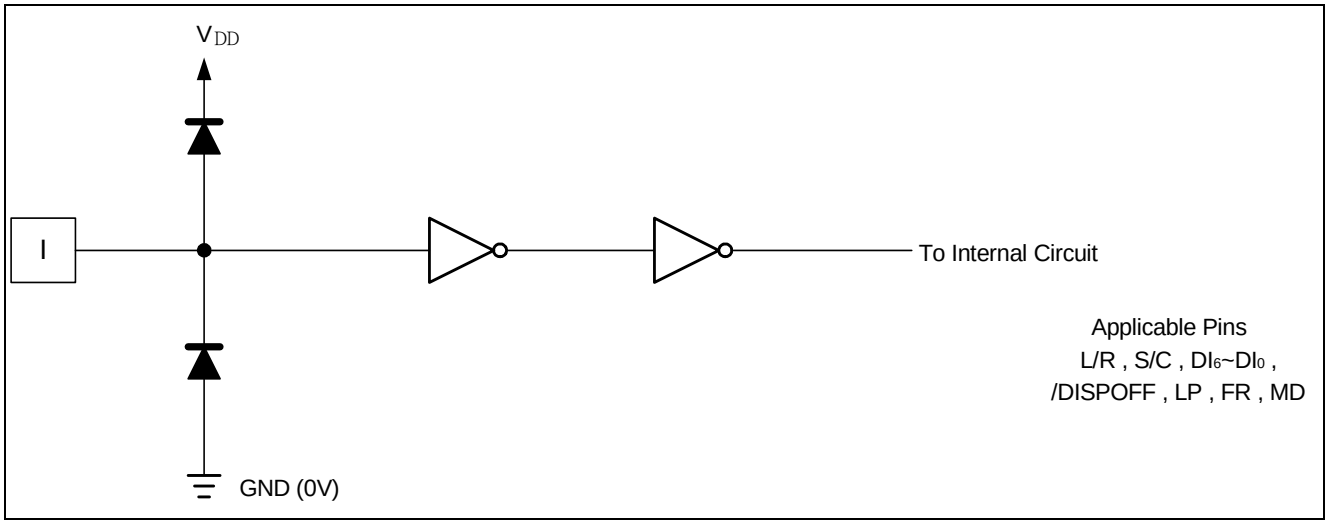


Figure 6-1 Input Circuit (1)

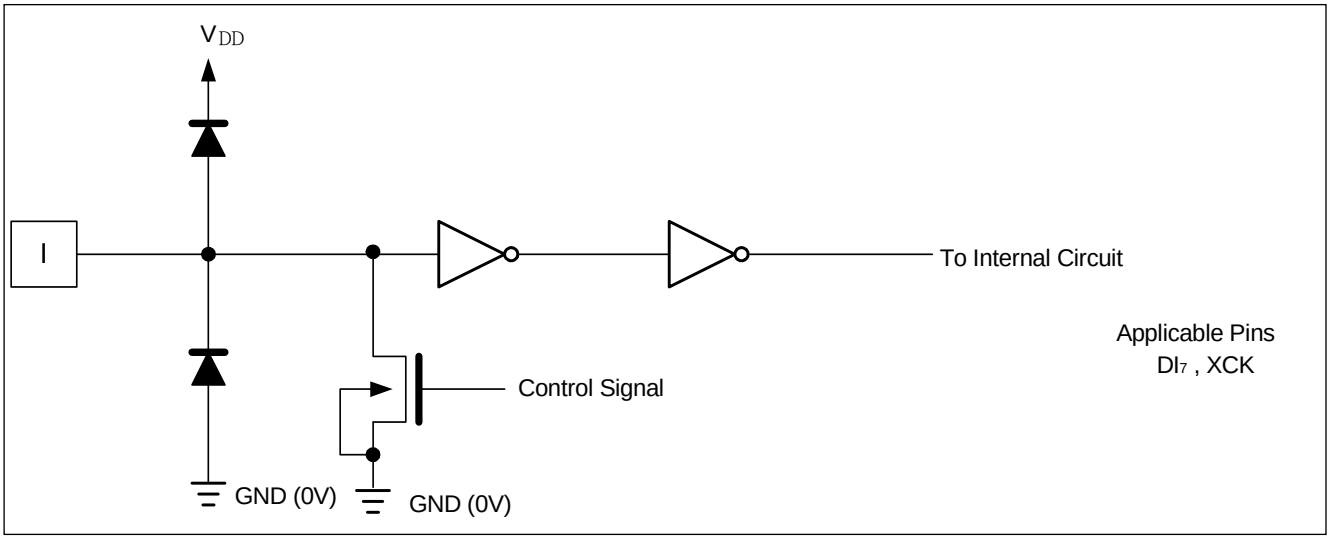


Figure 6-2 Input Circuit (2)

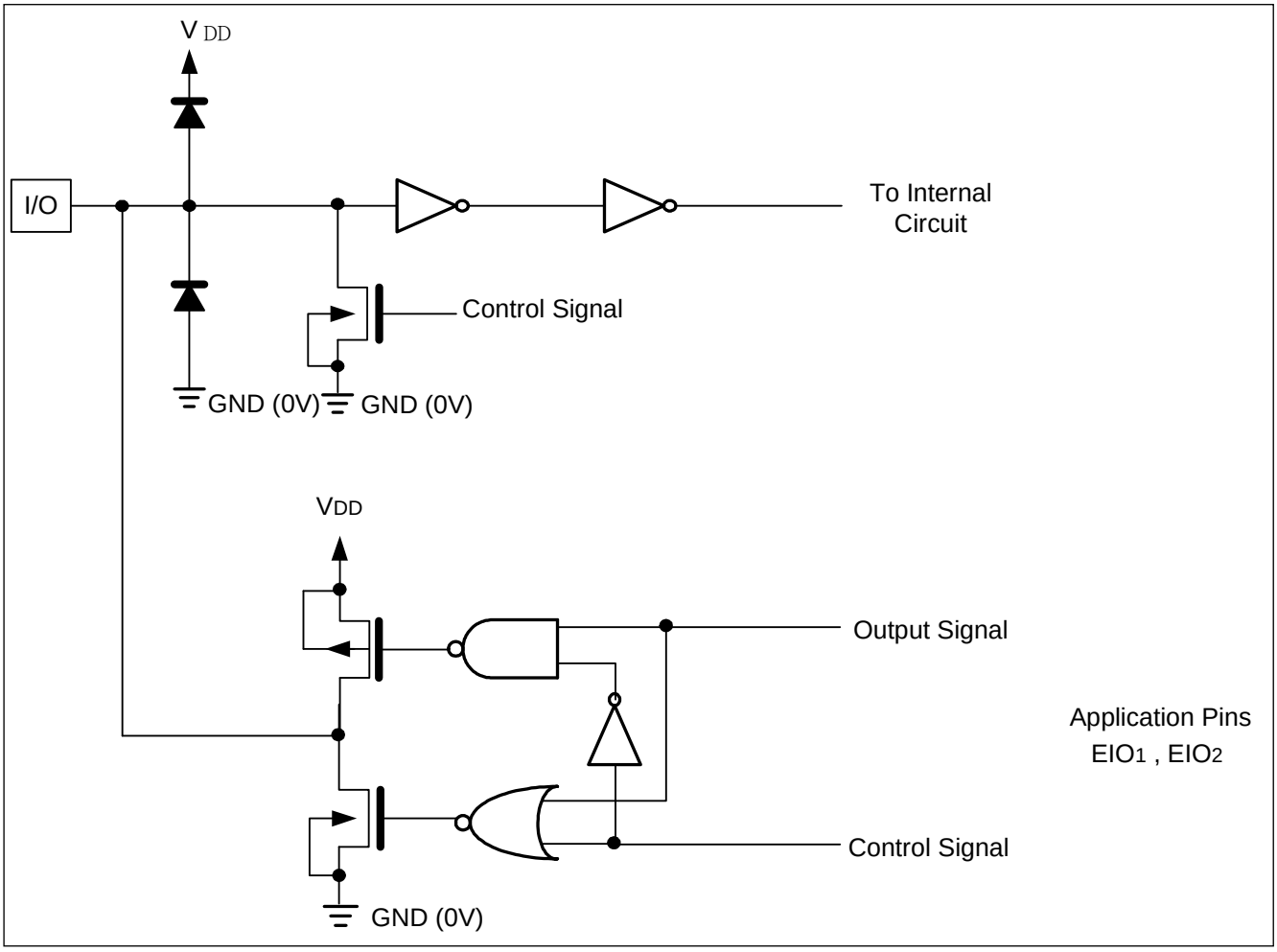


Figure 6-3 Input/Output Circuit

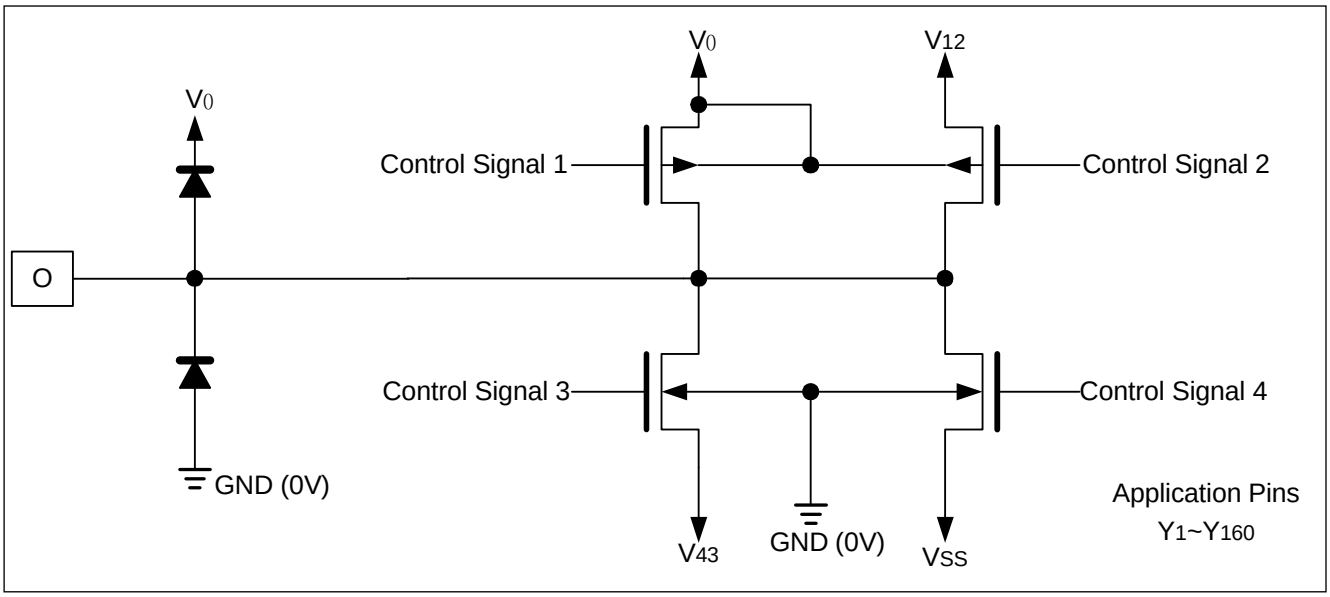


Figure 6-4 LCD Drive Output Circuit

7 FUNCTIONAL DESCRIPTION

7.1 Pin Functions

(Segment mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, • Connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider • Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$. • V_{iL} and V_{iR} (i = 0,12, 43) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin
DI_7-DI_0	Input pins for display data • In 4-bit parallel mode, DI_3-DI_0 are the display data input pins, and DI_7-DI_4 must be connected to LGND or V_{DD}. • In 8-bit parallel mode, All DI_7-DI_0 pins are the display data input pins. • Refer to section 7.2.2.
XCK	Clock input pin for taking display data • Data is read at the falling edge of the clock pulse.
LP	Latch pulse input pin for display data • Data is latched at the falling edge of the clock pulse.
L/R	Input pin for selecting the reading direction of display data • When set to LGND level "L", data is read sequentially from Y_{240} to Y_1. • When set to V_{DD} level "H", data is read sequentially from Y_1 to Y_{240}. Refer to section 7.2.2.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to LGND level "L", the LCD drive output pins (Y_1-Y_{240}) are set to level Vss. • When set to "L", the contents of the line latch are reset, but the display data are read in the data latch regardless of the condition of /DISPOFF. When the /DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), then outputs the contents of the data latch at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, it can not output the reading data correctly. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the line latch output signal and the FR signal. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
MD	Mode selection pin • When set to LGND level "L", 8-bit parallel input mode is set. • When set to V_{DD} level "H", 4-bit parallel input mode is set. • Refer to section 7.2.2.
S/C	Segment mode/common mode selection pin • When set to V_{DD} level "H", segment mode is set.
EIO_1, EIO_2	Input/output pins for chip selection • When L/R input is at LGND level "L", EIO_1 is set for output, and EIO_2 is set for input. • When L/R input is at V_{DD} level "H", $\overline{EIO_1}$ is set for input, and EIO_2 is set for output. • During output, set to "H" while LP • $\overline{XCK}$ is "H" and after 240 bits of data have been read, set to "L" for one cycle (from falling edge to failing edge of XCK), after which it returns to "H". • During input, the chip is selected while EI is set to "L" after the LP signal is input. The chip is non-selected after 240 bits of data have been read.

Y_1 -Y_{240}	LCD drive output pins • Corresponding directly to each bit of the data latch, one level (V_0, V_{12}, V_{43}, or V_{SS}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

(Common mode)

SYMBOL	FUNCTION
V_{DD}	Logic system power supply pin, connected to +2.5 to +5.5 V.
V_{SS}	Ground pin, connected to 0 V.
V_{0L}, V_{0R} V_{12L}, V_{12R} V_{43L}, V_{43R}	Bias power supply pins for LCD drive voltage • Normally use the bias voltages set by a resistor divider. • Ensure that voltages are set such that $V_{SS} < V_{43} < V_{12} < V_0$. • V_{iL} and V_{iR} (i = 0,12, 43) must connect to an external power supply, and supply regular voltage which is assigned by specification for each power pin.
EIO_1	Shift data input/output pin for bi-directional shift register • Output pin when L/R is at LGND level "L', input pin when L/R is at V_{DD} level "H". • When L/R = H, EIO_1 is used as input pin, it will be pulled down. • When L/R = L, EIO_1 is used as output pin, it won't be pulled down. • Refer to section 7.2.2.
EIO_2	Shift data input/output pin for bi-directional shift register • Input pin when L/R is at LGND level "L", output pin when L/R is at V_{DD} level "H". • When L/R = L, EIO_2 is used as input pin, it will be pulled down. • When L/R = H, EIO_2 is used as output pin, it won't be pulled down. • Refer to section 7.2.2.
LP	Shift clock pulse input pin for bi-directional shift register • Data is shifted at the falling edge of the clock pulse.
L/R	Input pin for selecting the shift direction of bi-directional shift register • Data is shifted from Y_{240} to Y_1 when set to LGND level "L", and data is shifted from Y_1 to Y_{240} when set to V_{DD} level "H". • Refer to section 7.2.2.
/DISPOFF	Control input pin for output of non-select level • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • When set to LGND level "L", the LCD drive output pins (Y_1-Y_{240}) are set to level LGND. • When set to "L", the contents of the shift register are reset to not reading data. When the /DISPOFF function is canceled, the driver outputs non-select level (V_{12} or V_{43}), and the shift data is read at the next falling edge of the LP. At that time, if /DISPOFF removal time does not correspond to what is shown in AC characteristics, the shift data is not read correctly. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
FR	AC signal input pin for LCD drive waveform • The input signal is level-shifted from logic voltage level to LCD drive voltage level, and controls the LCD drive circuit. • Normally it inputs a frame inversion signal. • The LCD drive output pins' output voltage levels can be set using the shift register output signal and the FR signal. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.
MD	Mode selection pin • When set to LGND level "L", single mode operation is selected; when set to V_{DD} level "H" dual mode operation is selected. • Refer to section 7.2.2.
DI_7	Dual mode data input pin • According to the data shift direction of the data shift register, data can be input starting from the 121st bit. When the chip is used in dual mode, DI_7 will be pulled down. When the chip is used in single mode, DI_7 won't be pulled down. • Refer to section 7.2.2.
S/C	Segment mode/common mode selection pin • When set to LGND level "L", common mode is set.

DI_6-DI_0	Not used • Connect DI_6-DI_0 to LGND or V_{DD}, avoiding floating.
XCK	Not used • XCK is pulled down in common mode, so connect to LGND or open.
Y_1 -Y_{240}	LCD drive output pins • Corresponding directly to each bit of the shift register, one level (V_0, V_{12}, V_{43}, or V_{SS}) is selected and output. • Table of truth values is shown in "TRUTH TABLE" in Functional Operations.

7.2 Functional Operations

7.2.1 Truth table

(Segment Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y240)
L	L	H	V_{43}
L	H	H	V_{SS}
H	L	H	V_{12}
H	H	H	V_0
X	X	L	V_{SS}

(Common Mode)

FR	LATCH DATA	/DISPOFF	LCD DRIVE OUTPUT VOLTAGE LEVEL (Y1-Y240)
L	L	H	V_{43}
L	H	H	V_0
H	L	H	V_{12}
H	H	H	V_{SS}
X	X	L	V_{SS}

NOTES:

- $V_{SS} < V_{43} < V_{12} < V_0$
- L: LGND (0 V), H: V_{DD} (+2.5 to +5.5 V), X: Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.
  There are two kinds of power supply (logic level voltage and LCD drive voltage) for the LCD driver. Supply regular voltage which is assigned by specification for each power pin.

7.2.2 Relationship between the display data and LCD drive output Pins

(Segment Mode)

4-bit Parallel Input Mode

MD	L/R	EIO_1	$EI0_2$	DATA INPUT	NUMBER OF CLOCKS						
					60 CLOCK	59 CLOCK	58 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
H	L	Output	Input	DI_0	Y_1	Y_5	Y_9	…	Y_{229}	Y_{233}	Y_{237}
				DI_1	Y_2	Y_6	Y_{10}	…	Y_{230}	Y_{234}	Y_{238}
				DI_2	Y_3	Y_7	Y_{11}	…	Y_{231}	Y_{235}	Y_{239}
				DI_3	Y_4	Y_8	Y_{12}	…	Y_{232}	Y_{236}	Y_{240}
H	H	Input	Output	DI_0	Y_{240}	Y_{236}	Y_{232}	…	Y_{12}	Y_8	Y_4
				DI_1	Y_{239}	Y_{235}	Y_{231}	…	Y_{11}	Y_7	Y_3
				DI_2	Y_{238}	Y_{234}	Y_{230}	…	Y_{10}	Y_6	Y_2
				DI_3	Y_{237}	Y_{233}	Y_{229}	…	Y_9	Y_5	Y_1

8-bit Parallel Input Mode

MD	L/R	EIO_1	$EI0_2$	DATA INPUT	NUMBER OF CLOCKS						
					30 CLOCK	29 CLOCK	28 CLOCK	…	3 CLOCK	2 CLOCK	1 CLOCK
L	L	Output	Input	DI_0	Y_1	Y_9	Y_{17}	…	Y_{217}	Y_{225}	Y_{233}
				DI_1	Y_2	Y_{10}	Y_{18}	…	Y_{218}	Y_{226}	Y_{234}
				DI_2	Y_3	Y_{11}	Y_{19}	…	Y_{219}	Y_{227}	Y_{235}
				DI_3	Y_4	Y_{12}	Y_{20}	…	Y_{220}	Y_{228}	Y_{236}
				DI_4	Y_5	Y_{13}	Y_{21}		Y_{221}	Y_{229}	Y_{237}
				DI_5	Y_6	Y_{14}	Y_{22}		Y_{222}	Y_{230}	Y_{238}
				DI_6	Y_7	Y_{15}	Y_{23}		Y_{223}	Y_{231}	Y_{239}
				DI_7	Y_8	Y_{16}	Y_{24}		Y_{224}	Y_{232}	Y_{240}
L	H	Input	Output	DI_0	Y_{240}	Y_{232}	Y_{224}	…	Y_{24}	Y_{16}	Y_8
				DI_1	Y_{239}	Y_{231}	Y_{223}	…	Y_{23}	Y_{15}	Y_7
				DI_2	Y_{238}	Y_{230}	Y_{222}	…	Y_{22}	Y_{14}	Y_6
				DI_3	Y_{237}	Y_{229}	Y_{221}	…	Y_{21}	Y_{13}	Y_5
				DI_4	Y_{236}	Y_{228}	Y_{220}	…	Y_{20}	Y_{12}	Y_4
				DI_5	Y_{235}	Y_{227}	Y_{219}	…	Y_{19}	Y_{11}	Y_3
				DI_6	Y_{234}	Y_{226}	Y_{218}	…	Y_{18}	Y_{10}	Y_2
				DI_7	Y_{233}	Y_{225}	Y_{217}	…	Y_{17}	Y_9	Y_1

(Common Mode)

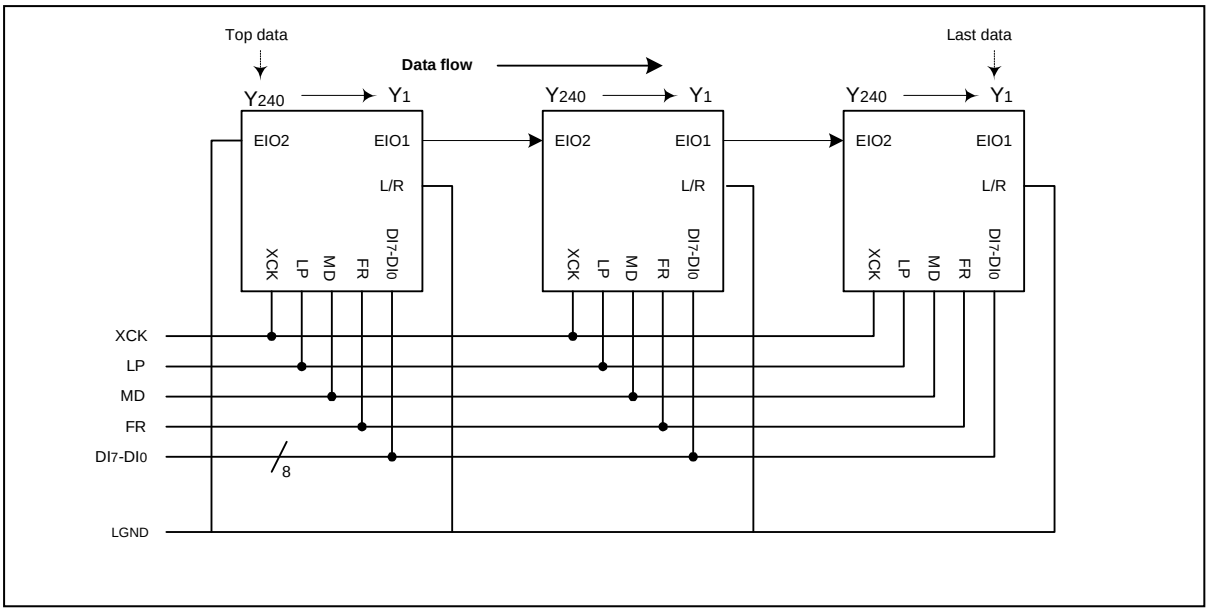
MD	L/R	DATA TRANSFER DIRECTION	EIO_1	$EI0_2$	DI_7
L (Single)	L	$Y_{240} \rightarrow Y_1$	Output	Input	X
	H	$Y_1 \rightarrow Y_{240}$	Input	Output	X
H (Dual)	L	$Y_{240} \rightarrow Y_{121}$ $Y_{120} \rightarrow Y_1$	Output	Input	Input
	H	$Y_1 \rightarrow Y_{120}$ $Y_{121} \rightarrow Y_{240}$	Input	Output	Input

NOTES:

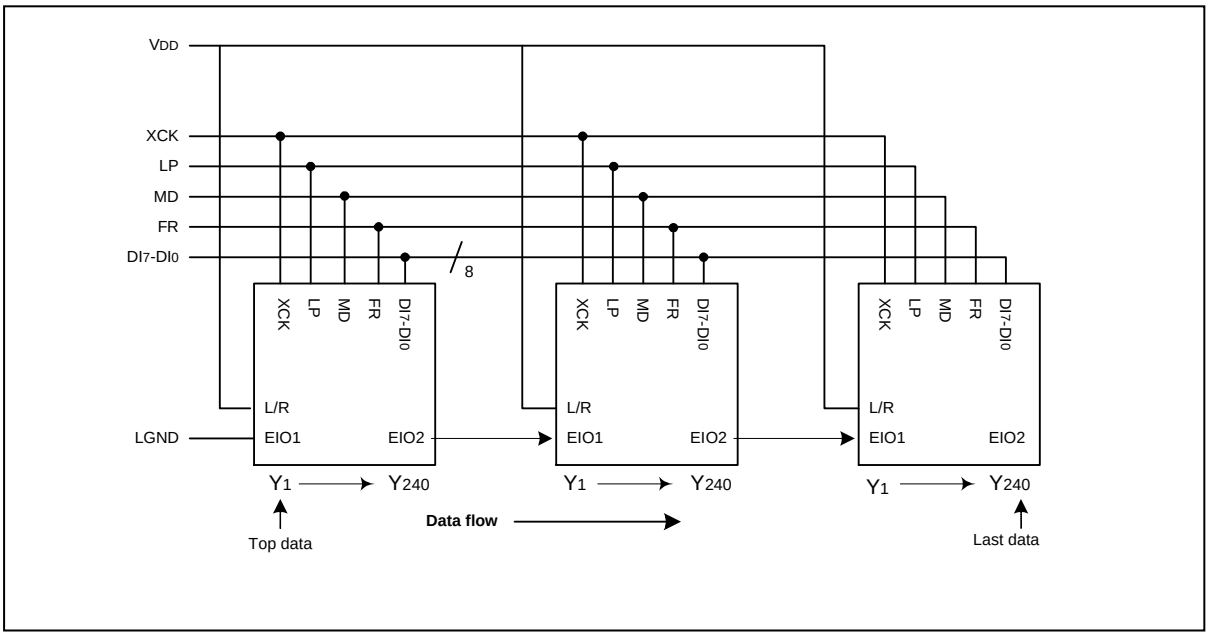
- L: LGND (0 V), H: V_{DD} (+2.5 to +5.5 V), X: Don't care
- "Don't care" should be fixed to "H" or "L", avoiding floating.

7.2.3 Connection examples of plural segment drivers

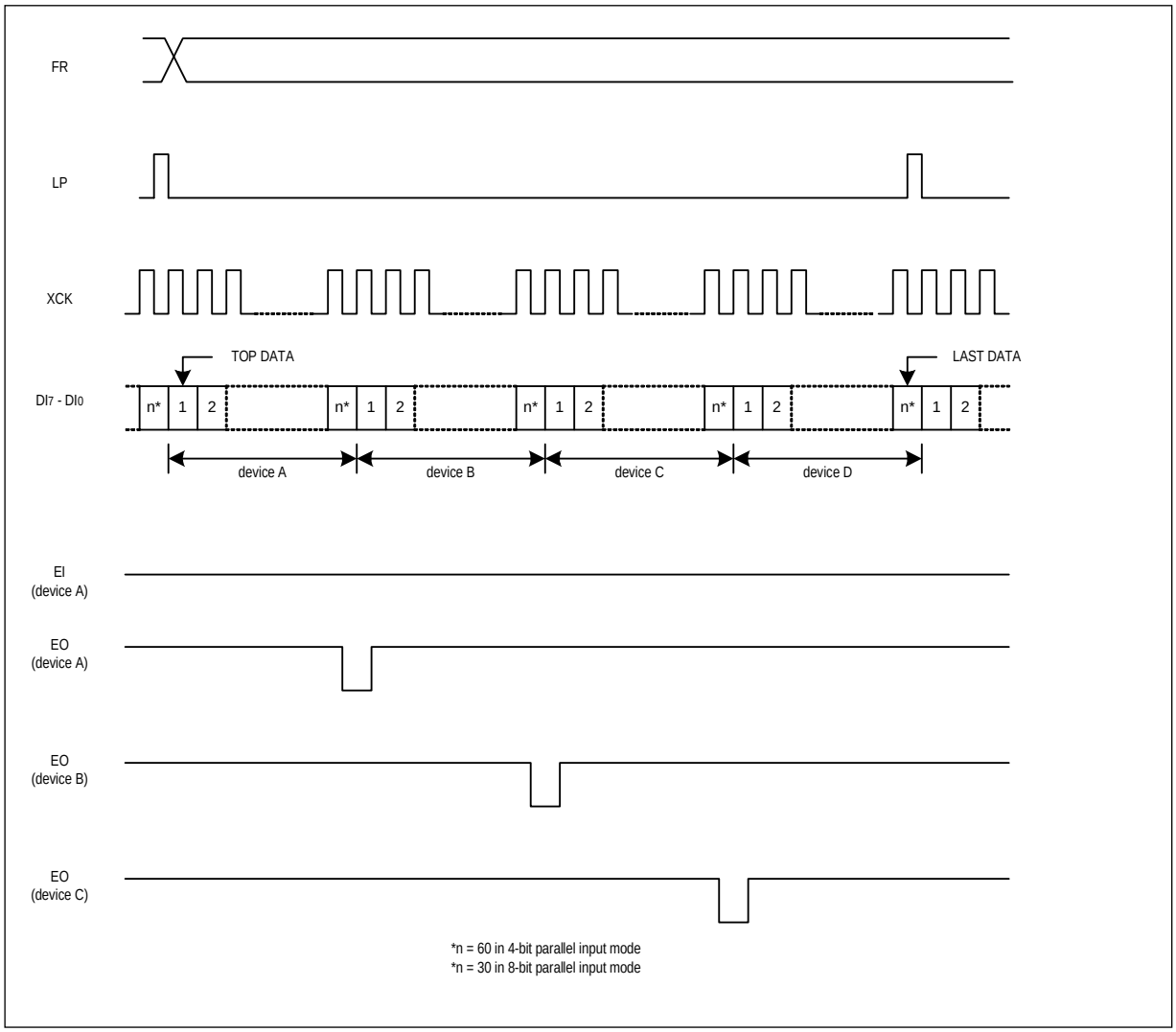
(a) When L/R = "L"



(b) When L/R = "H"

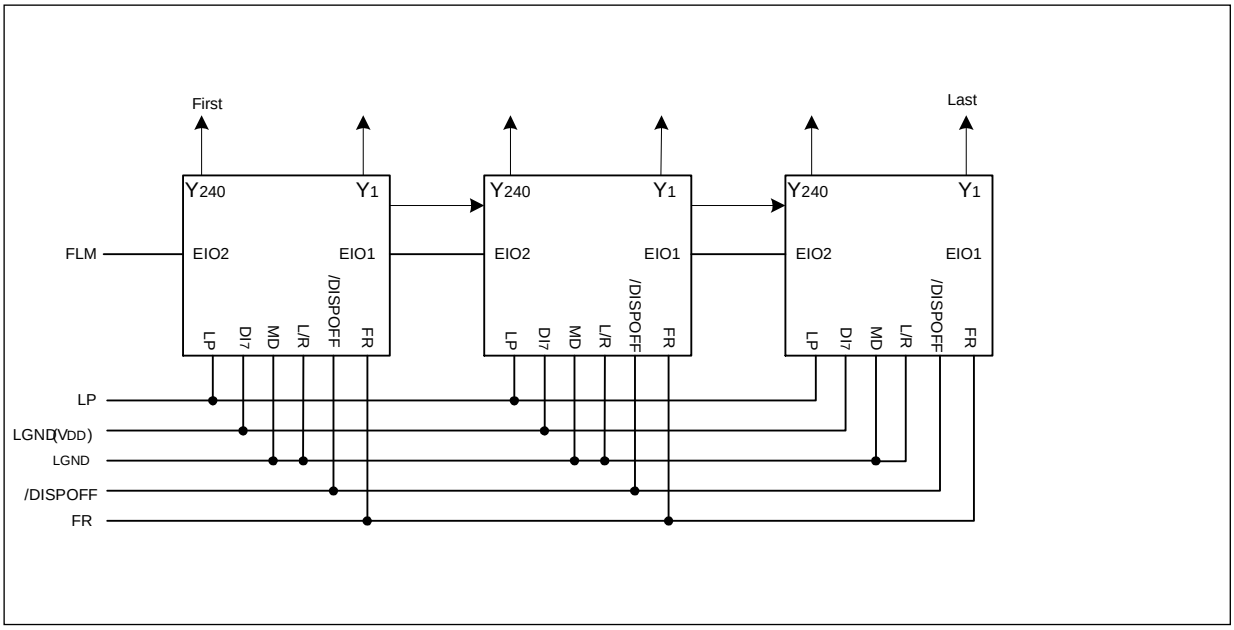


7.2.4 Timing chart of 4-device cascade connection of segment drivers

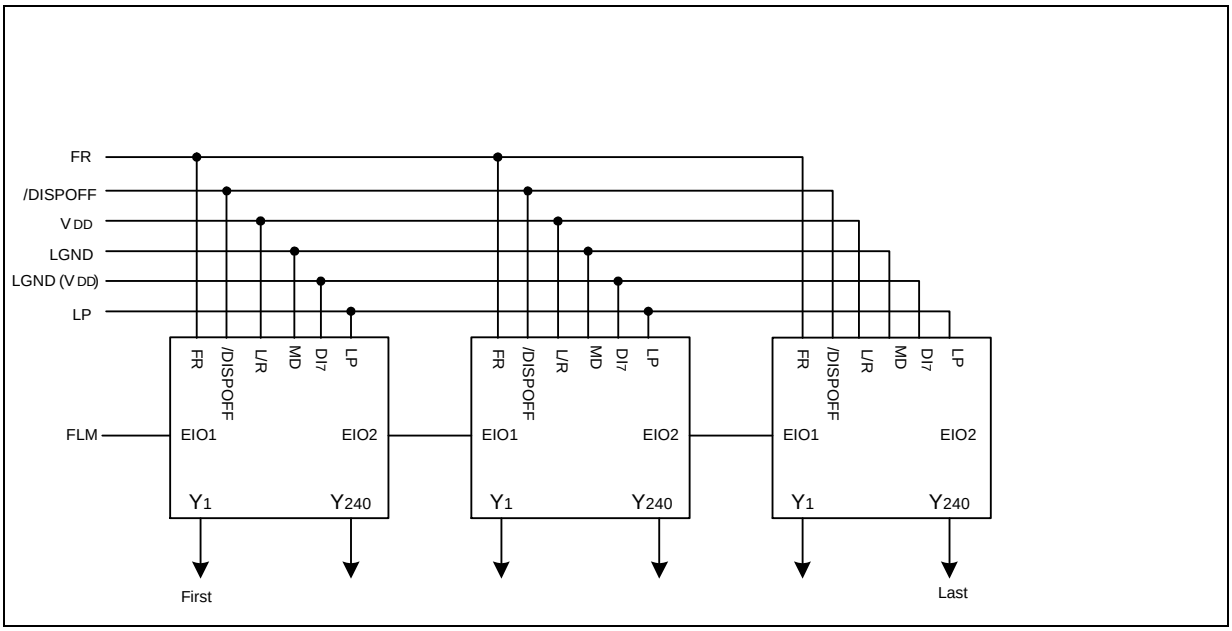


7.2.5 Connection examples for plural common drivers

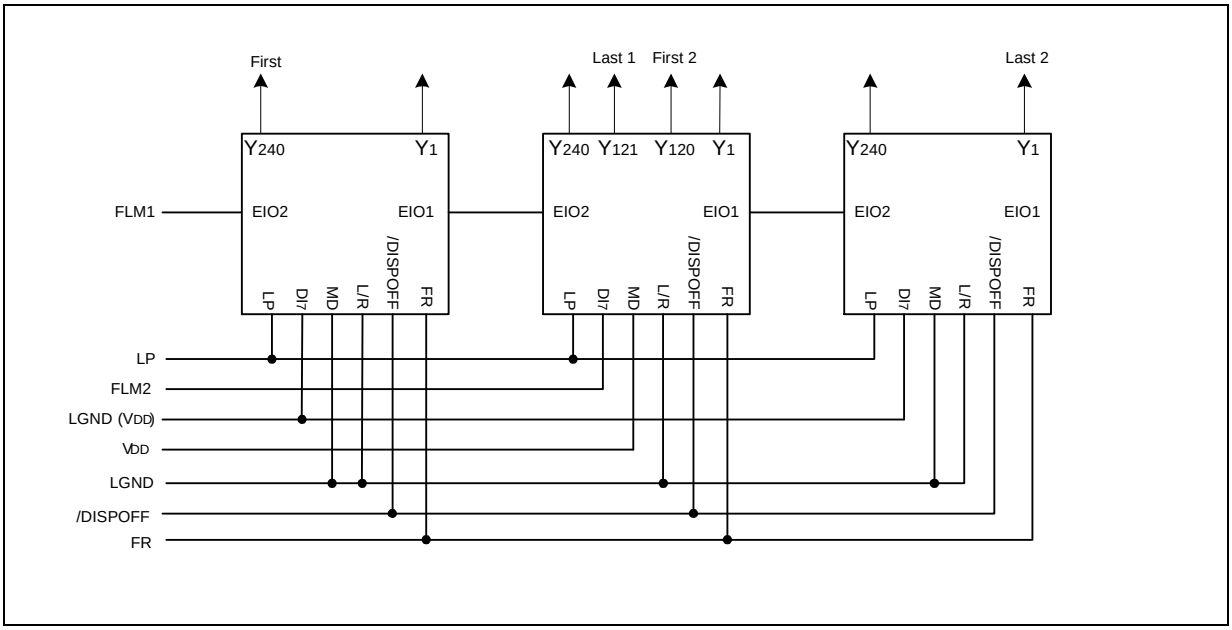
(a) Single Mode (L/R = "L")



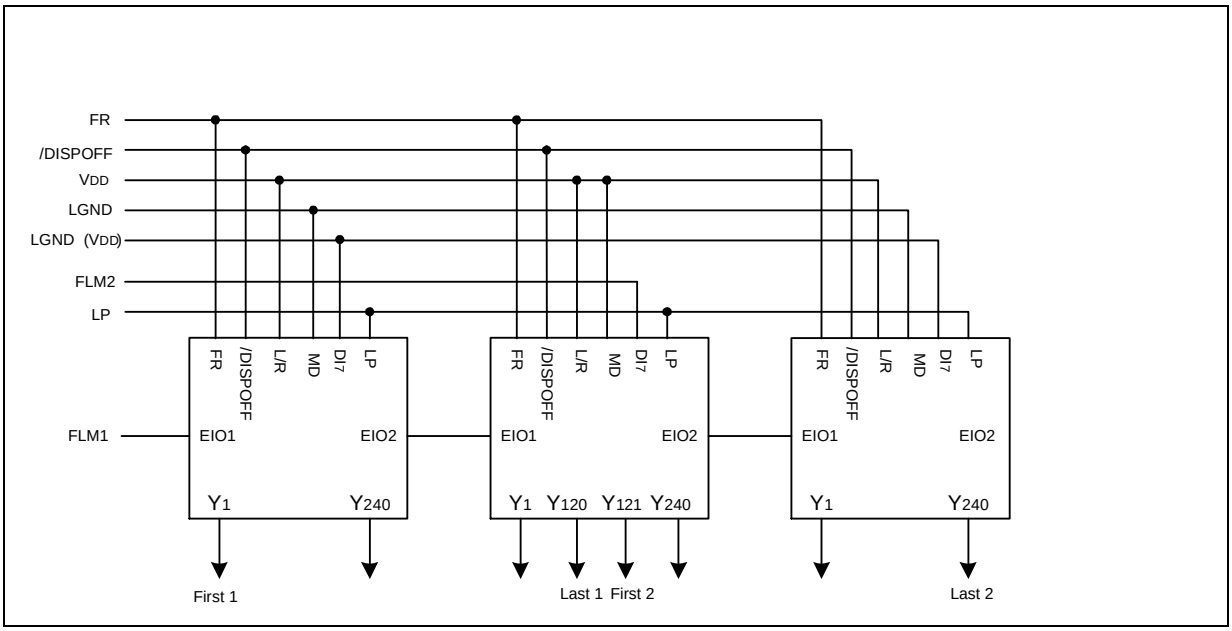
(b) Single Mode (L/R = "H")



(c) Dual Mode (L/R = "L")



(d) Dual mode (L/R = "H")

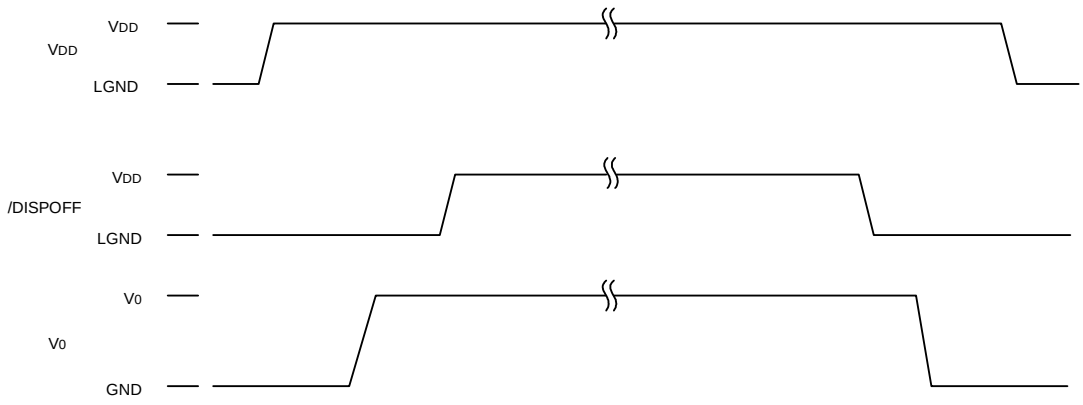


8 PRECAUTIONS

Precautions when connecting or disconnecting the power supply
This IC has a high-voltage LCD driver, so it may be permanently damaged by a high current which may flow if voltage is supplied to the LCD drive power supply while the logic system power supply is floating. The details are as follows,

- When connecting the power supply, connect the LCD drive power after connecting the logic system power. Furthermore, when disconnecting the power, disconnect the logic system power after disconnecting the LCD drive power
- It is advisable to connect the serial resistor (50 to 100 Ω) or fuse to the LCD drive power V_0 of the system as a current limiter. Set up a suitable value of the resistor in consideration of the display grade.

And when connecting the logic power supply, the logic condition of this IC inside is insecure. Therefore connect the LCD drive power supply after resetting logic condition of this IC inside on /DISPOFF function. After that, cancel the /DISPOFF function after the LCD drive power supply has become stable. Furthermore, when disconnecting the power, set the LCD drive output pins to level LGND on /DISPOFF function. Then disconnect the logic system power after disconnecting the LCD drive power.
When connecting the power supply, follow the recommended sequence shown here



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9 ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	APPLICABLE PINS	RATING	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	-0.3 to +7.0	V	1,2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	-0.3 to +33.0	V	
	V_{12}	V_{12L}, V_{12R}	-0.3 to V_0 + 0.3	V	
	V_{43}	V_{43L}, V_{43R}	-0.3 to V_0 + 0.3	V	
	V_{SS}	V_{SS}	-0.3 to V_0 + 0.3	V	
Input voltage	V_I	DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF	-0.3 to V_{DD} + 0.3	V	
Storage temperature	T_{STG}		-45 to +125	°C	

NOTES:
1. TA = +25 °C
2. The applicable voltage on logic pins with respect to LGND, high voltage pins with V_{SS} (0 V).
3. Stress over the “Absolute Max. Ratings” conditions will damaged the device permanently.

10 RECOMMENDED OPERATING CONDITIONS

PARAMETER	SYMBOL	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Supply voltage (1)	V_{DD}	V_{DD}	+2.5		+5.5	V	1, 2
Supply voltage (2)	V_0	V_{0L}, V_{0R}	+15.0		+30.0	V	
Operating temperature	T_{OPR}		-25		+85	°C	

NOTES:
1. The applicable voltage on logic pins with respect to LGND, high voltage pins with V_{SS} (0 V).
2. Ensure that voltages are set such that $V_{SS} < V_{43} < V_{I2} < V_0$.

11 ELECTRICAL CHARACTERISTICS

11.1 DC Characteristics

(Segment Mode) (LGND=V_{SS} =GND = 0V, V_{DD} = +2.5 ~ +5.5 V, V_0 = + 15.0 ~ +30.0V, T_{OPR} = -25 to +85°C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABLE PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			0.2V_{DD}	V	
Input "High" voltage	V_{IH}			0.8V_{DD}		V_{DD}+0.7	V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	V_I = LGND	DI_7-DI_0, XCK, LP, L/R, FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			-10.0	µA	
	I_{LIH}	V_I = V_{DD}				+10.0	µA	
Output resistance	R_{ON}	|ΔV_{ON}| =0.5V, V_0=30V	Y_1-Y_{240}		1.5	2.0	kΩ	
		|ΔV_{ON}| =0.5V, V_0=20V			2.0	2.5		
Standby current	I_{STB}		LGND			75.0	µA	1
Supply current (1) (Non-selection)	I_{DD1}		V_{DD}			2.0	mA	2
Supply current (2) (Selection)	I_{DD2}		V_{DD}			12.0	mA	3
Supply current (3)	I_0		V_{0L}, V_{0R}			1.5	mA	4

NOTES:

1. V_{DD} = +5.0 V, V_0 = +30.0 V, Vi = LGND.
2. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 20 MHz, no-load, EI = V_{DD}. The input data is turned over by data taking clock (4-bit parallel input mode).
3. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 20 MHz, no-load, EI = LGND. The input data is turned over by data taking clock (4-bit parallel input mode).
4. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{XCK} = 20 MHz, f_{LP} = 41.6 kHz, f_{FR} = 80 Hz, no-load. The input data is turned over by data taking clock (4-bit parallel input mode).

(Common Mode) (LGND=V_{SS} =GND = 0V, V_{DD} = +2.5 ~ +5.5V, V_0 = + 15.0 ~ +30.0V, T_{OPR} = -25 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	APPLICABL E PINS	MIN.	TYP.	MAX.	UNIT	NOTE
Input "Low" voltage	V_{IL}		DI_7-DI_0, XCK, LP, L/R FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			0.2V_{DD}	V	
Input "High" voltage	V_{IH}			0.8V_{DD}		V_{DD}+0.7	V	
Output "Low" voltage	V_{OL}	I_{OL} = +0.4 mA	EIO_1, EIO_2			+0.4	V	
Output "High" voltage	V_{OH}	I_{OH} = -0.4 mA		V_{DD}-0.4			V	
Input leakage current	I_{LIL}	V_I = LGND	DI_7-DI_0, XCK, LP, L/R FR, MD, S/C, EIO_1, EIO_2, /DISPOFF			-10.0	µA	
	I_{LIH}	V_I = V_{DD}	DI_6-DI_0, LP, L/R, FR, MD, S/C, /DISPOFF			+10.0	µA	
Input pull-down current	I_{PD}	V_I = V_{DD}	DI_7, XCK, EIO_1, EIO_2			100.0	µA	
Output resistance	R_{ON}	|ΔV_{ON}| =0.5V, V_0=30V	Y_1-Y_{240}		1.5	2.0	kΩ	
		|ΔV_{ON}| =0.5V, V_0=20V			2.0	2.5		
Standby current	I_{SPD}		LGND			75.0	µA	1
Supply current (1)	I_{DD}		V_{DD}			120.0	µA	2
Supply current (2)	I_0		V_{0L}, V_{0R}			240.0	µA	2

NOTES:

1. V_{DD} = +5.0 V, V_0 = +30.0 V, V_I = LGND
2. V_{DD} = +5.0 V, V_0 = +30.0 V, f_{LP} = 41.6 kHz, f_{FR} = 80 Hz, 1/480 duty operation, no-load.

11.2 AC Characteristics

(Segment Mode 1) (LGND=V_{SS} = GND = 0 V, V_{DD} = +5.0±0.5 V, V_0 = + 15.0 ~ +30.0V, T_{OPR} = -25 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	50			ns	1
Shift clock "H" pulse width	t_{WCKH}		15			ns	
Shift clock "L" pulse width	t_{WCKL}		15			ns	
Data setup time	t_{DS}		10			ns	
Data hold time	t_{DH}		12			ns	
Latch pulse "H" pulse width	t_{WLPH}		15			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		30			ns	
Latch pulse rise to shift clock rise time	t_{LS}		25			ns	
Latch pulse fall to shift clock fall time	t_{LH}		25			ns	
Enable setup time	t_S		10			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
/DISPOFF removal time	t_{SD}		100			ns	
/DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			30	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 2) (LGND=V_{SS} =GND = 0V, V_{DD} = +3.0 ~ +4.5V, V_0 = + 15.0 ~ +30.0V, T_{OPR} = -25 to +85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	66			ns	1
Shift clock "H" pulse width	t_{WCKH}		23			ns	
Shift clock "L" pulse width	t_{WCKL}		23			ns	
Data setup time	t_{DS}		15			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		50			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
/DISPOFF removal time	t_{SD}		100			ns	
/DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			41	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:
1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Segment Mode 3) (LGND=V_{SS} =GND = 0V, V_{DD} = +2.5 ~ +3.0V, V_0 = + 15.0 ~ +30.0V, T_{OPR} = -25 to+85 °C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT	NOTE
Shift clock period	t_{WCK}	t_R,t_F ≤ 10ns	82			ns	1
Shift clock "H" pulse width	t_{WCKH}		28			ns	
Shift clock "L" pulse width	t_{WCKL}		28			ns	
Data setup time	t_{DS}		20			ns	
Data hold time	t_{DH}		23			ns	
Latch pulse "H" pulse width	t_{WLPH}		30			ns	
Shift clock rise to latch pulse rise time	t_{LD}		0			ns	
Shift clock fall to latch pulse fall time	t_{SL}		65			ns	
Latch pulse rise to shift clock rise time	t_{LS}		30			ns	
Latch pulse fall to shift clock fall time	t_{LH}		30			ns	
Enable setup time	t_S		15			ns	
Input signal rise time	t_R				50	ns	2
Input signal fall time	t_F				50	ns	2
/DISPOFF removal time	t_{SD}		100			ns	
/DISPOFF "L" pulse width	t_{WDL}		1.2			µs	
Output delay time (1)	t_D	CL = 15 pF			57	ns	
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs	
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs	

NOTES:

1. Takes the cascade connection into consideration.
2. (t_{WCK} - t_{WCKH} - t_{WCKL})/2 is maximum in the case of high speed operation.

(Common Mode) (LGND=V_{SS} = 0 V, V_{DD} = +2.5 ~ +5.5V, V_0 = +15.0 ~ +30.0V, T_{OPR} = -25 to +85° C)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Shift clock period	t_{WLP}	t_R,t_F ≤ 20ns	250			ns
Shift clock "H" pulse width	t_{WLPH}	V_{DD} = +5.0± 0.5V	15			ns
		V_{DD} = +2.5+ 4.5V	30			ns
Data setup time	t_{SU}		30			ns
Data hold time	t_H		50			ns
Input signal rise time	t_R				50	ns
Input signal fall time	t_F				50	ns
/DISPOFF removal time	t_{SD}		100			ns
/DISPOFF "L" pulse width	t_{WDL}		1.2			µs
Output delay time (1)	t_{DL}	CL = 15 pF			200	ns
Output delay time (2)	t_{PD1}, t_{PD2}	CL = 15 pF			1.2	µs
Output delay time (3)	t_{PD3}	CL = 15 pF			1.2	µs

11.3 Timing Chart of Segment Mode

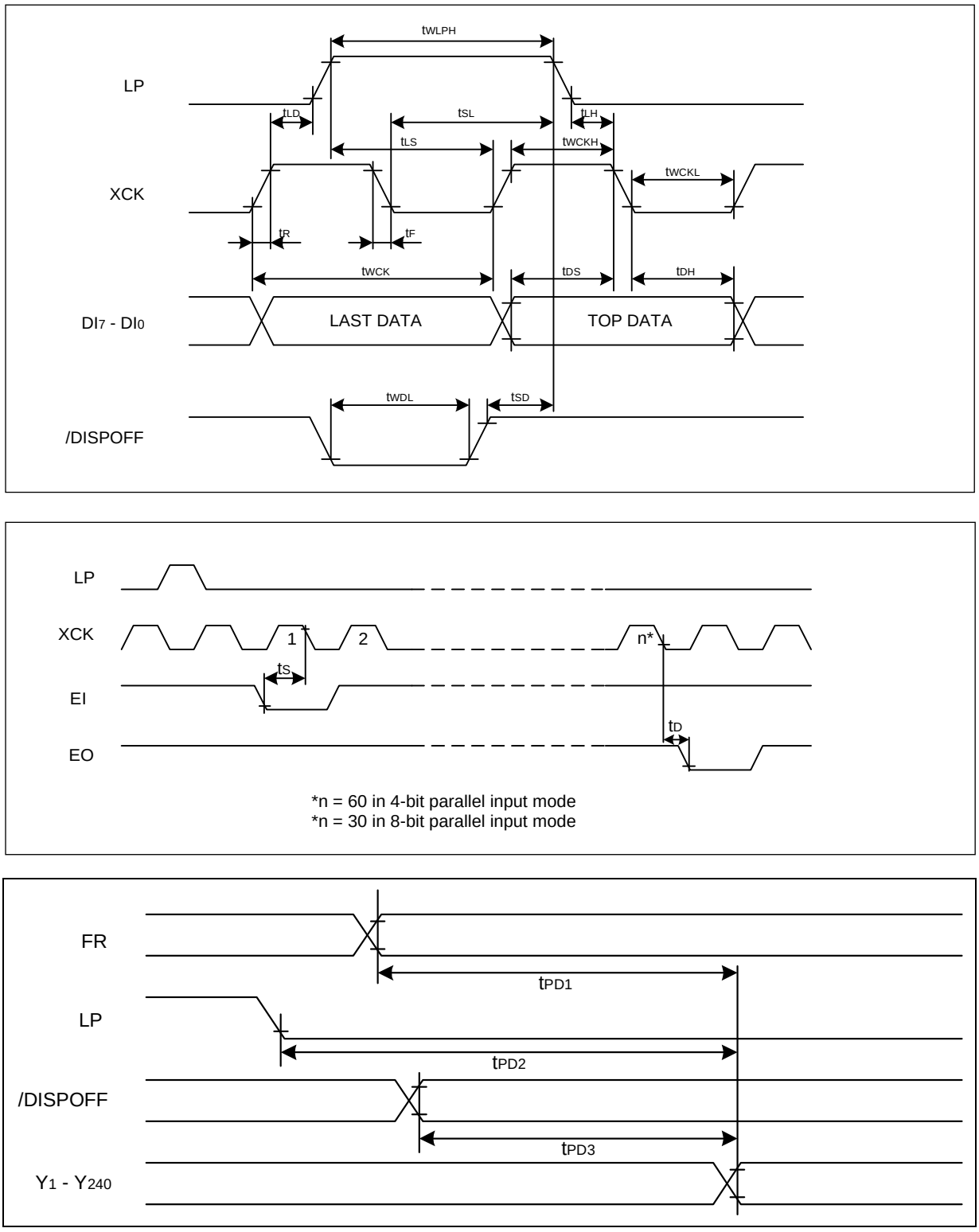
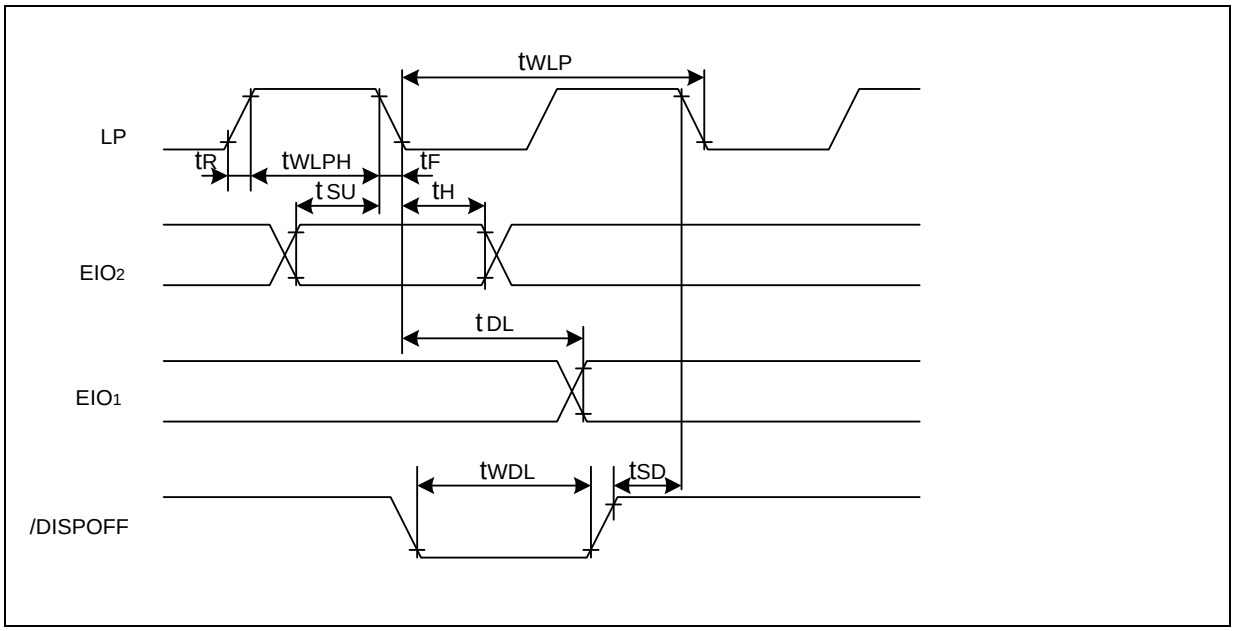
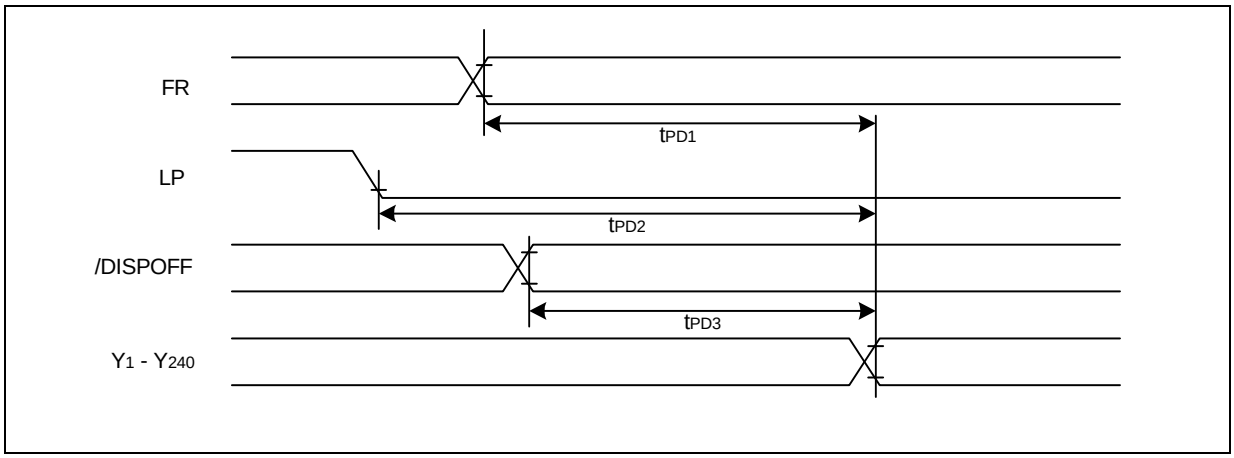


Figure 11-1 Timing Characteristics (3)

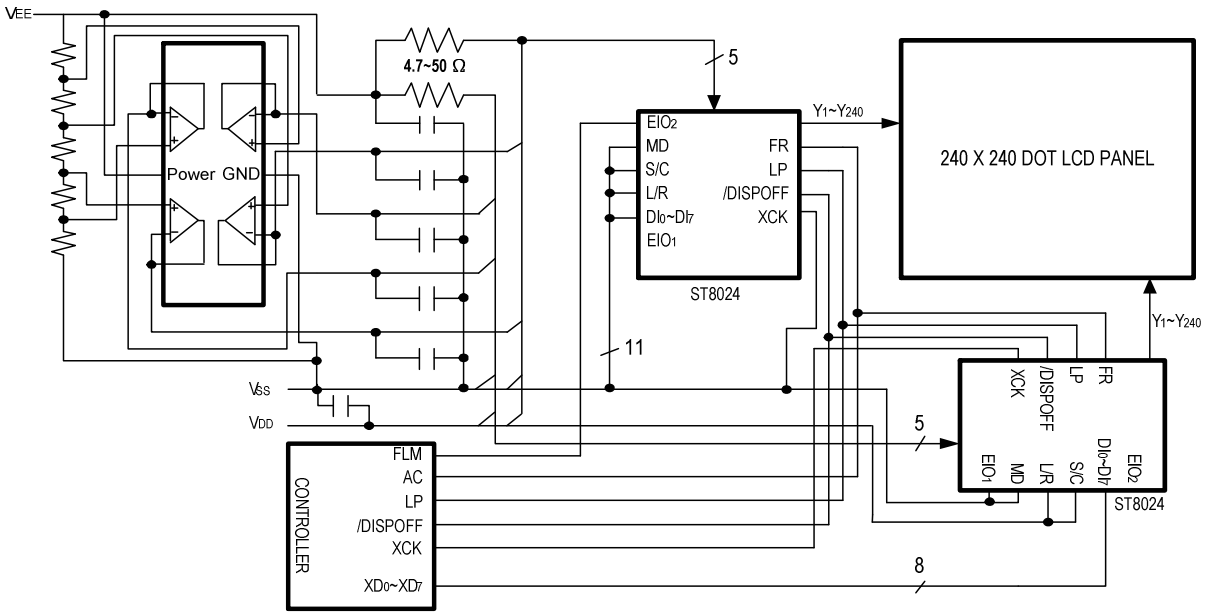
11.4 Timing Chart of Common Mode



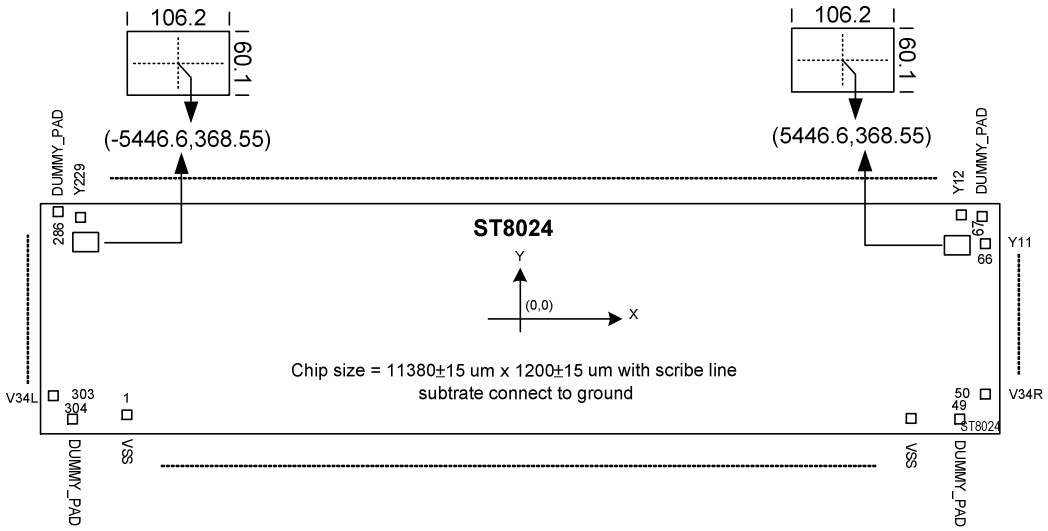


12 APPLICATION CIRCUIT

12.1 Application Circuit for Module



13 PAD DIAGRAM



Unit : um

Pad#	Name	X	Y	Pad#	Name	X	Y
1	VSS	-5464.70	-471.00	30	XCK	1191.70	-471.00
2	VSS	-5384.70	-471.00	31	DUMMY	1461.10	-471.00
3	GND	-5308.70	-471.00	32	/DISPOFF	1730.50	-471.00
4	GND	-5232.70	-471.00	33	DUMMY	1999.90	-471.00
5	VCC	-5156.70	-471.00	34	LP	2269.30	-471.00
6	VCC	-5080.70	-471.00	35	DUMMY	2538.70	-471.00
7	DUMMY	-5004.50	-471.00	36	EIO1	2808.10	-471.00
8	DBLKB	-4735.10	-471.00	37	DUMMY	3077.50	-471.00
9	DUMMY	-4465.70	-471.00	38	FR	3346.90	-471.00
10	S/C	-4196.30	-471.00	39	DUMMY	3616.30	-471.00
11	DUMMY	-3926.90	-471.00	40	L/R	3885.70	-471.00
12	EIO2	-3657.50	-471.00	41	DUMMY	4155.10	-471.00
13	DUMMY	-3388.10	-471.00	42	MD	4424.50	-471.00
14	DI0	-3118.70	-471.00	43	DUMMY	4693.90	-471.00
15	DUMMY	-2849.30	-471.00	44	TEST1	4963.30	-471.00
16	DI1	-2579.90	-471.00	45	GND	5232.70	-471.00
17	DUMMY	-2310.50	-471.00	46	GND	5308.70	-471.00
18	DI2	-2041.10	-471.00	47	VSS	5384.70	-471.00
19	DUMMY	-1771.70	-471.00	48	VSS	5464.70	-471.00
20	DI3	-1502.30	-471.00	49	DUMMY	5551.50	-471.00
21	DUMMY	-1232.90	-471.00	50	V34R	5557.00	-394.80
22	DI4	-963.50	-471.00	51	V34R	5557.00	-344.80
23	DUMMY	-694.10	-471.00	52	V12R	5557.00	-294.80
24	DI5	-424.70	-471.00	53	V12R	5557.00	-244.80
25	DUMMY	-155.30	-471.00	54	V0R	5557.00	-194.80
26	DI6	114.10	-471.00	55	V0R	5557.00	-144.80
27	DUMMY	383.50	-471.00	56	Y1	5557.00	-94.80
28	DI7	652.90	-471.00	57	Y2	5557.00	-44.80
29	DUMMY	922.30	-471.00	58	Y3	5557.00	5.20

59	Y4	5557.00	55.20	109	Y53	3375.00	467.00
60	Y5	5557.00	105.20	110	Y54	3325.00	467.00
61	Y6	5557.00	155.20	111	Y55	3275.00	467.00
62	Y7	5557.00	205.20	112	Y56	3225.00	467.00
63	Y8	5557.00	255.20	113	Y57	3175.00	467.00
64	Y9	5557.00	305.20	114	Y58	3125.00	467.00
65	Y10	5557.00	355.20	115	Y59	3075.00	467.00
66	Y11	5557.00	405.20	116	Y60	3025.00	467.00
67	DUMMY	5551.50	474.00	117	Y61	2975.00	467.00
68	Y12	5425.00	467.00	118	Y62	2925.00	467.00
69	Y13	5375.00	467.00	119	Y63	2875.00	467.00
70	Y14	5325.00	467.00	120	Y64	2825.00	467.00
71	Y15	5275.00	467.00	121	Y65	2775.00	467.00
72	Y16	5225.00	467.00	122	Y66	2725.00	467.00
73	Y17	5175.00	467.00	123	Y67	2675.00	467.00
74	Y18	5125.00	467.00	124	Y68	2625.00	467.00
75	Y19	5075.00	467.00	125	Y69	2575.00	467.00
76	Y20	5025.00	467.00	126	Y70	2525.00	467.00
77	Y21	4975.00	467.00	127	Y71	2475.00	467.00
78	Y22	4925.00	467.00	128	Y72	2425.00	467.00
79	Y23	4875.00	467.00	129	Y73	2375.00	467.00
80	Y24	4825.00	467.00	130	Y74	2325.00	467.00
81	Y25	4775.00	467.00	131	Y75	2275.00	467.00
82	Y26	4725.00	467.00	132	Y76	2225.00	467.00
83	Y27	4675.00	467.00	133	Y77	2175.00	467.00
84	Y28	4625.00	467.00	134	Y78	2125.00	467.00
85	Y29	4575.00	467.00	135	Y79	2075.00	467.00
86	Y30	4525.00	467.00	136	Y80	2025.00	467.00
87	Y31	4475.00	467.00	137	Y81	1975.00	467.00
88	Y32	4425.00	467.00	138	Y82	1925.00	467.00
89	Y33	4375.00	467.00	139	Y83	1875.00	467.00
90	Y34	4325.00	467.00	140	Y84	1825.00	467.00
91	Y35	4275.00	467.00	141	Y85	1775.00	467.00
92	Y36	4225.00	467.00	142	Y86	1725.00	467.00
93	Y37	4175.00	467.00	143	Y87	1675.00	467.00
94	Y38	4125.00	467.00	144	Y88	1625.00	467.00
95	Y39	4075.00	467.00	145	Y89	1575.00	467.00
96	Y40	4025.00	467.00	146	Y90	1525.00	467.00
97	Y41	3975.00	467.00	147	Y91	1475.00	467.00
98	Y42	3925.00	467.00	148	Y92	1425.00	467.00
99	Y43	3875.00	467.00	149	Y93	1375.00	467.00
100	Y44	3825.00	467.00	150	Y94	1325.00	467.00
101	Y45	3775.00	467.00	151	Y95	1275.00	467.00
102	Y46	3725.00	467.00	152	Y96	1225.00	467.00
103	Y47	3675.00	467.00	153	Y97	1175.00	467.00
104	Y48	3625.00	467.00	154	Y98	1125.00	467.00
105	Y49	3575.00	467.00	155	Y99	1075.00	467.00
106	Y50	3525.00	467.00	156	Y100	1025.00	467.00
107	Y51	3475.00	467.00	157	Y101	975.00	467.00
108	Y52	3425.00	467.00	158	Y102	925.00	467.00

159	Y103	875.00	467.00	209	Y153	-1625.00	467.00
160	Y104	825.00	467.00	210	Y154	-1675.00	467.00
161	Y105	775.00	467.00	211	Y155	-1725.00	467.00
162	Y106	725.00	467.00	212	Y156	-1775.00	467.00
163	Y107	675.00	467.00	213	Y157	-1825.00	467.00
164	Y108	625.00	467.00	214	Y158	-1875.00	467.00
165	Y109	575.00	467.00	215	Y159	-1925.00	467.00
166	Y110	525.00	467.00	216	Y160	-1975.00	467.00
167	Y111	475.00	467.00	217	Y161	-2025.00	467.00
168	Y112	425.00	467.00	218	Y162	-2075.00	467.00
169	Y113	375.00	467.00	219	Y163	-2125.00	467.00
170	Y114	325.00	467.00	220	Y164	-2175.00	467.00
171	Y115	275.00	467.00	221	Y165	-2225.00	467.00
172	Y116	225.00	467.00	222	Y166	-2275.00	467.00
173	Y117	175.00	467.00	223	Y167	-2325.00	467.00
174	Y118	125.00	467.00	224	Y168	-2375.00	467.00
175	Y119	75.00	467.00	225	Y169	-2425.00	467.00
176	Y120	25.00	467.00	226	Y170	-2475.00	467.00
177	Y121	-25.00	467.00	227	Y171	-2525.00	467.00
178	Y122	-75.00	467.00	228	Y172	-2575.00	467.00
179	Y123	-125.00	467.00	229	Y173	-2625.00	467.00
180	Y124	-175.00	467.00	230	Y174	-2675.00	467.00
181	Y125	-225.00	467.00	231	Y175	-2725.00	467.00
182	Y126	-275.00	467.00	232	Y176	-2775.00	467.00
183	Y127	-325.00	467.00	233	Y177	-2825.00	467.00
184	Y128	-375.00	467.00	234	Y178	-2875.00	467.00
185	Y129	-425.00	467.00	235	Y179	-2925.00	467.00
186	Y130	-475.00	467.00	236	Y180	-2975.00	467.00
187	Y131	-525.00	467.00	237	Y181	-3025.00	467.00
188	Y132	-575.00	467.00	238	Y182	-3075.00	467.00
189	Y133	-625.00	467.00	239	Y183	-3125.00	467.00
190	Y134	-675.00	467.00	240	Y184	-3175.00	467.00
191	Y135	-725.00	467.00	241	Y185	-3225.00	467.00
192	Y136	-775.00	467.00	242	Y186	-3275.00	467.00
193	Y137	-825.00	467.00	243	Y187	-3325.00	467.00
194	Y138	-875.00	467.00	244	Y188	-3375.00	467.00
195	Y139	-925.00	467.00	245	Y189	-3425.00	467.00
196	Y140	-975.00	467.00	246	Y190	-3475.00	467.00
197	Y141	-1025.00	467.00	247	Y191	-3525.00	467.00
198	Y142	-1075.00	467.00	248	Y192	-3575.00	467.00
199	Y143	-1125.00	467.00	249	Y193	-3625.00	467.00
200	Y144	-1175.00	467.00	250	Y194	-3675.00	467.00
201	Y145	-1225.00	467.00	251	Y195	-3725.00	467.00
202	Y146	-1275.00	467.00	252	Y196	-3775.00	467.00
203	Y147	-1325.00	467.00	253	Y197	-3825.00	467.00
204	Y148	-1375.00	467.00	254	Y198	-3875.00	467.00
205	Y149	-1425.00	467.00	255	Y199	-3925.00	467.00
206	Y150	-1475.00	467.00	256	Y200	-3975.00	467.00
207	Y151	-1525.00	467.00	257	Y201	-4025.00	467.00
208	Y152	-1575.00	467.00	258	Y202	-4075.00	467.00

259	Y203	-4125.00	467.00	282	Y226	-5275.00	467.00
260	Y204	-4175.00	467.00	283	Y227	-5325.00	467.00
261	Y205	-4225.00	467.00	284	Y228	-5375.00	467.00
262	Y206	-4275.00	467.00	285	Y229	-5425.00	467.00
263	Y207	-4325.00	467.00	286	DUMMY	-5551.50	474.00
264	Y208	-4375.00	467.00	287	Y230	-5557.00	405.20
265	Y209	-4425.00	467.00	288	Y231	-5557.00	355.20
266	Y210	-4475.00	467.00	289	Y232	-5557.00	305.20
267	Y211	-4525.00	467.00	290	Y233	-5557.00	255.20
268	Y212	-4575.00	467.00	291	Y234	-5557.00	205.20
269	Y213	-4625.00	467.00	292	Y235	-5557.00	155.20
270	Y214	-4675.00	467.00	293	Y236	-5557.00	105.20
271	Y215	-4725.00	467.00	294	Y237	-5557.00	55.20
272	Y216	-4775.00	467.00	295	Y238	-5557.00	5.20
273	Y217	-4825.00	467.00	296	Y239	-5557.00	-44.80
274	Y218	-4875.00	467.00	297	Y240	-5557.00	-94.80
275	Y219	-4925.00	467.00	298	V0L	-5557.00	-144.80
276	Y220	-4975.00	467.00	299	V0L	-5557.00	-194.80
277	Y221	-5025.00	467.00	300	V12L	-5557.00	-244.80
278	Y222	-5075.00	467.00	301	V12L	-5557.00	-294.80
279	Y223	-5125.00	467.00	302	V34L	-5557.00	-344.80
280	Y224	-5175.00	467.00	303	V34L	-5557.00	-394.80
281	Y225	-5225.00	467.00	304	DUMMY	-5551.50	-471.00

13.1 Gold Bump Size

Pad No.	X	Y	Area (um^2)
1~48(not DUMMY)	58	60	3480
50~66,287~303	74	35	2590
7~43(DUMMY only)	58	60	3480
68~285	35	74	2590
49,67,286,304	85	60	5100

Wafer thickness = 675±20um, Bump pad height = 15um, strength=30g

14 APPLITION NOTE (REFERENCE ONLY)

14.1 PCB and ITO layout notice:

Pin Name	ITO Resistor Values
LGND, GND, VDD, Vss	Less than 75Ω when VDD ≧ 3.0V, and the smaller the better
V0R, V0L	Less than 150Ω, and the smaller the better
V12R, V12L, V34R, V12L	Less than 250Ω, and the smaller the better

PS : Above resistor value test on 3” LCD panel.

14.2 We suggest the ITO resistor for LCD panel is less than 15Ω/Square, and the resistor value is as smaller as better.

14.3 Adjust V1 and V4 voltage to keep the V0-V1 = V4-VSS relation to get better display quality. The (V0-V1)-(V4-VSS) value had better less than 100mV.

14.4 Add 0.1uF high frequency by-pass capacitor to filter the noise on V0~V4 to VSS.

14.5 When OP follower circuit is used, please be sure the OP power is higher than V0 at least 1.5V.

14.6 EIO1 and EIO2 is enable pin for driver, please pay attention to the distance to avoid noise when cascade function is used. Two chip connecting distance is as shorter as better.

15 REVISION

REVISION	DESCRIPTION	PAGE	DATE
0.20	Add pad location and gold bump data		
0.21	Add BLANK contrast control information		
0.24	Add TCP (F4) information		
0.25	Remove TCP information to another PDF file ST8024TCP(F4).PDF		
0.26	Gold bump strength=30g, update IC diagram		
0.27	Correct wrong word mistake		
0.28	Correct parameter name		
0.29	Correct DI to FLM		
0.30	Change operating temperature from -20°C~85°C to -25°C~85°C		
0.31	Change description of TEST1 pin in PIN DESCRIPTION(TCP)		
1.0	Add 1 and 48 Gold Bump size		
1.2	Modify TCP package		
1.3	Rename V5 to Vss and some pins' description		
1.4	Modify PAD sequence		
1.5	Add alignment mark		
1.6	Add max value for input high voltage	16	2006/12/11
1.7	Add wafer thickness information and roughly TCP drawing information. Modify chip size and thickness with scribe line and Spec arrangement	1-27	2006/12/25
1.8	Modify all the data about absolute max voltage and recommend max voltage	2,16-19	2007/05/25
1.9	Modify Pad Diagram	23	2008/1/14
2.0	Add application note	27	2008/05/07
2.1	Modify Pad Location	24	2009/0819

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