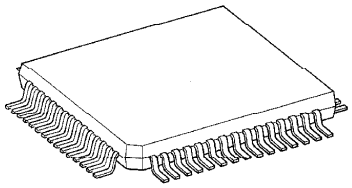
TOSHIBA CMOS DIGITAL INTEGRATED CIRCUIT SILICON MONOLITHIC

T7933

ROW DRIVER LSI FOR DOT MATRIX LCD

The T7933 is a row (common) driver LSI for a small- or medium-scale dot matrix LCD. The T7933 realizes low power LCD systems using the CMOS Si-Gate process.
The T7933 generates timing signals for the display using a built-in oscillator and also controls the T7932 column (segment) LCD driver.
Five duty options are available : 1/8, 1/12, 1/16, 1/24 and 1/32. The T7933 has 32 low-impedance output row drivers (1kΩ max).
The T7933 includes internal resistors to the divide bias voltage for 1/16 duty and 1/32 duty displays.



QFP60-P-1414-0.80A

Weight: 1.1g (typ.)

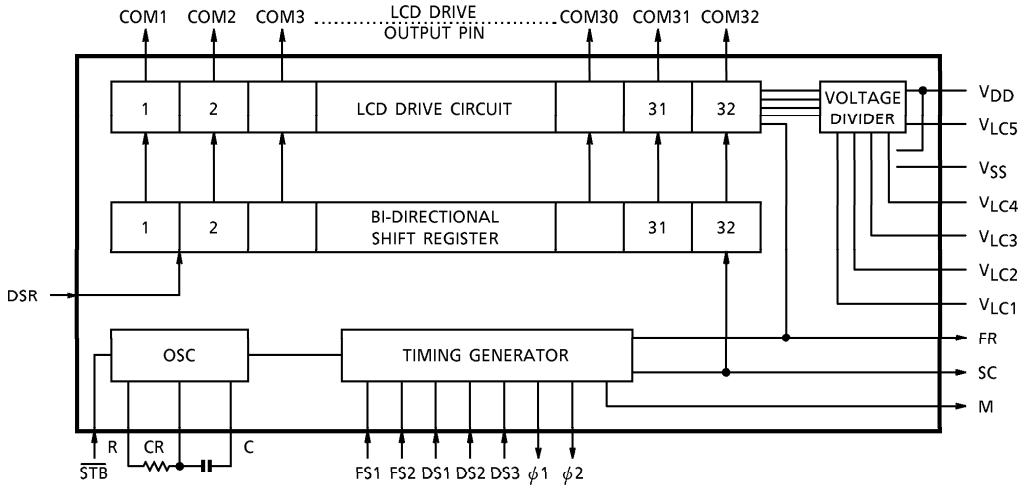
FEATURES

- Row signal output for LCD
- LCD drive outputs : 32 (low impedance)
- Built-in oscillator (additional external resistor and capacitor)
- Built-in voltage dividers for 1/16 and 1/32 duty cycle
- Duty : 1/8, 1/12, 1/16, 1/24, 1/32
- Low power consumption
- Logic power supply : $V_{DD} = 5V \pm 10\%$
- 60-pin flat plastic package

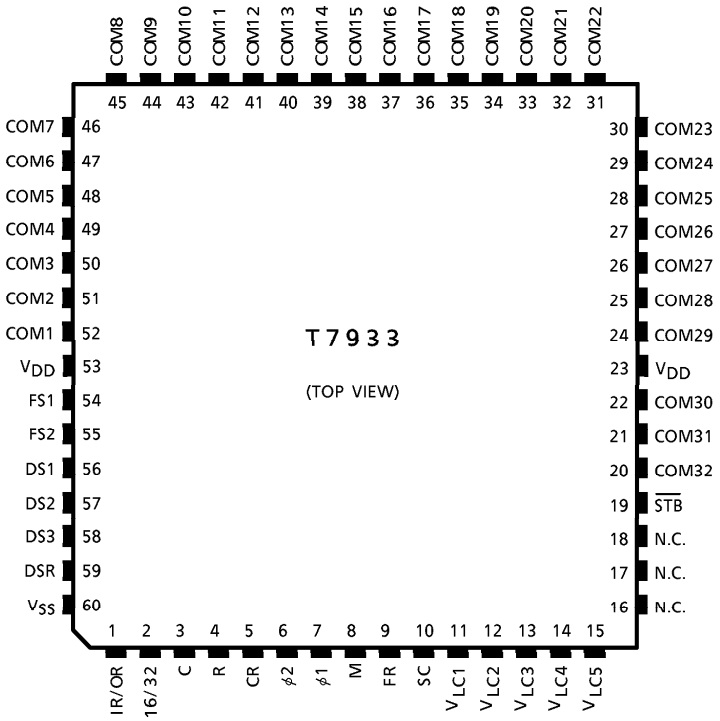
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BLOCK DIAGRAM



PIN ASSIGNMENT



PIN FUNCTIONS

<table>
<tr><th>PIN NAME</th><th>I/O</th><th>FUNCTIONS</th><th>SIGNAL VOLTAGE</th></tr>
<tr><td>COM1 to COM32</td><td>Output</td><td>LCD drive signal outputs</td><td>V_{DD} to V_{LC5}</td></tr>
<tr><td>CR, R, C</td><td>—</td><td>Pins for oscillator</td><td>—</td></tr>
<tr><td>FR</td><td>Output</td><td>Frame signal output</td><td>V_{DD} to V_{SS}</td></tr>
<tr><td>SC</td><td>Output</td><td>Shift clock pulse output</td><td>V_{DD} to V_{SS}</td></tr>
<tr><td>M</td><td>Output</td><td>Display synchronous signal</td><td>V_{DD} to V_{SS}</td></tr>
<tr><td>DS1 to DS3</td><td>Input</td><td>Display select pin
<table>
<tr><th>DISPLAY DUTY</th><th>1/8</th><th>1/16</th><th>1/12</th><th>1/32</th><th>1/24</th></tr>
<tr><td>DS1</td><td>L</td><td>L</td><td>L</td><td>H</td><td>H</td></tr>
<tr><td>DS2</td><td>L</td><td>H</td><td>H</td><td>L</td><td>L</td></tr>
<tr><td>DS3</td><td>L</td><td>L</td><td>H</td><td>L</td><td>H</td></tr>
</table></td><td>V_{DD} to V_{SS}</td></tr>
<tr><td>FS1, FS2</td><td>Input</td><td>Selects frequency
Select oscillation frequency
The relation between f_{FR} and f_{osc} is as follows:
<table>
<tr><th>FS1</th><th>FS2</th><th>f_{osc} (kHz)</th><th>f_M (Hz)</th><th>f_{FR}</th><th>f_{CP} (kHz)</th></tr>
<tr><td>L</td><td>L</td><td>107.5</td><td>70</td><td>35</td><td>53.8</td></tr>
<tr><td>H</td><td>L</td><td>107.5</td><td>70</td><td>35</td><td>53.8</td></tr>
<tr><td>L</td><td>H</td><td>215.0</td><td>70</td><td>35</td><td>107.5</td></tr>
<tr><td>H</td><td>H</td><td>430.0</td><td>70</td><td>35</td><td>215.0</td></tr>
</table>
f_{osc} : Oscillation frequency
f_M : Synchronous signal frequency
f_{FR} : Frame frequency
f_{CP} : Frequencies of $\phi 1$, $\phi 2$</td><td>V_{DD} to V_{SS}</td></tr>
<tr><td>$\overline{STB}$</td><td>Input</td><td>Input pin for test: usually connected to V_{DD}</td><td>—</td></tr>
<tr><td>DSR</td><td>Input</td><td>Shift Register Shift direction select pin
<table>
<tr><th>DSR</th><th>SHIFT DIRECTION</th></tr>
<tr><td>H</td><td>COM1→COM32</td></tr>
<tr><td>L</td><td>COM32→COM1</td></tr>
</table></td><td>V_{DD} to V_{SS}</td></tr>
<tr><td>$\phi 1$, $\phi 2$</td><td>Output</td><td>Operating clock output pins for T7932
The frequency of $\phi 1$, $\phi 2 = fosc \times \frac{1}{2}$</td><td>$V_{DD}$ to V_{SS}</td></tr>
<tr><td>IR/OR</td><td>Input</td><td>IR/OR = H : LCD power supply divided by built-in voltage divider
IR/OR = L : LCD power supply external input</td><td>V_{DD} to V_{SS}</td></tr>
</table>

PIN NAME	I / O	FUNCTIONS	SIGNAL VOLTAGE
16 / 32	Input	Select voltage divide factor. (LCD voltage supply using built-in divider) 16 / 32 = H : $\frac{1}{16}$ duty, 16 / 32 = L : $\frac{1}{32}$ duty	V_{DD} to V_{SS}
V_{LC1} to V_{LC5}	—	Power supply for LCD drive ● When IR / OR = H V_{LC1}, V_{LC4} : Output V_{LC2}, V_{LC3} : Output V_{LC5} : Input ● When IR / OR = L V_{LC1}, V_{LC4}, V_{LC5} : Input V_{LC2}, V_{LC3} : High Impedance	—
V_{DD}	—	Power supply (5V)	
V_{SS}	—	Power supply (0V)	

FUNCTION OF EACH BLOCK

- On-chip oscillator

  The T7933 includes a built-in oscillator. (An external resistor must be connected between R and CR, and an external capacitor must be connected between C and CR). The external resistor and capacitor cause the oscillation frequency to change.

- Timing generator

  This circuit divides the oscillation frequency and generates display timing signals suitable for the duty factor. The DS1 to DS3 inputs set the duty factor.

- Bi-directional shift register

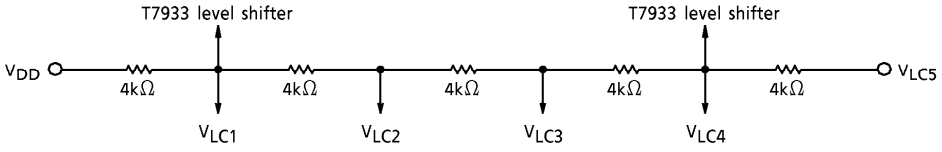
  The T7933 has a 32-bit bi-directional shift register. The DSR input sets the shift direction. The data shift is synchronized to the SC signal.

- LCD driver

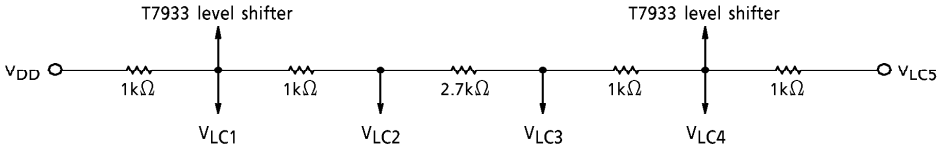
  The T7933 has 32 row drivers and four LCD drive voltage output levels. The display data latched from the latch circuit and the FR signal select one of the four LCD drive voltage levels.

- On-chip voltage divider (IR / OR = H)

  (1) 16 / 32 = H



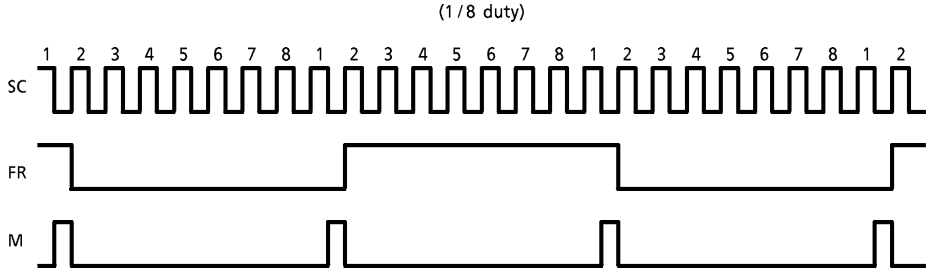
  (2) 16 / 32 = L



(Note 1) The T7933 can receive an external power supply via V_{LC1} and V_{LC4} when IR / OR = L.

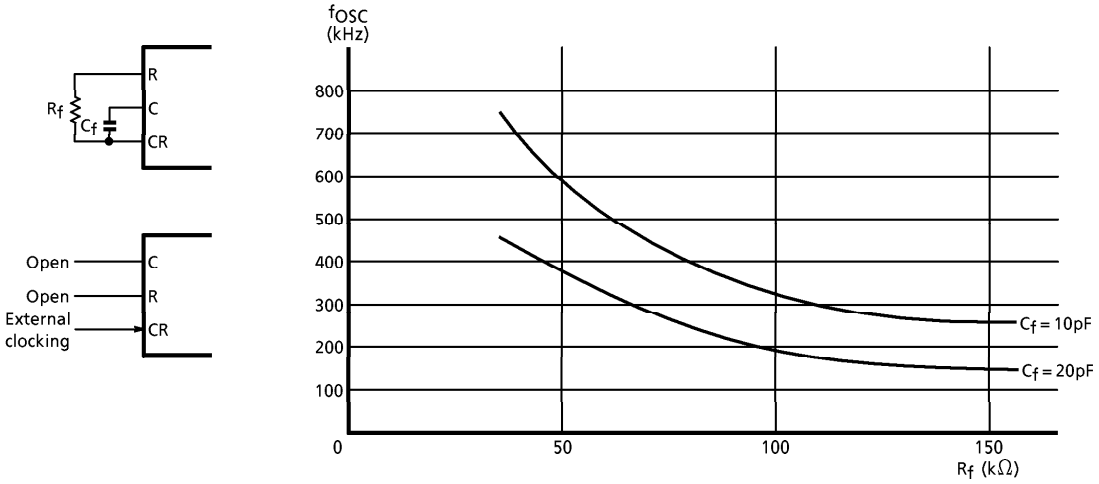
(Note 2) The T7933 can supply power to an external driver via V_{LC2} and V_{LC3} when IR / OR = H.

RELATION BETWEEN SC, FR AND M OF RELATIONAL



RELATION BETWEEN OSCILLATION FREQUENCY, RF AND CF

R_f, C_f connection



ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

ITEM	SYMBOL	RATING	UNIT
Supply Voltage (1)	V_{DD} (Note 1)	− 0.3 to 7.0	V
Supply Voltage (2)	V_{LC1}, V_{LC4}, V_{LC5} (Note 1, 2)	V_{DD} − 13.5 to V_{DD} + 0.3	V
Input Voltage	V_{IN} (Note 1)	− 0.3 to V_{DD} + 0.3	V
Operating Temperature	T_{opr}	− 20 to 75	°C
Storage Temperature	T_{stg}	− 55 to 125	°C

(Note 1) Referenced to V_{SS} = 0V
(Note 2) Ensure that the following condition is always maintained.
$V_{DD} \geqq V_{LC1} \geqq V_{LC4} \geqq V_{LC5}$

ELECTRICAL CHARACTERISTICS
DC CHARACTERISTICS
TEST CONDITIONS (Unless otherwise noted, V_{SS} = 0V, V_{DD} = 5.0V ± 10%, V_{LC5} = 0V, Ta = − 20 to 75°C)

ITEM		SYM-BOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Operating Voltage (1)		—	—	—	4.5	5.0	5.5	V	V_{DD}
Operating Voltage (2)		—	—	—	V_{DD} − 11	—	V_{DD} − 3.0	V	V_{LC5}
Input Voltage	H Level	V_{IH}	—	—	V_{DD} − 1.0	—	V_{DD}	V	CR, FS1, FS2, DS1 to DS3, M, $\overline{STB}$, IR / OR, DSR, 16 / 32, SC
	L Level	V_{IL}	—	—	0	—	1.0	V	
Output Voltage	H Level	V_{OH}	—	—	V_{DD} − 0.3	—	V_{DD}	V	M, FR, SC, ϕ1, ϕ2
	L Level	V_{OL}	—	—	0	—	0.3	V	M, FR, SC, ϕ1, ϕ2
Output Voltage	H Level	V_{OH}	—	—	V_{DD} − 0.3	—	V_{DD}	V	COM1 to COM32
	M Level	V_{OM}	—	$V_{LC1} = V_1$	V_1 − 0.3	—	V_1 + 0.3	V	COM1 to COM32
				$V_{LC4} = V_4$	V_4 − 0.3	—	V_4 + 0.3	V	COM1 to COM32
				$V_{LC2} = V_2$	V_2 − 0.3	—	V_2 + 0.3	V	V_{LC2}
				$V_{LC3} = V_3$	V_3 − 0.3	—	V_3 + 0.3	V	V_{LC3}
	L Level	V_{OL}	—	—	V_5	—	V_5 + 0.3	V	COM1 to COM32

ITEM		SYM-BOL	TEST CIR-CUIT	TEST CONDITIONS	MIN	TYP.	MAX	UNIT	PIN NAME
Output Resist-ance	H Level	R_{OH}	—	$V_{OUT} = V_{DD} - 0.5V$	—	—	1.0	kΩ	M, FR, SC, ϕ1, ϕ2
	L Level	R_{OL}	—	$V_{OUT} = 0.5V$	—	—	1.0	kΩ	M, FR, SC, ϕ1, ϕ2
Output Resist-ance	H Level	R_{OH}	—	$V_{OUT} = V_{DD} - 0.5V$	—	—	1.0	kΩ	COM1 to COM32
	M Level	R_{OM}	—	$V_{LC1} = V_1$, $V_{OUT} = V_1 \pm 0.5V$	—	—	1.0	kΩ	COM1 to COM32
				$V_{LC4} = V_4$, $V_{OUT} = V_4 \pm 0.5V$	—	—	1.0	kΩ	COM1 to COM32
	L Level	R_{OL}	—	$V_{OUT} = V_5 + 0.5V$ $V_{LC5} = V_5$	—	—	1.0	kΩ	COM1 to COM32
Operating Frequency		f_{osc}	—	Ta = – 10 to 70°C	70	—	500	kHz	CR
Current Consumption		I_{SS}	—	$V_{DD} = 5.0V$ $V_{LC5} = 0V$ $V_{LC1} = V_1$ $V_{LC4} = V_4$ $f_{osc} = 430kHz$ (Duty: 1 / 16) COM1 to COM32: No Load	—	—	400	μA	V_{SS}

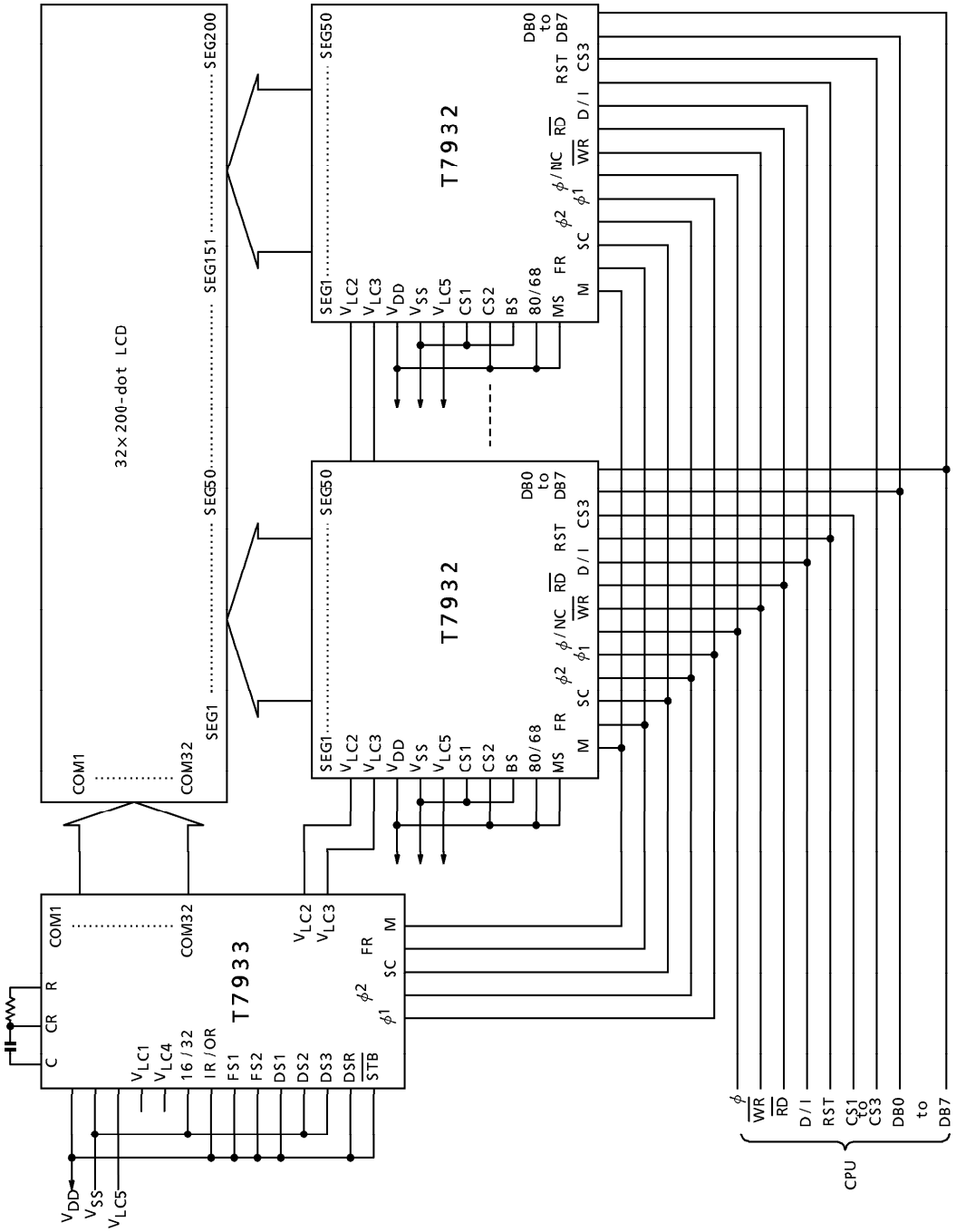
(Note 1) $V_1 = V_{DD} - \frac{1}{5}(V_{DD} - V_{LC5})$, $V_2 = V_{DD} - \frac{2}{5}(V_{DD} - V_{LC5})$

$V_4 = V_{DD} - \frac{4}{5}(V_{DD} - V_{LC5})$, $V_3 = V_{DD} - \frac{3}{5}(V_{DD} - V_{LC5})$

$V_5 = V_{LC5}$

(Note 2) Output resistance measured when the on-chip voltage dividers are not used.

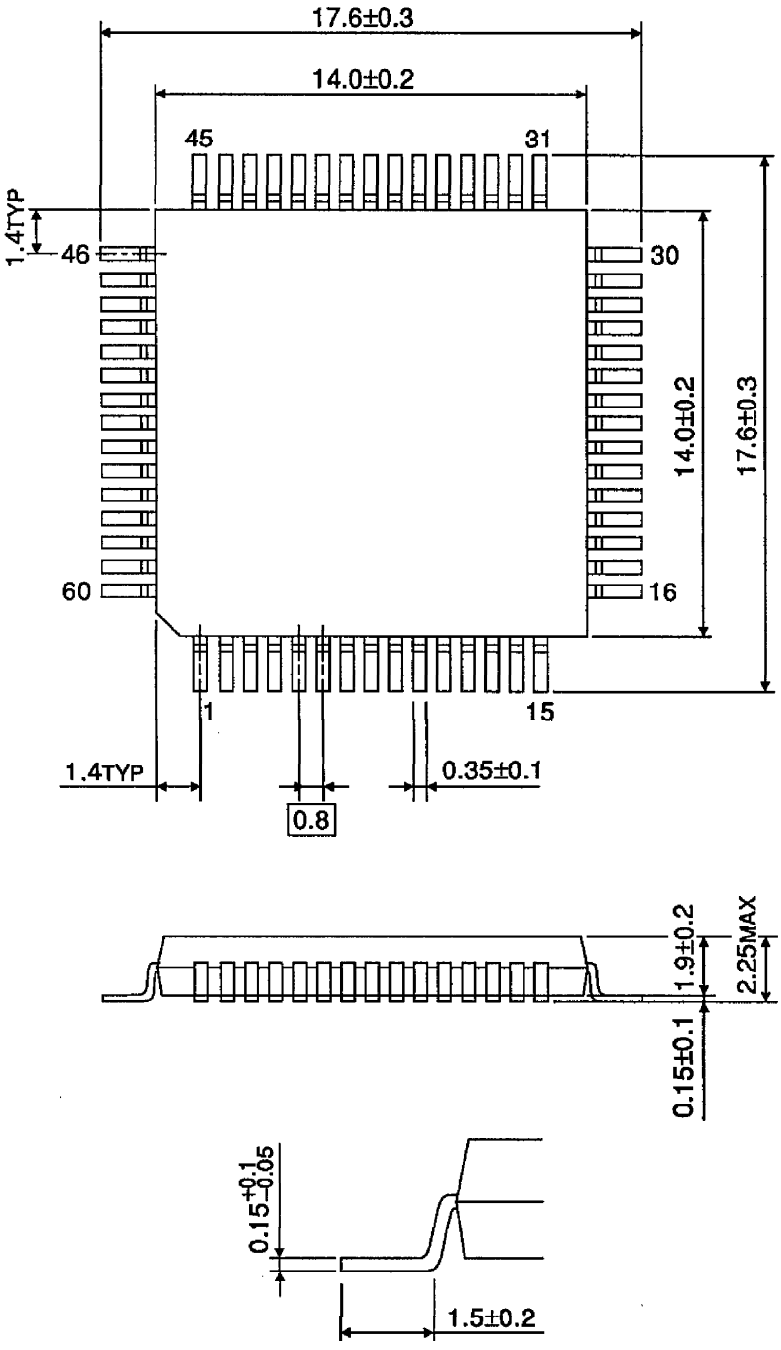
APPLICATION CIRCUIT



OUTLINE DRAWING

QFP60-P-1414-0.80A

Unit : mm



Weight : 1.1g (Typ.)