HARRIS Semiconductor

HIP2500

PART WITHDRAWN, PROCESS OBSOLETE
NO NEW DESIGNS, SEE
IR2110, IR2112
IR2113

July 1998

Half Bridge 500V_{DC} Driver

Features

- **Maximum Rating 500V**
- **Ability to Interface and Drive N-Channel Power Devices**
- **Floating Bootstrap Power Supply for Upper Rail Drive**
- **CMOS Schmitt-Triggered Inputs with Hysteresis and Pull-Down**
- **Up to 400kHz Operation**
- **Single Low Current Bias Supply**
- **Latch-Up Immune CMOS Logic**
- **Peak Drive. . . . . Up to 2.0A**
- **Gate Drive Rise Time (+125^{o}C) . . . . . < 25ns (Typ)**

Applications

- **High Frequency Switch-Mode Power Supply**
- **Induction Heating and Welding**
- **Switch Mode Amplifiers**
- **AC and DC Motor Drives**
- **Electronic Lamp Ballasts**
- **Battery Chargers**
- **UPS Inverters**
- **Noise Cancellation in Amplifier Systems**

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG NO.
HIP2500IP	-40 to +85	14 Ld PDIP	E14.3
HIP2500IP1	-40 to +85	16 Ld PDIP	E16.3
HIP2500IB	-40 to +85	16 Ld SOIC (W)	M16.3

Description

The HIP2500 is a high voltage integrated circuit (HVIC) optimized to drive N-Channel MOS gated power devices in half bridge topologies. It provides the necessary control for PWM motor drive, power supply, and UPS applications. The SD pin allows external shutdown of gate drive to both upper and lower gate outputs. Undervoltage lockout will not allow gating when the bias voltage is too low to drive the external switches into saturation.

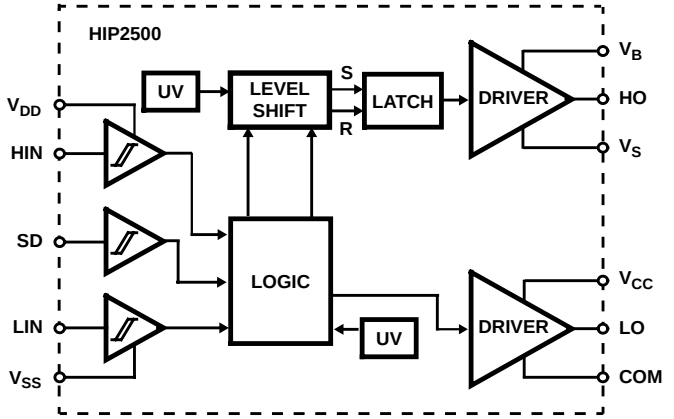
The HIP2500IP is pin and function compatible to the International Rectifier IR2110. The HIP2500 has superior ability to accept negative voltages from the V_S pin to the COM pin due to forward recovery of the lower flyback diode.

The HIP2500IB is a SOIC or small outline IC form of the HIP2500. The HIP2500IB drives high side and low side referenced power switches just like the HIP2500IP.

The HIP2500IP1 is a 16 lead Plastic DIP form of the HIP2500. Pins 4 and 5 removed from lead frame to provide extra creepage and strike distances in high voltage applications.

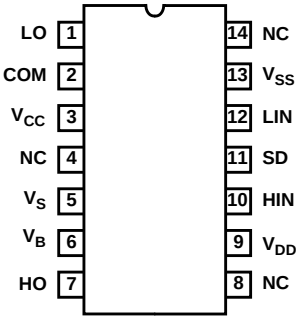
Please see Application Note AN9010 for more information.

Functional Block Diagram

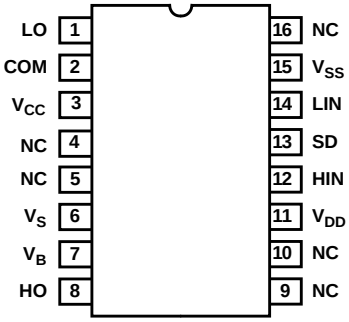


Pinouts

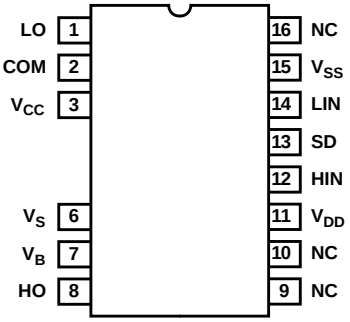
HIP2500 (PDIP)
TOP VIEW



HIP2500 (SOIC)
TOP VIEW



HIP2500 (PDIP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge. Users should follow proper I.C. Handling Procedures.

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File Number **2801.9**

Absolute Maximum Ratings

Full Temperature Range Unless Otherwise Noted, All Voltages Referenced to V_{SS} Unless Otherwise Noted.

Floating Supply Voltage, V_B . . . . . V_S-0.5V to V_S+18.0V (Positive Terminal)
Floating Supply Voltage, V_S . . . . . 500V (Common Terminal)
High Side Channel Output Voltage, V_{HO} . . . . . -0.5V to V_B+0.5V
Fixed Supply Voltage, V_{CC} . . . . . -0.5V to 18.0V
Low Side Channel Output Voltage, V_{LO} . . . . . -0.5V to V_{CC}+0.5V
Logic Supply Voltage, V_{DD} . . . . . -0.5V to 18.0V
Logic Input Voltage, V_{IN} . . . . . -0.5V to V_{DD}+0.5V [HIN, LIN & SD (Shutdown)]
V_{DD} to COM and V_{CC} to V_{SS} Voltage . . . . . -0.5V to 18.0V

Thermal Information

Thermal Resistance (Note 1, Typical)	θ_{JA}
HIP2500IP	75°C/W
HIP2500IP1	80°C/W
HIP2500IB	90°C/W

See Maximum Power Dissipation vs Temperature Curve
Junction Temperature Range . . . . . -40°C to +125°C
Storage Temperature Range, T_S . . . . . -40°C to +150°C
Operating Ambient Temperature Range, T_A . . . . . -40°C to +85°C

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Recommended DC Operating Conditions

Floating Supply Voltage, V_B . . . . . V_S+10V to V_S+15V (Floating Terminal)
High Side Channel Output Voltage, V_{HO} . . . . . 10V to V_B (With Respect to V_S)
Fixed Supply Voltage, V_{CC} . . . . . 10V to 15V
Low Side Channel Output Voltage, V_{LO} . . . . . 0V to V_{CC}
Logic Supply Voltage, V_{DD} . . . . . 4V to V_{CC}
Floating Supply Voltage, V_S . . . . . -4.0V to 500V (Common Terminal)
V_{SS} and COM potentials to be equal.

Electrical Specifications

$V_{CC} = (V_B - V_S) = V_{DD} = 15V$, COM = V_{SS} = 0, Unless Otherwise Noted

PARAMETER	SYMBOL	T_J = +25°C			T_J = -40°C TO +125°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
DC CHARACTERISTICS								
Quiescent V_{CC} Current	I_{QCC}	-	1.5	1.9	-	-	2.0	mA
Quiescent V_{BS} Current	I_{QBS}	-	300	400	-	300	435	µA
Quiescent V_{DD} Current	I_{QDD}	-	0.1	1	-	-	1.8	µA
Quiescent Leakage Current	I_S (500V)	-	0.4	3.0	-	-	-	µA
Logic Input Pulldown Current, $V_{IN} = V_{DD}$ (HIN, LIN, SD)	IN+	-	12	20	-	-	22	µA
Logic Input Leakage Current, $V_{IN} = V_{SS}$ (HIN, LIN, SD)	IN-	-	0	1	-	0	1	µA
Logic Input Positive Going Threshold (Note 2)	V_{TH}+	7.5	8.0	8.5	7.5	8.0	8.6	V
Logic Input Negative Going Threshold (Note 2)	V_{TH}-	5.5	5.9	6.3	5.5	5.9	6.4	V
Undervoltage Positive Going Threshold	UV+	8.0	9.35	9.99	7.8	-	9.99	V
Undervoltage Negative Going Threshold	UV-	7.7	9.05	9.69	7.5	-	9.69	V
Undervoltage Hysteresis (V_{CC})	UVHYS (V_{CC})	250	-	450	170	-	530	mV
Undervoltage Hysteresis (V_{BS})	UVHYS (V_{BS})	250	-	450	170	-	530	mV
Output High Open Circuit Voltage (HO, LO)	V_{OUT}+	14.95	15	-	14.95	15	-	V
Output Low Open Circuit Voltage (HO, LO)	V_{OUT}-	-	-	0.05	-	-	0.05	V
Output High Short Circuit Current (Sourcing)	I_{OUT}+	1.65	2.1	-	1.15	1.6	-	A
Output Low Short Circuit Current (Sinking)	I_{OUT}-	1.85	2.3	-	1.35	1.7	-	A

NOTE:

2. See Figure 8 for logic supply voltages other than 15.0V.

Switching Specifications

PARAMETER	SYMBOL	T_J = +25°C			T_J = -40°C TO +125°C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
HIGH SIDE CHANNEL WITH 500V OFFSET, C_L = 1000pF								
High Side Turn-On Propagation Delay	t_{ON}	320	420	525	230	-	725	ns
High Side Turn-Off Propagation Delay	t_{OFF}	260	385	450	190	-	625	ns
High Side Rise Time	t_R	-	25	50	-	25	50	ns
High Side Turn-Off Fall Time	t_F	-	25	50	-	25	50	ns
LOW SIDE CHANNEL, C_L = 1000pF								
Low Side Turn-On Propagation Delay	t_{ON}	250	365	450	190	-	600	ns
Low Side Turn-Off Propagation Delay	t_{OFF}	175	295	370	125	-	475	ns
Low Side Turn-On Rise Time	t_R	-	25	50	-	30	50	ns
Low Side Turn-Off Fall Time	t_F	-	25	50	-	30	50	ns
Shutdown Propagation Delay High Side Shutdown	t_{SDHO}	300	400	490	200	-	650	ns
Low Side Shutdown	t_{SDLO}	175	320	400	125	-	500	ns
HIGH SIDE CHANNEL WITH 500V OFFSET, C_L = 1000pF								
Turn-On Propagation Delay Matching (Between HO and LO)	M_t	0	-	125	0	-	185	ns
Minimum On Output Pulse Width (HO, LO)	$PW_{OUT(MIN)}$	-	35	50	-	35	55	ns
Minimum Off Output Pulse Width (HO, LO)	$PW_{\overline{OUT}MIN}$	275	440	640	250	440	650	ns
Minimum On Input Pulse Width (HIN, LIN)	$PW_{ON(MIN)}$	-	100	145	-	100	175	ns
Minimum Off Input Pulse Width (HIN, LIN)	$PW_{OFF(MIN)}$	-	110	200	-	110	220	ns
Deadtime LO Turn-Off to HO Turn-On	DHt_{ON}	-	125	-	-	125	-	ns
Deadtime HO Turn-Off to LO Turn-On	DLt_{ON}	-	-20	-	-	-20	-	ns
MAXIMUM TRANSIENT CONDITIONS								
Offset Supply Operating Transient	dV_S/dt	-	-	50	-	-	50	V/ns

Logic Truth Table

HIN	LIN	UV_H	UV_L	SD	HO	LO	COMMENTS
0	0	0	0	0	0	0	Normal Off
0	1	0	0	0	0	1	Lower On
1	0	0	0	0	1	0	Upper On
1	1	0	0	0	1	1	Both On
X	X	X	X	1	0	0	Chip Disabled
X	X	1	1	X	0	0	V_{CC} UV Lockout and V_{BS} Lockout
X	1	1	0	0	0	1	V_{BS} UV Lockout
1	X	0	1	0	1	0	V_{CC} UV Lockout

Typical Performance Curves

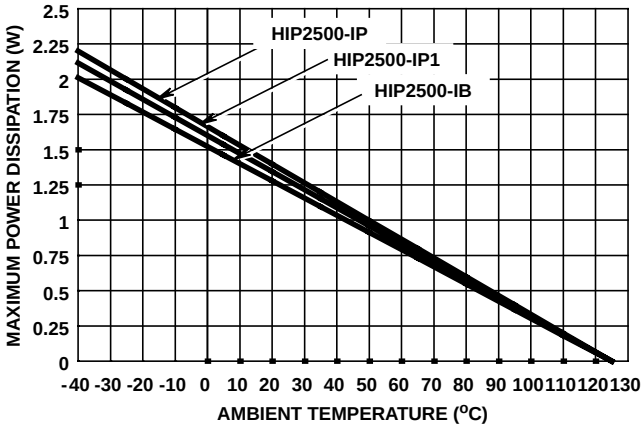


FIGURE 1. MAXIMUM POWER DISSIPATION vs TEMPERATURE

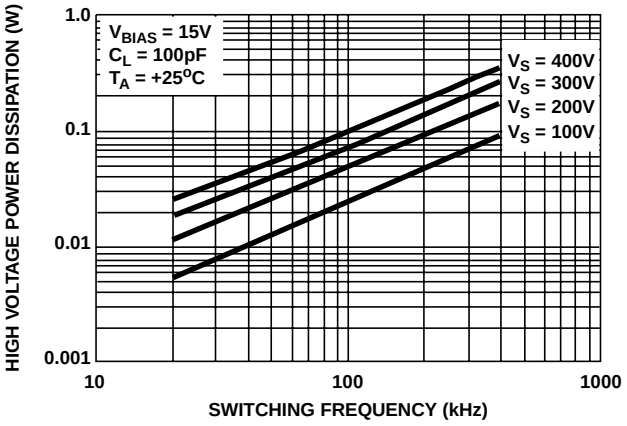
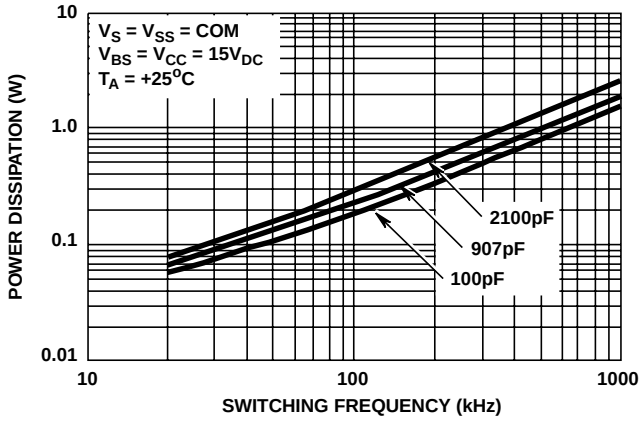


FIGURE 2. HIGH VOLTAGE POWER DISSIPATION vs SWITCHING FREQUENCY



NOTE: All switching losses assumed to be in IC.

FIGURE 3. LOW VOLTAGE POWER DISSIPATION vs FREQUENCY

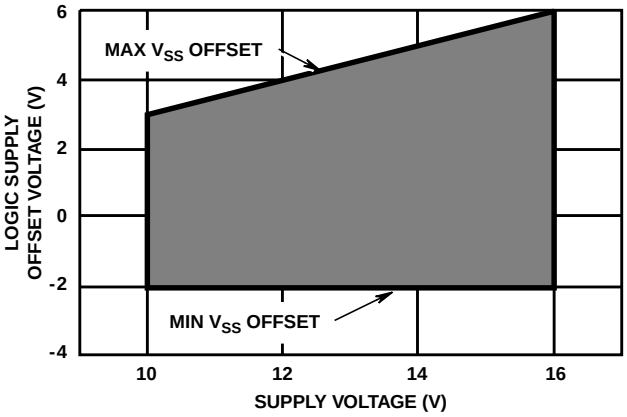


FIGURE 4. V_{SS} OFFSET vs V_{CC} SUPPLY VOLTAGE

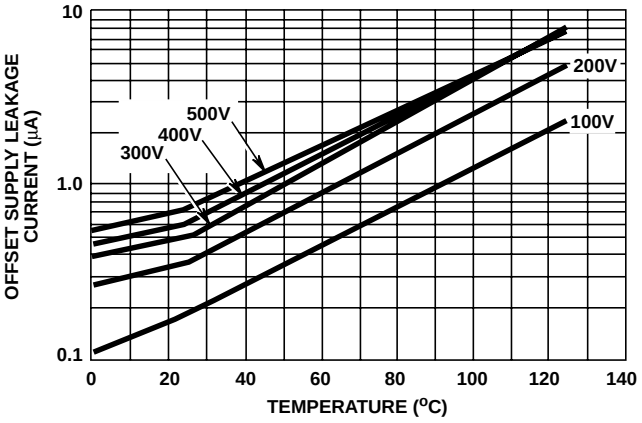


FIGURE 5. OFFSET SUPPLY LEAKAGE vs TEMPERATURE

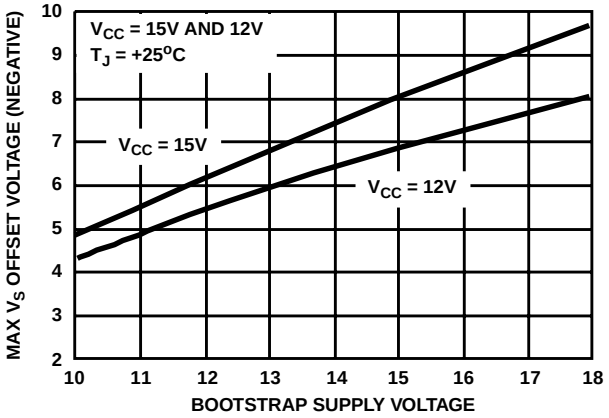


FIGURE 6. MAXIMUM NEGATIVE V_S OFFSET VOLTAGE vs V_{BS} VOLTAGE

Typical Performance Curves (Continued)

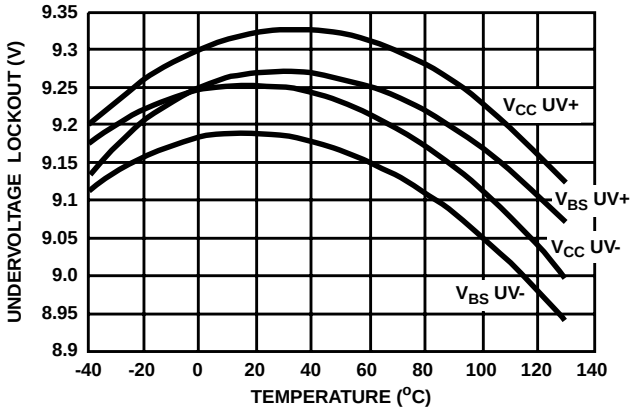


FIGURE 7. UNDERVOLTAGE LOCKOUT vs TEMPERATURE

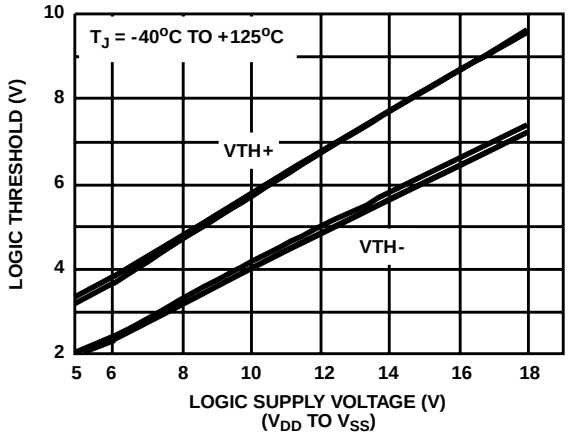


FIGURE 8. INPUT LOGIC THRESHOLD vs SUPPLY VOLTS

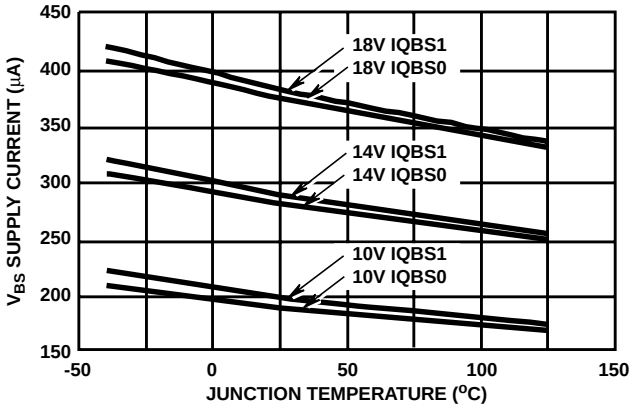


FIGURE 9. QUIESCENT V_{BS} SUPPLY CURRENT vs TEMPERATURE

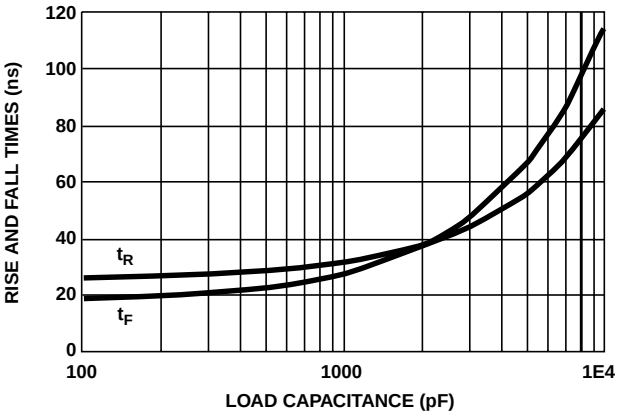


FIGURE 10. RISE AND FALL TIME vs LOAD CAPACITANCE

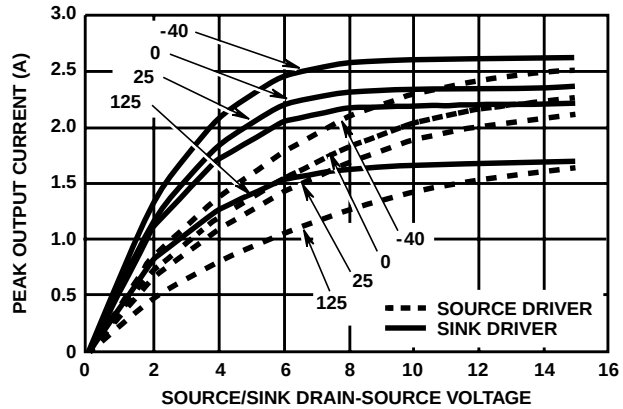


FIGURE 11. DRIVER SINK/SOURCE V-I CHARACTERISTIC

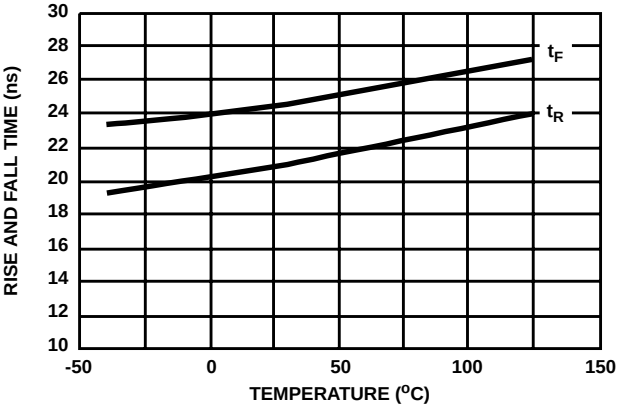


FIGURE 12. RISE AND FALL TIME vs TEMPERATURE

Typical Performance Curves (Continued)

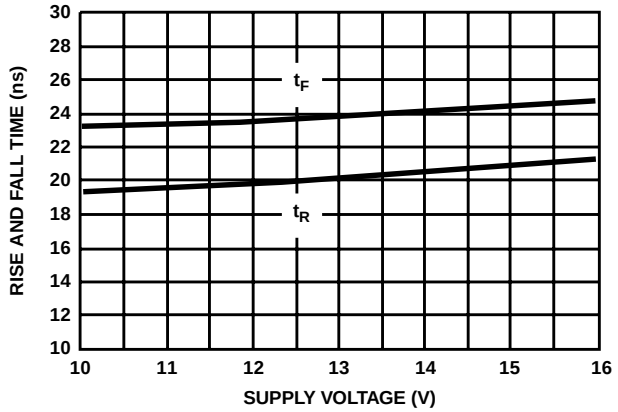


FIGURE 13. RISE AND FALL TIME vs SUPPLY VOLTAGE

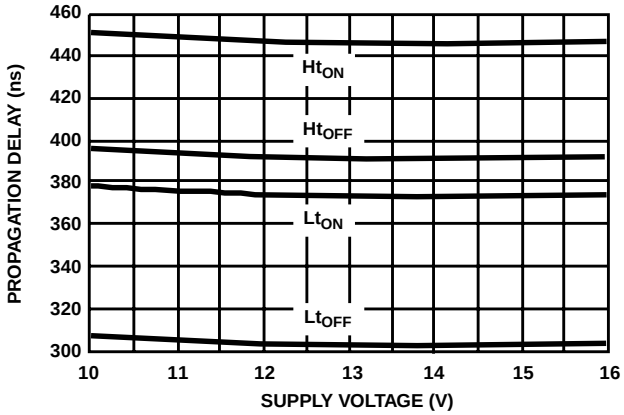


FIGURE 14. PROPAGATION DELAY vs SUPPLY VOLTAGE

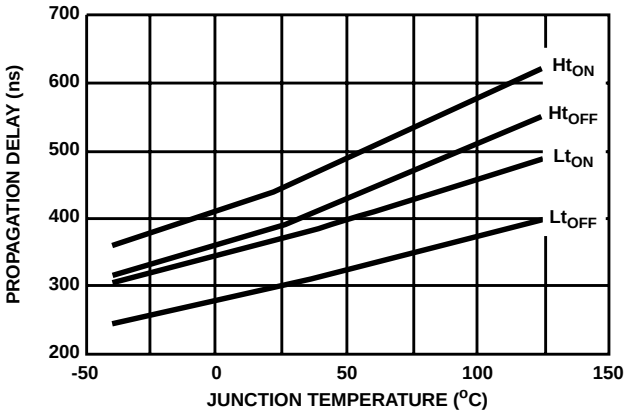
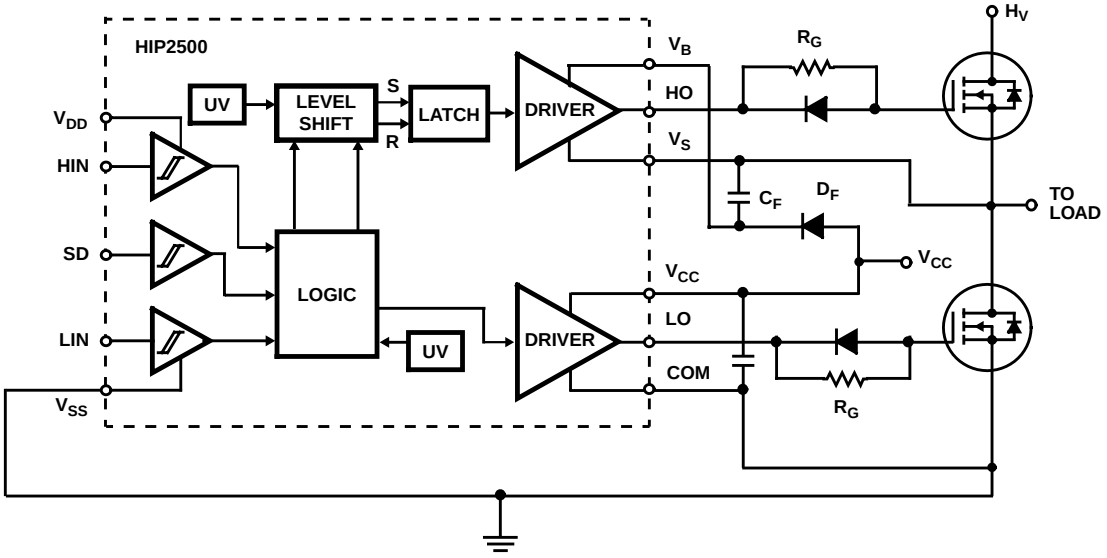
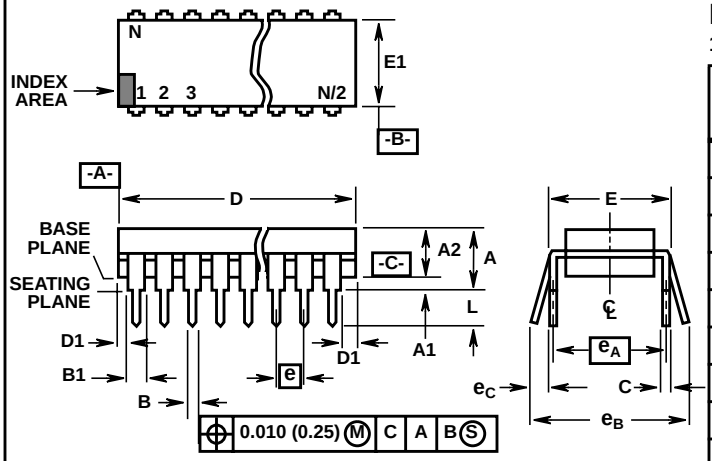


FIGURE 15. PROPAGATION DELAYS AT V_{CC} = 15V

Typical Application Diagram



Dual-In-Line Plastic Packages (PDIP)



NOTES:

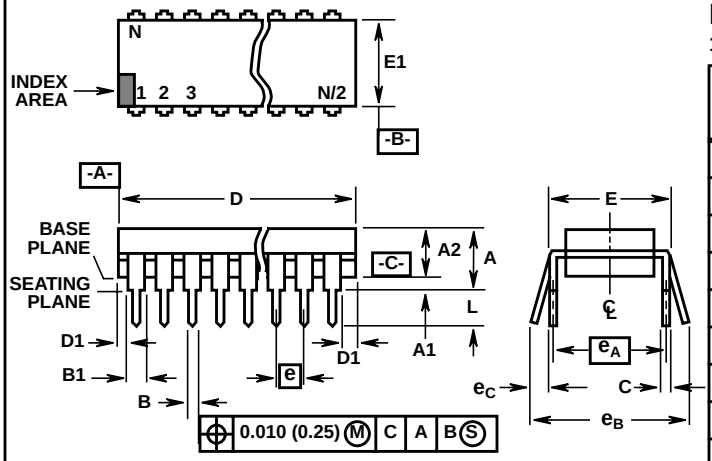
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E14.3 (JEDEC MS-001-AA ISSUE D)
14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

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Dual-In-Line Plastic Packages (PDIP)



NOTES:

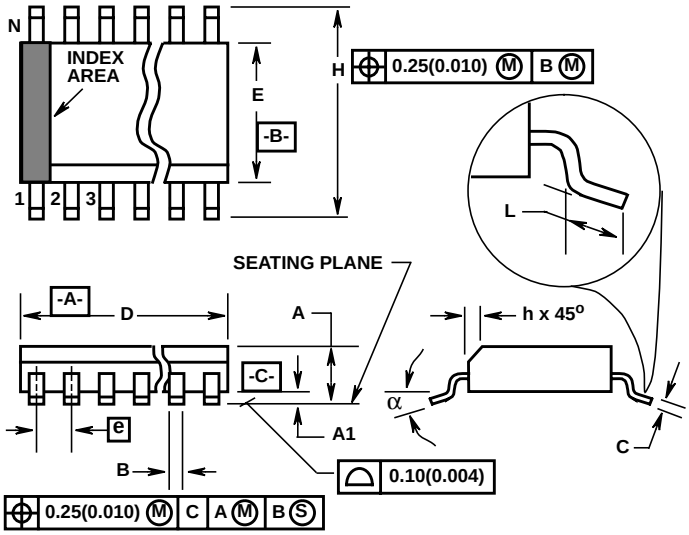
1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

E16.3 (JEDEC MS-001-BB ISSUE D)
16 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	16		16		9

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Small Outline Plastic Packages (SOIC)



M16.3 (JEDEC MS-013-AA ISSUE C)
16 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.0200	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.3977	0.4133	10.10	10.50	3
E	0.2914	0.2992	7.40	7.60	4
e	0.050 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	16		16		7
α	0^o	8^o	0^o	8^o	-

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NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.