Pb-Free and RoHS Compliant

October 25, 2005 FN4105.2

8-Bit, 50MSPS, Video A/D Converter with Clamp Function

The HI2302 is an 8-bit CMOS A/D Converter for video with synchronizing clamp function. The adoption of two-step parallel method achieves low power consumption and a maximum conversion rate of 50MSPS. For pin compatible lower sample rate converters refer to HI1179 (35MSPS) or HI1176 (20MSPS) data sheets.

Ordering Information

PART NUMBER	TEMP. RANGE (^{o}C)	PACKAGE	PKG. NO.
HI2302JCQ	-40 to 85	32 Ld MQFP	Q32.7x7-S

Applications

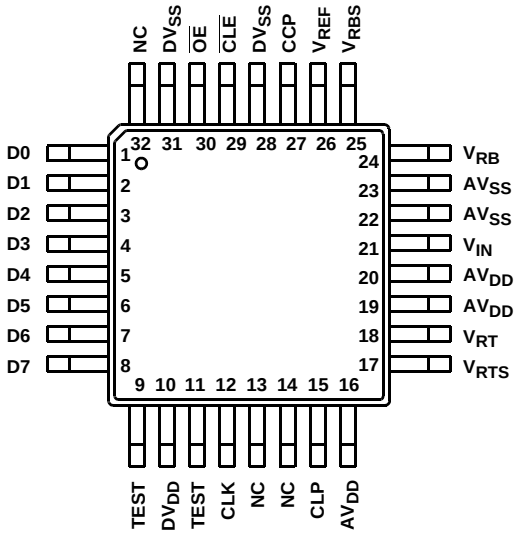
- Video Digitizing
- Wireless Receivers
- LCD Projectors/Panels
- Cable Modems
- RGB Graphics Processing
- Camcorders
- Instrumentation

Features

- Resolution . . . . . 8-Bit ±0.5 LSB (DNL)
- Maximum Sampling Frequency . . . . . 50 MSPS
- Low Power Consumption . . . . . .125mW (Reference Current Excluded)
- Built-In Input Clamp Function (DC Restore)
- Clamp ON/OFF Function
- Internal Voltage Reference
- Input CMOS/TTL Compatible
- Three-State TTL Compatible Output
- Power Supply . . . . . +5V Single or +5V/3.3V Dual
- Direct Replacement for Sony CXD2302Q

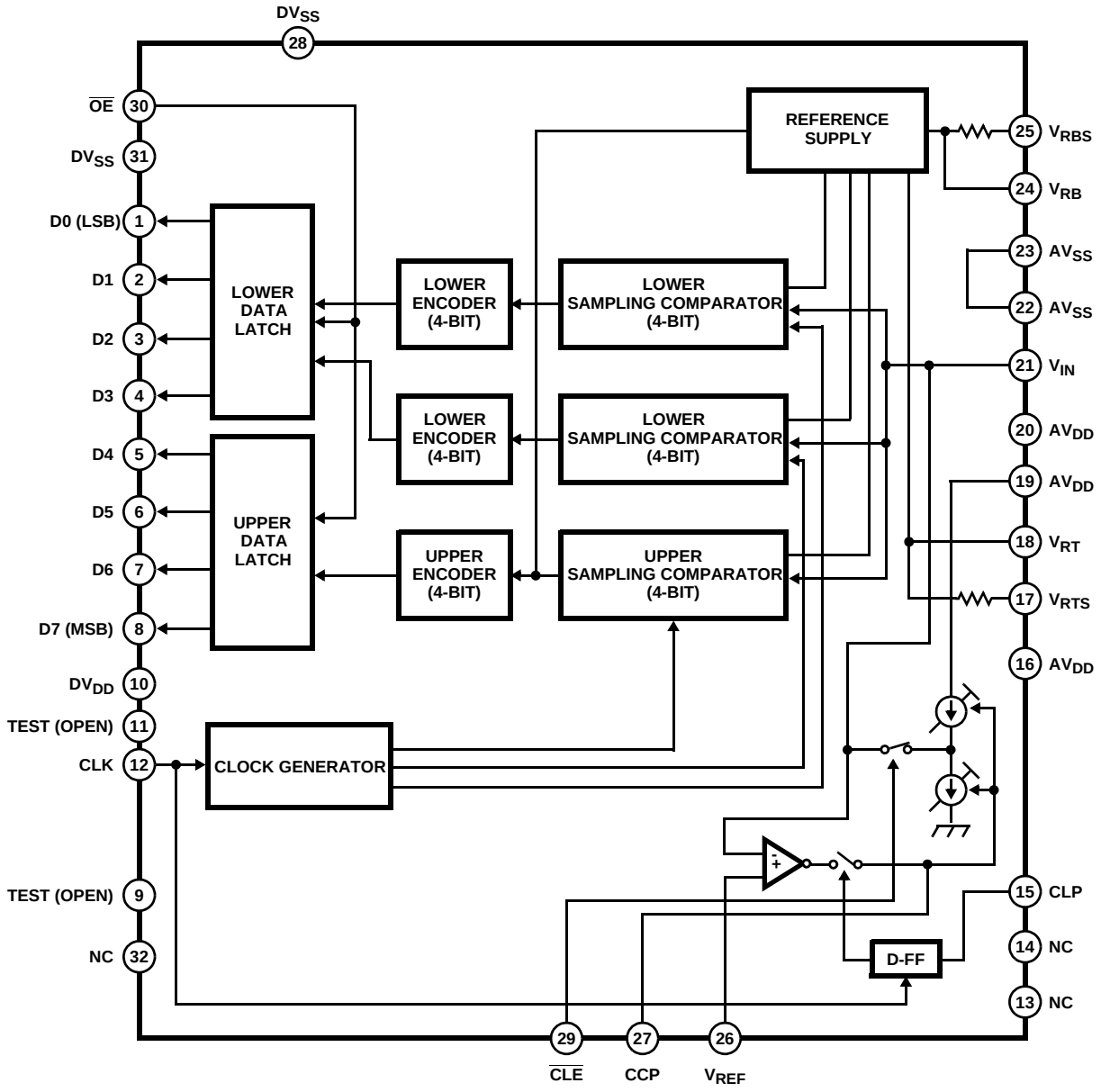
Pinout

HI2302 (MQFP)
TOP VIEW



CAUTION: These devices are sensitive to electrostatic discharge; follow proper IC Handling Procedures.
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Functional Block Diagram



Absolute Maximum Ratings $T_A = 25^oC$

Supply Voltage (V_{DD}) 7V
Reference Voltage (V_{RT}, V_{RB}) . . . . . .V_{DD} +0.5 to V_{SS} -0.5V
Input Voltage (Analog) (V_{IN}) . . . . . .V_{DD} +0.5 to V_{SS} -0.5V
Input Voltage (Digital) (V_I) . . . . . .V_{DD} +0.5 to V_{SS} -0.5V
Output Voltage (Digital) (V_O) . . . . . .V_{DD} +0.5 to V_{SS} -0.5V

Operating Conditions

Supply Voltage
(AV_{DD}, AV_{SS}) . . . . . 4.75 to 5.25V
(DV_{DD}, DV_{SS}) . . . . . 3.0 to 5.5V
(DV_{SS}-AV_{SS}) . . . . . .0 to 100mV
Reference Input Voltage
(V_{RB}) . . . . . 0 and Above V
(V_{RT}) . . . . . .2.7 and Below V
Analog Input (V_{IN}) . . . . . 1.7V_{P-P} Above
Clock Pulse Width (t_{PW1}, t_{PW0}) . . . . . 10ns (Min)
Ambient Temperature (T_{OPR}) . . . . . -40^{o}C to 85^{o}C

Thermal Information

Thermal Resistance (Typical, Note 1)	θ_{JA} (^{o}C/W)
MQFP Package	122

Maximum Junction Temperature (Plastic Package) . . . . . .150^{o}C
Maximum Storage Temperature Range . . . . . -55^{o}C to 150^{o}C
Maximum Lead Temperature (Soldering 10s) . . . . . .300^{o}C
(MQFP - Lead Tips Only)

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on an evaluation PC board in free air.

Electrical Specifications f_C = 50 MSPS, AV_{DD} = 5V, DV_{DD} = 3 to 5.5V, V_{RB} = 0.5V, V_{RT} = 2.5V, $T_A = 25^oC$

PARAMETER	SYMBOL	TEST CONDITIONS		NOTES	MIN	TYP	MAX	UNITS
ANALOG CHARACTERISTICS								
Maximum Conversion Rate	f_C Max	AV_{DD} = 4.75 to 5.25V, T_A = 20 to 75^{o}C, V_{IN} = 0.5 to 2.5V, f_{IN} = 1kHz Triangular Wave			50	65	-	MSPS
Minimum Conversion Rate	f_C Min				-	-	0.5	MSPS
Input Bandwidth Full Scale	BW	Envelope R_{IN} = 33Ω	-1dB		-	60	-	MHz
			-3dB		-	100	-	MHz
Differential Nonlinearity Error	E_D	End Point			-	±0.3	±0.5	LSB
Integral Nonlinearity Error	E_L				-	+0.7	±1.5	LSB
Offset Voltage	E_{OT}	Potential Difference to V_{RT}		Note 2	-70	-50	-30	mV
	E_{OB}	Potential Difference to V_{RB}			20	40	60	mV
Differential Gain Error	DG	NTSC 40 IRE Mod Ramp f_C = 14.3 MSPS			-	3	-	%
Differential Phase Error	DP				-	1.5	-	Degrees
Sampling Delay	t_{SD}				-	0	-	ns
Clamp Offset Voltage	E_{OC}	V_{IN} = DC, C_{IN} = 10µF t_{PCW} = 2.75µs, f_C = 14.3 MSPS, f_{CLP} = 15.75kHz	V_{REF} = 0.5V		0	20	40	mV
			V_{REF} = 2.5V		0	20	40	mV
Signal-To-Noise Ratio	SNR	f_{IN} = 100kHz			-	45	-	dB
		f_{IN} = 500kHz			-	44	-	dB
		f_{IN} = 1MHz			-	44	-	dB
		f_{IN} = 3MHz			-	43	-	dB
		f_{IN} = 10MHz			-	38	-	dB
		f_{IN} = 25MHz			-	32	-	dB
Spurious Free Dynamic	SFDR	f_{IN} = 100kHz			-	51	-	dB
		f_{IN} = 500kHz			-	46	-	dB
		f_{IN} = 1MHz			-	49	-	dB
		f_{IN} = 3MHz			-	46	-	dB
		f_{IN} = 10MHz			-	45	-	dB
		f_{IN} = 25MHz			-	45	-	dB

Electrical Specifications f_C = 50 MSPS, AV_{DD} = 5V, DV_{DD} = 3 to 5.5V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C **(Continued)**

PARAMETER	SYMBOL	TEST CONDITIONS		NOTES	MIN	TYP	MAX	UNITS
DC CHARACTERISTICS f_C = 50 MSPS, AV_{DD} = 5V, DV_{DD} = 5V or 3.3V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C								
Supply Current	$I_{AD} + I_{DD}$	NTSC Ramp, Wave Input, $\overline{CLE}$ = 0V	DV_{DD} = 5V		-	25	36	mA
Analog	I_{AD}		DV_{DD} = 3.3V		-	23	33	mA
Digital	I_{DD}				-	2	3	mA
Reference Current	I_{REF}				4.1	5.4	7.7	mA
Reference Resistance (V_{RT} - V_{RB})	R_{REF}				260	370	480	Ω
Self-Bias Voltage	V_{RB}	Shorts V_{RTS} and A_{VDD} Shorts V_{RBS} and A_{VSS}			0.52	0.56	0.60	V
	V_{RT} - V_{RB}				1.80	1.92	2.04	V
Input Capacitance	C_{AI1}	V_{IN}, V_{IN} = 1.5V + 0.07V_{RMS}			-	15	-	pF
	C_{AI2}	V_{RTS}, V_{RT}, V_{RB}, V_{RBS}, V_{REF}			-	-	11	pF
	C_{DIN}	TEST, CLK, CLP, $\overline{CLE}$, $\overline{OE}$			-	-	11	pF
Output Capacitance	C_{AO}	CCP			-	-	11	pF
	C_{DO}	D0 to D7, TEST			-	-	11	pF
Digital Input Voltage	V_{IH}	AV_{DD} = 4.75 to 5.25V, DV_{DD} = 3 to 5.5V, T_A = -20°C to 75°C			2.2	-	-	V
	V_{IL}				-	-	0.8	V
Digital Input Current	I_{IH} I_{IL}	V_I = 0V to AV_{DD}, T_A = 20°C to 75°C	CLK		-240	-	240	µA
			TEST, CLP, $\overline{CLE}$		-240	-	40	µA
			$\overline{OE}$		-40	-	240	µA
Digital Output Current	I_{OH}	$\overline{OE}$ = 0V, DV_{DD} = 5V T_A = 20°C to 75°C	V_{OH} = DV_{DD} - 0.8V		-	-	-2	mA
	I_{OL}		V_{OL} = 0.4V		4	-	-	mA
	I_{OH}	$\overline{OE}$ = 0V DV_{DD} = 3.3V T_A = -20°C to 75°C	V_{OH} = DV_{DD} - 0.8V		-	-	-1.2	mA
	I_{OL}		V_{OL} = 0.4V		2.4	-	-	mA
	I_{OZH}	$\overline{OE}$ = 3V DV_{DD} = 3 to 5.5V T_A = -20°C to 75°C	V_{OH} = DV_{DD}		-40	-	40	µA
	I_{OZL}		V_{OL} = 0V		-40	-	40	µA
TIMING f_C = 50 MSPS, AV_{DD} = 5V, DV_{DD} = 5V or 3.3V, V_{RB} = 0.5V, V_{RT} = 2.5V, T_A = 25°C								
Output Data Delay	t_{PZH}	CL = 15pF $\overline{OE}$ = 0V	DV_{DD} = 5V		5.5	9.5	12.0	ns
	t_{PHL}					8.5		ns
	t_{PLH}		DV_{DD} = 3.3V		4.3	11.8	16.3	ns
	t_{PHL}					7.6		ns
Three-State Output Enable Time	t_{PZH}	R_L = 1kΩ C_L = 15pF $\overline{OE}$ = 3V→0V	DV_{DD} = 5V		2.5	4.5	8.0	ns
	t_{PZL}					6.0		ns
	t_{PZH}		DV_{DD} = 3.3V		3.0	7.0	9.0	ns
	t_{PZL}					5.0		ns
Three-State Output Enable Time	t_{PHZ}, t_{PLZ}	R_L = 1kΩ, C_L = 15pF $\overline{OE}$ = 3V→0V	DV_{DD} = 5V		3.5	5.5	7.5	ns
	t_{PZH}, t_{PZL}		DV_{DD} = 3.3V		2.5	5.5	8.0	ns
Clamp Pulse Width	t_{CPW}	f_C = 14.3MHz, C_{IN} = 10µF for NTSC Wave		Note 4	1.75	2.75	3.75	µs

NOTES:

2. The offset voltage E_{OB} is a potential difference between V_{RB} and a point of position where the voltage drops equivalent to $^1/_2$ LSB of the voltage when the output data changes from “00000000” to “00000001”. E_{OT} is a potential difference between V_{RT} and a potential point where the voltage rises equivalent to $^1/_2$ LSB of the voltage when the output data changes from “11111111” to “11111110”.
3. The voltage of up to (AV_{DD} + 0.5V) can be input when DV_{DD} = 3.3V. But the output pin voltage is less than the DV_{DD} voltage. When the digital output is in the high impedance mode, the IC may be damaged by applying the voltage which is more than the (DV_{DD} + 0.5V) voltage to the digital output.
4. The clamp pulse width is for NTSC as an example. Adjust the rate to the clamp pulse cycle (1/15.75kHz for NTSC) for other processing systems to equal the values for NTSC.

Timing Diagrams

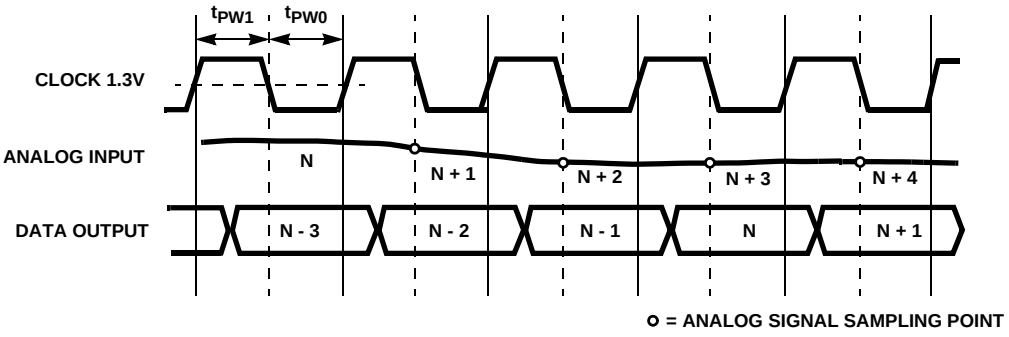


FIGURE 1A. TIMING CHART

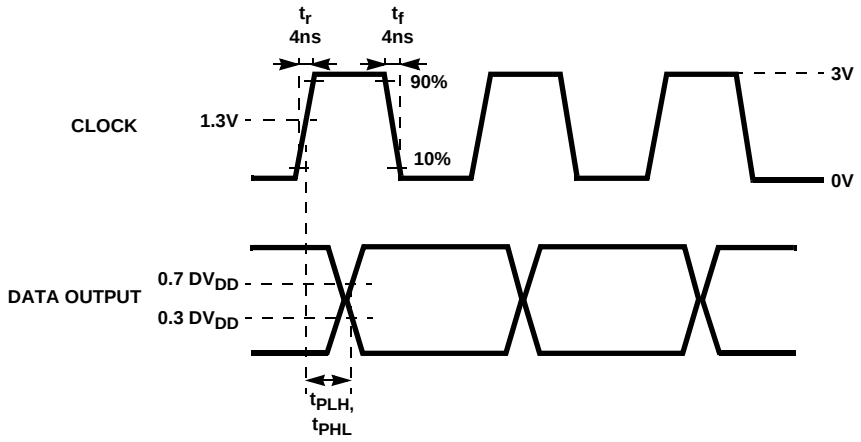


FIGURE 1B. TIMING CHART

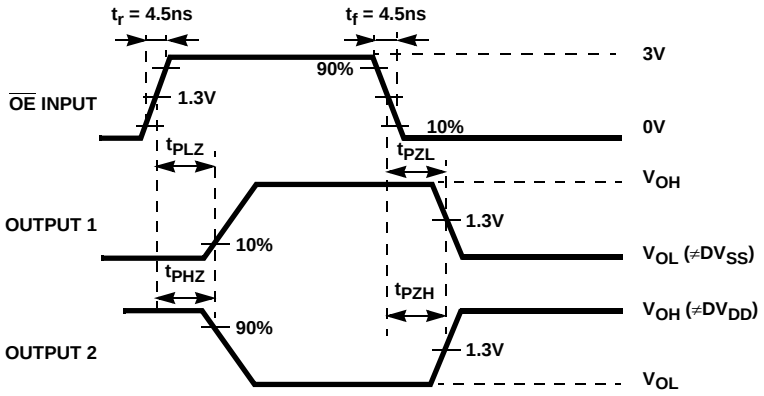


FIGURE 1C. TIMING CHART

Timing Diagrams (Continued)

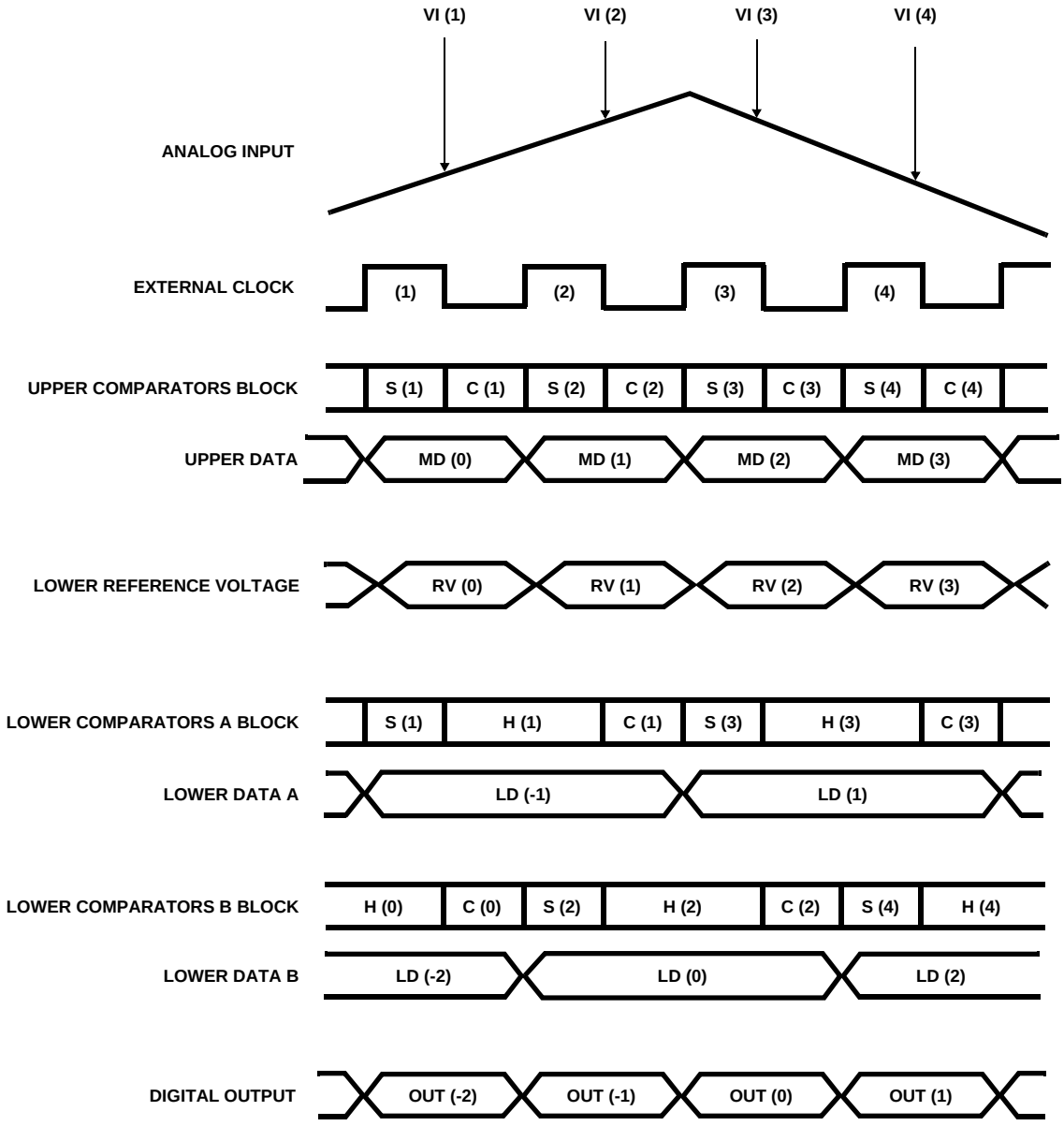
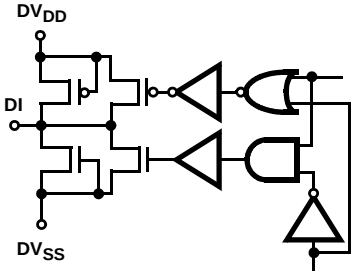
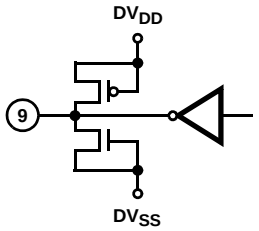
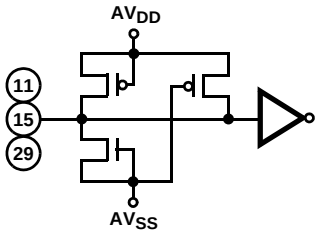
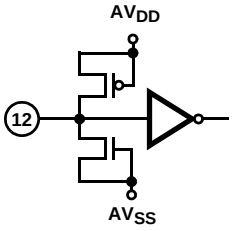
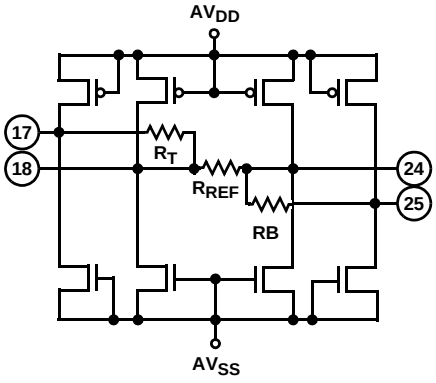
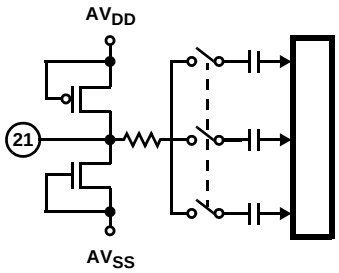


FIGURE 1D. TIMING CHART II

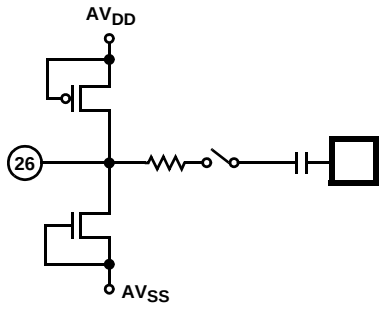
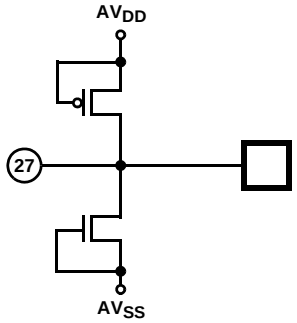
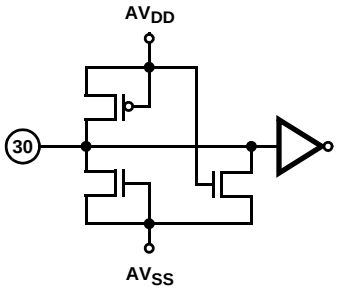
Pin Descriptions

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
1 to 8	D0 to D7		D0 (LSB) to D7 (MSB) Output.

Pin Descriptions (Continued)

PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
9	TEST		Leave open for normal use.
10	DV_{DD}		Digital Power Supply +5V or +3.3V.
11	TEST		Leave open for normal use. Pull-up resistor is built in.
15	CLP		Input for the clamp pulse. Clamps the signal voltage during low interval. Pull-up resistor is built in.
29	$\overline{CLE}$		The clamp function is enabled when $\overline{CLE}$ = Low. The clamp function is off and the device functions as a normal A/D converter when $\overline{CLE}$ = High. Pull-up resistor is built in.
12	CLK		Clock Input. Set to Low level when no clock is input.
13, 14, 32	NC		
16, 19, 20	AV_{DD}		Analog Power Supply +5V.
17	V_{RTS}		Generates approximately +2.5V when shorted with AV_{DD}.
18	V_{RT}		Reference Voltage (Top).
24	V_{RB}		Reference Voltage (Bottom).
25	V_{RBS}		Generates approximately +0.6V when shorted with AV_{SS}.
21	V_{IN}		Analog Input.

Pin Descriptions (Continued)

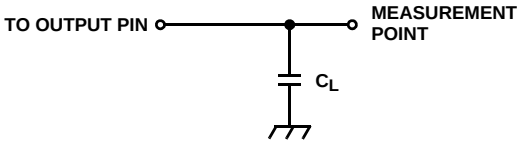
PIN NO.	SYMBOL	EQUIVALENT CIRCUIT	DESCRIPTION
22, 23	AV_{SS}		Analog Ground.
26	V_{REF}		Clamp Reference Voltage Input. Clamps so that the reference voltage and the input signal during clamp interval are equal.
27	CCP		Integrates the clamp control voltage. The relationship between the changes in CCP voltage and in V_{IN} voltage is positive phase.
28, 31	DV_{SS}		Digital Ground.
30	$\overline{OE}$		Data is output when $\overline{OE}$ = Low. Pins D0 to D7 are at high impedance when $\overline{OE}$ = High. Pull-down resistor is built in.

Digital Output

The following table shows the relationship between analog input voltage and digital output code.

INPUT SIGNAL VOLTAGE	STEP	DIGITAL OUTPUT CODE							
		MSB							LSB
V_{RT}	0	1	1	1	1	1	1	1	1
•	•				•				
•	•				•				
•	•				•				
•	127	1	0	0	0	0	0	0	0
•	128	0	1	1	1	1	1	1	1
•	•				•				
•	•				•				
•	•				•				
V_{RB}	255	0	0	0	0	0	0	0	0

Electrical Specifications Measurement Circuits



NOTE: C_L includes capacitance of probes.

FIGURE 2. OUTPUT DATA DELAY MEASUREMENT CIRCUIT

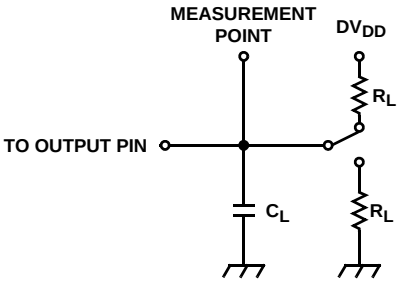


FIGURE 3. THREE-STATE OUTPUT MEASUREMENT CIRCUIT

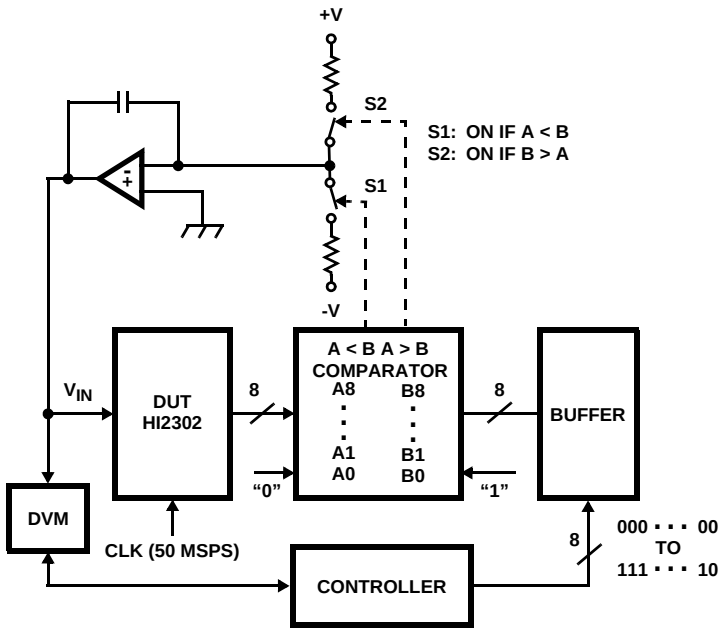


FIGURE 4. INTEGRAL NONLINEARITY ERROR/DIFFERENTIAL NONLINEARITY ERROR/OFFSET VOLTAGE TEST CIRCUIT

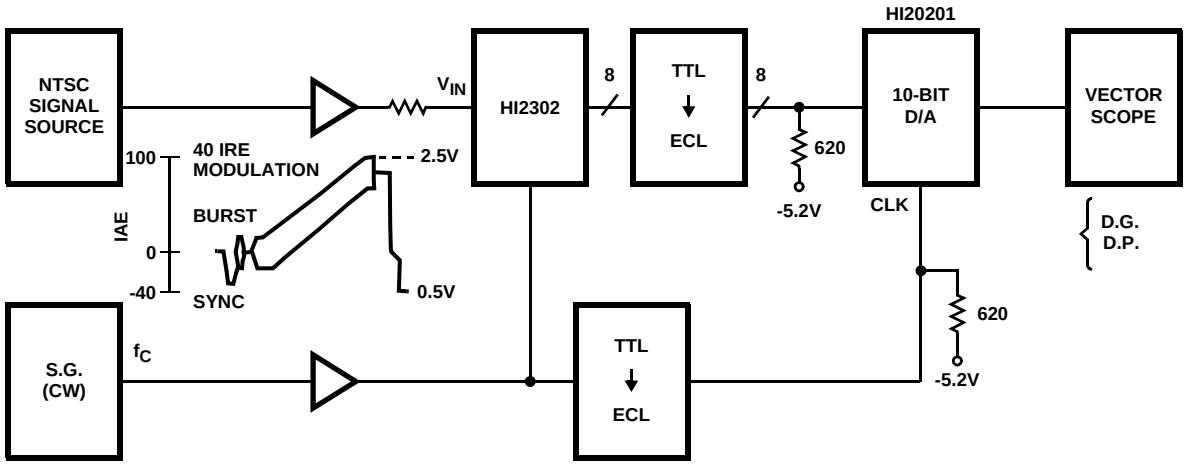


FIGURE 5. DIFFERENTIAL GAIN ERROR, DIFFERENTIAL PHASE ERROR TEST CIRCUIT

Electrical Specifications Measurement Circuits (Continued)

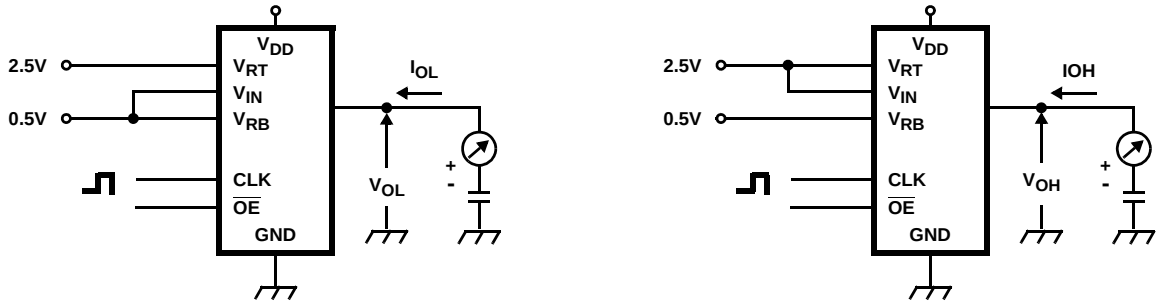


FIGURE 6. DIGITAL OUTPUT CURRENT TEST CIRCUIT

Operation (See Block diagram and Timing Chart II)

- The HI2302 is a two-step parallel system A/D converter featuring a 4-bit upper comparator block and two lower comparator blocks of 4-bit each. The reference voltage that is equal to the voltage between V_{RT} - V_{RB}/16 is constantly applied to the upper 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower 4-bit comparator block. Voltage that corresponded to the upper data is fed through the reference supply to the lower 4-bit comparator block. V_{RTS} and V_{RBS} pins serve for the self generation of V_{RT} (reference voltage top) and V_{RB} (reference voltage bottom), and they are also used as the sense pins as shown in the Application Circuit examples Figures 10 and 11.
- This IC uses an offset cancel type comparator which operates synchronously with an external clock. It features the following operating modes which are respectively indicated on the Timing Chart II with S, H, C symbols. That is input sampling (auto zero) mode, input hold mode and comparison mode.
- The operation of respective parts is as indicated in the Timing Chart II. For instance, input voltage VI (1) is sampled with the falling edge of the external clock (1) by means of the upper comparator block and the lower comparator A block.
  The upper comparator block finalizes comparison data MD (1) with the rising edge of the external clock (2). Simultaneously the reference supply generates the lower reference voltage RV (1) that corresponded to the upper results. The lower comparator A Block finalizes comparison data LD (1) with the rising edge of the external clock (3). MD (1) and LD (1) are combined and output as Out (1) with the rising edge of the external clock (4). Accordingly there is a 2.5 clock delay from the analog input sampling point to the digital data output.

Notes On Operation

- V_{DD}, V_{SS}
  To reduce noise effects, separate the analog and digital systems close to the device. For both the digital and analog V_{DD} pins, use a ceramic capacitor of about 0.1µF set as close as possible to the pin to bypass to the respective GNDs.
- Analog Input
  Compared with the flash type A/D converter, the input capacitance of the analog input is rather small. However, it is necessary to conduct the drive with an amplifier featuring sufficient band and drive capability. When driving with an amplifier of low output impedance, parasitic oscillation may occur. That may be prevented by insetting a resistance of about 33Ω in series between the amplifier output and A/D input. When the V_{IN} signal of pin No. 21 is monitored, the kickback noise of clock is. However, this has no effect on the characteristics of A/D conversion.
- Clock Input
  The clock line wiring should be as short as possible also, to avoid any interference with other signals, separate it from other circuits.
- Reference Input
  Voltage V_{RT} to V_{RB} is compatible with the dynamic range of the analog input. Bypassing V_{RT} and V_{RB} pins to GND, by means of a capacitor about 0.1µF, stable characteristics are obtained. By shorting V_{DD} and V_{RTS}, V_{SS} and V_{RBS} respectively, the self-bias function that generates V_{RT} = about 2.5V and V_{RB} = about 0.6V, is activated.
- Timing
  Analog input is sampled with the falling edge of CLK and output as digital data synchronized with a delay of 2.5 clocks and with the following rising edge. The delay from the clock rising edge to the data output is about 9ns (DV_{DD} = 5V).
- $\overline{OE}$ Pin
  Pins 1 to 8 (D_0 to D_7) are in the output mode by leaving $\overline{OE}$ open or connecting it to DV_{SS}, and they are in the high impedance mode by connecting it to DV_{DD}.

Application Circuits

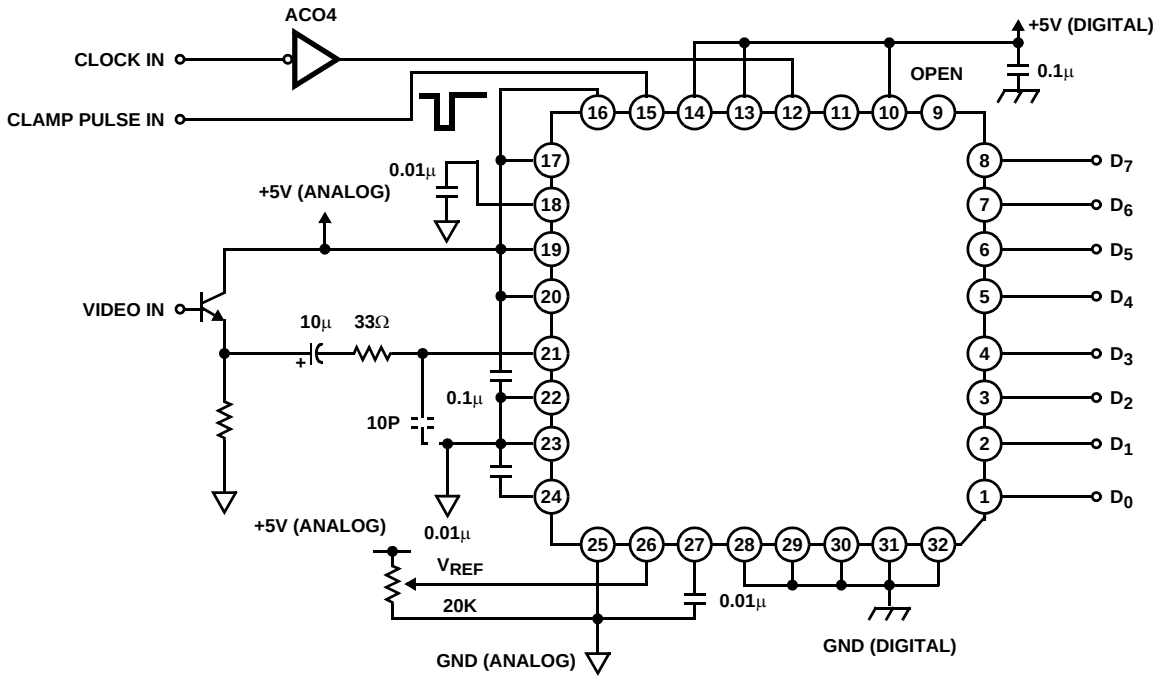
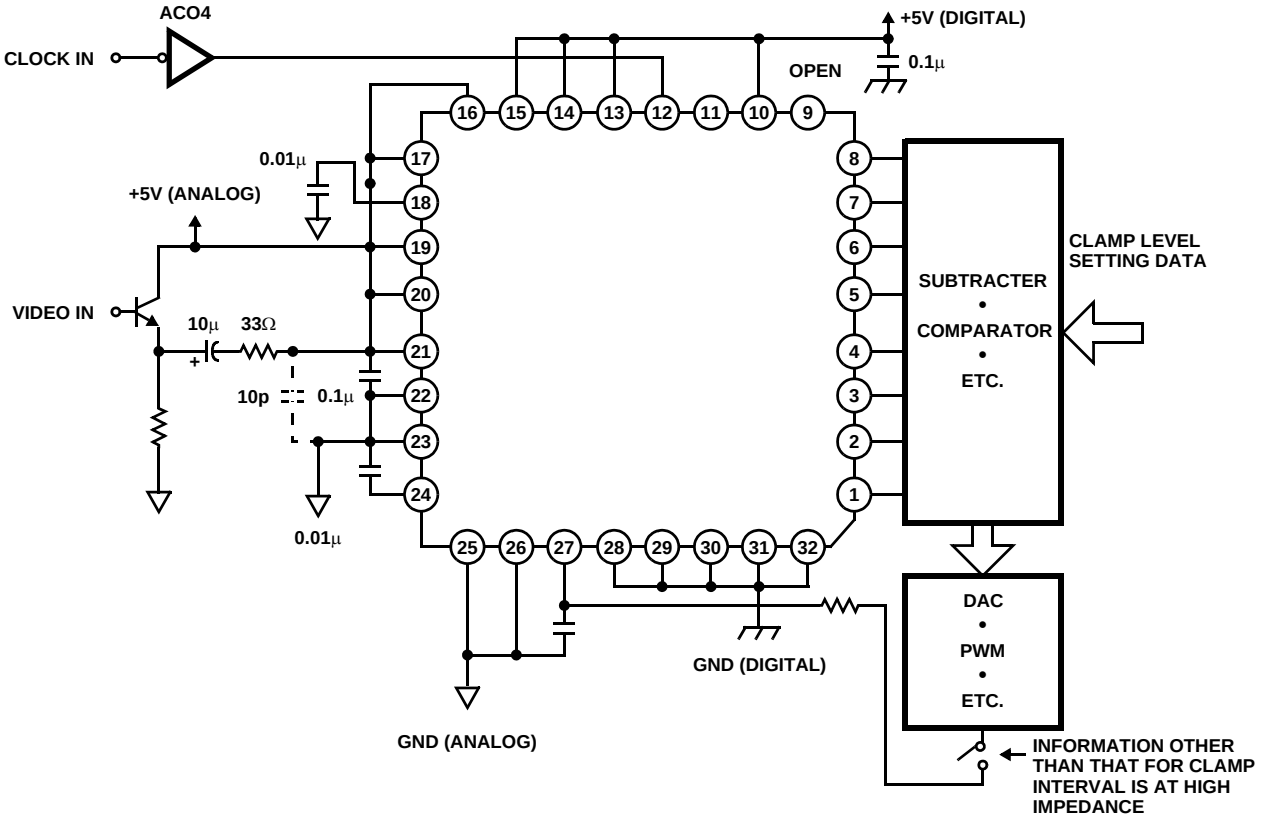


FIGURE 7. SINGLE +5V POWER SUPPLY WHEN CLAMP IS USED (SELF-BIAS USED)



NOTES:

5. The relationship between the changes in CCP voltage (Pin 27) and in V_{IN} voltage is positive phase.
6. $\Delta V_{IN} / \Delta V_{CCP} = 3.0$ (f_S = 20 MSPS).

FIGURE 8. SINGLE +5V POWER SUPPLY DIGITAL CLAMP (SELF-BIAS USED)

Application Circuits (Continued)

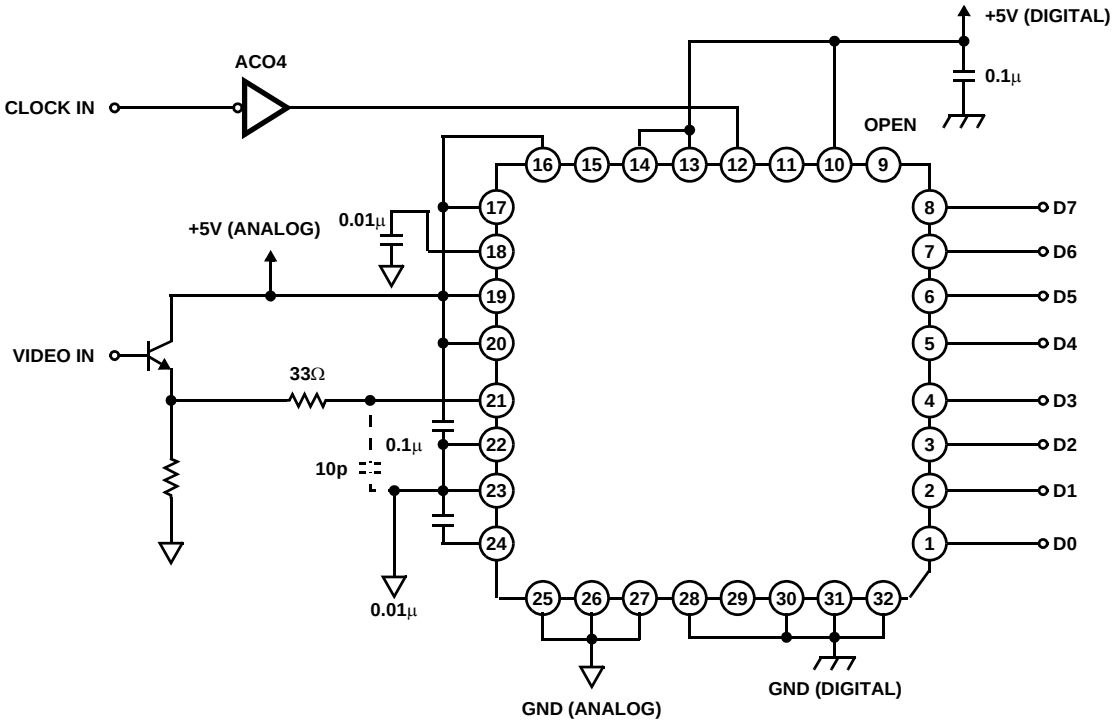


FIGURE 9. SINGLE +5V POWER SUPPLY WHEN CLAMP IS NOT USED (SELF-BIAS USED)

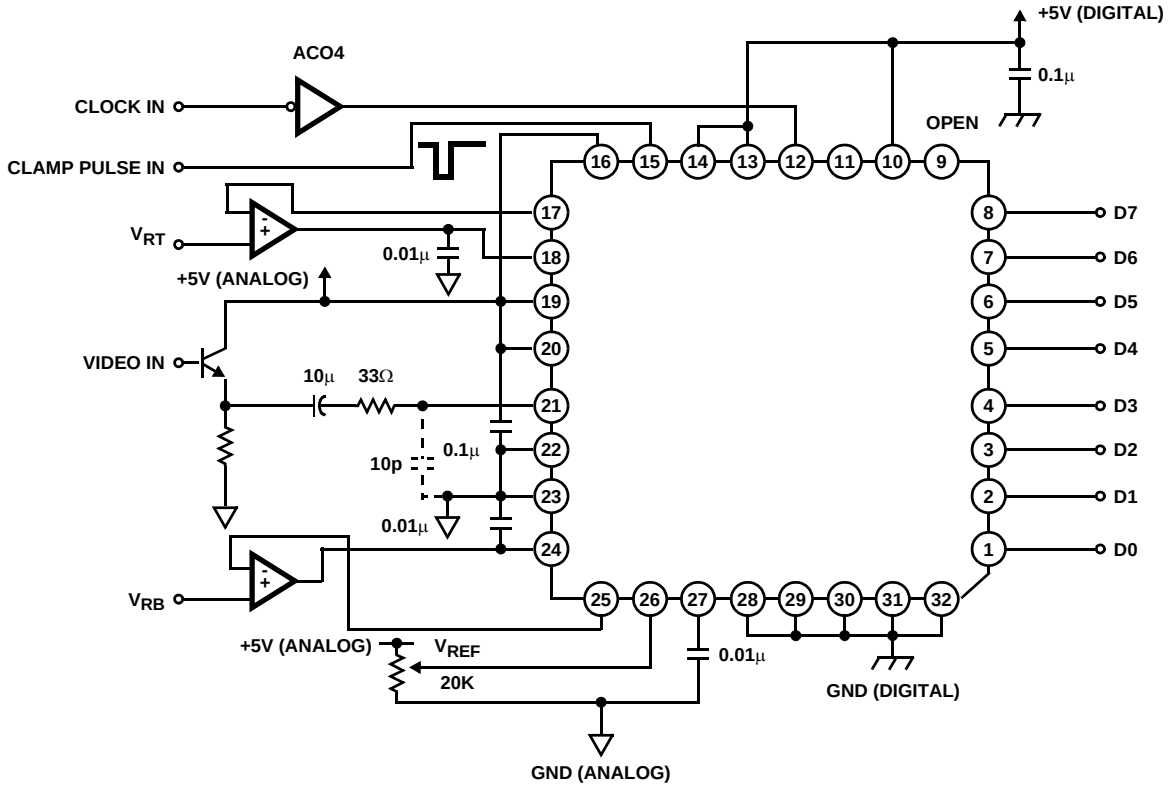


FIGURE 10. WHEN CLAMP IS USED (SELF-BIAS NOT USED)

Application Circuits (Continued)

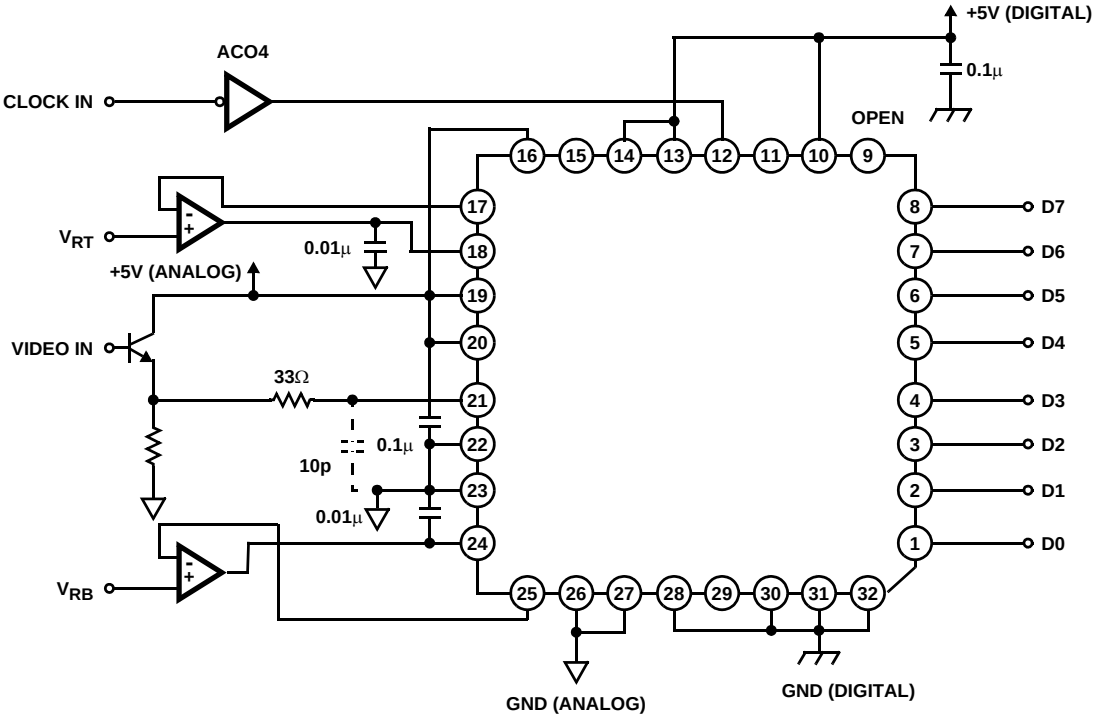


FIGURE 11. SINGLE +5V POWER SUPPLY WHEN CLAMP IS NOT USED (SELF-BIAS NOT USED)

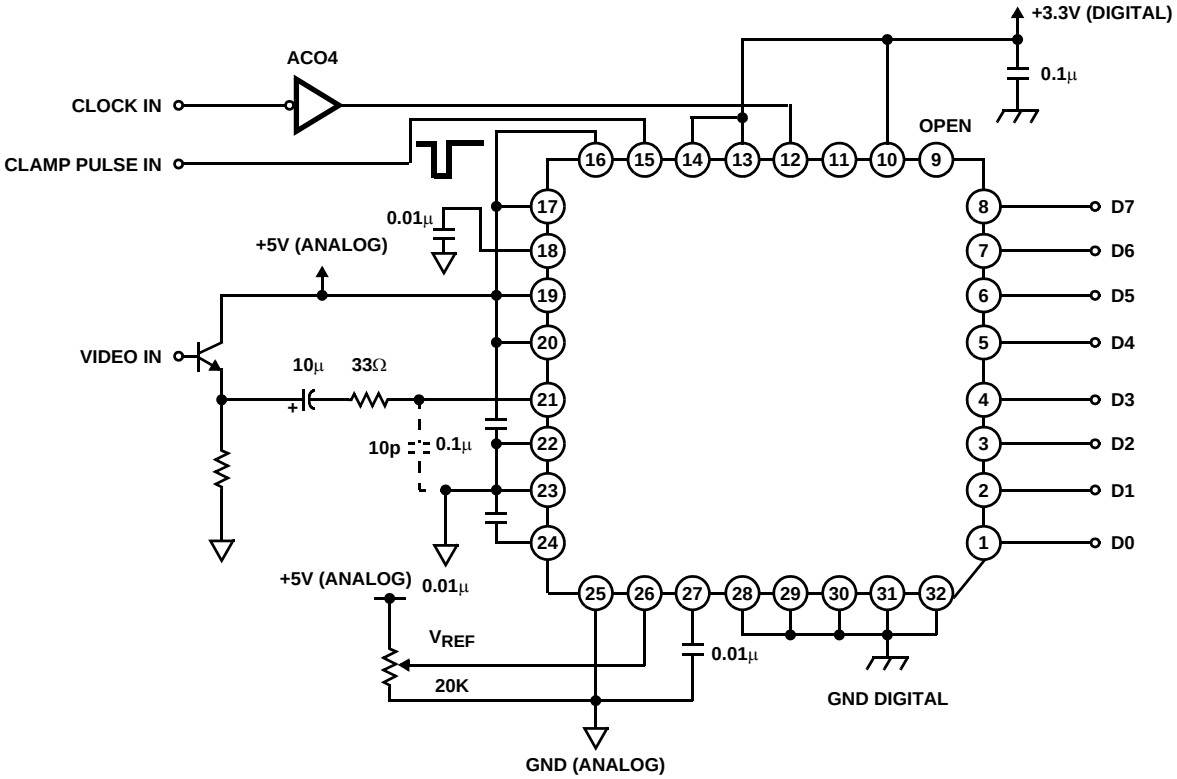


FIGURE 12. DUAL +5V/+3.3V POWER SUPPLY WHEN CLAMP IS USED (SELF-BIAS USED)

Typical Performance Curves

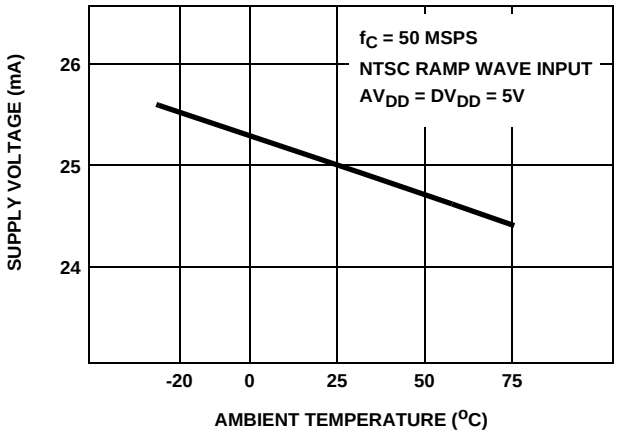


FIGURE 13. AMBIENT TEMPERATURE vs SUPPLY CURRENT

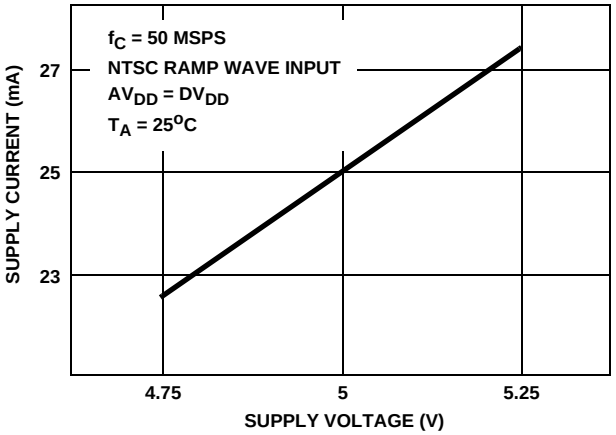


FIGURE 14. SUPPLY VOLTAGE vs SUPPLY CURRENT

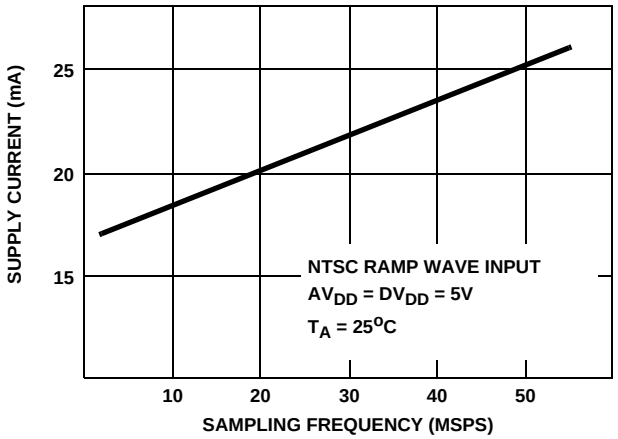


FIGURE 15. SAMPLING FREQUENCY vs SUPPLY CURRENT

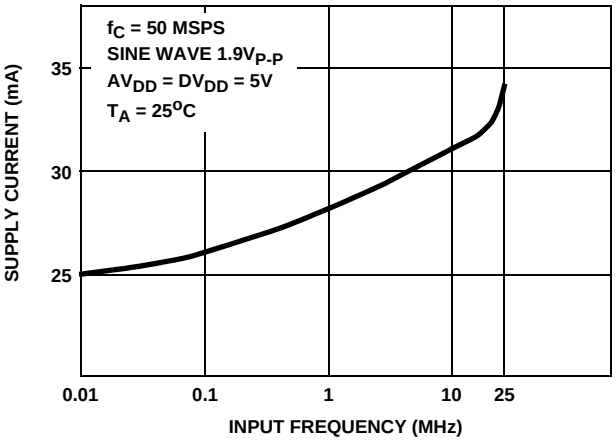


FIGURE 16. INPUT FREQUENCY vs SUPPLY CURRENT

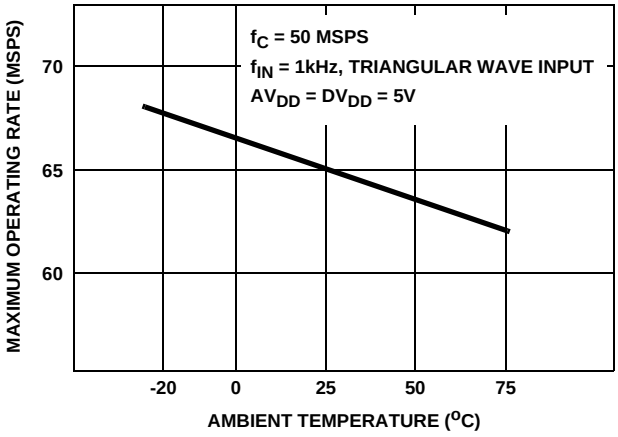


FIGURE 17. AMBIENT TEMPERATURE vs MAXIMUM OPERATING FREQUENCY

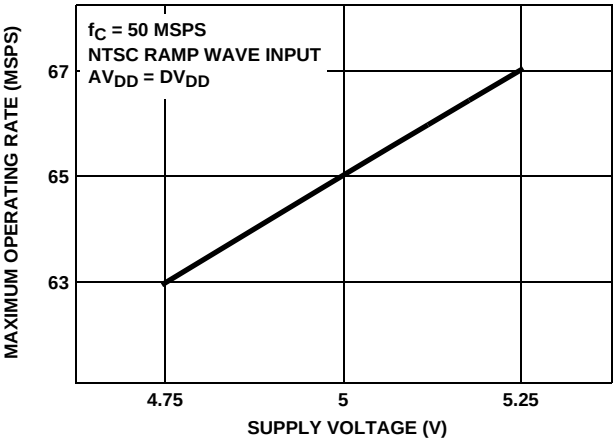


FIGURE 18. SUPPLY VOLTAGE vs MAXIMUM OPERATING FREQUENCY

Typical Performance Curves (Continued)

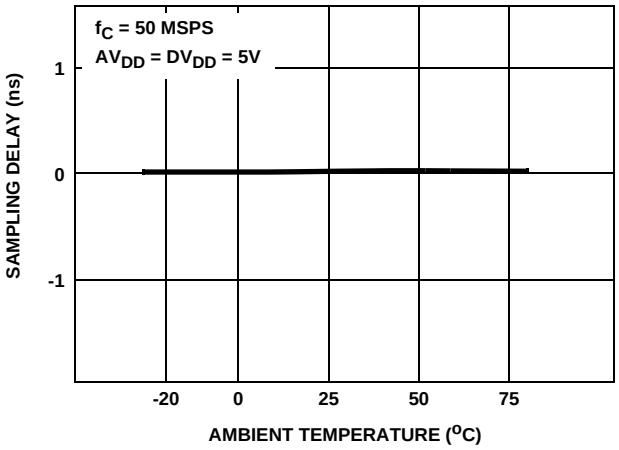


FIGURE 19. AMBIENT TEMPERATURE vs SAMPLING DELAY

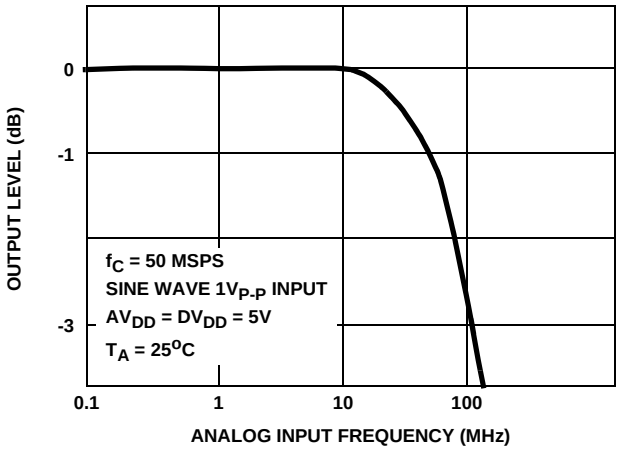


FIGURE 20. FULL SCALE INPUT BANDWIDTH

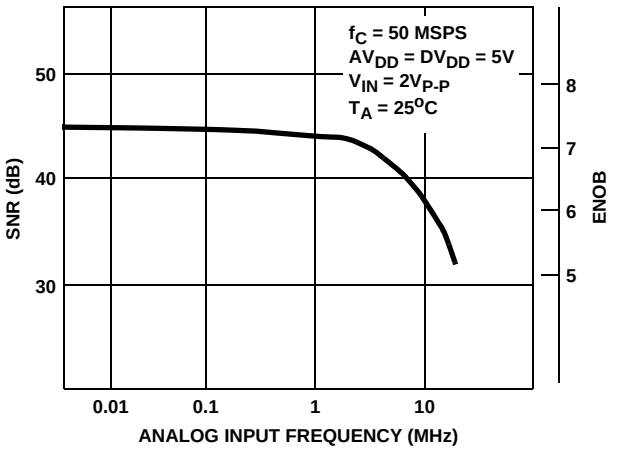


FIGURE 21. ANALOG INPUT FREQUENCY vs SNR, EFFECTIVE NUMBER OF BITS (ENOB)

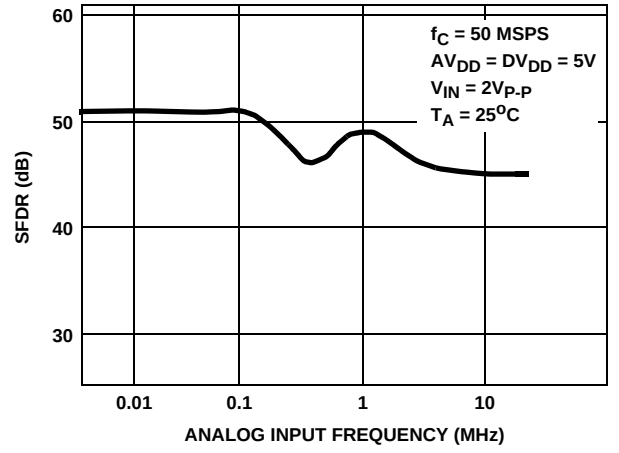


FIGURE 22. ANALOG INPUT FREQUENCY vs SFDR

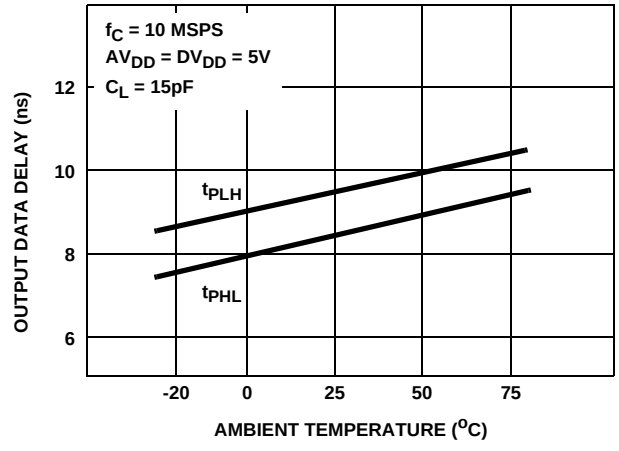


FIGURE 23. AMBIENT TEMPERATURE vs OUTPUT DATA DELAY

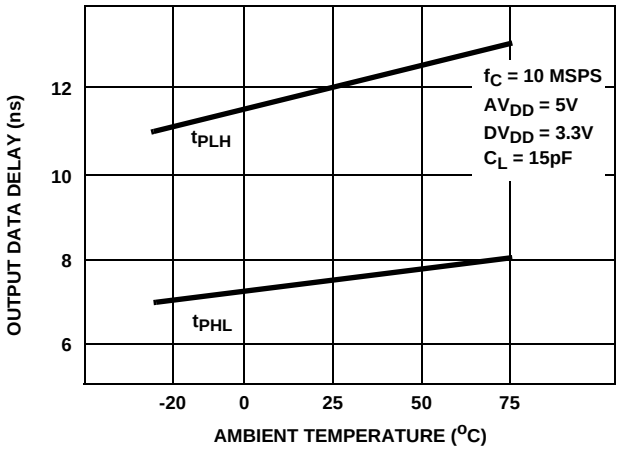


FIGURE 24. AMBIENT TEMPERATURE vs OUTPUT DATA DELAY

Typical Performance Curves (Continued)

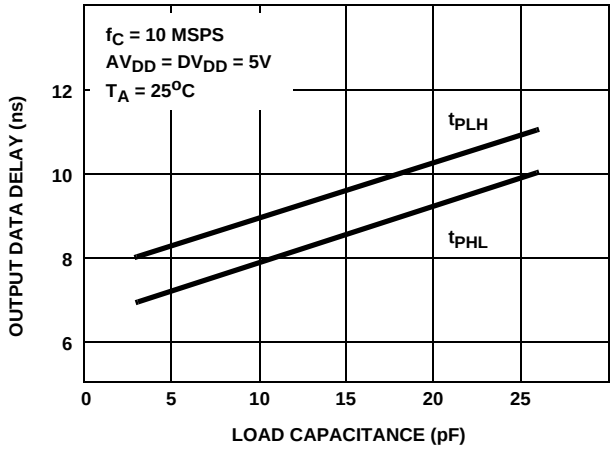


FIGURE 25. LOAD CAPACITANCE vs OUTPUT DATA DELAY

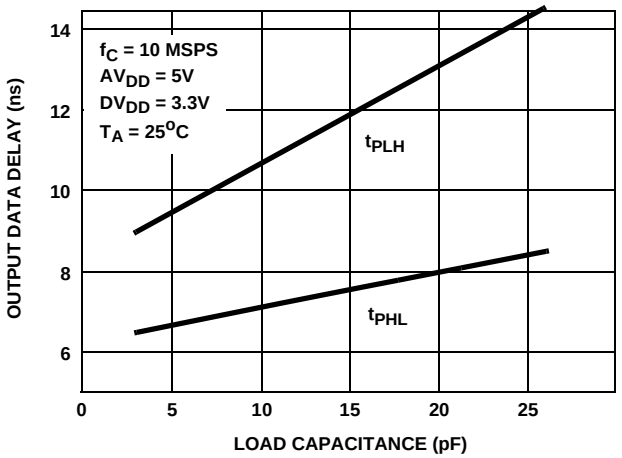


FIGURE 26. LOAD CAPACITANCE vs OUTPUT DATA DELAY

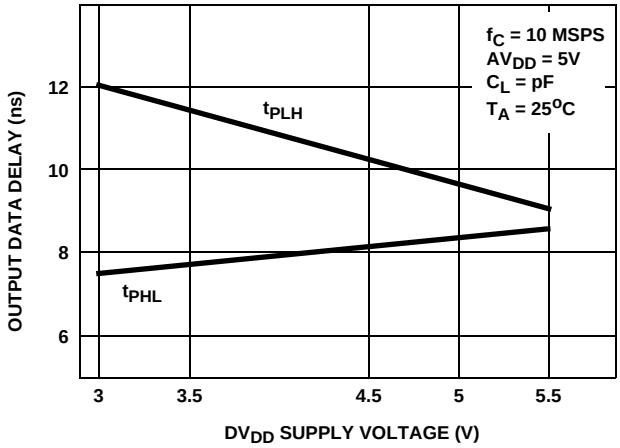


FIGURE 27. DV_{DD} SUPPLY VOLTAGE vs OUTPUT DATA DELAY

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