LP62S2048-T Series

256K X 8 BIT LOW VOLTAGE CMOS SRAM

Features

- Power supply range: 2.7V to 3.3V
- Access times: 70/100 ns (max.)
- Current:
  Low power version: Operating: 30mA (max.)
  Standby: 50µA (max.)
  Very low power version: Operating: 30mA (max.)
  Standby: 10µA (max.)
- Full static operation, no clock or refreshing required
- All inputs and outputs are directly TTL-compatible
- Common I/O using three-state output
- Output enable and two chip enable inputs for easy application
- Data retention voltage: 2V (min.)
- Available in 32-pin SOP, TSOP, TSSOP (8 X 13.4mm) and 36-pin CSP packages

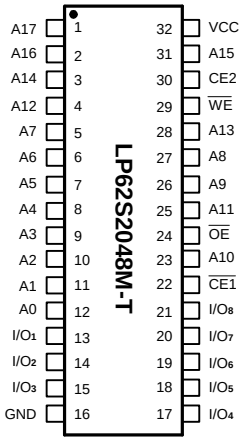
General Description

The LP62S2048-T is a low operating current 2,097,152-bit static random access memory organized as 262,144 words by 8 bits and operates on a low power supply range: 2.7V to 3.3V. It is built using AMIC's high performance CMOS process.
Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

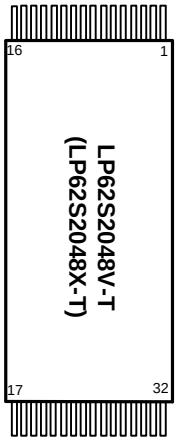
Two chip enable inputs are provided for POWER-DOWN and device enable and an output enable input is included for easy interfacing.
Data retention is guaranteed at a power supply voltage as low as 2V.

Pin Configurations

■ **SOP**



■ **TSOP/(TSSOP)**



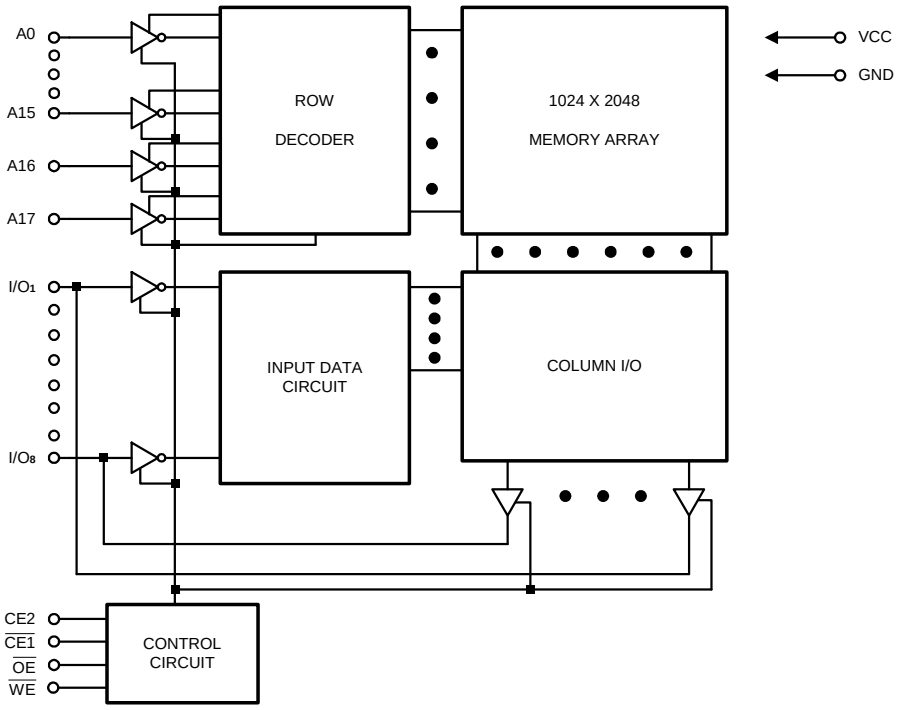
Pin No.	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16
Pin Name	A11	A9	A8	A13	$\overline{WE}$	CE2	A15	VCC	A17	A16	A14	A12	A7	A6	A5	A4
Pin No.	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32
Pin Name	A3	A2	A1	A0	I/O1	I/O2	I/O3	GND	I/O4	I/O5	I/O6	I/O7	I/O8	$\overline{CE1}$	A10	$\overline{OE}$

■ **CSP (Chip Size Package)**

36-pin Top View

	1	2	3	4	5	6
A	A0	A1	CE2	A3	A6	A8
B	I/O5	A2	$\overline{WE}$	A4	A7	I/O1
C	I/O6		NC	A5		I/O2
D	GND					VCC
E	VCC					GND
F	I/O7		NC	A17		I/O3
G	I/O8	$\overline{OE}$	$\overline{CE1}$	A16	A15	I/O4
H	A9	A10	A11	A12	A13	A14

Block Diagram



Pin Description - SOP

Pin No.	Symbol	Description
1 - 12, 23, 25 - 28, 31	A0 - A17	Address Inputs
13 - 15, 17 - 21	I/O1 - I/O8	Data Input/Outputs
16	GND	Ground
22	$\overline{CE1}$	Chip Enable
24	$\overline{OE}$	Output Enable
29	$\overline{WE}$	Write Enable
30	CE2	Chip Enable
32	VCC	Power Supply

Pin Descriptions - TSOP/TSSOP

Pin No.	Symbol	Description
1 - 4, 7, 9 - 20, 31	A0 - A17	Address Inputs
5	$\overline{WE}$	Write Enable
6	CE2	Chip Enable
8	VCC	Power Supply
9	NC	No Connection
21 - 23, 25 - 29	I/O1 - I/O8	Data Input/Outputs
24	GND	Ground
30	$\overline{CE1}$	Chip Enable
32	$\overline{OE}$	Output Enable

Pin Description - CSP

Symbol	Description	Symbol	Description
A0 - A17	Address Inputs	NC	No Connection
$\overline{WE}$	Write Enable	I/O_1 - I/O_8	Data Input/Output
$\overline{OE}$	Output Enable	VCC	Power Supply
$\overline{CE1}$	Chip Enable	GND	Ground
CE2	Chip Enable	--	--

Recommended DC Operating Conditions

(T_A = -25°C to + 85°C)

Symbol	Parameter	Min.	Typ.	Max.	Unit
VCC	Supply Voltage	2.7	3.0	3.3	V
GND	Ground	0	0	0	V
V_{IH}	Input High Voltage	2.0	-	VCC + 0.3	V
V_{IL}	Input Low Voltage	-0.3	-	+0.6	V
C_L	Output Load	-	-	30	pF
TTL	Output Load	-	-	1	-

Absolute Maximum Ratings*

VCC to GND . . . . . -0.5V to + 4.6V
IN, IN/OUT Volt to GND . . . . . -0.5V to VCC + 0.5V
Operating Temperature, Topr . . . . . -25°C to + 85°C
Storage Temperature, Tstg . . . . -55°C to + 125°C
Temperature Under Bias, Tbias . . . . . -10°C to + 85°C
Power Dissipation, P_T 0.7W
Soldering Temp. & Time . . . . . 260°C, 10 sec

*Comments

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to this device. These are stress ratings only. Functional operation of this device at these or any other conditions above those indicated in the operational sections of this specification is not implied or intended. Exposure to the absolute maximum rating conditions for extended periods may affect device reliability.

DC Electrical Characteristics

(T_A = -25°C to + 85°C, VCC = 2.7V to 3.3V, GND = 0V)

Symbol	Parameter	LP62S2048-70LT/10LT		LP62S2048-70LLT/10LLT		Unit	Conditions
		Min.	Max.	Min.	Max.		
$\lvert I_{LI} \rvert$	Input Leakage Current	-	1	-	1	µA	V_{IN} = GND to VCC
$\lvert I_{LO} \rvert$	Output Leakage Current	-	1	-	1	µA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL} or $\overline{OE}$ = V_{IH} or $\overline{WE}$ = V_{IL} $V_{I/O}$ = GND to VCC
I_{CC}	Active Power Supply Current	-	3	-	3	mA	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} $I_{I/O}$ = 0mA
I_{CC1}	Dynamic Operating Current	-	30	-	30	mA	Min. Cycle, Duty = 100% $\overline{CE1}$ = V_{IL}, CE2 = V_{IH} $I_{I/O}$ = 0mA
I_{CC2}		-	5	-	5	mA	$\overline{CE1}$ = V_{IL}, CE2 = V_{IH} V_{IH} = VCC, V_{IL} = 0V f = 1 MHz, $I_{I/O}$ = 0mA

DC Electrical Characteristics (continued)

Symbol	Parameter	LP62S2048-70LT/10LT		LP62S2048-70LLT/10LLT		Unit	Conditions
		Min.	Max.	Min.	Max.		
I_{SB}	Standby Power Supply Current	-	0.5	-	0.5	mA	$\overline{CE1}$ = V_{IH} or CE2 = V_{IL}
I_{SB1}		-	50	-	10	µA	$\overline{CE1}$ ≥ VCC - 0.2V V_{IN} ≥ 0V
I_{SB2}		-	50	-	10	µA	CE2 ≤ 0.2V V_{IN} ≥ 0V
V_{OL}	Output Low Voltage	-	0.4	-	0.4	V	I_{OL} = 2.1mA
V_{OH}	Output High Voltage	2.2	-	2.2	-	V	I_{OH} = -1.0mA

Truth Table

Mode	$\overline{CE1}$	CE2	$\overline{OE}$	$\overline{WE}$	I/O Operation	Supply Current
Standby	H	X	X	X	High Z	I_{SB}, I_{SB1}
	X	L	X	X	High Z	I_{SB}, I_{SB2}
Output Disable	L	H	H	H	High Z	I_{CC}, I_{CC1}, I_{CC2}
Read	L	H	L	H	D_{OUT}	I_{CC}, I_{CC1}, I_{CC2}
Write	L	H	X	L	D_{IN}	I_{CC}, I_{CC1}, I_{CC2}

Note: X = H or L

Capacitance (T_A = 25°C, f = 1.0MHz)

Symbol	Parameter	Min.	Max.	Unit	Conditions
C_{IN}*	Input Capacitance		6	pF	V_{IN} = 0V
$C_{I/O}$*	Input/Output Capacitance		8	pF	$V_{I/O}$ = 0V

* These parameters are sampled and not 100% tested.

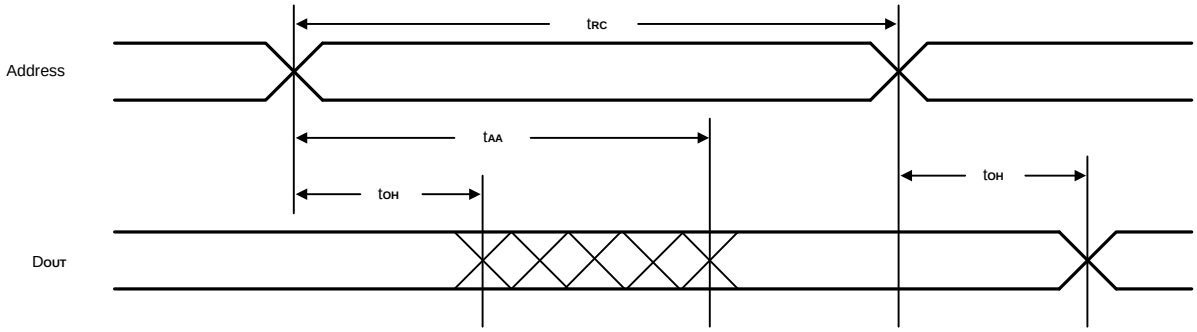
AC Characteristics (T_A = -25°C to + 85°C, VCC = 2.7V to 3.3V)

Symbol	Parameter		LP62S2048-70LT/LLT		LP62S2048-10LT/LLT		Unit
			Min.	Max.	Min.	Max.	
Read Cycle							
t_{RC}	Read Cycle Time		70	-	100	-	ns
t_{AA}	Address Access Time		-	70	-	100	ns
t_{ACE1}	Chip Enable Access Time	$\overline{CE1}$	-	70	-	100	ns
t_{ACE2}		CE2	-	70	-	100	ns
t_{OE}	Output Enable to Output Valid		-	35	-	50	ns
t_{CLZ1}	Chip Enable to Output in Low Z	$\overline{CE1}$	10	-	10	-	ns
t_{CLZ2}		CE2	10	-	10	-	ns
t_{OLZ}	Output Enable to Output in Low Z		5	-	5	-	ns
t_{CHZ1}	Chip Disable to Output in High Z	$\overline{CE1}$	0	25	0	35	ns
t_{CHZ2}		CE2	0	25	0	35	ns
t_{OHZ}	Output Disable to Output in High Z		0	25	0	35	ns
t_{OH}	Output Hold from Address Change		10	-	10	-	ns
Write Cycle							
t_{WC}	Write Cycle Time		70	-	100	-	ns
t_{CW}	Chip Enable to End of Write		60	-	80	-	ns
t_{AS}	Address Setup Time		0	-	0	-	ns
t_{AW}	Address Valid to End of Write		60	-	80	-	ns
t_{WP}	Write Pulse Width		50	-	60	-	ns
t_{WR}	Write Recovery Time		0	-	0	-	ns
t_{WHZ}	Write to Output in High Z		0	25	0	35	ns
t_{DW}	Data to Write Time Overlap		30	-	40	-	ns
t_{DH}	Data Hold from Write Time		0	-	0	-	ns
t_{OW}	Output Active from End of Write		5	-	5	-	ns

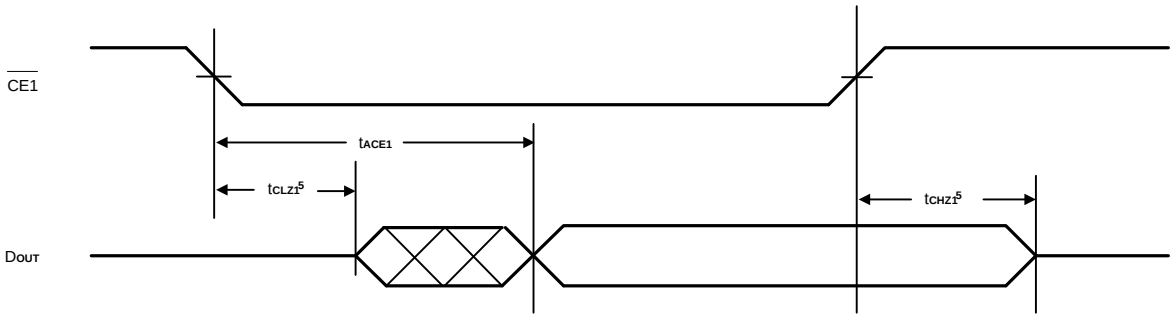
Notes: t_{CHZ1}, t_{CHZ2}, t_{OHZ}, and t_{WHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

Timing Waveforms

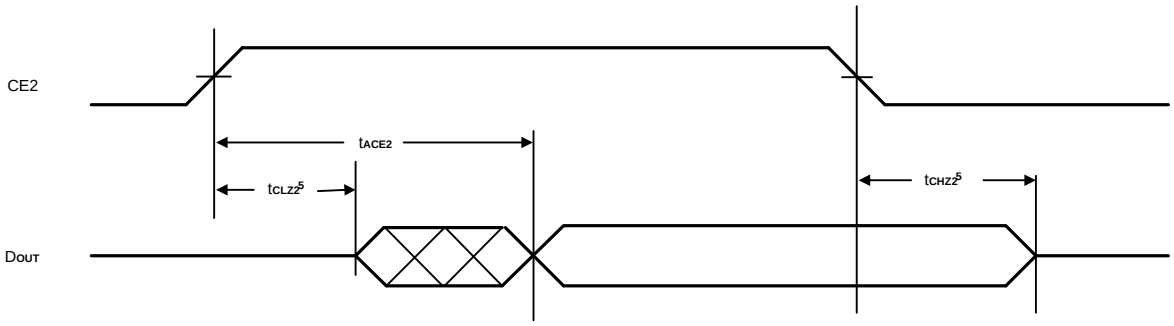
Read Cycle 1 (1, 2, 4)



Read Cycle 2 (1, 3, 4, 6)

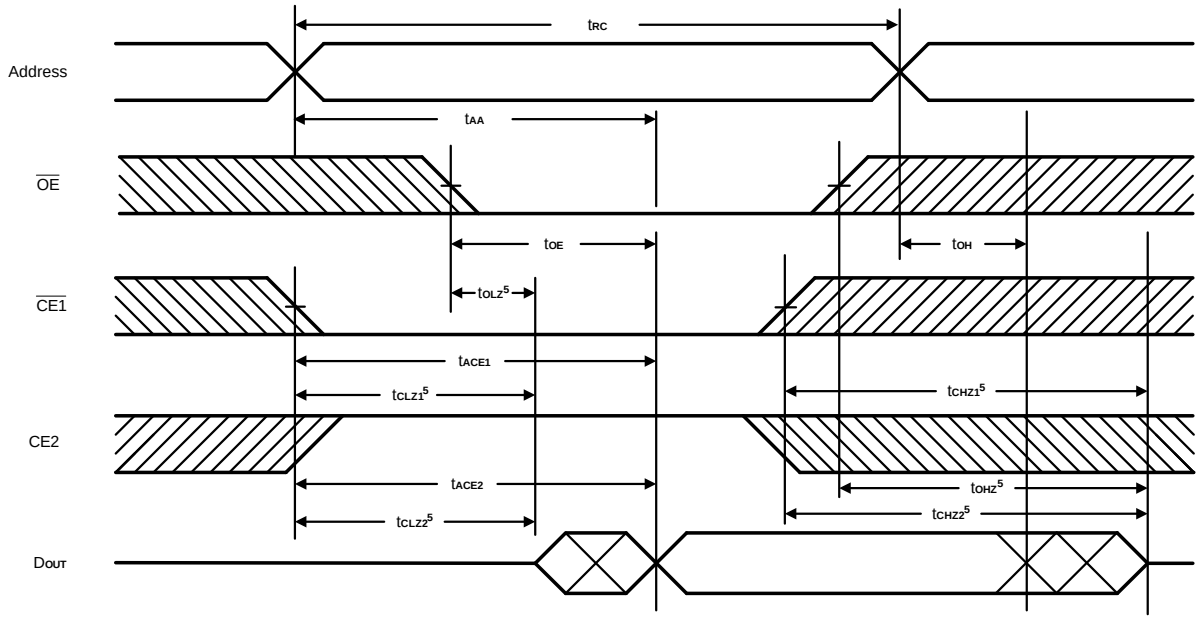


Read Cycle 3 (1, 4, 7, 8)



Timing Waveforms (continued)

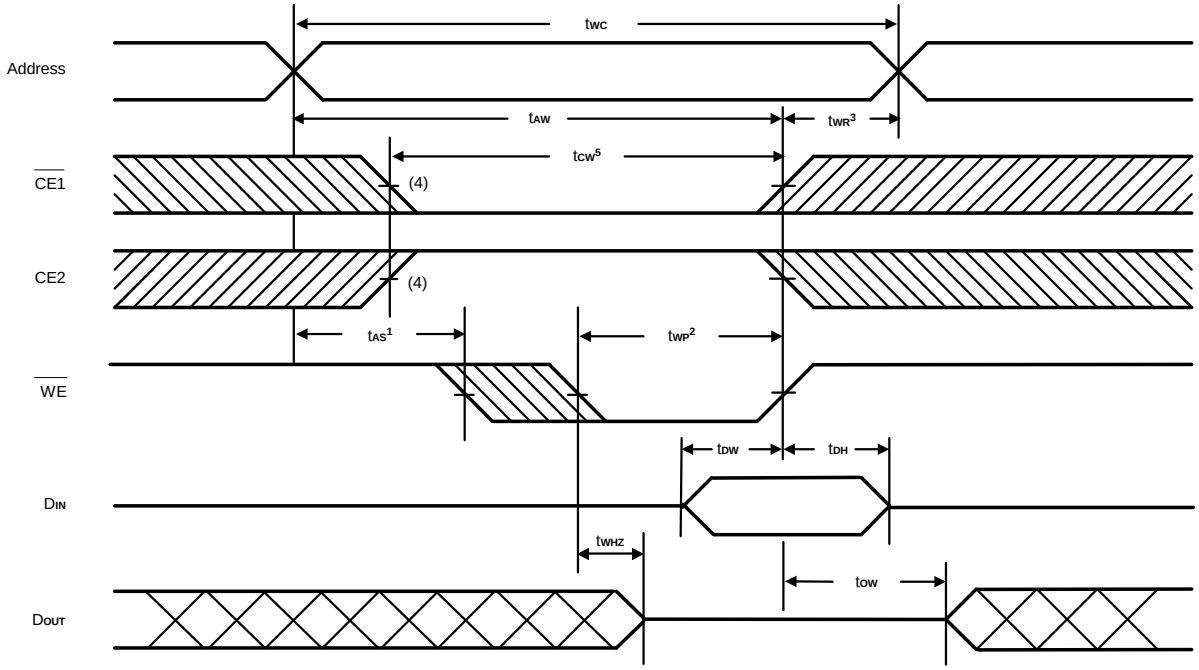
Read Cycle 4 (1)



Notes: 1. $\overline{WE}$ is high for Read Cycle.
2. Device is continuously enabled $\overline{CE1}$ = V_{IL} and CE2 = V_{IH}.
3. Address valid prior to or coincident with $\overline{CE1}$ transition low.
4. $\overline{OE}$ = V_{IL}.
5. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.
6. CE2 is high.
7. $\overline{CE1}$ is low.
8. Address valid prior to or coincident with CE2 transition high.

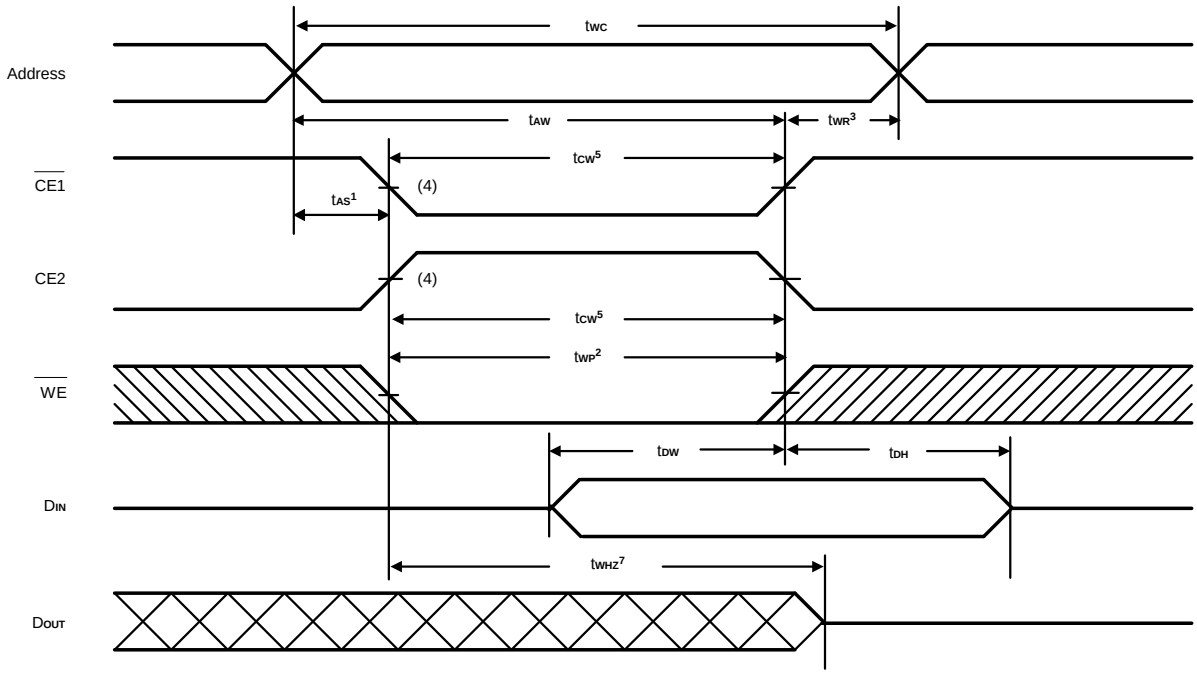
Timing Waveforms (continued)

Write Cycle 1 [6]
(Write Enable Controlled)



Timing Waveforms (continued)

Write Cycle 2
(Chip Enable Controlled)



Notes: 1. t_{AS} is measured from the address valid to the beginning of Write.
2. A Write occurs during the overlap (t_{WP}) of a low $\overline{CE1}$, a high CE2 and a low $\overline{WE}$.
3. t_{WR} is measured from the earliest of $\overline{CE1}$ or $\overline{WE}$ going high or CE2 going low to the end of the Write cycle.
4. If the $\overline{CE1}$ low transition or the CE2 high transition occurs simultaneously with the $\overline{WE}$ low transition or after the $\overline{WE}$ transition, outputs remain in a high impedance state.
5. t_{CW} is measured from the later of $\overline{CE1}$ going low or CE2 going high to the end of Write.
6. $\overline{OE}$ is continuously low. ($\overline{OE}$ = V_{IL})
7. Transition is measured ±500mV from steady state. This parameter is sampled and not 100% tested.

AC Test Conditions

Input Pulse Levels	0.4V to 2.4V
Input Rise and Fall Time	5 ns
Input and Output Timing Reference Levels	1.5V
Output Load	See Figures 1 and 2

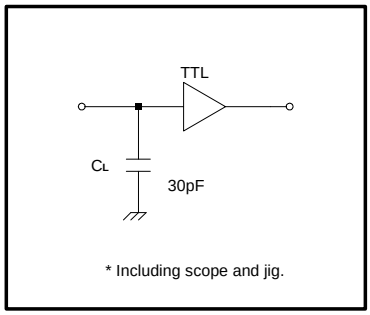


Figure 1. Output Load

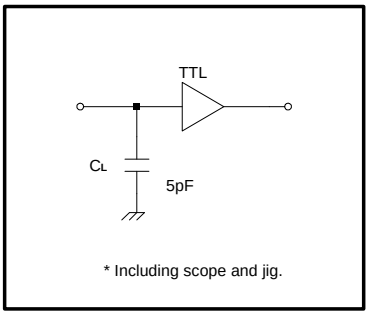


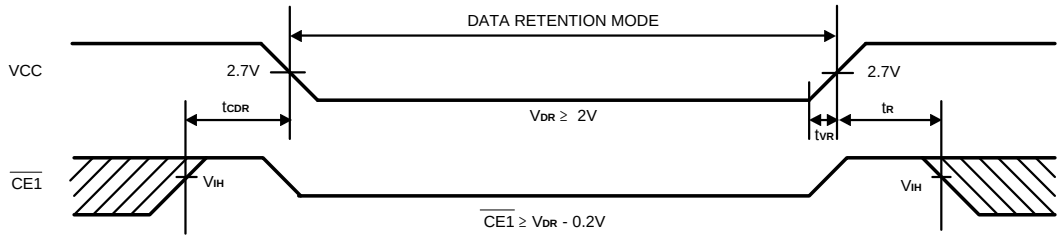
Figure 2. Output Load for t_{CLZ1}, t_{CLZ2}, t_{OHZ}, t_{OLZ}, t_{CHZ1}, t_{CHZ2}, t_{WHZ}, and t_{OW}

Data Retention Characteristics (T_A = -25°C to 85°C)

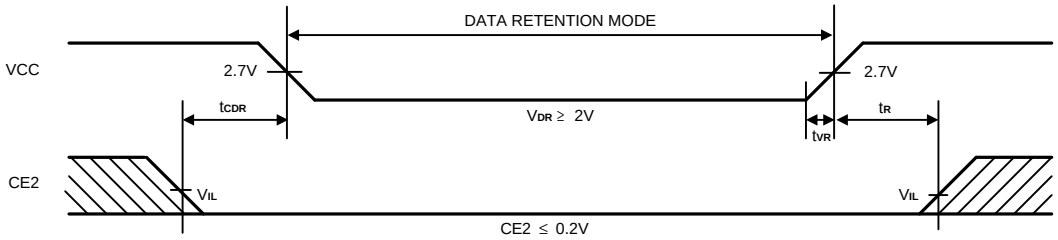
Symbol	Parameter		Min.	Max.	Unit	Conditions
V_{DR1}	VCC for Data Retention		2.0	3.3	V	$\overline{CE1} \geq$ VCC - 0.2V
V_{DR2}			2.0	3.3	V	CE2 $\leq$ 0.2V,
I_{CCDR1}	Data Retention Current	L-Version	-	20*	µA	VCC = 2.0V, $\overline{CE1} \geq$ VCC - 0.2V, $V_{IN} \geq$ 0V
		LL-Version	-	5**		
I_{CCDR2}		L-Version	-	20*	µA	VCC = 2.0V, CE2 $\leq$ 0.2V, $V_{IN} \geq$ 0V
		LL-Version	-	5**		
t_{CDR}	Chip Disable to Data Retention Time		0	-	ns	See Retention Waveform
t_R	Operation Recovery Time		t_{RC}	-	ns	
t_{VR}	VCC Rising Time from Data Retention Voltage to Operating Voltage		5	-	ms	

** LP62S2048-70LLT/10LLT I_{CCDR}: max. 1µA at T_A = 0°C to + 40°C
* LP62S2048-70LT/10LT I_{CCDR}: max. 5µA at T_A = 0°C to + 40°C

Low VCC Data Retention Waveform (1) ($\overline{CE1}$ Controlled)



Low VCC Data Retention Waveform (2) (CE2 Controlled)



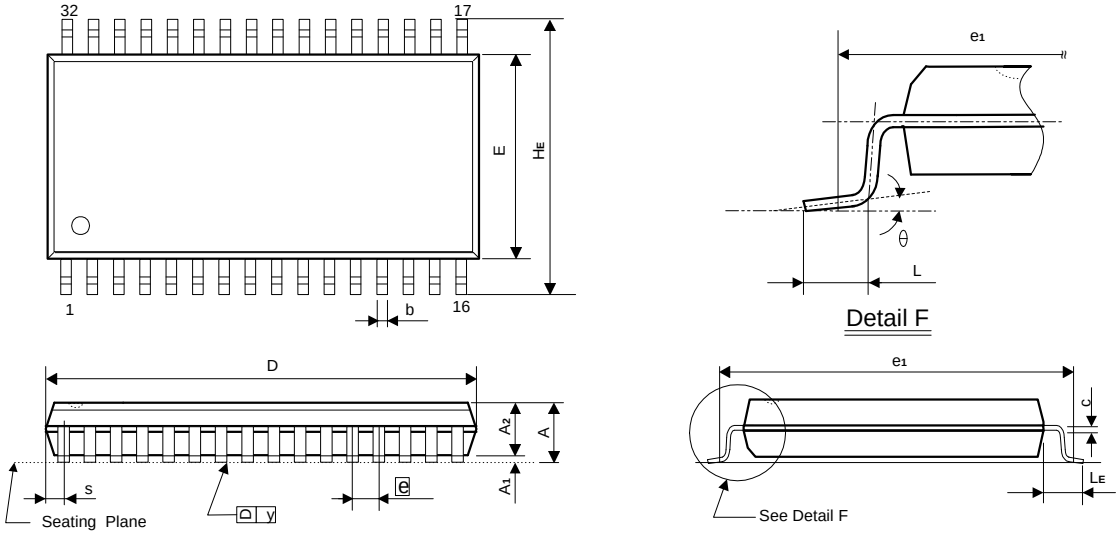
Ordering Information

Part No.	Access Time (ns)	Operating Current Max. (mA)	Standby Current Max. (mA)	Package
LP62S2048M-70LT	70	30	50	32L SOP
LP62S2048M-70LLT		30	10	32L SOP
LP62S2048V-70LT		30	50	32L TSOP
LP62S2048V-70LLT		30	10	32L TSOP
LP62S2048X-70LT		30	50	32L TSSOP
LP62S2048X-70LLT		30	10	32L TSSOP
LP62S2048U-70LT		30	50	36L CSP
LP62S2048U-70LLT		30	10	36L CSP
LP62S2048M-10LT	100	30	50	32L SOP
LP62S2048M-10LLT		30	10	32L SOP
LP62S2048V-10LT		30	50	32L TSOP
LP62S2048V-10LLT		30	10	32L TSOP
LP62S2048X-10LT		30	50	32L TSSOP
LP62S2048X-10LLT		30	10	32L TSSOP
LP62S2048U-10LT		30	50	36L CSP
LP62S2048U-10LLT		30	10	36L CSP

Package Information

SOP (W.B.) 32L Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.118 Max.	3.00 Max.
A_1	0.004 Min.	0.10 Min.
A_2	0.106±0.005	2.69±0.13
b	0.016 +0.004 -0.002	0.41 +0.10 -0.05
c	0.008 +0.004 -0.002	0.20 +0.10 -0.05
D	0.805 Typ. (0.820 Max.)	20.45 Typ. (20.83 Max.)
E	0.445±0.010	11.30±0.25
e	0.050 ±0.006	1.27±0.15
e_1	0.525 NOM.	13.34 NOM.
H_E	0.556±0.010	14.12±0.25
L	0.031±0.008	0.79±0.20
L_E	0.055±0.008	1.40±0.20
S	0.044 Max.	1.12 Max.
y	0.004 Max.	0.10 Max.
θ	0° ~ 10°	0° ~ 10°

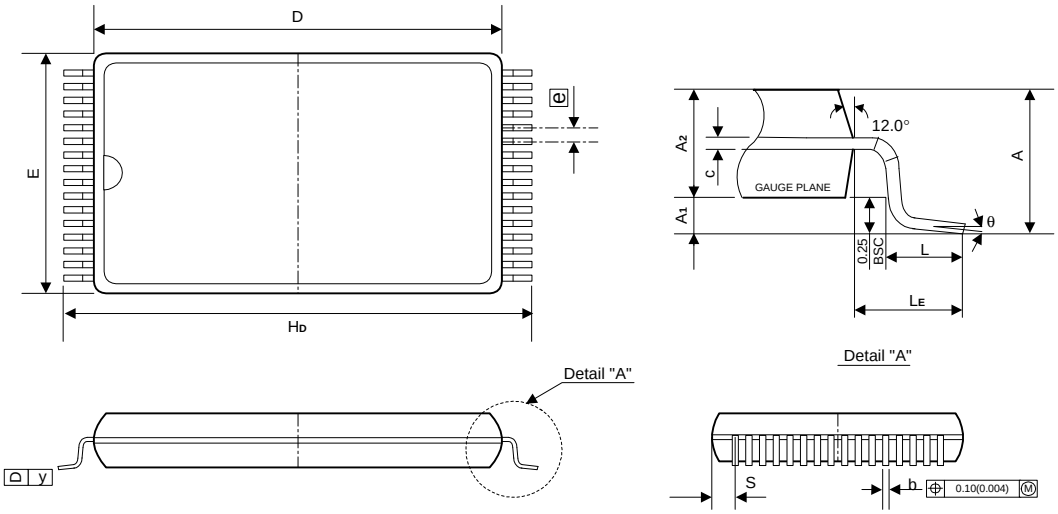
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information

TSOP 32L TYPE I (8 X 20mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.047 Max.	1.20 Max.
A_1	0.004±0.002	0.10±0.05
A_2	0.039±0.002	1.00±0.05
b	0.008±0.001	0.20±0.03
c	0.006±0.001	0.15±0.02
D	0.724±0.004	18.40±0.10
E	0.315±0.004	8.00±0.10
e	0.020 TYP.	0.50 TYP.
H_D	0.787±0.007	20.00±0.20
L	0.020±0.004	0.50±0.10
L_E	0.031 TYP.	0.80 TYP.
S	0.0167 TYP.	0.425 TYP.
Y	0.004 Max.	0.10 Max.
θ	0° ~ 6°	0° ~ 6°

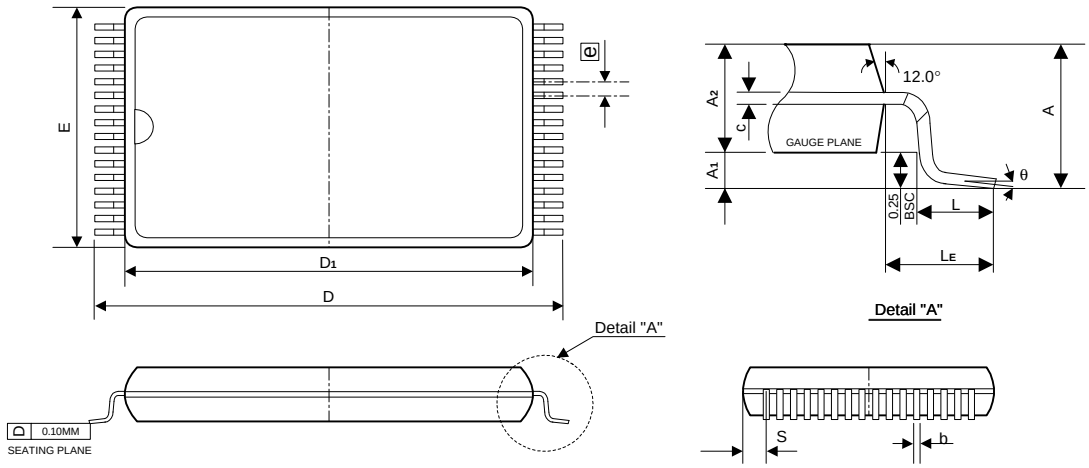
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information

TSSOP 32L TYPE I (8 X 13.4mm) Outline Dimensions

unit: inches/mm



Symbol	Dimensions in inches	Dimensions in mm
A	0.049 Max.	1.25 Max.
A_1	0.002 Min.	0.05 Min.
A_2	0.039±0.002	1.00±0.05
b	0.008±0.001	0.20±0.03
c	0.006±0.0003	0.15±0.008
E	0.315±0.004	8.00±0.10
e	0.020 TYP.	0.50 TYP.
D	0.528±0.008	13.40±0.20
D_1	0.465±0.004	11.80±0.10
L	0.02±0.008	0.50±0.20
L_E	0.0266 Min.	0.675 Min.
S	0.0109 TYP.	0.278 TYP.
y	0.004 Max.	0.10 Max.
θ	0° ~ 6°	0° ~ 6°

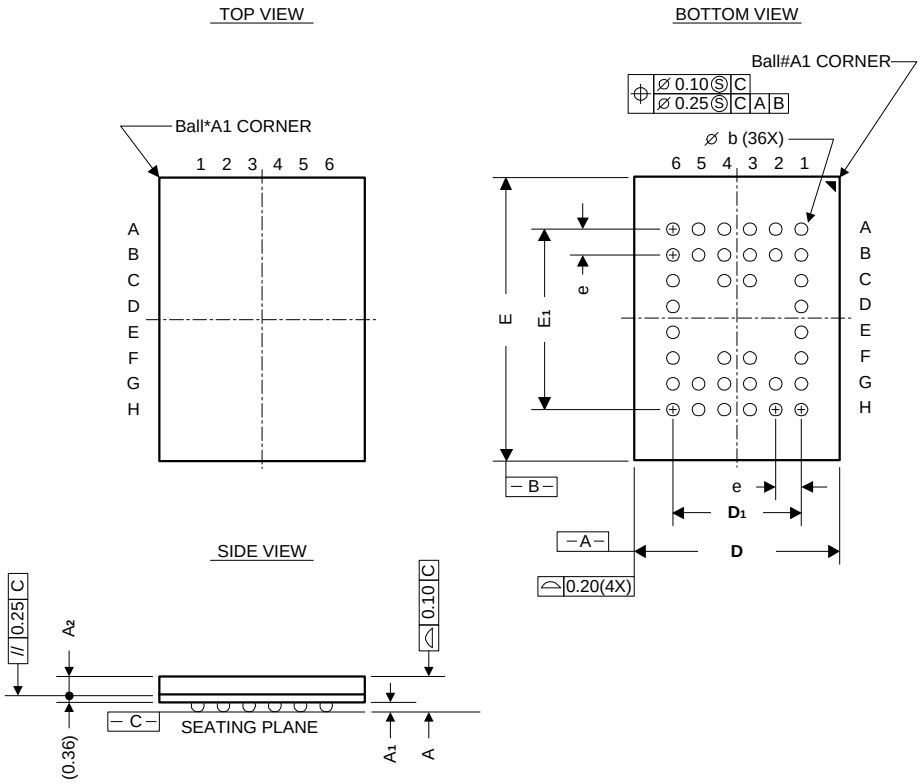
Notes:

1. The maximum value of dimension D includes end flash.
2. Dimension E does not include resin fins.
3. Dimension e_1 is for PC Board surface mount pad pitch design reference only.
4. Dimension S includes end flash.

Package Information

36LD CSP (6 x 8 mm) Outline Dimensions

unit: mm



Symbol	Dimensions in mm		
	MIN.	NOM.	MAX.
A	1.00	1.10	1.20
A_1	0.16	0.21	0.26
A_2	0.48	0.53	0.58
D	5.80	6.00	6.20
E	7.80	8.00	8.20
D_1	---	3.75	---
E_1	---	5.25	---
e	---	0.75	---
b	0.25	0.30	0.35

Note:

1. THE BALL DIAMETER, BALL PITCH, STAND-OFF & PACKAGE THICKNESS ARE DIFFERENT FROM JEDEC SPEC MO192 (LOW PROFILE BGA FAMILY).
2. PRIMARY DATUM C AND SEATING PLANE ARE DEFINED BY THE SPHERICAL CROWNS OF THE SOLDER BALLS.
3. DIMENSION b IS MEASURED AT THE MAXIMUM.
   THEERE SHALL BE A MINIMUM CLEARANCE OF 0.25mm BETWEEN THE EDGE OF THE SOLDER BALL AND THE BODY EDGE.
4. BALL PAD OPENING OF SUBSTRATE IS Φ 0.25mm (SMD)
   SUGGEST TO DESIGN THE PCB LAND SIZE AS Φ 0.25mm (NSMD)